19-4059; Rev 1; 9/08

1.2A PWM Step-Down Converter in 2mm x 2mm WLP/UCSP for PA Power

General Description

The MAX8836Z high-frequency step-down converter is optimized to provide a fixed output voltage with ultra-low dropout. The device integrates a high-efficiency PWM step-down converter for medium- and low-power transmission, and a 60mΩ typical bypass FET for ultra low-dropout operation. A 200mA low-noise, high-PSRR low-dropout regulator (LDO) is also integrated.

Fast-switching allows the use of small ceramic input and output capacitors while maintaining low ripple voltage. The feedback network is integrated, further reducing external component count and total solution size. At high duty cycle, the MAX8836Z automatically switches to the bypass mode, connecting the input to the output through a low-impedance (60mΩ typ) MOSFET. The LDO in the MAX8836Z is designed for low-noise operation (35μV_{RMS} typ). Both the PWM step-down and LDO are individually enabled through separate logic-control interfaces.

The MAX8836Z is available in 16-bump, 2mm x 2mm WLP and UCSP™ packages (0.7mm max height).

Applications

WCDMA/NCDMA Cellular Handsets

Wireless PDAs

Smartphones

Ordering Information

PART	PIN-PACKAGE	TEMP RANGE
MAX8836ZEWEEE+T	16 WLP (W162B2+1)	-40°C to +85°C
MAX8836ZEREEE+T	16 UCSP (R162A2+1)	-40°C to +85°C

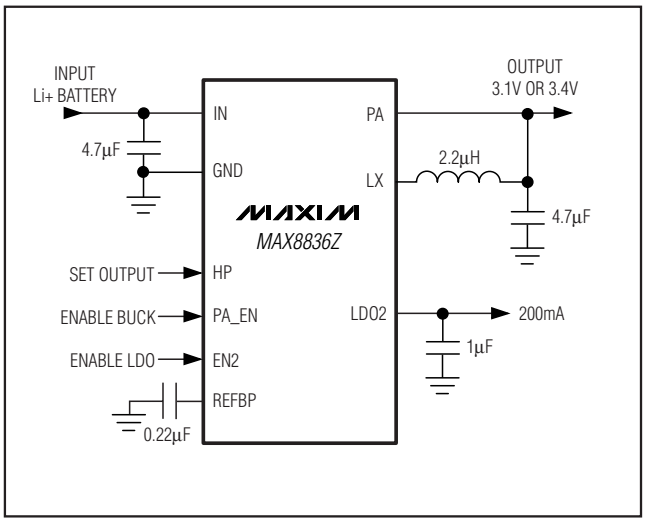
+Denotes a lead-free/RoHS-compliant package.

T = Tape and reel.

Features

- **PA Step-Down Converter**
  - **Selectable Output Voltage (3.1V or 3.4V)**
  - **25µs Settling Time for 3.1V to 3.4V_{OUT} Change**
  - **60mΩ PFET at 100% Duty-Cycle for Low Dropout**
  - **Low Output Voltage Ripple**
  - **1.2A Output Drive Capability**
  - **±2% Output Voltage Accuracy**
  - **Tiny External Components**
- **Low-Noise LDO**
  - **Low 35μV_{RMS} (typ) Output Noise**
  - **High 65dB (typ) PSRR**
  - **Guaranteed 200mA Output Current Drive Capability**
  - **ON/OFF Control**
- **Low 0.1µA Shutdown Current**
- **2.7V to 5.5V Supply Voltage Range**
- **Thermal Shutdown**
- **Tiny 2mm x 2mm x 0.7mm WLP and UCSP Packages (4 x 4 Grid)**

Typical Operating Circuit



Pin Configuration appears at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

1.2A PWM Step-Down Converter in 2mm x 2mm WLP/UCSP for PA Power

ABSOLUTE MAXIMUM RATINGS

IN1A, IN1B, IN2, EN2, REFBP to AGND.....-0.3V to +6.0V
PAA, PAB, PA_EN, HP to AGND....-0.3V to (V_{IN1A}/V_{IN1B} + 0.3V)
LDO2 to AGND .....-0.3V to (V_{IN2} + 0.3V)
IN2 to IN1B/IN1A .....-0.3V to +0.3V
PGND to AGND .....-0.3V to +0.3V
LX Current .....0.7A_{RMS}
IN1A/IN1B and PAA/PAB Current .....2A_{RMS}
PAA and PAB Short Circuit to GND or IN.....Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Bump WLP (derate 12.5mW/°C above +70°C).....1W
16-Bump UCSP (derate 12.5mW/°C above +70°C) 1W
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Bump Temperature (soldering, reflow).....+260°C

Note: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Preheating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1A} = V_{IN1B} = V_{IN2} = V_{PA_EN} = V_{EN2} = 3.6V, V_{HP} = 0V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLY						
Input Voltage	V_{IN1A}, V_{IN1B}, V_{IN2}		2.7		5.5	V
Input Undervoltage Threshold	V_{IN1A}, V_{IN1B}, V_{IN2} rising, 180mV typical hysteresis		2.52	2.63	2.70	V
HP, PA_EN, EN2 Pulldown Resistor			400	800	1600	kΩ
Shutdown Supply Current	V_{PA_EN} = V_{EN2} = 0V	T_A = +25°C		0.1	4	µA
		T_A = +85°C		0.1		
No-Load Supply Current	V_{PA_EN} = 0V, I_{LDO2} = 0A			100	150	µA
	V_{EN2} = 0V, I_{PA} = 0A, switching			3500		
	V_{EN2} = 0V, I_{PA} = 0A, no switching			180		
THERMAL PROTECTION						
Thermal Shutdown	T_A rising, 20°C typical hysteresis			+160		°C
LOGIC CONTROL						
PA_EN, EN2, HP Logic-Input High Voltage			1.3			V
PA_EN, EN2, HP Logic-Input Low Voltage					0.4	V
Logic-Input Current (PA_EN, EN2, HP)	V_{IL} = 0V	T_A = +25°C		0.01	1	µA
		T_A = +85°C		0.1		
PA OUTPUT VOLTAGE						
Output Voltage	I_{LX} = 0A, V_{IN1A} = V_{IN1B} = V_{IN2} = 3.9V	HP = 0	3.365	3.434	3.503	V
		HP = 1	3.010	3.065	3.190	
Output Voltage Load Regulation				I_{LX} x R_L/2		V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1A} = V_{IN1B} = V_{IN2} = V_{PA_EN} = V_{EN2} = 3.6V, V_{HP} = 0V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LX						
On-Resistance	p-channel MOSFET switch, I_{LX} = -40mA			0.15		Ω
	n-channel MOSFET rectifier, I_{LX} = 40mA			0.15		
LX Leakage Current	V_{IN1A} = V_{IN1B} = V_{IN2} = 5.5V, V_{LX} = 0V	T_A = +25°C		0.1	5	µA
		T_A = +85°C		1		
p-Channel MOSFET Peak Current Limit	V_{LX} = 0V		1.3	1.5	1.8	A
n-Channel MOSFET Valley Current Limit			1.1	1.3	1.6	A
Minimum On- and Off-Times				0.07		µs
Power-Up Delay	From PA_EN rising to LX rising			80	190	µs
BYPASS						
On-Resistance	p-channel MOSFET bypass, I_{PA} = -90mA	T_A = +25°C		0.060	0.1	Ω
		T_A = +85°C		0.1		
Bypass Current Limit	V_{PA} = 0V		0.8	1.4	1.8	A
Total Bypass Current Limit	V_{LX} = V_{PA} = 0V		2.1	2.9	3.6	A
Bypass Threshold	V_{IN2} rising, 150mV hysteresis			0.985 x V_{PA}		V/V
Bypass Off-Leakage Current	V_{IN1A} = V_{IN1B} = V_{IN2} = 5.5V, V_{PAA} = V_{PAB} = 0V	T_A = +25°C		0.01	5	µA
		T_A = +85°C		0.1		
LDO2						
Output Voltage V_{LDO2}	V_{IN2} = 5.5V, I_{LDO2} = 1mA; V_{IN2} = 3.4V, I_{LDO2} = 1mA		2.765	2.85	2.936	V
Output Current			200			mA
Current Limit	V_{LDO2} = 0V		250	550	750	mA
Dropout Voltage	I_{LDO2} = 100mA, T_A = +25°C (V_{LDO2} ≥ 2.5V)			70		mV
Line Regulation	V_{IN2} stepped from 3.5V to 5.5V, I_{LDO2} = 100mA			2.4		mV
Load Regulation	I_{LDO2} stepped from 50µA to 200mA			25		mV
Power-Supply Rejection $\Delta V_{LDO2}/\Delta V_{IN2}$	10Hz to 10kHz, C_{LDO2} = 1µF, I_{LDO2} = 30mA			65		dB
Output Noise	100Hz to 100kHz, C_{LDO2} = 1µF, I_{LDO2} = 30mA			35		$µV_{RMS}$
Output Capacitor for Stable Operation	0 < I_{LDO2} < 10mA			100		nF
	0 < I_{LDO2} < 200mA			1		µF
Shutdown Output Impedance	V_{EN2} = 0V			1		kΩ
REFBP						
REFBP Output Voltage	0 ≤ I_{REFBP} ≤ 1µA		1.237	1.250	1.263	V
REFBP Supply Rejection	V_{IN2} stepped from 2.55V to 5.5V			0.2	5	mV

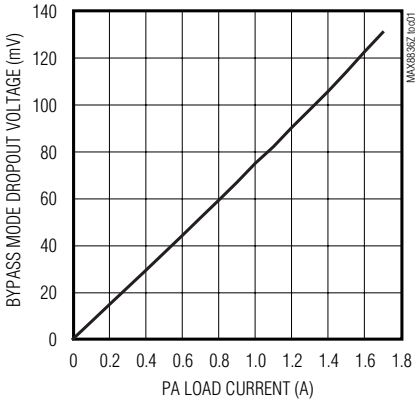
Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

1.2A PWM Step-Down Converter in 2mm x 2mm WLP/UCSP for PA Power

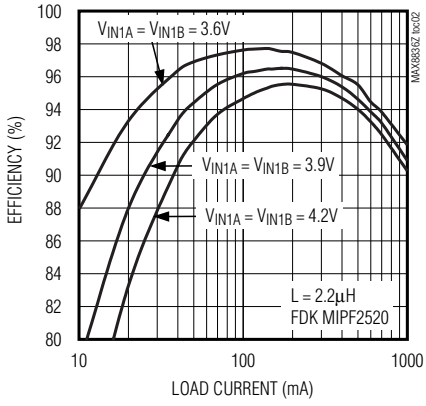
Typical Operating Characteristics

(V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V, V_{PA} = 3.4V, V_{LDO2} = 2.85V, R_{PA} = 7.5Ω, circuit of MAX8805WEVKIT, T_A = +25°C, unless otherwise noted.)

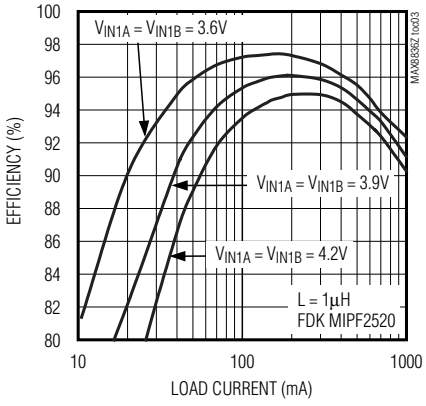
BYPASS MODE DROPOUT VOLTAGE vs. PA LOAD CURRENT



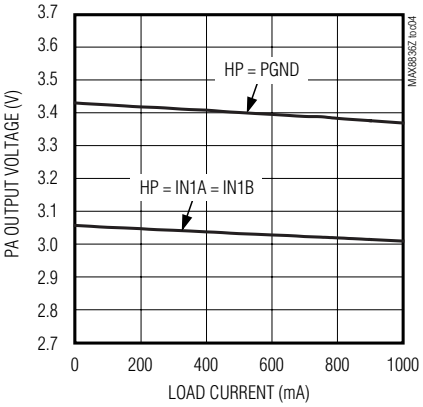
PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT



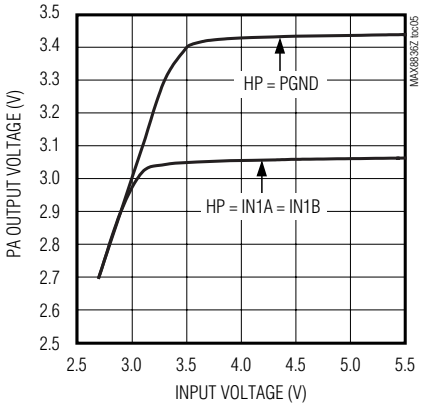
PA STEP-DOWN CONVERTER EFFICIENCY vs. LOAD CURRENT



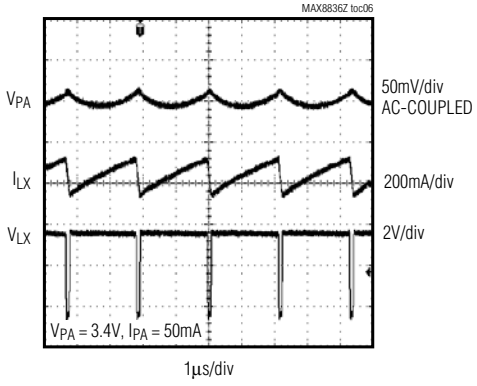
PA STEP-DOWN CONVERTER OUTPUT VOLTAGE vs. LOAD CURRENT



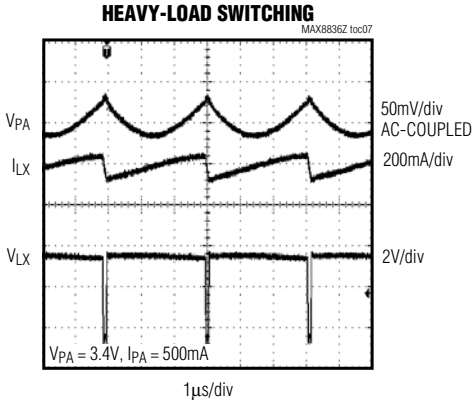
PA STEP-DOWN CONVERTER OUTPUT VOLTAGE vs. INPUT VOLTAGE



PA STEP-DOWN CONVERTER LIGHT-LOAD SWITCHING WAVEFORMS



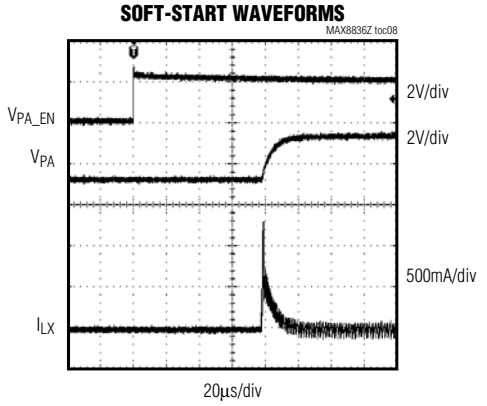
PA STEP-DOWN CONVERTER HEAVY-LOAD SWITCHING



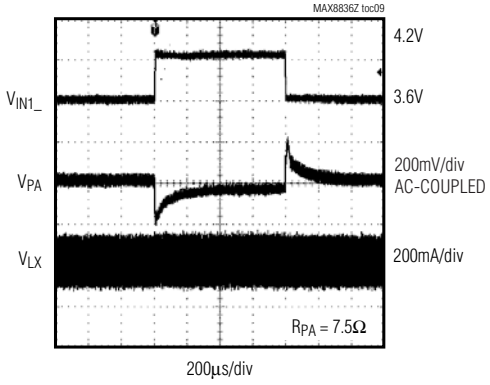
Typical Operating Characteristics (continued)

(V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V, V_{PA} = 3.4V, V_{LDO2} = 2.85V, R_{PA} = 7.5Ω, circuit of MAX8805WEVKIT, T_A = +25°C, unless otherwise noted.)

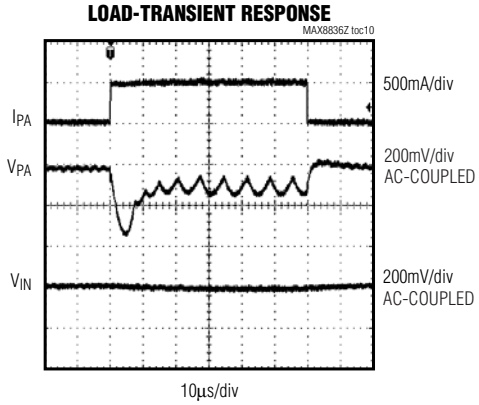
PA STEP-DOWN CONVERTER SOFT-START WAVEFORMS



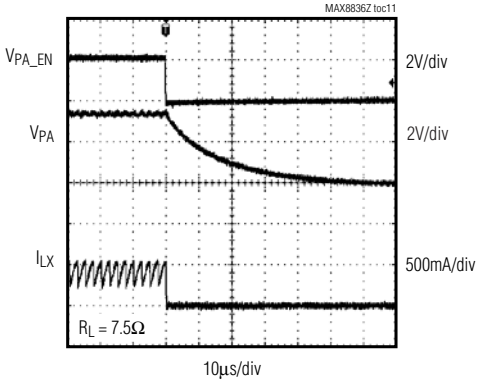
PA STEP-DOWN CONVERTER LINE-TRANSIENT RESPONSE



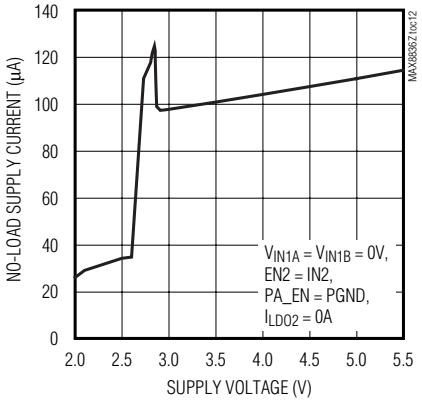
PA STEP-DOWN CONVERTER LOAD-TRANSIENT RESPONSE



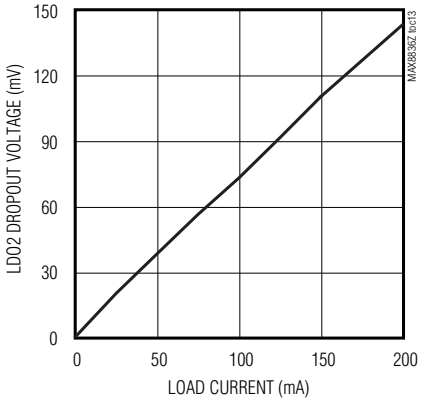
PA STEP-DOWN CONVERTER SHUTDOWN RESPONSE



LDO2 SUPPLY CURRENT vs. SUPPLY VOLTAGE



LDO2 DROPOUT VOLTAGE vs. LOAD CURRENT

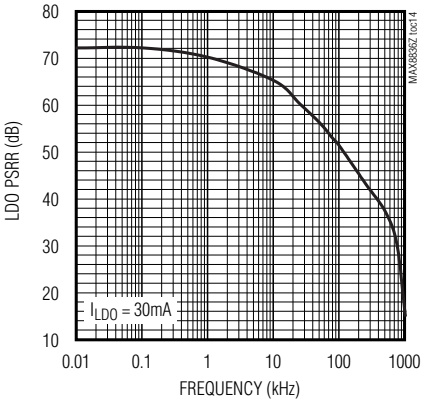


1.2A PWM Step-Down Converter in 2mm x 2mm WLP/UCSP for PA Power

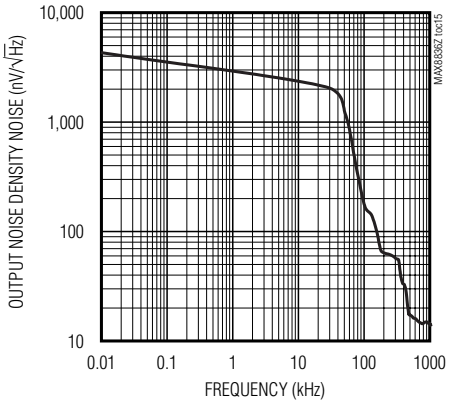
Typical Operating Characteristics (continued)

(V_{IN1A} = V_{IN1B} = V_{IN2} = 3.6V, V_{PA} = 3.4V, V_{LDO2} = 2.85V, R_{PA} = 7.5Ω, circuit of MAX8805WEVKIT, T_A = +25°C, unless otherwise noted.)

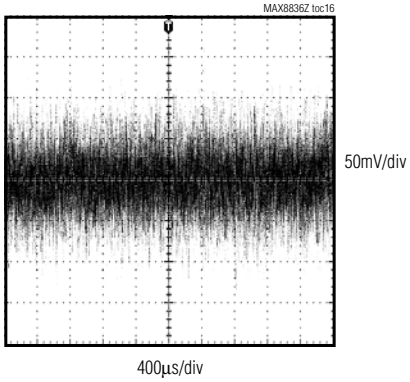
LDO POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



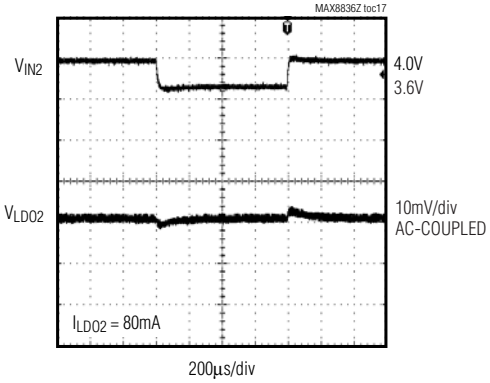
LDO OUTPUT NOISE SPECTRAL DENSITY vs. FREQUENCY



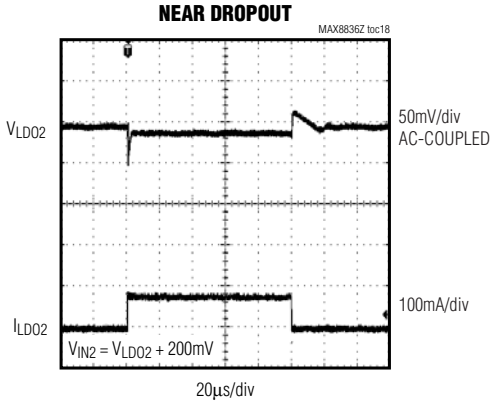
LDO2 OUTPUT NOISE WAVEFORM



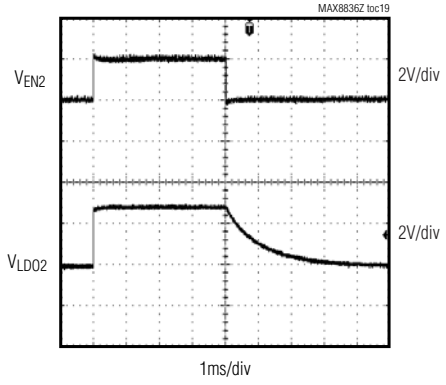
LDO2 LINE-TRANSIENT RESPONSE



LDO2 LOAD-TRANSIENT RESPONSE NEAR DROPOUT



LDO2 SHUTDOWN RESPONSE



Pin Description

PIN	NAME	FUNCTION
A1	REFBP	Reference Noise Bypass. Bypass REFBP to AGND with a 0.22µF ceramic capacitor to reduce noise on the LDO outputs. REFBP is internally pulled down through a 1kΩ resistor during shutdown.
A2	AGND	Low-Noise Analog Ground. Connect AGND to PGND using a common ground plane. Refer to the MAX8805W Evaluation Kit for more information.
A3	N.I.C.	Not Internally Connected. Connect to AGND for improved thermal performance.
A4	PGND	Power Ground for PA Step-Down Converter. Connect AGND to PGND using a common ground plane. Refer to the MAX8805W Evaluation Kit for more information.
B1	LDO2	200mA LDO Regulator 2 Output. Bypass LDO2 with a 1µF ceramic capacitor as close as possible to LDO2 and AGND. LDO2 is internally pulled down through a 1kΩ resistor when this regulator is disabled.
B2	PA_EN	PA Step-Down Converter Enable. Active-high enable input. Connect to IN1A/IN1B or logic-high for normal operation. Pulled down to ground through an internal 800kΩ resistor.
B3	EN2	LDO2 Enable. Active-high enable input. Connect to IN2 or logic-high for normal operation. Pulled down to ground through an internal 800kΩ resistor.
B4	LX	Inductor Connection. Connect an inductor from LX to the output of the PA step-down converter.
C1	IN2	Supply Voltage Input for LDO2 and Internal Reference. Connect IN2 to a battery or supply voltage from 2.7V to 5.5V. Bypass IN2 with a 2.2µF ceramic capacitor as close as possible to IN2 and AGND. Connect IN2 to the same source as IN1A and IN1B.
C2	HP	PA Output Voltage Select. Pulled down to ground through an internal 800kΩ resistor.
C3, C4	IN1B, IN1A	Supply Voltage Input for PA Step-Down Converter. Connect IN1_ to a battery or supply voltage from 2.7V to 5.5V. Bypass the connection of IN1_ with a 4.7µF ceramic capacitor as close as possible to IN1_ and PGND. IN1A and IN1B are internally connected together. Connect IN1_ to the same source as IN2.
D1	N.C.	Internally Connected to IN2. Do not connect to this pin.
D2	T.P.	Test Point. This pin is used internally for factory test. This pin must be either externally connected to AGND or unconnected. This pin has an internal 120kΩ pulldown to AGND.
D3, D4	PAB, PAA	PA Connection for Bypass Mode. Internally connected to IN1_ using the internal bypass MOSFET during bypass mode. PA_ is connected to the internal feedback network. Bypass PA_ with a 4.7µF ceramic capacitor as close as possible to PA_ and PGND.

1.2A PWM Step-Down Converter in 2mm x 2mm WLP/UCSP for PA Power

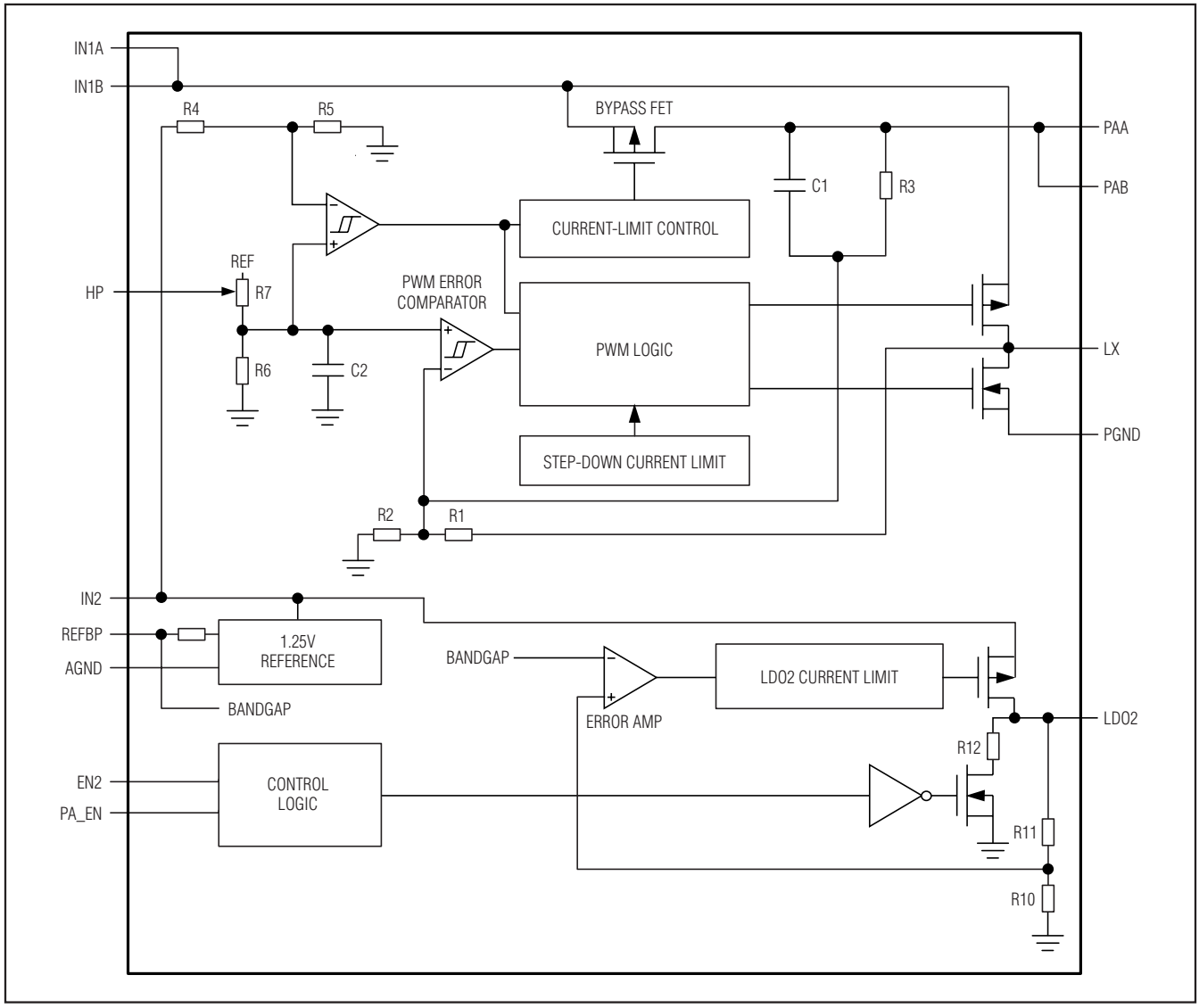


Figure 1. Block Diagram

Detailed Description

The MAX8836Z is designed to provide a fixed output voltage of 3.4V with ultra-low dropout. The device contains a high-frequency, high-efficiency step-down converter, and 200mA low-noise LDO. The step-down converter delivers over 1.2A. The hysteretic PWM control scheme provides extremely fast transient response. A 60mΩ bypass FET connects directly to the battery during high-power transmission.

Step-Down Converter Control Scheme

A hysteretic PWM control scheme ensures high efficiency, fast switching, fast transient response, low-output ripple, and physically tiny external components. The control scheme is simple: when the output voltage is below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch. This high-side switch remains on until the minimum on-time expires and the output voltage is within regulation, or the inductor current is above the current-limit threshold. Once off, the high-side switch remains off until the minimum off-time expires and the output voltage falls again below the regulation threshold. During the off period, the low-side synchronous rectifier turns on and remains on until the high-side switch turns on again. The internal synchronous rectifier eliminates the need for an external Schottky diode.

Voltage-Positioning Load Regulation

The MAX8836Z step-down converter utilizes a unique feedback network. By taking DC feedback from the LX node through R1 in Figure 1, the usual phase lag due to the output capacitor is removed, making the loop exceedingly stable and allowing the use of very small ceramic output capacitors. To improve the load regulation, resistor R3 is included in the feedback. This configuration yields load regulation equal to half of the inductor's series resistance multiplied by the load current. This voltage-positioning load regulation greatly reduces overshoot during load transients or when changing the output voltage from one level to another.

Step-Down Converter Bypass Mode

During high-power transmission, the bypass mode connects IN1A and IN1B directly to PAA and PAB with the internal 60mΩ (typ) bypass FET, while the step-down converter is forced into 100% duty-cycle operation. The low on-resistance in this mode provides low dropout, long battery life, and high output current capability.

Automatic Bypass Mode

Forced bypass mode is automatically invoked when the DC-DC converter operates at more than 99% duty cycle (typ). See Figure 2. Note that IN2 is used instead of IN1 to prevent switching noise from causing false engagement of automatic bypass mode. For this reason, IN2 must be connected to the same source as IN1.

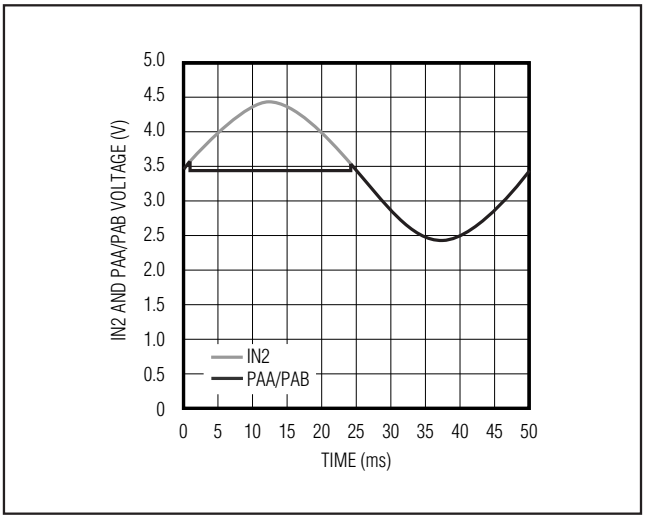


Figure 2. V_{IN2} and $V_{PA_}$ with Automatic Entry/Exit into Bypass Mode

Shutdown Mode

Connect PA_EN to GND or logic-low to place the MAX8836Z PA step-down converter in shutdown mode. In shutdown, the control circuitry, internal switching MOSFET, and synchronous rectifier turn off and LX becomes high impedance. Connect PA_EN to IN1_ or logic-high for normal operation.

Connect EN2 to GND or logic-low to place LDO2 in shutdown mode. In shutdown, the output of the LDO is pulled to ground through an internal 1kΩ resistor.

When the PA step-down and LDO are in shutdown, the MAX8836Z enters a very low power state, where the input current drops to 0.1µA (typ).

Step-Down Converter Soft-Start

The MAX8836Z PA step-down converter has internal soft-start circuitry that limits inrush current at startup, reducing transients on the input source. Soft-start is particularly useful for supplies with high output impedance such as Li+ and alkaline cells. See the PA Step-Down Converter Soft-Start Waveforms in the *Typical Operating Characteristics.*

1.2A PWM Step-Down Converter in 2mm x 2mm WLP/UCSP for PA Power

Thermal Shutdown

Thermal shutdown limits total power dissipation in the MAX8836Z. If the junction temperature exceeds +160°C, thermal-shutdown circuitry turns off the IC, allowing it to cool. The IC turns on and begins soft-start after the junction temperature cools by 20°C. This results in a pulsed output during continuous thermal-overload conditions.

Applications Information

Output Voltages

The MAX8836Z provides a fixed output voltage of 3.4V (HP = 0), or BYPASS mode if duty cycle is higher than 99% (typ).

If HP = 1, the MAX8836Z provides a 3.1V fixed output voltage.

The LDO2 output voltage is factory preset to 2.85V.

LDO Dropout Voltage

The regulator's minimum input/output differential (or dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the MAX8836Z LDO uses a p-channel MOSFET pass transistor, the dropout voltage is a function of drain-to-source on-resistance ($R_{DS(ON)}$) multiplied by the load current (see the *Typical Operating Characteristics*).

Inductor Selection

The MAX8836Z operates with a switching frequency of 1.6MHz and utilizes a 2.2µH inductor. The switching frequency of the MAX8836Z results in great efficiency with a physically small inductor. See the *Typical Operating Characteristics* for efficiency graphs.

The inductor's DC current rating only needs to match the maximum load of the application because the MAX8836Z features zero current overshoot during start-up and load transients. For optimum transient response and high efficiency, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. See Table 1 for suggested inductors and manufacturers.

Output Capacitor Selection

For the PA step-down converter, the output capacitor (C_{PA}) is required to keep the output voltage ripple small and ensure regulation loop stability. C_{PA} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. A 4.7µF capacitor is recommended for most applications. For optimum load-transient performance and very low output ripple, the output capacitor value can be increased.

For LDO2, the minimum output capacitance required is dependent on the load currents. For loads less than 10mA, it is sufficient to use a 0.1µF capacitor for stable operation over the full temperature range. With rated maximum load currents, a minimum of 1µF is recommended. Reduce output noise and improve load-transient response, stability, and power-supply rejection by using larger output capacitors.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it is necessary to use 2.2µF or larger to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, 1µF is sufficient at all operating temperatures. These regulators are optimized for ceramic capacitors. Tantalum capacitors are not recommended.

Input Capacitor Selection

The input capacitor (C_{IN1}) of the PA converter reduces the current peaks drawn from the battery or input power source and reduces switching noise in the MAX8836Z. The impedance of C_{IN1} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. A 4.7µF capacitor is recommended for most applications. For optimum noise immunity and low input ripple, the input capacitor value can be increased.

Table 1. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (Ω)	CURRENT RATING (mA)	DIMENSIONS (mm)
Coilcraft	LPO3310	1.0 1.5 2.2	0.07 0.10 0.13	1600 1400 1100	3.3 x 3.3 x 1.0 = 11mm^3
FDK	MIPF2520	1.0 1.5 2.2	0.05 0.07 0.08	1500 1500 1300	2.5 x 2.0 x 1.0 = 5mm^3
	MIPS2520	1.3 2.0	0.09 0.11	1500 1200	2.5 x 2.0 x 1.0 = 5mm^3
	MIPF2016	1.0 2.2	0.11	1100	2.0 x 1.6 x 1.0 = 3.2mm^3
Murata	LQH32C_53	1.0 2.2	0.06 0.10	1000 790	3.2 x 2.5 x 1.7 = 14mm^3
Sumida	CDRH2D09	1.2 1.5 2.2	0.08 0.09 0.12	590 520 440	3.0 x 3.0 x 1.0 = 9mm^3
Taiyo Yuden	CDRH2D11	1.5 2.2 3.3	0.05 0.08 0.10	680 580 450	3.2 x 3.2 x 1.2 = 12mm^3
	CB2518T	2.2 4.7	0.09 0.13	510 340	2.5 x 1.8 x 2.0 = 9mm^3
TOKO	D3010FB	1.0	0.20	1170	3.0 x 3.0 x 1.0 = 9mm^3
	D2812C	1.2 2.2	0.09 0.15	860 640	3.0 x 3.0 x 1.2 = 11mm^3
	D310F	1.5 2.2	0.13 0.17	1230 1080	3.6 x 3.6 x 1.0 = 13mm^3
	D312C	1.5 2.2	0.10 0.12	1290 1140	3.6 x 3.6 x 1.2 = 16mm^3

For the LDO, use an input capacitance equal to the value of the output capacitance of LDO2. Larger input capacitor values and lower ESR provide better noise rejection and line-transient response.

Note that some ceramic dielectrics exhibit large capacitance and ESR variation with temperature. With dielectrics such as Z5U and Y5V, it may be necessary to use two times the output capacitor value of LDO2 (or larger) to ensure stability at temperatures below -10°C. With X7R or X5R dielectrics, a capacitance equal to the output capacitor value is sufficient at all operating temperatures.

Thermal Considerations

In most applications, the MAX8836Z does not dissipate much heat due to the high efficiency. However, in applications where the MAX8836Z operates at high ambient temperature with heavy loads, the heat dissipated may exceed the maximum junction temperature of the IC. If the junction temperature reaches approximately +160°C, all power switches are turned off and LX and PA_ become high impedance, and LDO2 is pulled down to ground through an internal 1kΩ pull-down resistor.

1.2A PWM Step-Down Converter in 2mm x 2mm WLP/UCSP for PA Power

The MAX8836Z maximum power dissipation depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipated in the device is:

$$P_{DISS} = P_{PA} \times (1/\eta_{PA} - 1) + I_{LDO2} \times (V_{IN2} - V_{LDO2})$$

where η_{PA} is the efficiency of the PA step-down converter and P_{PA} is the output power of the PA step-down converter.

The maximum allowed power dissipation is:

$$P_{MAX} = (T_{JMAX} - T_A)/\theta_{JA}$$

where $(T_{JMAX} - T_A)$ is the temperature difference between the MAX8836Z die junction and the surrounding air; θ_{JA} is the thermal resistance of the junction through the PCB, copper traces, and other materials to the surrounding air.

PCB Layout

High switching frequencies and relatively large peak currents make the PCB layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, resulting in a stable and well-regulated output. Connect C_{IN1} close to IN1A/IN1B and PGND. Connect the inductor and output capacitor as close as possible to the IC and keep their traces short, direct, and wide. Keep noisy traces, such as the LX node, as short as possible. Figure 3 illustrates an example PCB layout and routing scheme. Note that Figure 3 does not show the common ground plane connection of AGND and PGND. Refer to the MAX8805W Evaluation Kit for more information.

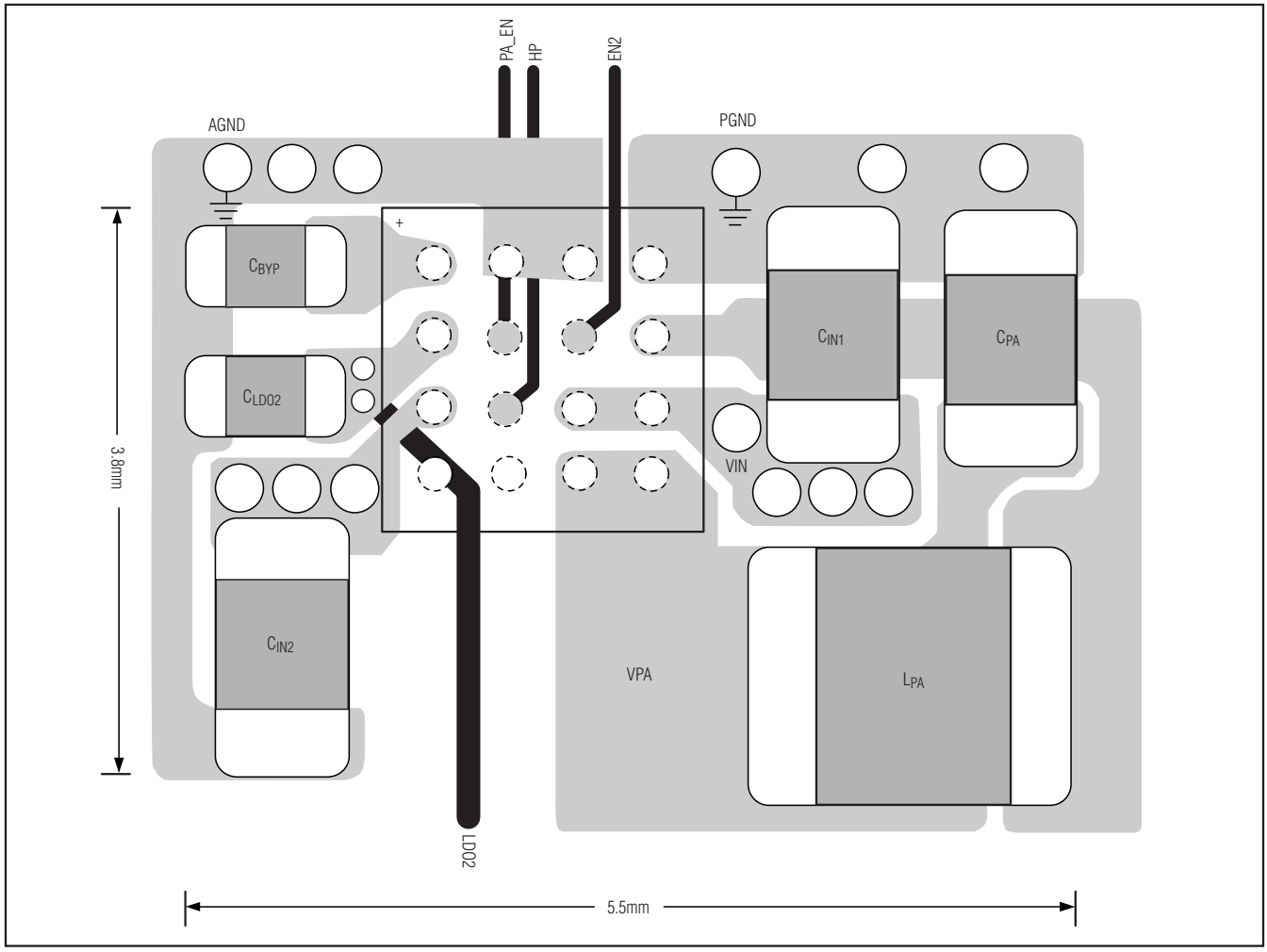


Figure 3. Recommended PCB Layout

1.2A PWM Step-Down Converter in 2mm x 2mm WLP/UCSP for PA Power

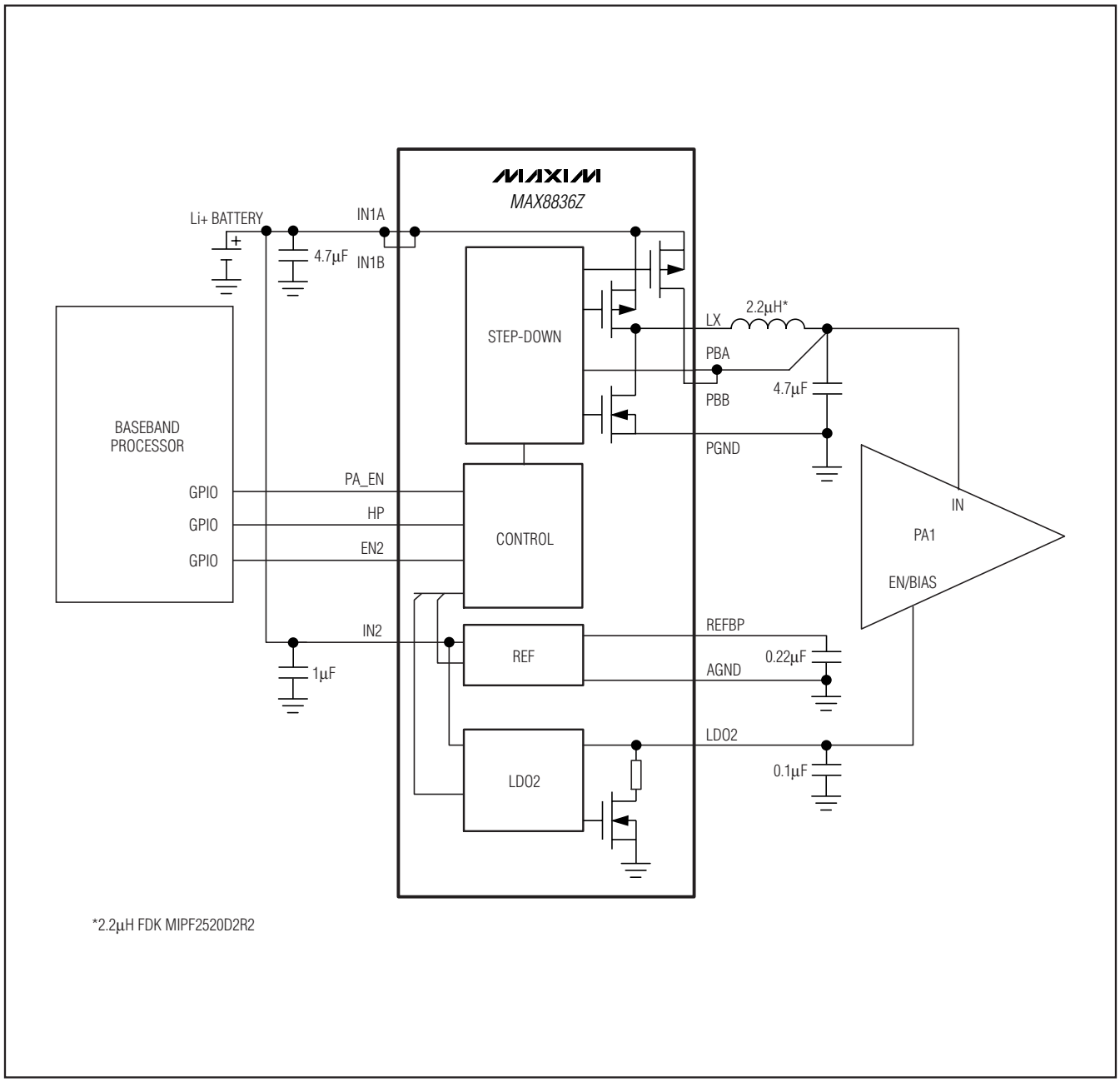


Figure 4. Typical Application Circuit Using LDO for PA Enable/Bias

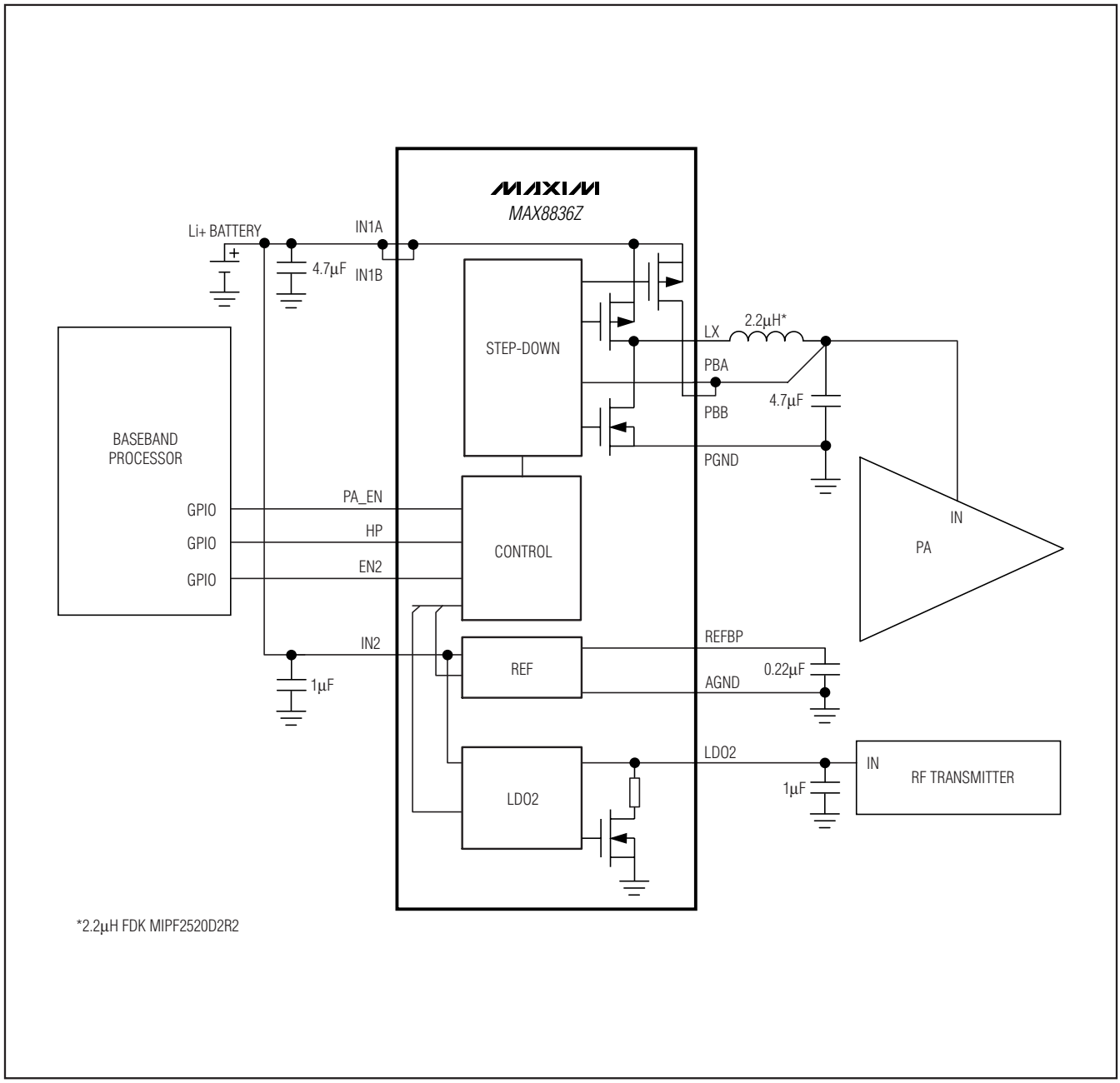
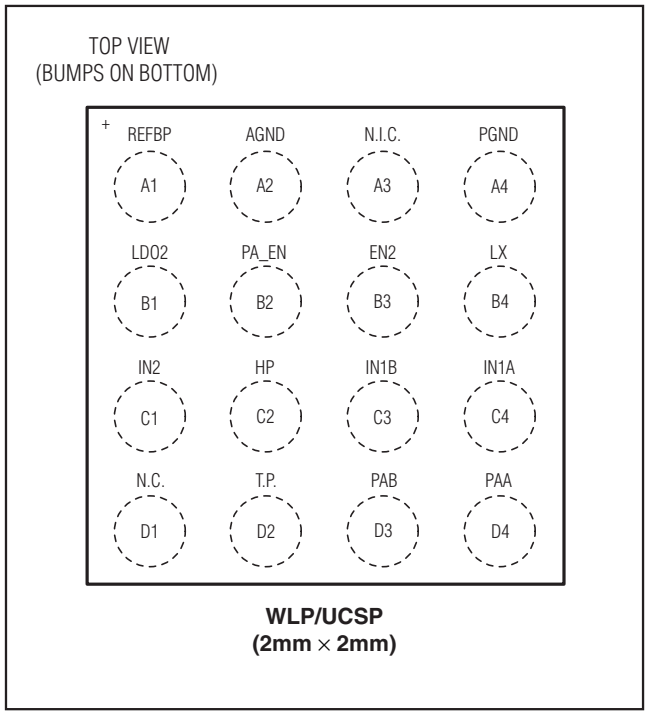


Figure 5. Typical Application Circuit Using LDO for RF Power

1.2A PWM Step-Down Converter in 2mm x 2mm WLP/UCSP for PA Power

Pin Configuration



WLP/UCSP
(2mm × 2mm)

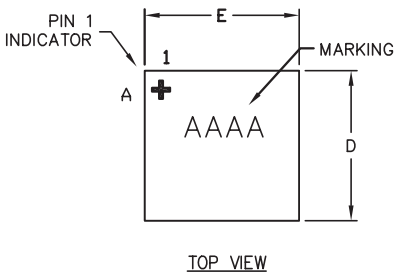
Chip Information

PROCESS: BiCMOS

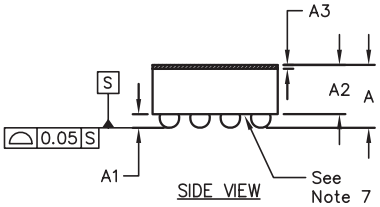
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
16 UCSP	R162A2+1	**21-0226**
16 WLP	W162B2+1	**21-0200**

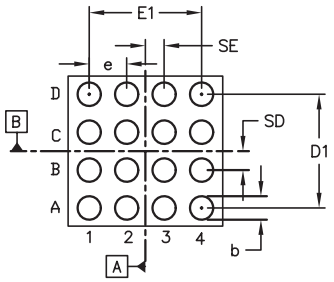


TOP VIEW



SIDE VIEW

COMMON DIMENSIONS	
A	0.64±0.05
A1	0.24±0.03
A2	0.40 REF
A3	0.025 BASIC
b	ø0.31±0.03
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC



BOTTOM VIEW

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W162B2+1	1.98	2.11	1.98	2.11	NONE
W162C2+1	2.12	2.26	1.99	2.13	NONE
W162D2+1	1.99	2.01	1.99	2.01	B3, C2

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front–side finish can be either Black or Clear.

MAXIM

TITLE:
PACKAGE OUTLINE
16 BUMPS, WLP PKG. 0.5mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0200	E	1/1

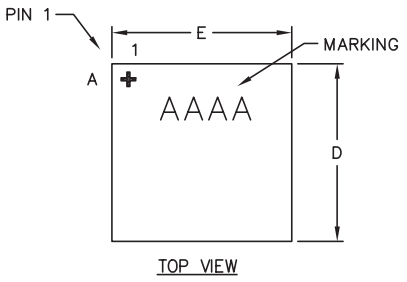
–DRAWING NOT TO SCALE–

1.2A PWM Step-Down Converter in 2mm x 2mm WLP/UCSP for PA Power

Package Information (continued)

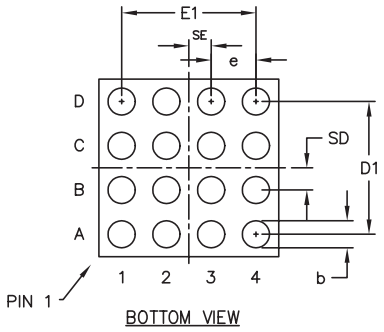
For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

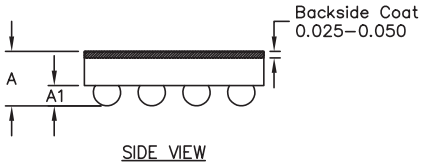
UCSP.EPS



COMMON DIMENSIONS	
A	0.64±0.05
A1	0.24±0.03
b	ø0.30 REF
D1	1.50 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.25 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS				DEPOPULATED BUMPS
	E		D		
	MIN	MAX	MIN	MAX	
R162A2+1	1.98	2.11	1.98	2.11	NONE





NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension (D & E) is defined by center lines between scribe lines.
3. All dimensions in millimeters.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02mm unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.

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MAXIM

TITLE:
PACKAGE OUTLINE
16 BUMPS, 4x4 ARRAY, UCSP (R) PKG.

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0226	B	1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/08	Initial release	—
1	9/08	Added UCSP package option	1, 2, 16

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