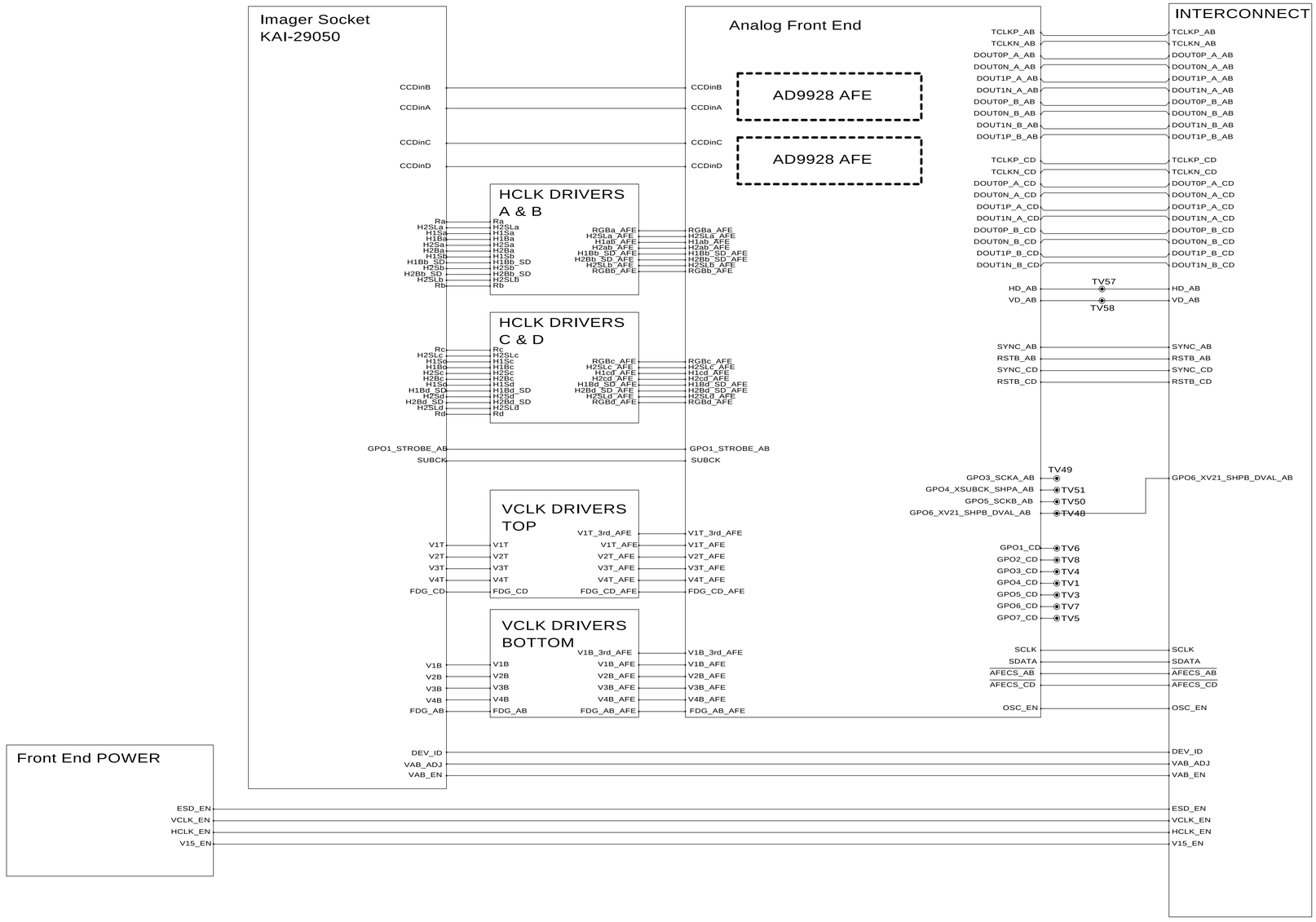
REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL
		Assy 20361640 - Revision 3 See Page 16 VSUB and Electronic Shutter		April 2016



Lens Mounting Holes

N3 N4 N6 N5

FM1
FM2 Pic-n-Place Fids Top
FM3

FM4
FM5 Pic-n-Place Fids Bot
FM6

20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QUANITY REQD	

UNLESS OTHERWISE SPECIFIED
DIM. ARE IN
2 PL DEC TOL ±
3 PL DEC TOL ±
ANGULAR TOL ±
SURF ROUGHNESS
EDGES
INSIDE RADII

MATERIAL

FINISH

DEVIATIONS FROM INTENDED SHAPE
FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.

DIMENSIONS APPLY AFTER FINISH
WHERE TOTAL TOLERANCE OS .001
INCHES OR LESS AND ON ALL
THREADS. IN ALL OTHER PLACES
DIMENSIONS APPLY BEFORE FINISH.

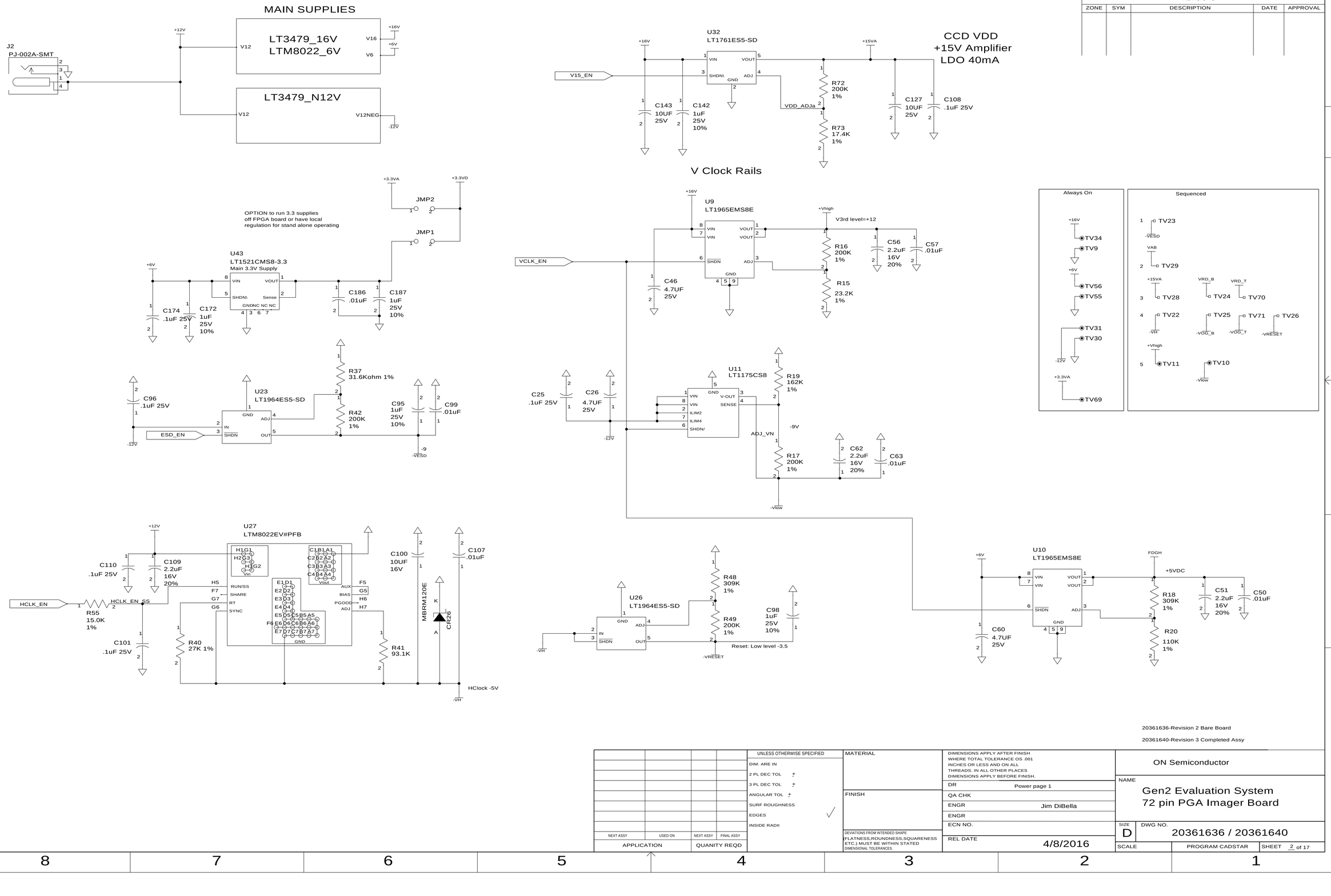
DR Top Level Drawing
QA CHK
ENGR Jim DiBella
ENGR
ECN NO.
REL DATE 4/8/2016

ON Semiconductor

NAME
Gen2 Evaluation System
72 pin PGA Imager Board

SIZE D | DWG NO. 20361636 / 20361640

SCALE | PROGRAM CADSTAR | SHEET 1 of 17



REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL

20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

				UNLESS OTHERWISE SPECIFIED	MATERIAL
				DIM. ARE IN	
				2 PL DEC TOL ±	
				3 PL DEC TOL ±	
				ANGULAR TOL ±	FINISH
				SURF ROUGHNESS	
				EDGES ✓	
				INSIDE RADII	
NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY		DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.
APPLICATION		QUANITY REQD			

DIMENSIONS APPLY AFTER FINISH
WHERE TOTAL TOLERANCE OS .001
INCHES OR LESS AND ON ALL
THREADS. IN ALL OTHER PLACES
DIMENSIONS APPLY BEFORE FINISH.

DR	Power page 1
QA CHK	
ENGR	Jim DiBella
ENGR	
ECN NO.	
REL DATE	4/8/2016

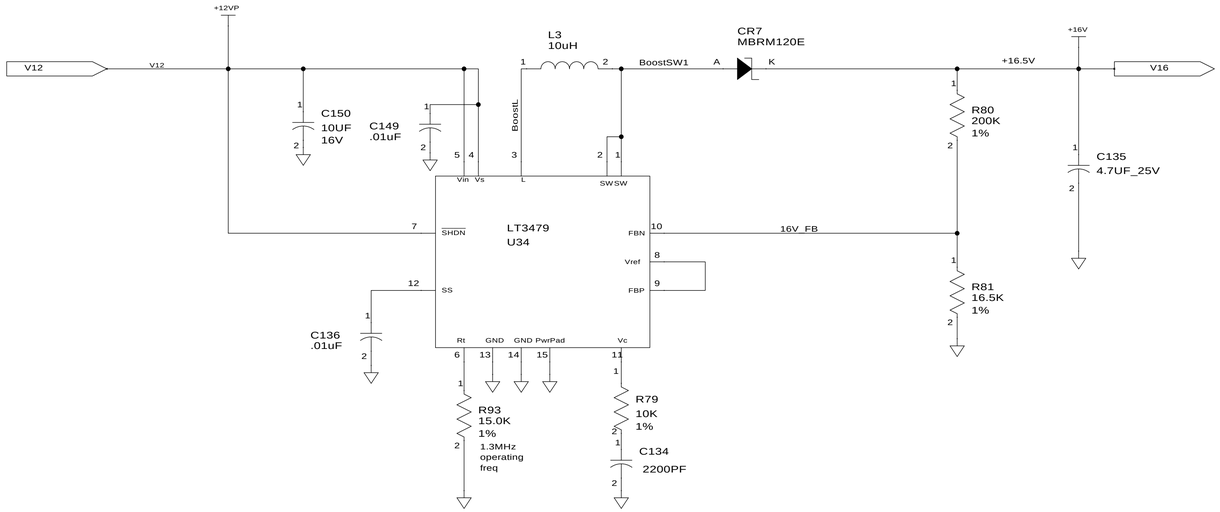
ON Semiconductor

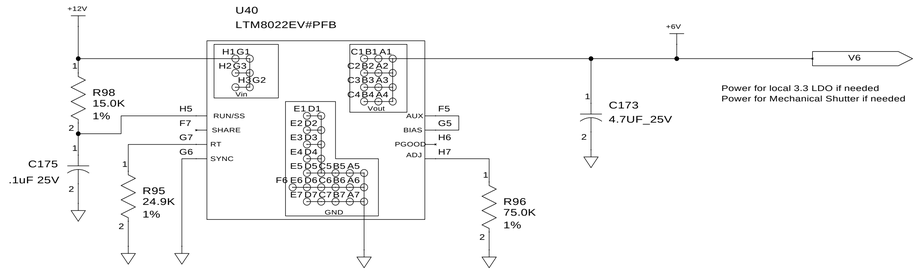
NAME

Gen2 Evaluation System
72 pin PGA Imager Board

SIZE	DWG NO.
D	20361636 / 20361640
SCALE	PROGRAM CADSTAR
SHEET 2 of 17	

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL





20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY	APPLICATION	QUANITY REQD		

UNLESS OTHERWISE SPECIFIED

DIM. ARE IN

2 PL DEC TOL ±

3 PL DEC TOL ±

ANGULAR TOL ±

SURF ROUGHNESS

EDGES

INSIDE RADII

MATERIAL

FINISH

DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.

DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE OS .001
INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.

DR Power page 2 LT3471

QA CHK

ENGR Jim DiBella

ENGR

ECN NO.

REL DATE 4/8/2016

ON Semiconductor

NAME

Gen2 Evaluation System
72 pin PGA Imager Board

SIZE D

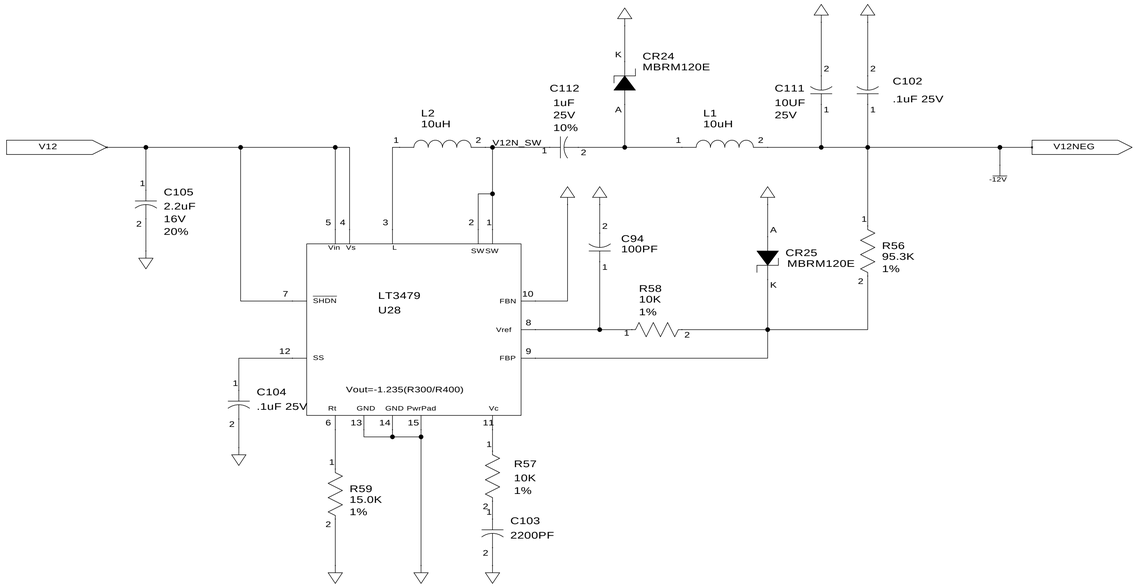
DWG NO. 20361636 / 20361640

SCALE

PROGRAM CADSTAR

SHEET 3 of 17

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL



20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QUANITY REQD	

UNLESS OTHERWISE SPECIFIED
DIM. ARE IN
2 PL DEC TOL ±
3 PL DEC TOL ±
ANGULAR TOL ±
SURF ROUGHNESS
EDGES
INSIDE RADII

MATERIAL

FINISH

DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.

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DR Power page 3 LT3479
QA CHK
ENGR Jim DiBella
ENGR
ECN NO.
REL DATE 4/8/2016

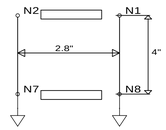
ON Semiconductor

NAME
Gen2 Evaluation System
72 pin PGA Imager Board

SIZE D | DWG NO. 20361636 / 20361640

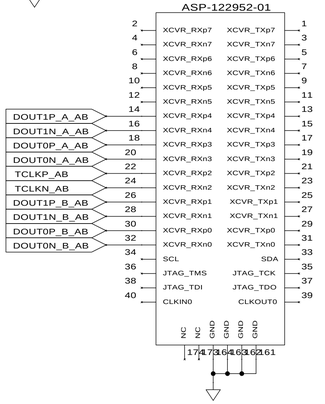
SCALE | PROGRAM CADSTAR | SHEET 4 of 17

B-B Connector Spacing 4"
B-B Mounting posts per Altera HSMC Spec

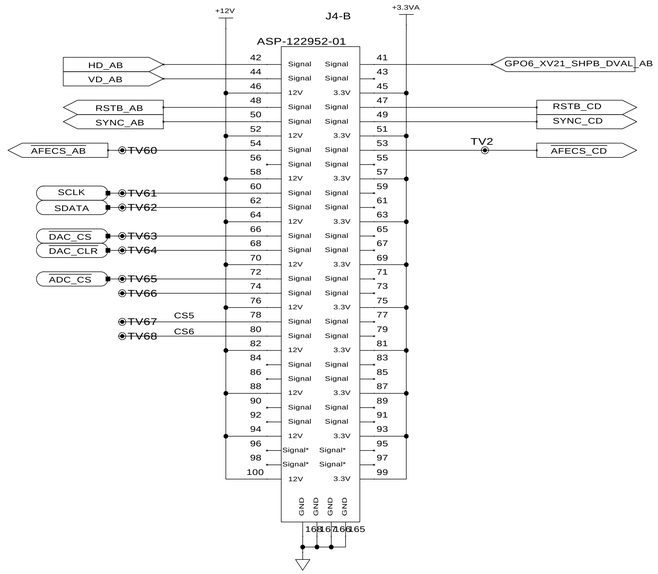


REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL

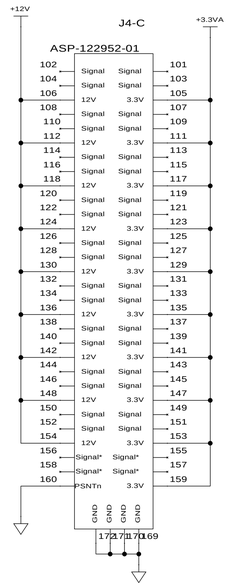
J4-A

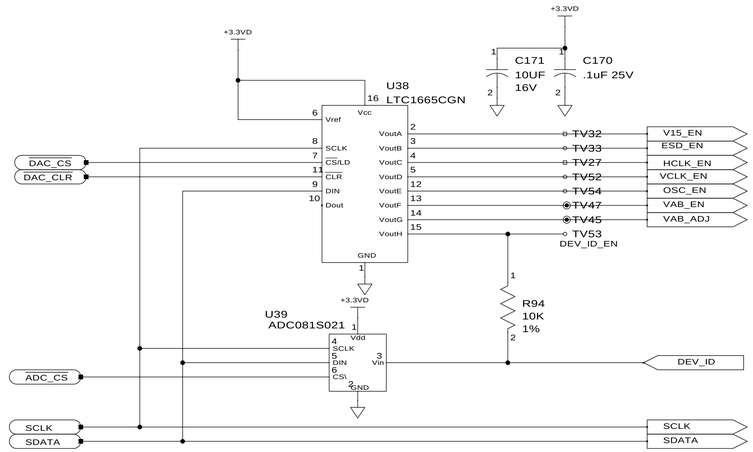


J4-B

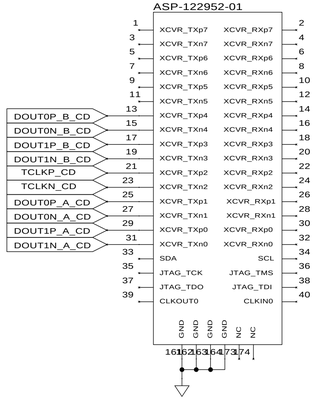


J4-C

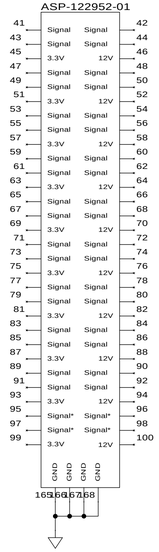




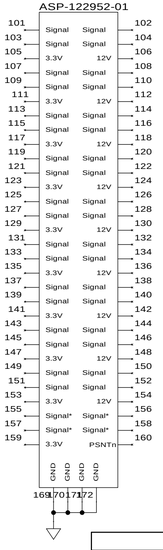
J1-A



J1-B



J1-C



20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

				UNLESS OTHERWISE SPECIFIED	MATERIAL
				DIM. ARE IN	
				2 PL DEC TOL ±	
				3 PL DEC TOL ±	
				ANGULAR TOL ±	FINISH
				SURF ROUGHNESS	
				EDGES ✓	
				INSIDE RADII	
NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY		DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.
APPLICATION		QUANITY REQD			

DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE OS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.

ON Semiconductor

DR Board to Board Interconnect

QA CHK

ENGR Jim DiBella

ENGR

ECN NO.

REL DATE 4/8/2016

NAME
Gen2 Evaluation System
72 pin PGA Imager Board

SIZE D | DWG NO. 20361636 / 20361640

SCALE | PROGRAM CADSTAR | SHEET 5 of 17

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL

AD Conversion Channel A,B

CCDinA
CCDinB

TCLKP_AB
TCLKN_AB
DOUT0P_A_AB
DOUT0N_A_AB
DOUT1P_A_AB
DOUT1N_A_AB
DOUT0P_B_AB
DOUT0N_B_AB
DOUT1P_B_AB
DOUT1N_B_AB

AD Conversion Channel C,D

CCDinC
CCDinD

TCLKP_CD
TCLKN_CD
DOUT0P_A_CD
DOUT0N_A_CD
DOUT1P_A_CD
DOUT1N_A_CD
DOUT0P_B_CD
DOUT0N_B_CD
DOUT1P_B_CD
DOUT1N_B_CD

Timing Horizontal_Clocks GIO

HD_AB
VD_AB
SCLK
SDATA
AFECS_AB
AFECS_CD
SYNC_AB
SYNC_CD
RSTB_AB
RSTB_CD
GPO1_STROBE_AB
GPO2_MSHUT_AB
GPO3_SCKA_AB
GPO4_XSUBCK_SHPA_AB
GPO5_SCKB_AB
GPO6_XV21_SHPB_DVAL_AB
GPO7_XV23_VDR_EN_AB
GPO1_CD
GPO2_CD
GPO3_CD
GPO4_CD
GPO5_CD
GPO6_CD
GPO7_CD
AFE_CLOCK_AB
AFE_CLOCK_CD

RGBa_AFE
H2SLa_AFE
H1ab_AFE
H2ab_AFE
H1Bb_SD_AFE
H2Bb_SD_AFE
H2SLb_AFE
RGBb_AFE

Change Phase to support Single or Dual clocking

Use Mode 3 Configuration
H1A=H3A=/H2A=/H4A
H1B=H3B=/H2B=/H4B

RGBc_AFE
H2SLc_AFE
H1cd_AFE
H2cd_AFE
H1Bd_SD_AFE
H2Bd_SD_AFE
H2SLd_AFE
RGBd_AFE

Change Phase to support Single or Dual clocking

Use Mode 3 Configuration
H1A=H3A=/H2A=/H4A
H1B=H3B=/H2B=/H4B

+3.3VD
OSC_VDD
BD1
BLM18AG601SN1D
C106
.1uF 25V
U25
40.0 MHZ
VCC
EN
OUT
GND
OSC_EN
U24-B
C97
.1uF 25V
74LVC2G04DBVR
U24-A
74LVC2G04DBVR

TV59

74LVC2G04DBVR
U42-B
U42-A
1=S1
0=S2

BUFFERED USER ACCESS TO SIGNALS
CONTROL OF THESE SIGNALS IS PROGRAMMED
THROUGH THE AFE

104363-4
J3
+6V
R101
15.0K
1%
R100
15.0K
1%
Q2
3904
U44
ZXMD63C03X
PFET
NFET
S2
S1

Vertical Clocks

GPO7_XV23_VDR_EN_AB

V1B_3rd_AFE
V1B_AFE
V2B_AFE
V3B_AFE
V4B_AFE
V1T_3rd_AFE
V1T_AFE
V2T_AFE
V3T_AFE
V4T_AFE
SUBCK
FDG_AB_AFE
FDG_CD_AFE

TV46

20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY	APPLICATION	QUANITY REQD

UNLESS OTHERWISE SPECIFIED
DIM. ARE IN
2 PL DEC TOL ±
3 PL DEC TOL ±
ANGULAR TOL ±
SURF ROUGHNESS
EDGES
INSIDE RADII

MATERIAL

FINISH

DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.

DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE OS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.

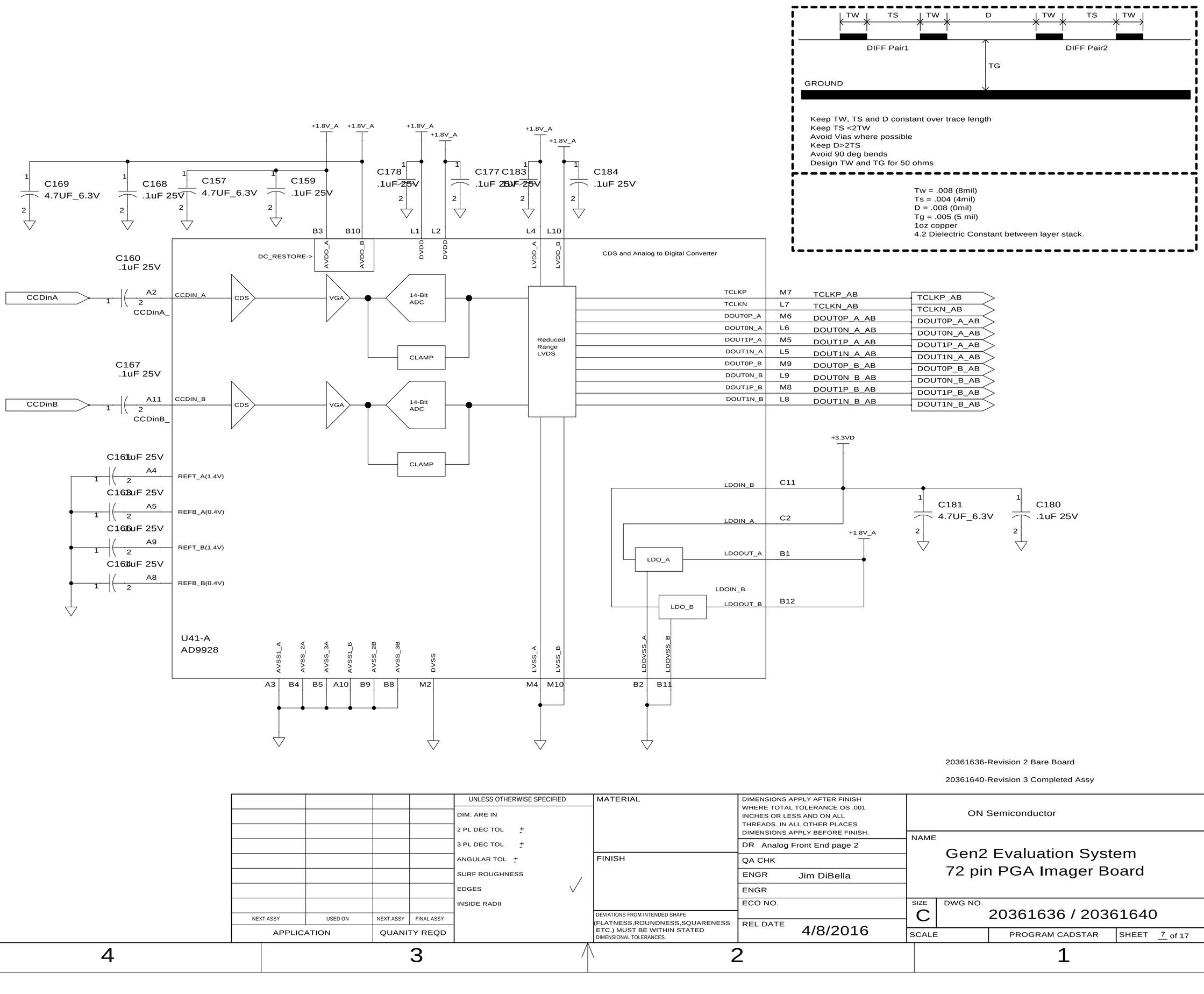
DR Analog Front End page 1
QA CHK
ENGR Jim DiBella
ENGR
ECN NO.
REL DATE 4/8/2016

ON Semiconductor

NAME
Gen2 Evaluation System
72 pin PGA Imager Board

SIZE D | DWG NO. 20361636 / 20361640

SCALE | PROGRAM CADSTAR | SHEET 6 of 17



20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QUANITY REQD	

UNLESS OTHERWISE SPECIFIED
DIM. ARE IN
2 PL DEC TOL ±
3 PL DEC TOL ±
ANGULAR TOL ±
SURF ROUGHNESS
EDGES
INSIDE RADII

MATERIAL

FINISH

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DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE OS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.

DR Analog Front End page 2

QA CHK

ENGR Jim DiBella

ENGR

ECO NO.

REL DATE 4/8/2016

ON Semiconductor

NAME

Gen2 Evaluation System
72 pin PGA Imager Board

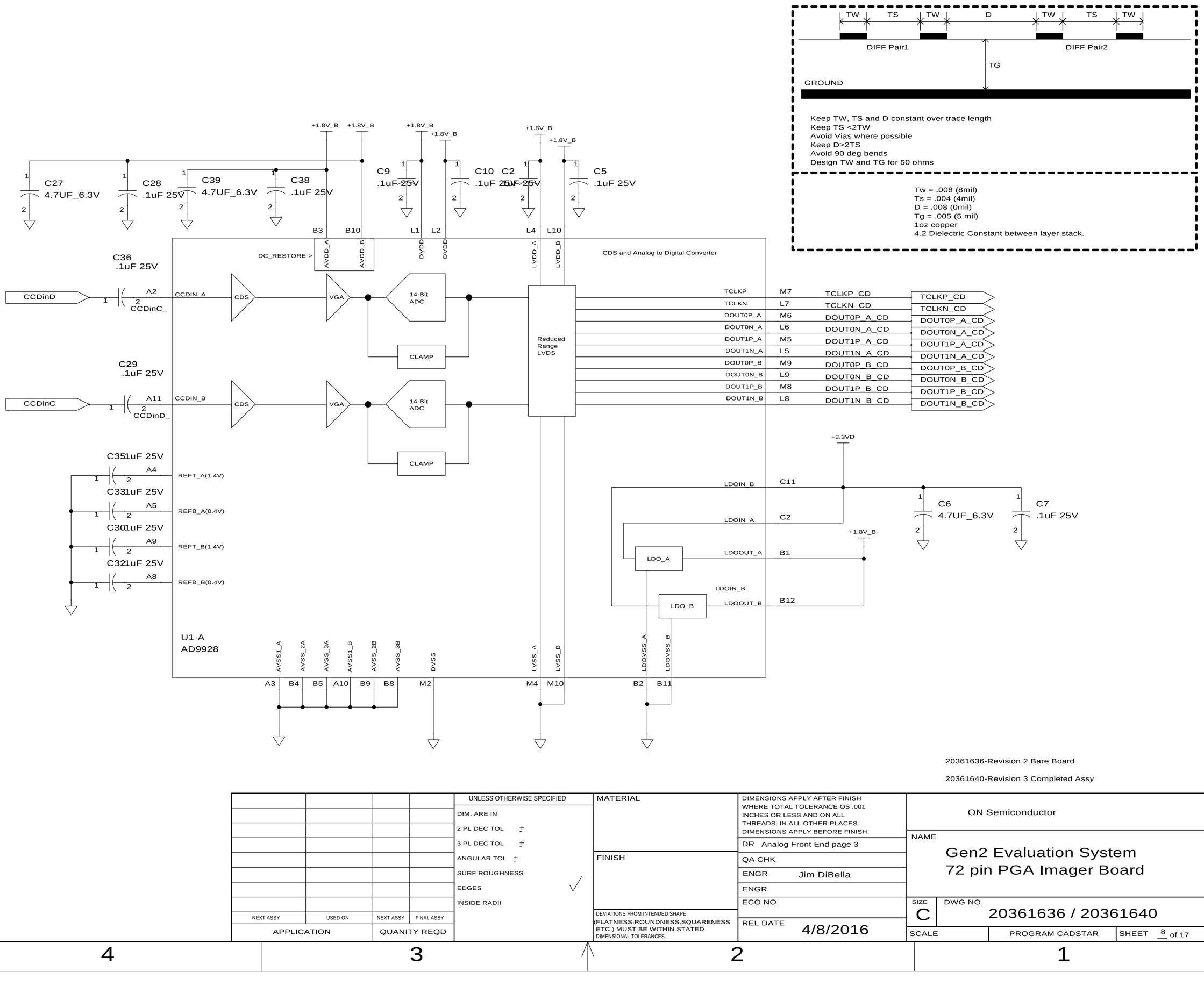
SIZE C

DWG NO. 20361636 / 20361640

SCALE

PROGRAM CADSTAR

SHEET 7 of 17



20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QUANITY REQD	

UNLESS OTHERWISE SPECIFIED
DIM. ARE IN
2 PL DEC TOL ±
3 PL DEC TOL ±
ANGULAR TOL ±
SURF ROUGHNESS
EDGES
INSIDE RADII

MATERIAL

FINISH

DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.

DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE OS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.

DR Analog Front End page 3

QA CHK

ENGR Jim DiBella

ENGR

ECO NO.

REL DATE 4/8/2016

ON Semiconductor

NAME

Gen2 Evaluation System
72 pin PGA Imager Board

SIZE C

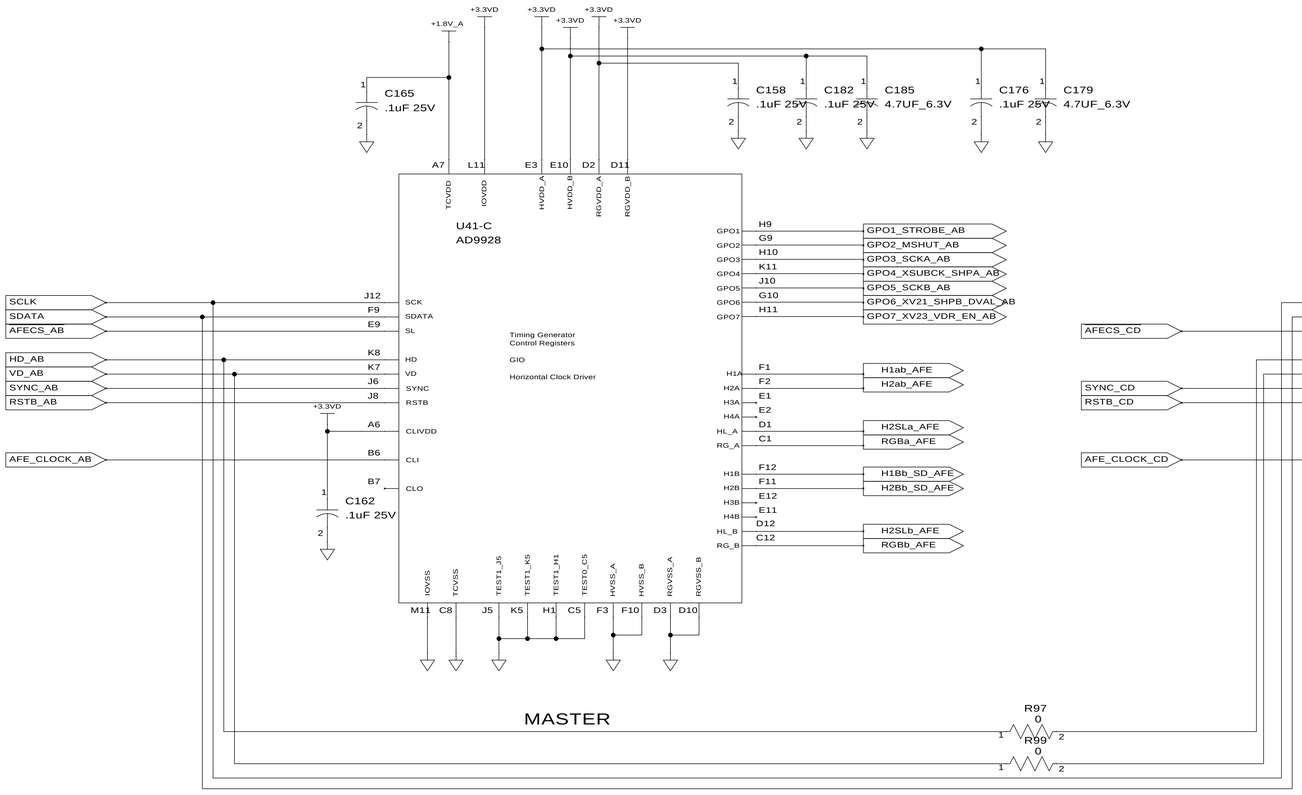
DWG NO. 20361636 / 20361640

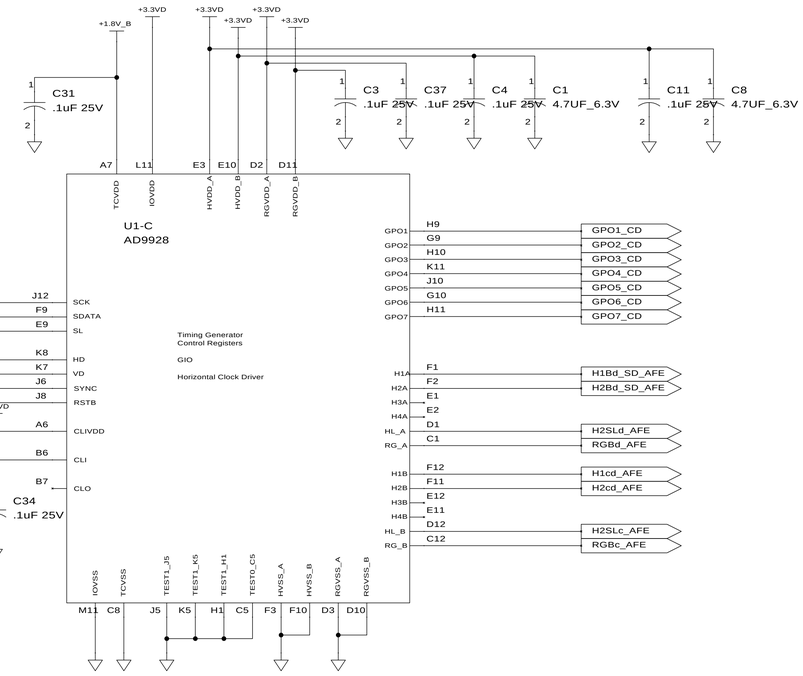
SCALE

PROGRAM CADSTAR

SHEET 8 of 17

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL





20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

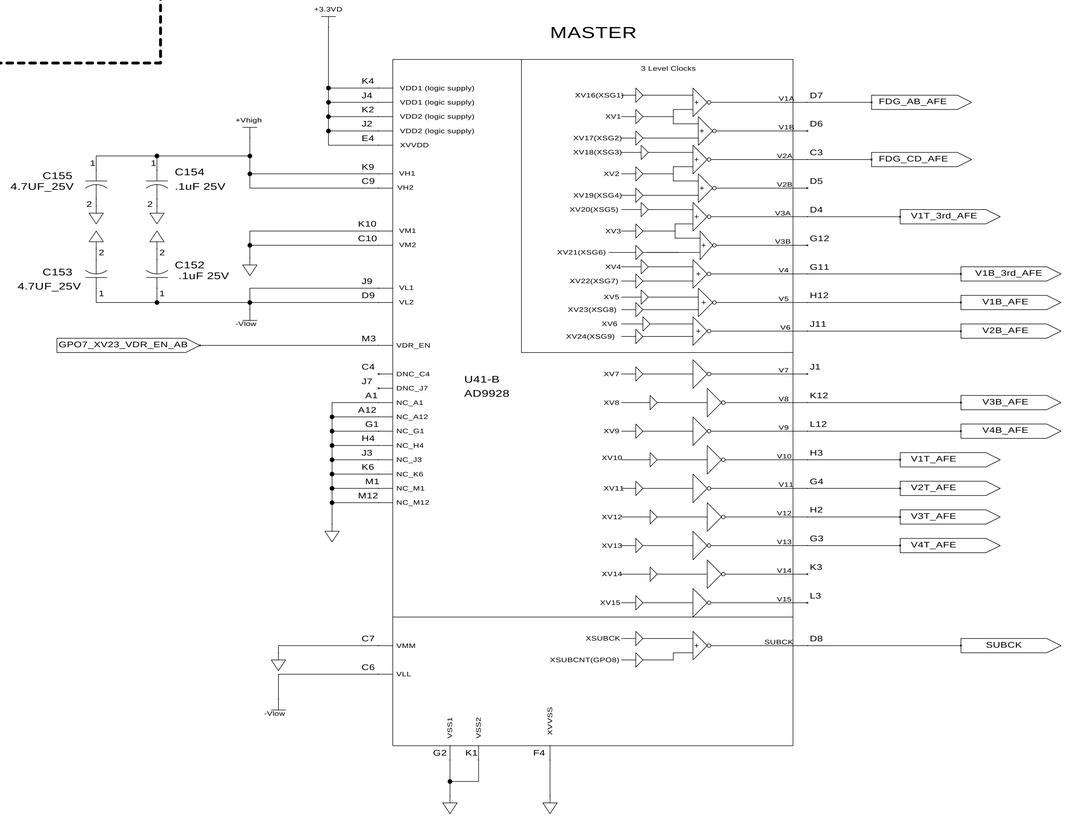
				UNLESS OTHERWISE SPECIFIED	MATERIAL	DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE OS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.	ON Semiconductor
				DIM. ARE IN		DR Analog Front End page 4	NAME
				2 PL DEC TOL ±	FINISH	QA CHK	Gen2 Evaluation System 72 pin PGA Imager Board
				3 PL DEC TOL ±		ENGR Jim DiBella	
				ANGULAR TOL ±		ENGR	SIZE D / DWG NO. 20361636 / 20361640
				SURF ROUGHNESS		ECN NO.	
				EDGES ✓	DEVIATIONS FROM INTENDED SHAPE FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.	REL DATE 4/8/2016	SCALE / PROGRAM CADSTAR / SHEET 9 of 17
				INSIDE RADII			
NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY				
APPLICATION		QUANITY REQD					

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL

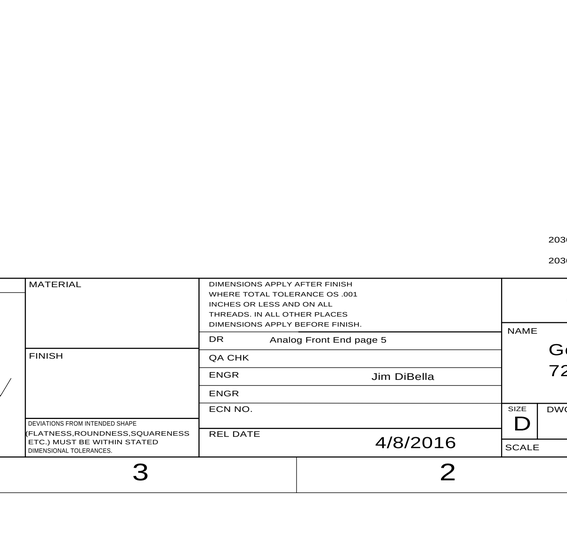
For 3V logic levels of V clock outputs
Set:
Vh to > 8VDC
Vm to +3.3
Vl to 0VDC

Use GIO for Sub Clock

MASTER



SLAVE



20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

				UNLESS OTHERWISE SPECIFIED	MATERIAL
				DIM. ARE IN	
				2 PL DEC TOL ±	
				3 PL DEC TOL ±	
				ANGULAR TOL ±	FINISH
				SURF ROUGHNESS	
				EDGES √	
				INSIDE RADII	
NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY		DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.
APPLICATION		QUANITY REQD			

DIMENSIONS APPLY AFTER FINISH
WHERE TOTAL TOLERANCE OS .001
INCHES OR LESS AND ON ALL
THREADS, IN ALL OTHER PLACES
DIMENSIONS APPLY BEFORE FINISH.

DR Analog Front End page 5

QA CHK

ENGR Jim DiBella

ENGR

ECN NO.

REL DATE 4/8/2016

ON Semiconductor

NAME
Gen2 Evaluation System
72 pin PGA Imager Board

SIZE D | DWG NO. 20361636 / 20361640

SCALE | PROGRAM CADSTAR | SHEET 10 of 17

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL

H1Bb_SD_AFE — TV41 — C121 .1uF 25V — R65 200K 1% — CR4-A HSMS-2805 (K1, A1)

H2Bb_SD_AFE — TV42 — C122 .1uF 25V — R66 200K 1% — CR4-B HSMS-2805 (K2, A2)

H2SLb_AFE — TV43 — C123 .1uF 25V — H2SLb_in — R67 200K 1% — CR5-A HSMS-2805 (K1, A1)

RGBb_AFE — TV44 — C125 .1uF 25V — RGBb_in — R69 200K 1% — CR5-B HSMS-2805 (K2, A2)

RGBa_AFE — TV35 — C114 .1uF 25V — RGBa_in — R60 200K 1% — CR2-A HSMS-2805 (K1, A1)

H2SLa_AFE — TV36 — C116 .1uF 25V — H2SLa_in — R62 200K 1% — CR2-B HSMS-2805 (K2, A2)

H2ab_AFE — TV37 — C117 .1uF 25V — R63 200K 1% — CR3-A HSMS-2805 (K1, A1)

H1ab_AFE — TV38 — C118 .1uF 25V — R64 200K 1% — CR3-B HSMS-2805 (K2, A2)

TV40, TV39

U31 74LCX541BQX — VCC — GND — PPAD — C113 .1uF 25V

U30 74LCX541BQX — VCC — GND — PPAD — C86 .1uF 25V

U29 74LCX541BQX — VCC — GND — PPAD — C119 .1uF 25V

H2SLb, H2Bb_SD, H1Bb_SD, H1Sb, H2Sb, H2Sa, H1Sa, H1Ba, H2Ba, H2SLa

C124 .1uF 25V — RESET CLOCKS NEED TO BE LEVEL SHIFTED — Rb — R68 200K 1% — CR13-A HSMS-2805 (K1, A1) — -VRESET

C115 .1uF 25V — RESET CLOCKS NEED TO BE LEVEL SHIFTED — Ra — R61 200K 1% — CR14-B HSMS-2805 (K2, A2) — -VRESET

Single
H1_AFE = H1SL,H1BL,H1SR,H2BR*
H2_AFE = H2SL,H2BL,H2SR,H1BR*

Dual
H1_AFE = H1SL,H1BL,H1SR,H1BR*
H2_AFE = H2SL,H2BL,H2SR,H2BR*

20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY		
APPLICATION		QUANITY REQD			

UNLESS OTHERWISE SPECIFIED
DIM. ARE IN
2 PL DEC TOL ±
3 PL DEC TOL ±
ANGULAR TOL ±
SURF ROUGHNESS
EDGES
INSIDE RADII

MATERIAL

FINISH

DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.

DIMENSIONS APPLY AFTER FINISH
WHERE TOTAL TOLERANCE OS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.

DR AB Hclock drivers
QA CHK
ENGR Jim DiBella
ENGR
ECN NO.
REL DATE 4/8/2016

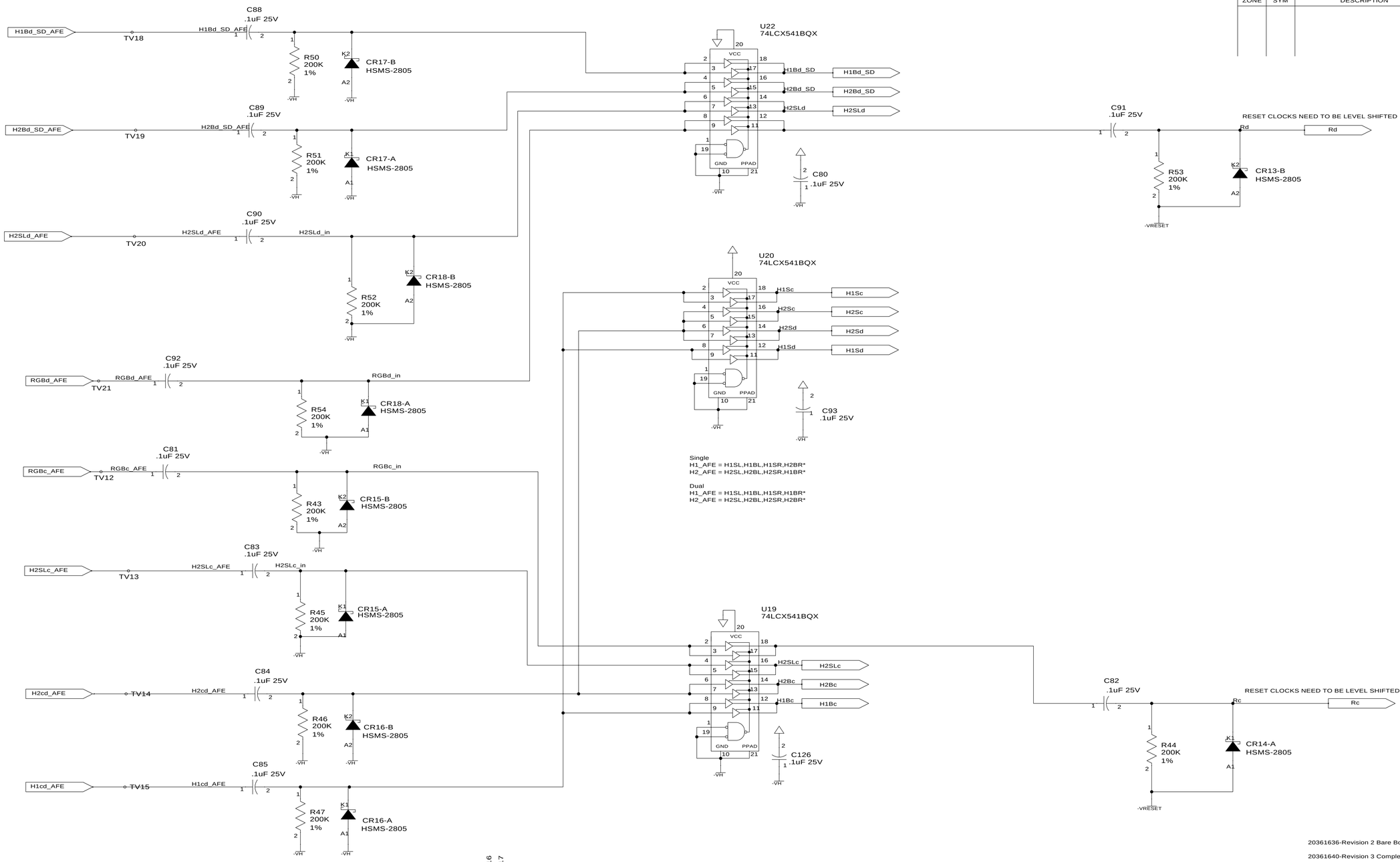
ON Semiconductor

NAME
Gen2 Evaluation System
72 pin PGA Imager Board

SIZE D | DWG NO. 20361636 / 20361640

SCALE | PROGRAM CADSTAR | SHEET 11 of 17

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL



Single
H1_AFE = H1SL,H1BL,H1SR,H2BR*
H2_AFE = H2SL,H2BL,H2SR,H1BR*

Dual
H1_AFE = H1SL,H1BL,H1SR,H1BR*
H2_AFE = H2SL,H2BL,H2SR,H2BR*

20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QUANITY REQD	

UNLESS OTHERWISE SPECIFIED
DIM. ARE IN
2 PL DEC TOL ±
3 PL DEC TOL ±
ANGULAR TOL ±
SURF ROUGHNESS
EDGES
INSIDE RADII

MATERIAL

FINISH

DEVIATIONS FROM INTENDED SHAPE FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.

DIMENSIONS APPLY AFTER FINISH
WHERE TOTAL TOLERANCE OS .001
INCHES OR LESS AND ON ALL
THREADS. IN ALL OTHER PLACES
DIMENSIONS APPLY BEFORE FINISH.

DR CD H Clock Drivers
QA CHK
ENGR Jim DiBella
ENGR
ECN NO.
REL DATE 4/8/2016

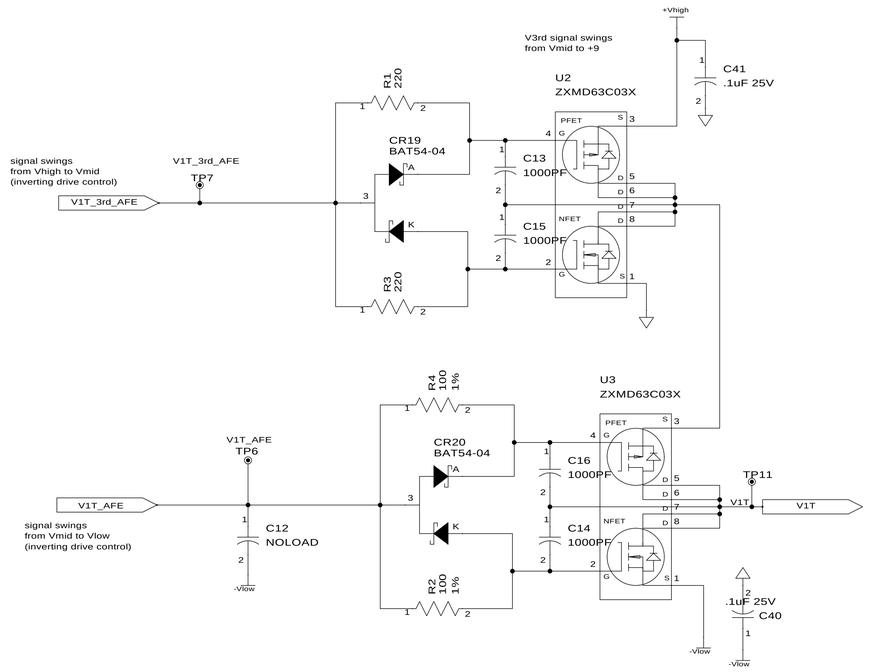
ON Semiconductor

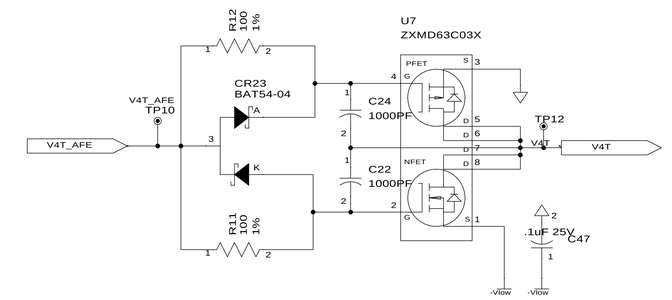
NAME
Gen2 Evaluation System
72 pin PGA Imager Board

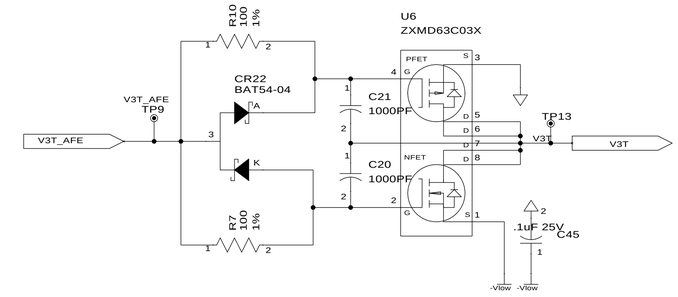
SIZE D | DWG NO. 20361636 / 20361640

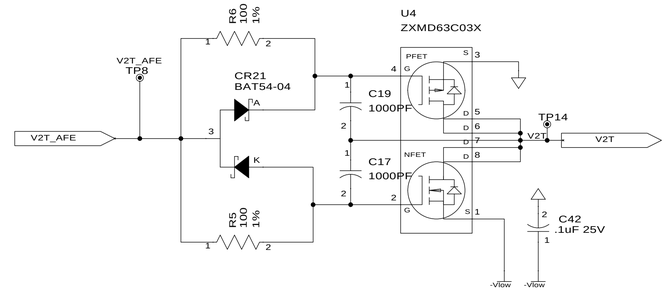
SCALE | PROGRAM CADSTAR | SHEET 12 of 17

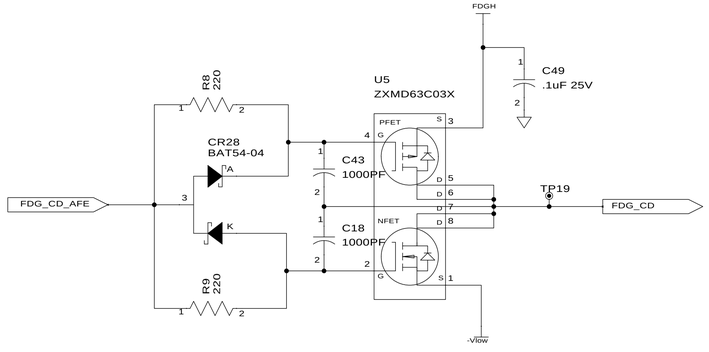
REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL









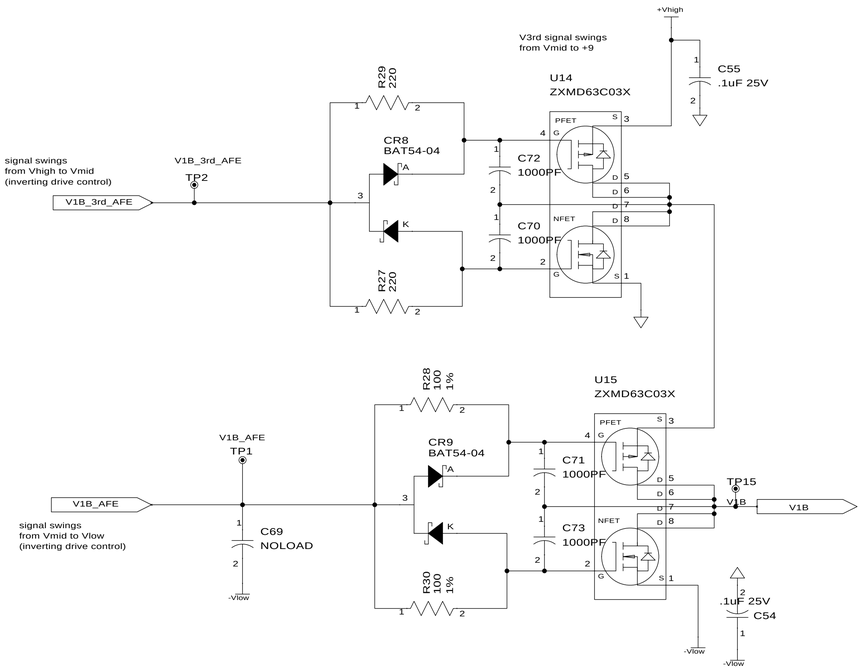


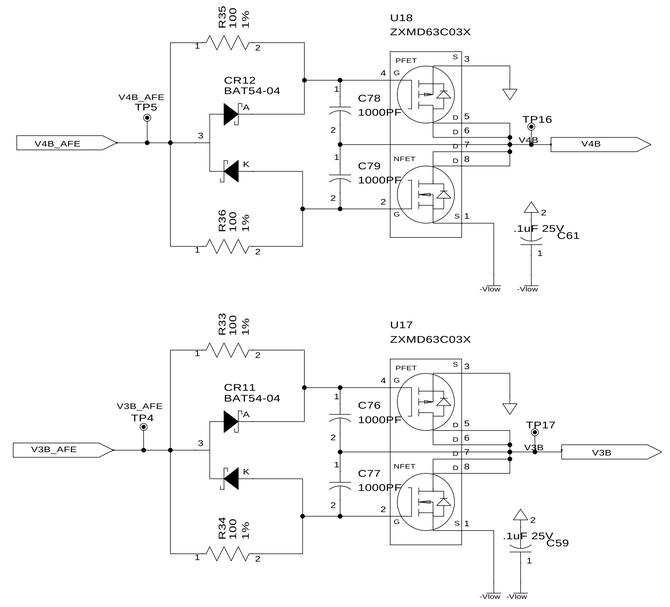
20361636-Revision 2 Bare Board

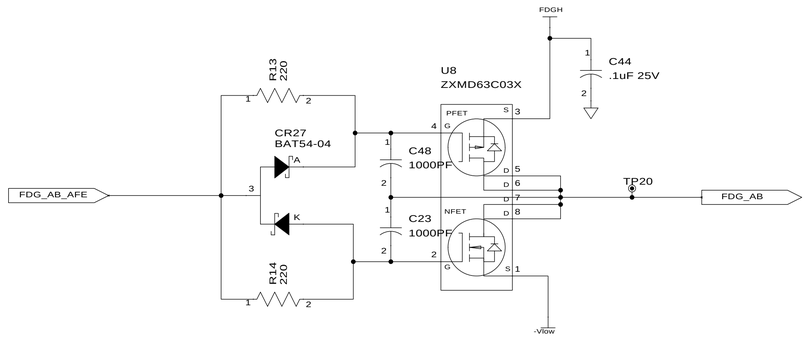
20361640-Revision 3 Completed Assy

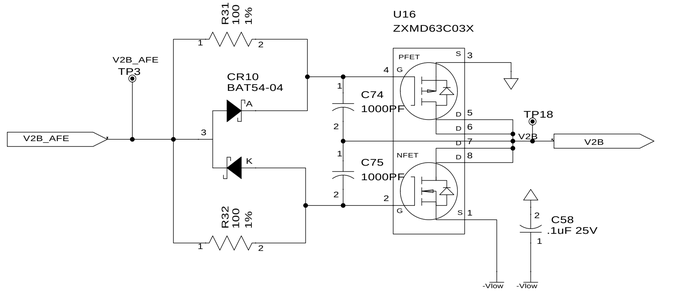
				UNLESS OTHERWISE SPECIFIED	MATERIAL	DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE OS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.	ON Semiconductor
				DIM. ARE IN		DR Top V Clock Drivers	NAME
				2 PL DEC TOL ±	FINISH	QA CHK	Gen2 Evaluation System
				3 PL DEC TOL ±		ENGR Jim DiBella	72 pin PGA Imager Board
				ANGULAR TOL ±		ENGR	SIZE D / DWG NO. 20361636 / 20361640
				SURF ROUGHNESS		ECN NO.	
				EDGES	DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.	REL DATE 4/8/2016	SCALE / PROGRAM CADSTAR / SHEET 13 of 17
				INSIDE RADII			
NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY				
APPLICATION		QUANITY REQD					

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL









20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

				UNLESS OTHERWISE SPECIFIED	MATERIAL	DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE OS .001 INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.	ON Semiconductor
				DIM. ARE IN			
				2 PL DEC TOL ±		DR Bottom V Clock Drivers	NAME Gen2 Evaluation System 72 pin PGA Imager Board
				3 PL DEC TOL ±			
				ANGULAR TOL ±	FINISH	QA CHK	
				SURF ROUGHNESS		ENGR Jim DiBella	
				EDGES ✓		ENGR	
				INSIDE RADII		ECN NO.	SIZE D / DWG NO. 20361636 / 20361640
NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY		DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.	REL DATE 4/8/2016	SCALE / PROGRAM CADSTAR / SHEET 14 of 17
APPLICATION		QUANITY REQD					

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL

VSUB
VAB_ADJ
VAB_EN
SUBCK
GPO1_STROBE_AB
VSUB

Rc
H2SLc
H1Sc
H1Bc
H2Sc
H2Bc
H1Sd
H1Bd_SD
H2Sd
H2Bd_SD
H2SLd
Rd

U21
KAI-29050

Video Outputs
CCDoutC
CCDoutD
CCDinC
CCDinD
CCDinC
CCDinD

+15VA
R24
49.9K
1%
VRD_T
+12VDC
C66
.1uF 25V
R23
200K
1%

C87
.1uF 25V
R39
27K 1%
-VOG_T
-2
R38
39.2K
1%
-VH
-5V

V3T V1T VDDc GND Rc H2SLc H1Bc H2Sc N/C SUB H2Sd H1Bd H2SLd Rd GND VDDd V1T V3T
ESD V4T V2T VOUTc RDc OGc H2Bc H1Sc H1Sd H2Bd OGd RDd VOUTd V2T V4T DevID
-VESD
-VOG_T
FDGcd FDGcd
DEV_ID

FDG_CD
V1T
V2T
V3T
V4T
V1B
V2B
V3B
V4B
FDG_AB

+15VA VRD_B VSUB FDGab FDGab VRD_B +15VA
N/C V4B V2B VOUTA RDa OGa H2Ba H1Sa FDGab FDGab H1Sb H2Bb OGb RDb VOUTb V2B V4B ESD
V3B V1B VDDa GND Ra H2SLa H1Ba H2Sa SUB N/C H2Sb H1Bb H2SLb Rb GND VDDb V1B V3B
-VESD
-VOG_B
-VOG_B

Ra
H2SLa
H1Sa
H1Ba
H2Sa
H2Ba
H1Sb
H1Bb_SD
H2Sb
H2Bb_SD
H2SLb
Rb

CCDoutB
CCDoutA
CCDinB
CCDinA
CCDinB
CCDinA

+15VA
R84
49.9K
1%
VRD_B
+12VDC
C139
.1uF 25V
R85
200K
1%

C120
.1uF 25V
R71
27K 1%
-VOG_B
-2
R70
39.2K
1%
-VH
-5V

20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QUANITY REQD	

UNLESS OTHERWISE SPECIFIED
DIM. ARE IN
2 PL DEC TOL ±
3 PL DEC TOL ±
ANGULAR TOL ±
SURF ROUGHNESS
EDGES
INSIDE RADII

MATERIAL

FINISH

DEVIATIONS FROM INTENDED SHAPE
FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.

DIMENSIONS APPLY AFTER FINISH
WHERE TOTAL TOLERANCE OS .001
INCHES OR LESS AND ON ALL
THREADS. IN ALL OTHER PLACES
DIMENSIONS APPLY BEFORE FINISH.

DR	Imager Interface
QA CHK	
ENGR	Jim DiBella
ENGR	
ECN NO.	
REL DATE	4/8/2016

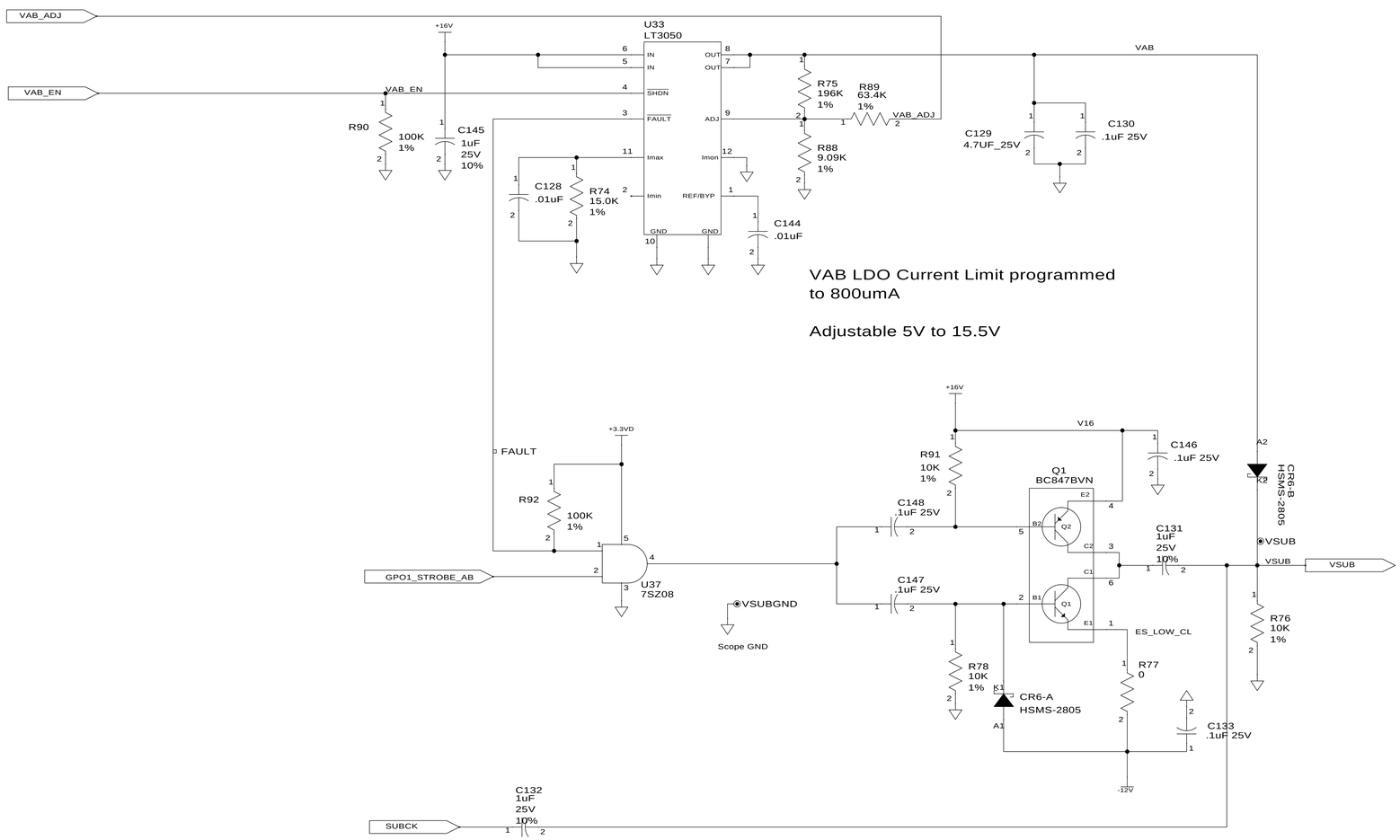
ON Semiconductor

NAME
Gen2 Evaluation System
72 pin PGA Imager Board
Imager PCB Interface

SIZE D | DWG NO. 20361636 / 20361640

SCALE | PROGRAM CADSTAR | SHEET 15 of 17

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL
C4		Assy 20361640-Revision 2 to 3 Change R75 from 200K to 196K Change R89 from 71.5K to 63.4K		April 2016



20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QUANITY REQD	

UNLESS OTHERWISE SPECIFIED
DIM. ARE IN
2 PL DEC TOL ±
3 PL DEC TOL ±
ANGULAR TOL ±
SURF ROUGHNESS
EDGES
INSIDE RADII

MATERIAL

FINISH

DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.

DIMENSIONS APPLY AFTER FINISH
WHERE TOTAL TOLERANCE OS .001
INCHES OR LESS AND ON ALL
THREADS. IN ALL OTHER PLACES
DIMENSIONS APPLY BEFORE FINISH.

DR VSUB and Electronic Shutter
QA CHK
ENGR Jim DiBella
ENGR
ECN NO.
REL DATE 4/8/2016

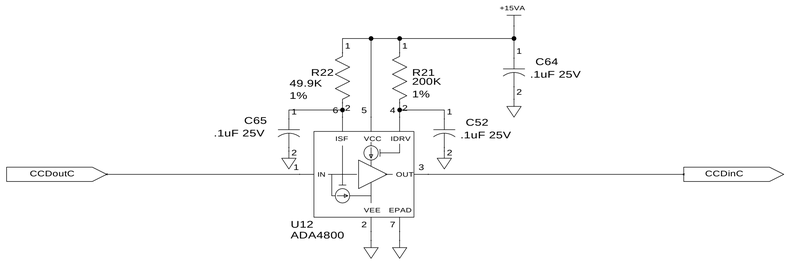
ON Semiconductor

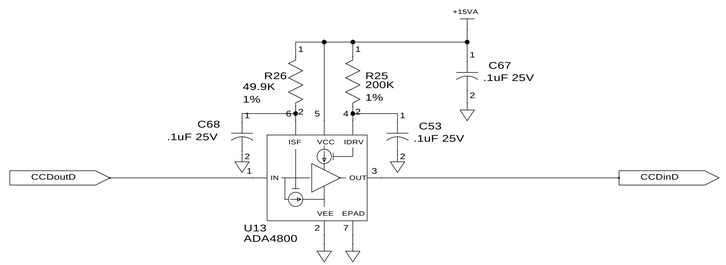
NAME
Gen2 Evaluation System
72 pin PGA Imager Board

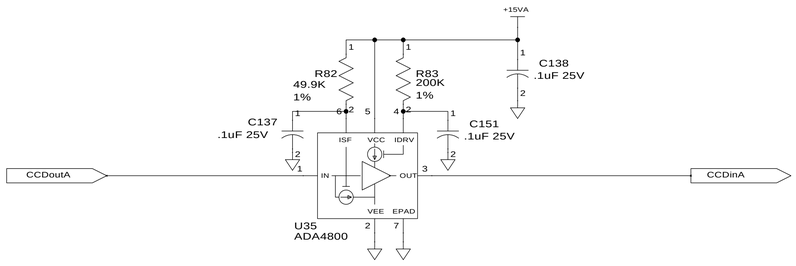
SIZE D | DWG NO. 20361636 / 20361640

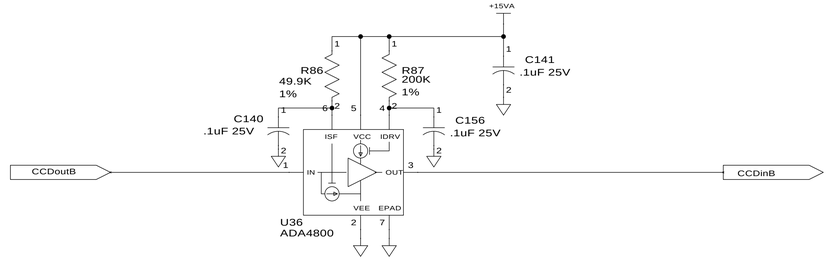
SCALE | PROGRAM CADSTAR | SHEET 16 of 17

REVISIONS				
ZONE	SYM	DESCRIPTION	DATE	APPROVAL









20361636-Revision 2 Bare Board

20361640-Revision 3 Completed Assy

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY		
APPLICATION		QUANITY REQD			

UNLESS OTHERWISE SPECIFIED

DIM. ARE IN

2 PL DEC TOL ±

3 PL DEC TOL ±

ANGULAR TOL ±

SURF ROUGHNESS

EDGES ✓

INSIDE RADII

MATERIAL

FINISH

DEVIATIONS FROM INTENDED SHAPE (FLATNESS,ROUNDNESS,SQUARENESS ETC.) MUST BE WITHIN STATED DIMENSIONAL TOLERANCES.

DIMENSIONS APPLY AFTER FINISH WHERE TOTAL TOLERANCE OS .001
INCHES OR LESS AND ON ALL THREADS. IN ALL OTHER PLACES DIMENSIONS APPLY BEFORE FINISH.

DR Video Output Buffers

QA CHK

ENGR Jim DiBella

ENGR

ECN NO.

REL DATE 4/8/2016

ON Semiconductor

NAME

Gen2 Evaluation System
72 pin PGA Imager Board

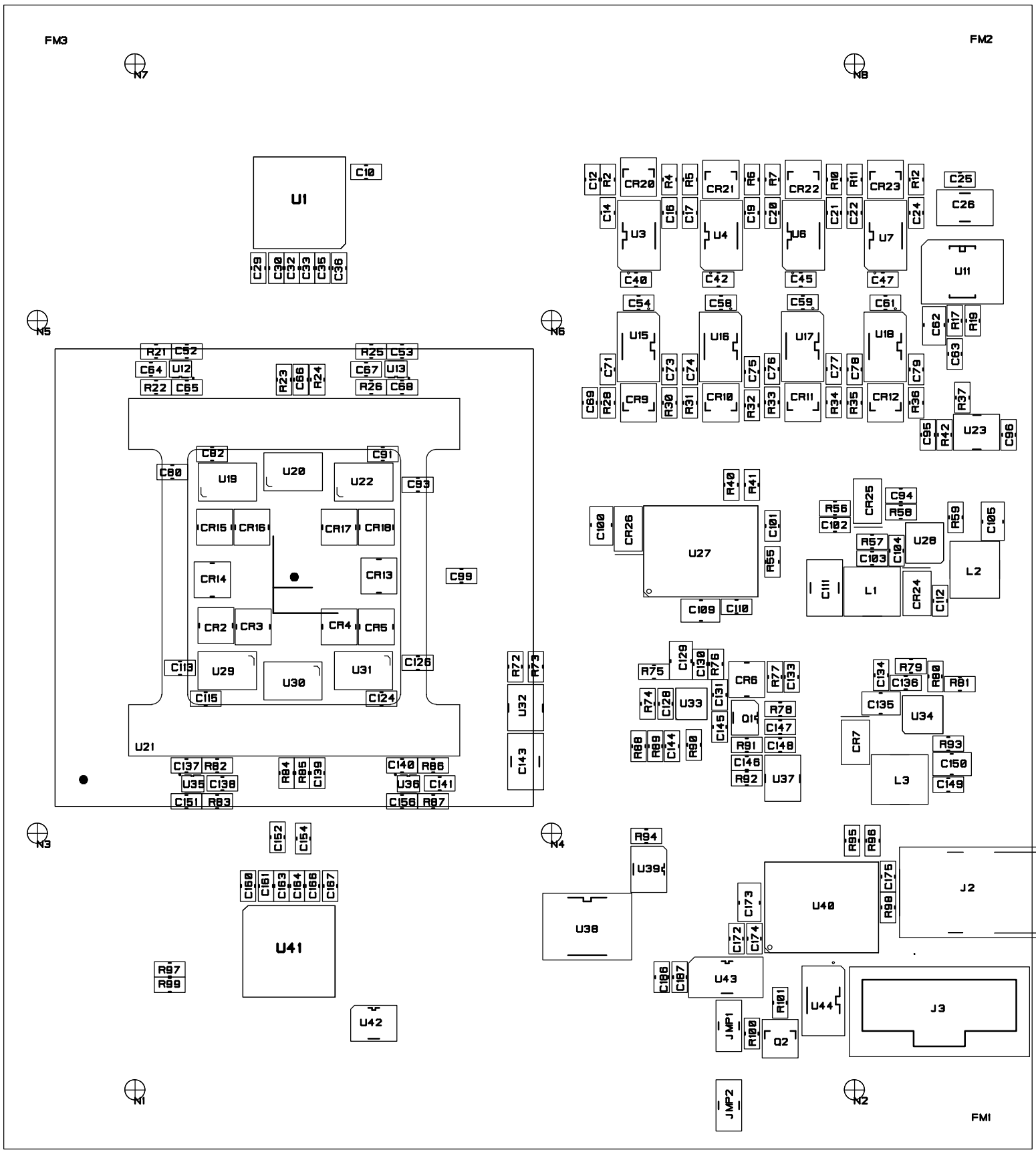
SIZE D

DWG NO. 20361636 / 20361640

SCALE

PROGRAM CADSTAR

SHEET 17of 17


FM3
FM2
N7
N8
U1
C10
C29
C30
C32
C33
C35
C36
C12
R2
CR20
R4
R5
CR21
R6
R7
CR22
R10
R11
CR23
R12
C25
C26
C14
U3
C16
C17
U4
C19
C20
U6
C21
C22
U7
C24
C40
C42
C45
C47
U11
C54
C58
C59
C61
C82
R17
R19
C63
U15
U16
U17
U18
C71
C73
C74
C75
C76
C77
C78
C79
C69
R28
CR9
R30
R31
CR10
R32
R33
CR11
R34
R35
CR12
R36
R37
C95
R42
U23
C96
N5
N6
R21
C52
C64
U12
R22
C65
R23
C66
R24
R25
C53
C67
U13
R26
C68
C82
C91
C80
U19
U20
U22
C93
CR15
CR16
CR17
CR18
CR14
CR13
C99
CR2
CR3
CR4
CR5
C113
U29
U30
U31
C126
C115
C124
U21
R72
R73
U32
C143
C137
R82
U35
C138
C151
R83
R84
R85
C139
C140
R86
U36
C141
C156
R87
C100
CR26
U27
C101
R55
R40
R41
C109
C110
CR25
C94
R56
C102
R58
R57
C103
C104
U28
R59
C105
C111
L1
CR24
C112
L2
C129
C130
R76
R75
CR6
R77
C133
R74
C128
U33
C131
C145
Q1
R78
C147
R88
R89
C144
R90
R91
C148
C146
R92
U37
C134
R79
C136
R80
R81
C135
U34
CR7
R93
C150
L3
C149
N3
N4
C152
C154
C160
C161
C163
C164
C166
C167
U41
R97
R99
U42
R94
U39
U38
R95
R96
C175
J2
C173
U40
C172
C174
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R101
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R100
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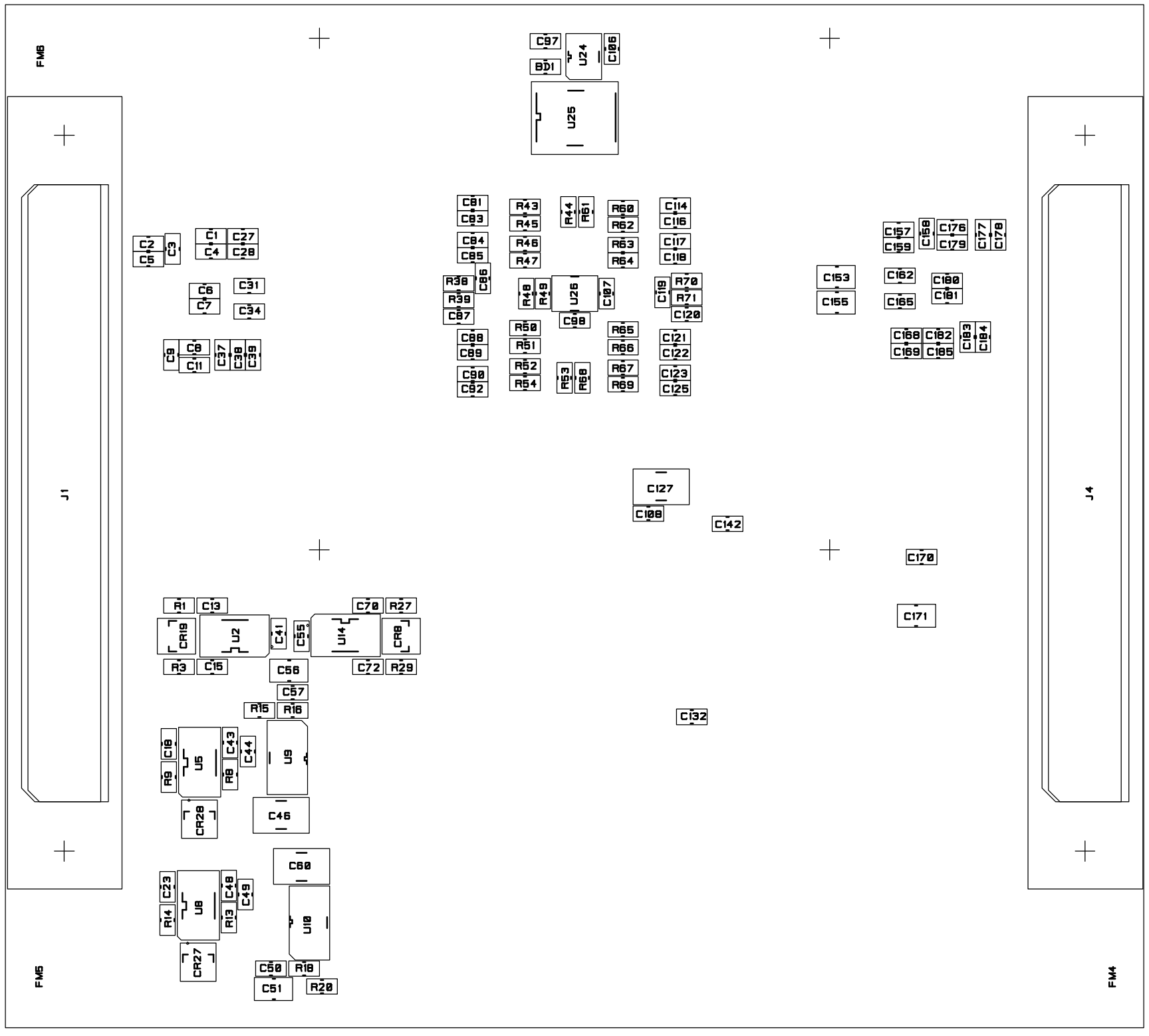
JMP2
N1
N2
FM1


FM6
J1
J4
FM5
FM4
C97
BD1
U24
C106
U25
C81
C83
R43
R45
R44
R61
R60
R62
C114
C116
C84
C85
R46
R47
C117
C118
R63
R64
R38
C86
R48
R49
U26
C107
C119
R70
R71
C120
R39
C87
C98
R50
R51
C121
C122
C88
C89
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R66
R52
R54
R53
R68
R67
R69
C123
C125
C90
C92
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C108
C142
C153
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C171
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C1
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C39
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U2
C41
C55
U14
C70
R27
CR8
R3
C15
C56
C72
R29
C57
R15
R16
C18
R9
U5
C43
R8
C44
U9
CR28
C46
C60
C23
R14
U8
C48
R13
C49
U10
CR27
C50
R18
C51
R20

20361640 REV3 KAI 72 PIN PGA Imager

Part Name	Part Number	Description	Qty	Comps
BLM18AG601SN1D	BLM18AG601SN1D	FERRITE CHIP 600 OHM 500MA 0603	1	BD1
C4.7UF_0603_6V3_10	GRM188R60J475KE19D	CERCAP 4.7UF 6.3WVDC 10%	10	C1 C6 C8 C27 C39 C157 C169 C179 C181 C185
C10UF_0805_16V_80	GRM21BF51C106ZE15L	CAP 10UF 16WVDC 80%	3	C100 C150 C171
C2200PF_0603_50V_10%	C0603C222K5RACTU	CAP 2200PF X7R 50WVDC 10%	2	C103 C134
C10UF_1210_25V_20	ECJ-4YB1E106M	CAP 10UF 25WVDC 20% X5R	3	C111 C127 C143
C4.7UF_0805_25V20	GRM21BR61E475MA12L	CERCAP 4.7UF 25WVDC 20% X5R	5	C129 C135 C153 C155 C173
C1000PF_0603	C0603C102K5RACTU	CAP 1000PF X7R 50VDC 10%	24	C13-24 C43 C48 C70-79 C2-5 C7 C9-11 C25 C28-38 C40-42 C44-45 C47 C49 C52-55 C58-59 C61 C64-68 C80-93 C96-97 C101-102 C104 C106 C108 C110 C113-126 C130 C133 C137-141 C146-148 C151-152 C154 C156 C158-168
C.1UF_0603_25V	C0603C104K3RACTU	CAP .1UF 25WVDC +10%	110	C170 C174-178 C180 C182-184
C4.7UF_1210_25V20	TMK325B7475KN-T	CAP 4.7UF 25WVDC 20%	3	C26 C46 C60
C.01UF_0603	C0603C103K5RAC	CAP .01UF 50WVDC 10%	10	C50 C57 C63 C99 C107 C128 C136 C144 C149 C186
C2.2UF_0805_16V	GRM21BF51C225ZA01	CAP 2.2UF 16WVDC 20% Y5V	5	C51 C56 C62 C105 C109
C100PF_0603	C0603C101J5GAC	CAP 100PF 50WVDC 5%	1	C94
C1UF_0603_25V_10	GRM188R61E105KA12D	CAP 1UF 25V 10%	8	C95 C98 C112 C131 C142 C145 C172 C187
HSMS2805	HSMS-2805-TR1G	DIODE DUAL	11	CR2-6 CR13-18
MBRM120E	MBRM120ET3G	SCHOTTKY BARRIER RECTIFIER 1A 20V	4	CR7 CR24-26
BAT54-04	BAT54-04	SCHOTTKY DUAL SERIES	12	CR8-12 CR19-23 CR27-28
ASP-122952-01	ASP-122952-01	CONNECTOR 5mm BOARD TO BOARD Mezzanine	2	J1 J4
104363-4	5-104363-4	5 POS SHROUDED MTE HDR ASS	1	J3
JUMP_1206_SMT	NONE	1206 SMT JUMPER	1	JMP2
NRS5020T100MMGJ	NRS5020T100MMGJ	INDUCTOR 10uH 1.3A	3	L1-3
BC847BVN	BC847BVN-7	TRANSISTOR DUAL DIGITAL PNP/NPN	1	Q1
MMBT3904LT1	MMBT3904LT1G	TRANSISTOR G.P. NPN	1	Q2
R220_0603	CRCW0603220RJNEA	RESISTOR 220 1/16W 5%	8	R1 R3 R8-9 R13-14 R27 R29
R2322_0603	CRCW060323K2FKEA	RESISTOR 23.2K 1/16W 1%	1	R15
R2003_0603	CRCW0603200KFKEA	RESISTOR 200K 1/16W 1%	32	R16-17 R21 R23 R25 R42-47 R49-54 R60-69 R72 R80 R83 R85 R87
R3093_0603	CRCW0603309KFKEA	RESISTOR 309K 1/16W 1%	2	R18 R48
R1623_0603	CRCW0603162KFKEA	RESISTOR 162K 1/16W 1%	1	R19
R1000_0603	CRCW0603100RFKEA	RESISTOR 100 1/16W 1%	16	R2 R4-7 R10-12 R28 R30-36
R1103_0603	CRCW0603110KFKEA	RESISTOR 110K 1/16W 1%	1	R20
R4992_0603	CRCW060349K9FKEA	RESISTOR 49.9K 1/16W 1%	6	R22 R24 R26 R82 R84 R86
R3162_0603	CRCW060331K6FKEA	RESISTOR 31.6K ohm 1/16W 1%	1	R37
R3922_0603	CRCW060339K2FKEA	RESISTOR 39.2K 1/10W 1%	2	R38 R70
R2702_0603	ERJ-3GEYJ273V	RESISTOR 27K ohm 1/16W 1%	3	R39-40 R71
R9312_0603	CRCW060393K1FKEA	RESISTOR 93.1K 1/16W 1%	1	R41
R1502_0603	ERJ-3EKF1502V	RESISTOR 15.0K 1/16W 1%	7	R55 R59 R74 R93 R98 R100-101
R9532_0603	CRCW060395K3FKEA	RESISTOR 95.3K 1/16W 1%	1	R56
R1002_0603	CRCW060310K0FKEA	RESISTOR 10K 1/16W 1%	7	R57-58 R76 R78-79 R91 R94
R1742_0603	CRCW060317K4FKEA	RESISTOR 17.4K 1/16W 1%	1	R73
R1963_0603	CRCW0603196KFKEA	RESISTOR 196K 1/10W 1%	1	R75
R0_0603	CRCW06030000Z0EA	RESISTOR 0	3	R77 R97 R99
R1652_0603	CRCW060316K5FKEA	RESISTOR 16.5K 1/16W 1%	1	R81
R9091_0603	CRCW06039K09FKEA	RESISTOR 9.09K 1/16W 1%	1	R88
R6342_0603	CRCW06036342FT	RESISTOR 63.4 K 1/16W 1%	1	R89
R1003_0603	CRCW0603100KFKEA	RESISTOR 100K 1/16W 1%	2	R90 R92
R2492_0603	CRCW060324K9FKEA	RESISTOR 24.9K 1/16W 1%	1	R95

R7502_0603	CRCW060375K0FKEA	RESISTOR 75.0K 1/16W 1%	1	R96
AD9928	AD9928	CCD DUAL Signal Processor with HV Timing Generator	2	U1 U41
LT1175CS8	LT1175CS8#PBF	ADJ REGULATOR LOW DROPOUT NEG	1	U11
ADA4800	ADA4800ACPZ-R7	CCD BUFFER AMPLIFIER	4	U12-13 U35-36
74LCX541BQX	74LCX541BQX	OCTAL BUFFER DQFN package	6	U19-20 U22 U29-31
Socket KAI-29050	IS230-1371D-75M-R29-L14-A	Socket for KAI-29050	1	U21
LT1964ES5-SD	LT1964ES5-SD#TRMPBF	REGULATOR LOW DROPOUT NEG with SHUTDOWN	2	U23 U26
SN74LVC2G04	SN74LVC2G04DBVR	IC DUAL INVERTER GATE SOT-23-6	2	U24 U42
LTM8022	LTM8022EV#PBF	Step Down uModule Regulator	2	U27 U40
ZXMD63C03X	ZXMD63C03XTA	IC N/P-CHANNEL FAST SWITCH FET	13	U2-8 U14-18 U44
LT3479EDE	LT3479EDE#PBF	3A DC/DC Converter	2	U28 U34
LT1761ES5-SD	LT1761ES5-SD#TRMPBF	ADJ REGULATOR LOW DROPOUT STDBY	1	U32
LT3050	LT3050EDDB#TRMPBF	100mA LDO with current limit and fault detect	1	U33
NC7SZ08	NC7SZ08M5X	TINY AND GATE	1	U37
LTC1665C	LTC1665CGN#PBF	IC 8 BIT DAC 8CH	1	U38
ADC081	ADC081S021	IC 8 BIT ADC	1	U39
LT1521-3.3	LT1521CMS8-3.3#PBF	REG LDO 3.3V 300mA	1	U43
LT1965EMS8E	LT1965EMS8E#PBF	REGULATOR LOW DROPOUT NEG	2	U9-10

NO LOADS

xxx	CAP 1UF 25V 10% DO NOT POPULATE	1	C132
xxx	1206 SMT JUMPER DO NOT POPULATE	1	JMP1
xxx	CAP NOLOAD	1	C12
xxx	CAP NOLOAD	1	C69
xxx	JACK POWER 2.1mm DO NOT POPULATE	1	J2
xxx	FIDUCIAL BOARD LOCAL 40 DO NOT POPULATE	6	FM1-6
xxx	Mounting Hole 150/95 DO NOT POPULATE	8	N1-8