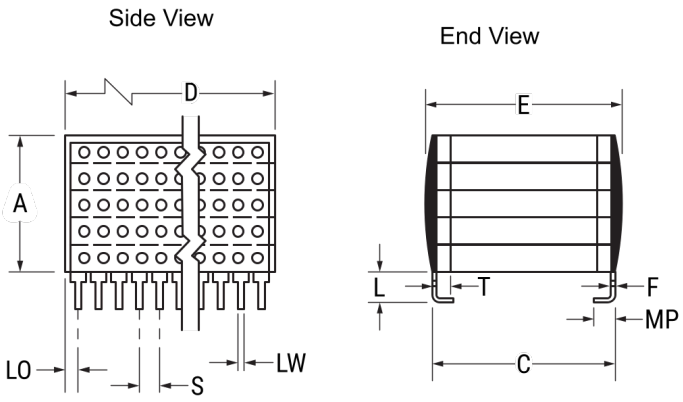
L1WJ30C825MS36

KPS LDD Comm SMPS, Ceramic, 8.2 uF, 20%, 500 VDC, X7R, N/A



Click here for the 3D model.

Dimensions

D	25.715mm +/-1.585mm
L	1.78mm +/-0.25mm
T	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
A	9.144mm MAX
C	11.43mm +/-0.635mm
E	12.7mm MAX
LO	1.586mm MAX
LW	0.508mm +/-0.051mm
MP	1.27mm MIN

Packaging Specifications

Packaging	Waffle, Box
Packaging Quantity	28

General Information

Series	KPS LDD Comm SMPS
Style	Leaded Stacked Chip
Description	Low ESR, High Current Stacked Ceramic Chips
Features	Low ESR, High Current, High Performance
RoHS	No
Prop 65	⚠ **WARNING:** Cancer and reproductive harm - http://www.p65warnings.ca.gov.
SCIP Number	4221181d-d71c-4d0a-af45-5eab760732b2
Termination	60/40 Solder Coated
Lead	J Leads
Failure Rate	N/A
Testing and Reliability	Commercial
AEC-Q200	No
Notes	Note: Number of chips in stack depends on design. Number of Chips in this stack = 3. Note: Turn Radius For Lead Extension Is 0.1 Radians (Typical). Note: Lead alignment within pin rows shall be within ±.0.13 mm.

Specifications

Capacitance	8.2 uF
Capacitance Tolerance	20%
Voltage DC	500 VDC
Dielectric Withstanding Voltage	750 VDC
Temperature Range	-55/+125°C
Temperature Coefficient	X7R
Dissipation Factor	2.5% 1 kHz 25C
Aging Rate	3% Loss/Decade Hour
Insulation Resistance	12.2 GOhms