ALPHA & OMEGA SEMICONDUCTOR

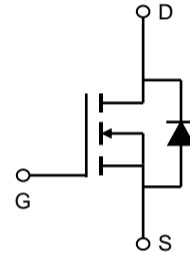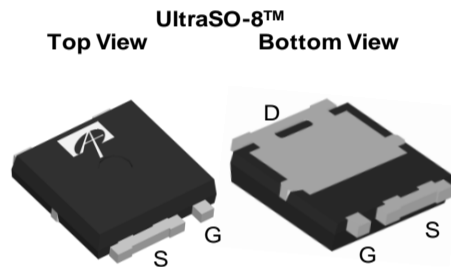# AOL1454G
40V N-Channel AlphaSGT™

General Description

- Trench Power AlphaSGT™ technology
- Low $R_{DS(ON)}$
- Logic Level Driving
- Excellent Gate Charge x $R_{DS(ON)}$ Product (FOM)
- RoHS and Halogen-Free Compliant

Applications

- High Frequency Switching and Synchronous Rectification
- DC-Motor Driver

Product Summary

V_{DS}	40V
I_D (at V_{GS}=10V)	46A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 5.9mΩ
$R_{DS(ON)}$ (at V_{GS}=4.5V)	< 9.2mΩ

100% UIS Tested
100% Rg Tested

Green Product

UltraSO-8™
Top View   **Bottom View**

Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOL1454G	Ultra SO8	Tape & Reel	3000

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [G]	T_C=25°C	I_D	46	A
	T_C=100°C		46	
Pulsed Drain Current [C]		I_{DM}	155	
Continuous Drain Current	T_A=25°C	I_{DSM}	25	A
	T_A=70°C		20	
Avalanche Current [C]		I_{AS}	20	A
Avalanche energy L=0.3mH [C]		E_{AS}	60	mJ
Power Dissipation [B]	T_C=25°C	P_D	52	W
	T_C=100°C		20.5	
Power Dissipation [A]	T_A=25°C	P_{DSM}	6.2	W
	T_A=70°C		4.0	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{θJA}$	15	20	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		40	50	°C/W
Maximum Junction-to-Case	Steady-State	$R_{θJC}$	1.9	2.4	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV$_{DSS}$	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V		40			V
I$_{DSS}$	Zero Gate Voltage Drain Current	V_{DS}=40V, V_{GS}=0V				1	µA
			T_J=55°C			5	
I$_{GSS}$	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V				±100	nA
V$_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250µA		1.5	2.0	2.5	V
R$_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A			4.8	5.9	mΩ
			T_J=125°C		7.3	8.9	
		V_{GS}=4.5V, I_D=20A			7.2	9.2	mΩ
g$_{FS}$	Forward Transconductance	V_{DS}=5V, I_D=20A			70		S
V$_{SD}$	Diode Forward Voltage	I_S=1A, V_{GS}=0V			0.7	1	V
I$_S$	Maximum Body-Diode Continuous Current [G]					46	A
DYNAMIC PARAMETERS							
C$_{iss}$	Input Capacitance	V_{GS}=0V, V_{DS}=20V, f=1MHz			1480		pF
C$_{oss}$	Output Capacitance				245		pF
C$_{rss}$	Reverse Transfer Capacitance				13		pF
R$_g$	Gate resistance	f=1MHz		0.9	1.8	2.7	Ω
SWITCHING PARAMETERS							
Q$_g$(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=20V, I_D=20A			20	30	nC
Q$_g$(4.5V)	Total Gate Charge				8.5	14	nC
Q$_{gs}$	Gate Source Charge				5.5		nC
Q$_{gd}$	Gate Drain Charge				3		nC
Q$_{oss}$	Output Charge	V_{GS}=0V, V_{DS}=20V			10		nC
t$_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=20V, R_L=1.0Ω, R_{GEN}=3Ω			7.5		ns
t$_r$	Turn-On Rise Time				2		ns
t$_{D(off)}$	Turn-Off DelayTime				23		ns
t$_f$	Turn-Off Fall Time				3		ns
t$_{rr}$	Body Diode Reverse Recovery Time	I_F=20A, di/dt=500A/µs			11		ns
Q$_{rr}$	Body Diode Reverse Recovery Charge	I_F=20A, di/dt=500A/µs			21		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The Power dissipation P_{DSM} is based on R $_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.
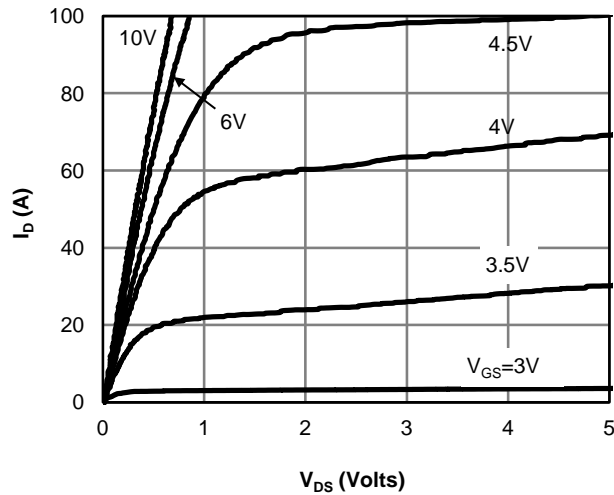E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.
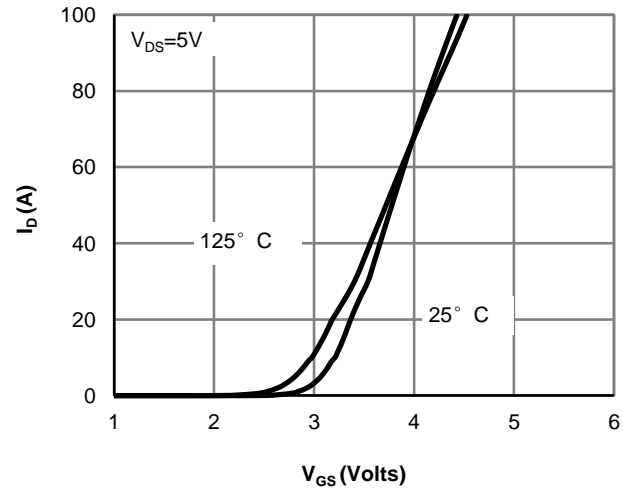G. The maximum current rating is package limited.
H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C.
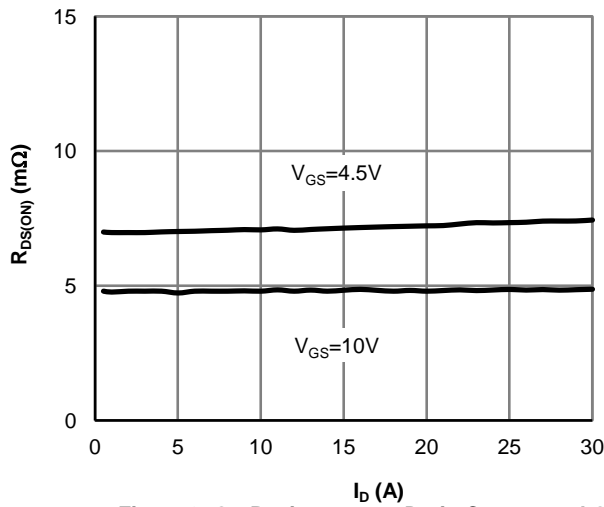
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS
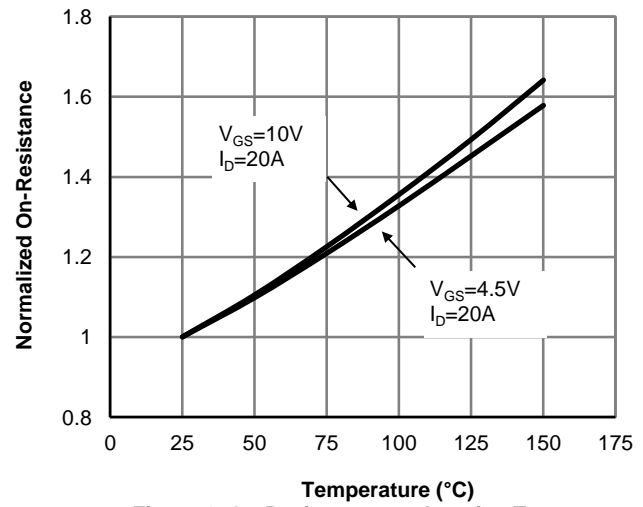

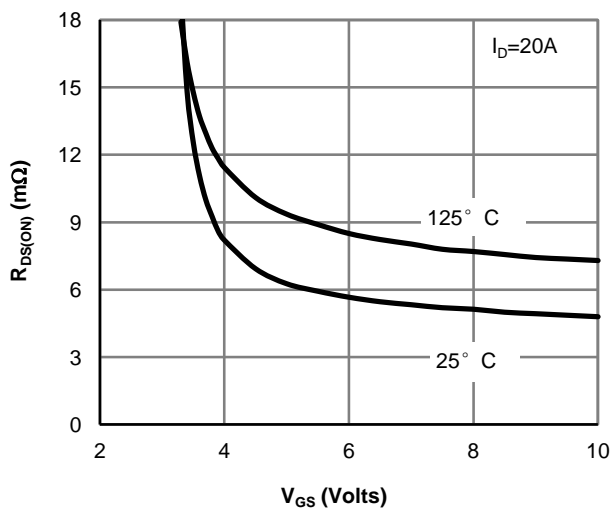**Figure 1: On-Region Characteristics (Note E)**

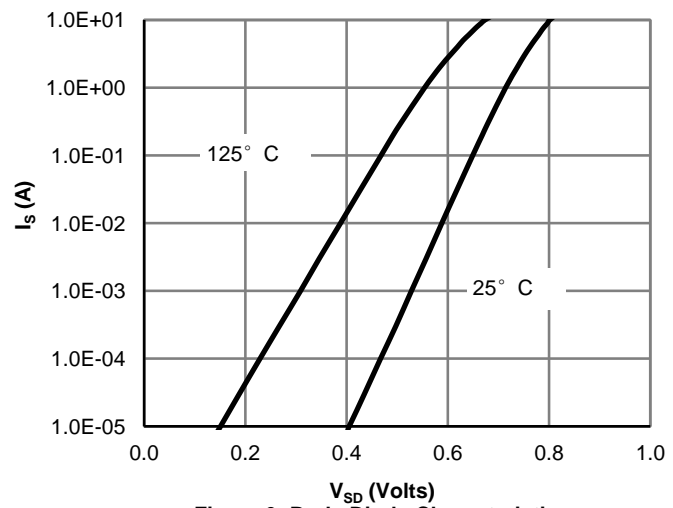**Figure 2: Transfer Characteristics (Note E)**

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

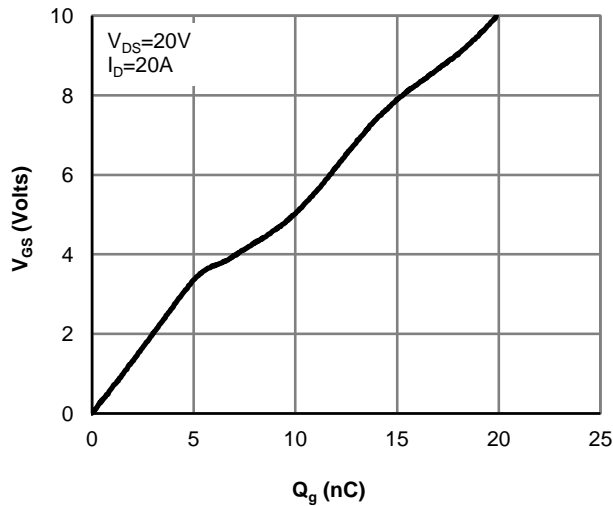**Figure 4: On-Resistance vs. Junction Temperature (Note E)**

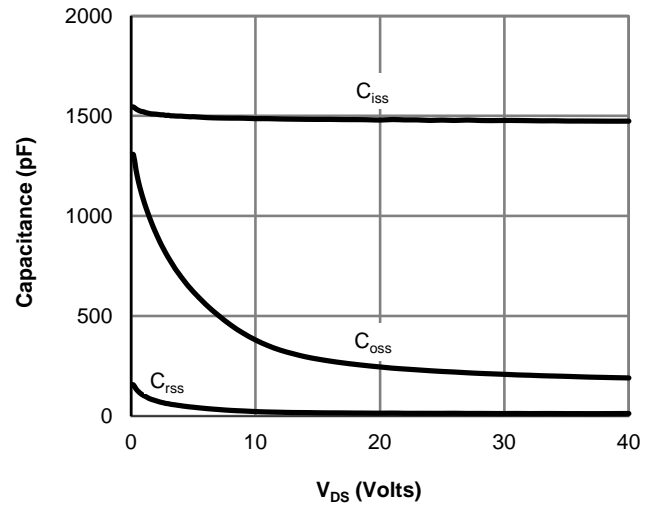**Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)**
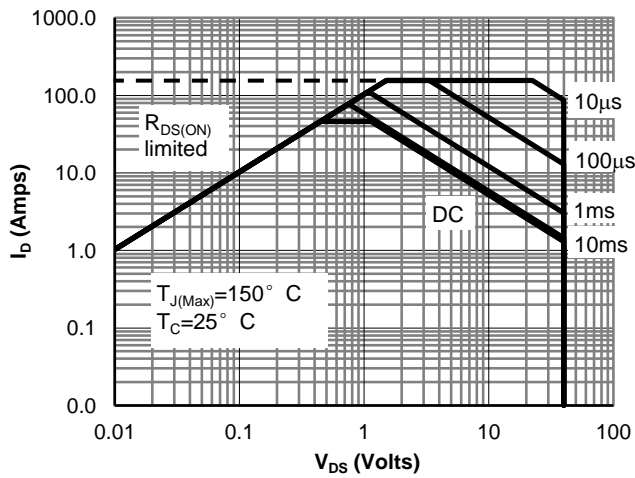

Figure 6: Body-Diode Characteristics (Note E)

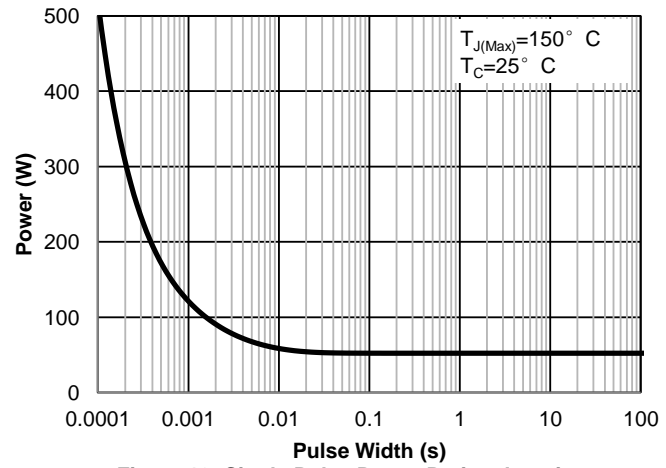## TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

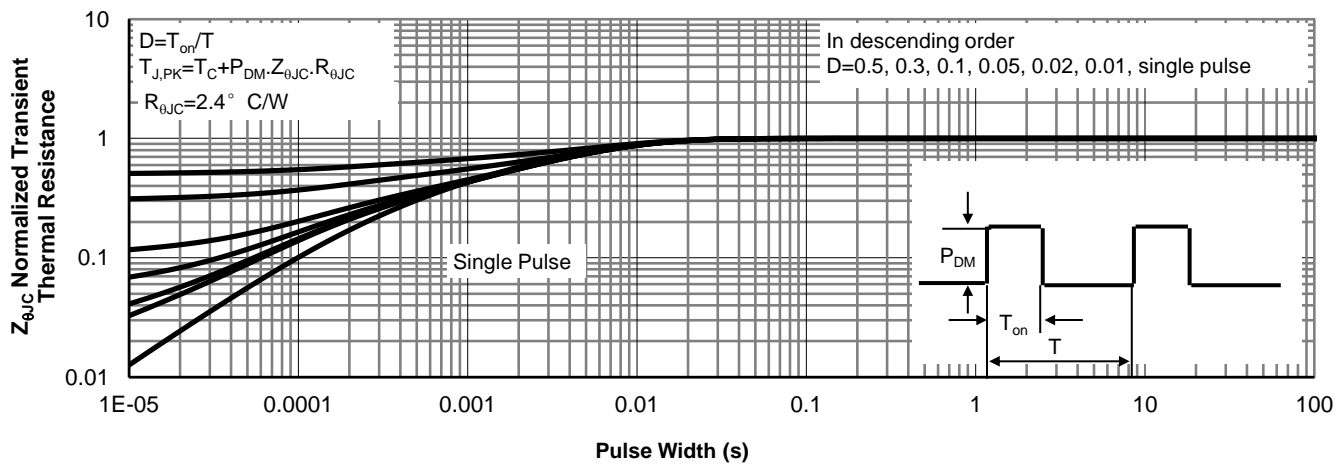**Figure 7: Gate-Charge Characteristics**

Figure 8: Capacitance Characteristics

Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)
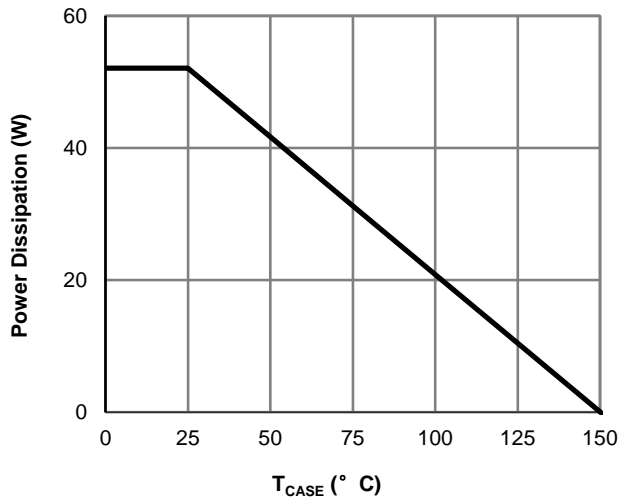
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

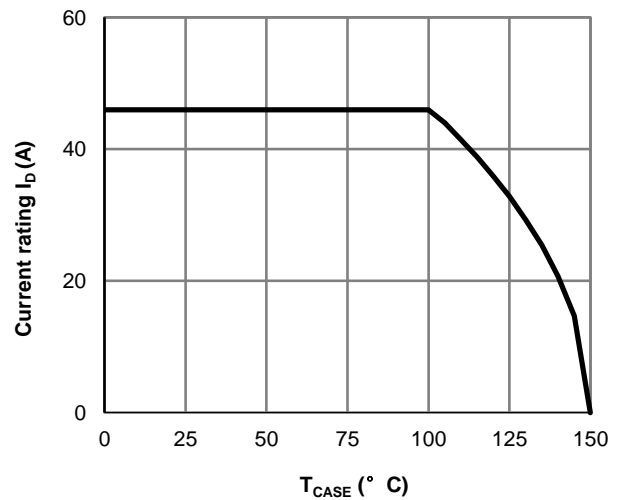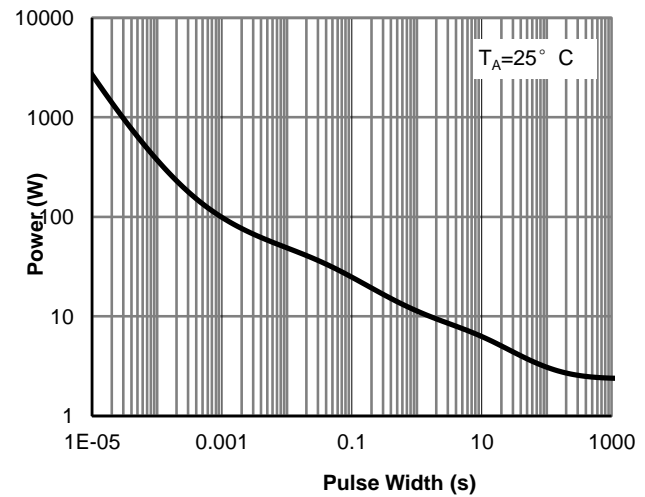**Figure 12: Power De-rating (Note F)**

X-axis: T_{CASE} (°C) — Y-axis: Power Dissipation (W)

Figure 13: Current De-rating (Note F)

X-axis: T_{CASE} (°C) — Y-axis: Current rating I_D (A)

Figure 14: Coss stored Energy

X-axis: V_{DS} (Volts) — Y-axis: Eoss(uJ)

Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

X-axis: Pulse Width (s) — Y-axis: Power (W) — T_A=25°C

Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Y-axis: $Z_{\theta JA}$ Normalized Transient Thermal Resistance — X-axis: Pulse Width (s)

$D=T_{on}/T$
$T_{J PK}=T_A+P_{DM} \cdot Z_{\theta JA} \cdot R_{\theta JA}$
$R_{\theta JA}=50°C/W$

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse

Single Pulse
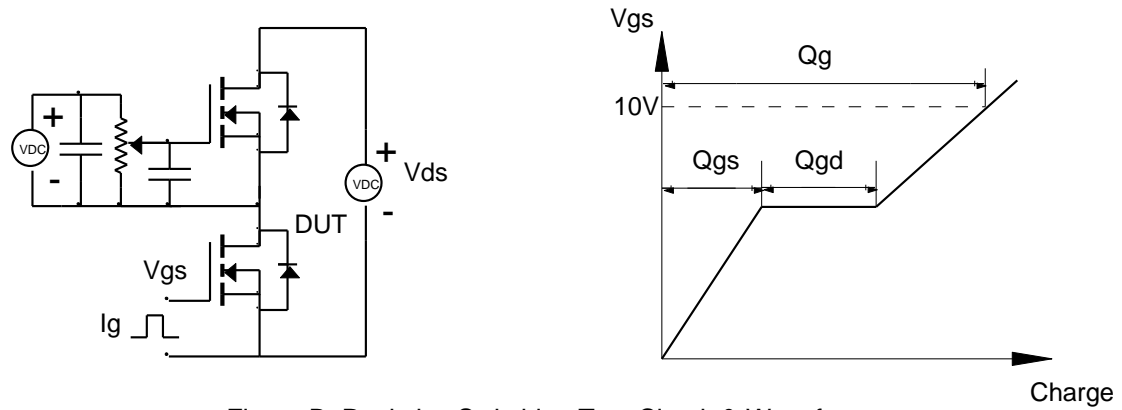
P_{DM}

T_{on}

T

Figure A: Gate Charge Test Circuit & Waveforms

Figure B: Resistive Switching Test Circuit & Waveforms

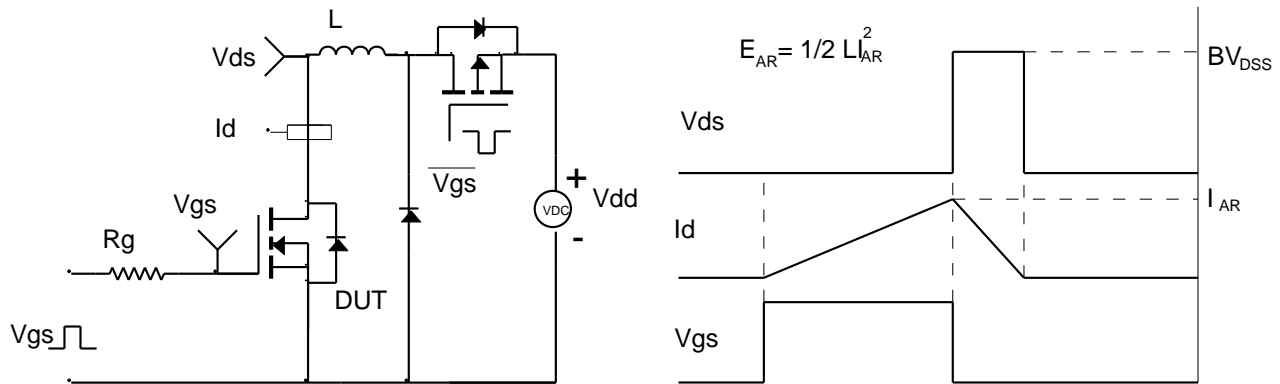Figure C: Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

$$E_{AR} = 1/2 \ LI_{AR}^2$$

Figure D: Diode Recovery Test Circuit & Waveforms

$$Q_{rr} = \int Idt$$