Microsemi Corporation

January 18, 2017

Product/Process Change Notification No: PCN17005

Change Classification: Major

Subject: Important Changes in SmartFusion2 and IGLOO2 Devices

Summary of Changes: The PCN17005 notifies about several changes and impacts in SmartFusion2 and IGLOO2 devices.

Contents

PCN Summary Actions

PCN #	Change	Affected Devices	Effective Date	Required Action
1	Dynamic use of certain registers in the SYSREG block	005 and 010 SmartFusion2 devices	Effective immediately with Libero SoC v11.7 SP3 release	Review dynamic use of system registers
2	Timing Model Adjustment	All SmartFusion2 and IGLOO2 devices	Effective immediately with Libero SoC v11.7 SP3 release	Re-analyze timing
3	Default PLL Lock Window Settings	All SmartFusion2 and IGLOO2 devices	Effective immediately with Libero SoC v11.7 SP3 release	Use the proper settings when the internal RC oscillators are used as a clock reference

PCN 17005.1 Registers in the SYSREG Block

Change

Application traffic across the FIC_0 interface could cause certain bits in the SYSREG block to change state if these bits are changed from their default power-up values during runtime. In addition, not all SYSREG register settings are available in the existing MSS Configurator. Libero v11.7 SP3 introduces a new MSS configurator to expose all SYSREG bits. If you do not dynamically modify the bits listed in Table 1 at runtime, you are not impacted. Note that Microsemi's Firmware Driver Library does not use the affected registers.

Table 1 lists the subset of SYSREG registers and specific bit definitions that are affected.

Table 1. Affected System Registers

System Register	Fields
SOFT_RESET_CR	All 32 Bits
M3_CR	STCALIB
FAB_IF	FAB0_AHB_BYPASS, FAB1_AHB_BYPASS, FAB0_AHB_MODE, FAB1_AHB_MODE, SW_FIC_REG_SEL
LOOPBACK_CR	MSS_MMUARTLOOPBACK, MSS_SPILOOPBACK, MSS_I2CLOOPBACK, MSS_GPIOLOOPBACK
GPIO_SYSRESET_SEL	MSS_GPIO_7_0_SYSRESET_SEL, MSS_GPIO_15_8_SYSRESET_SEL, MSS_GPIO_23_16_SYSRESET_SEL, MSS_GPIO_3_124_SYSRESET_SEL
GPIN_SRC_SEL_CR	MSS_GPINSOURCE
MDDR_CR	MDDR_CONFIG_LOCAL, SDR_MODE, F_AXI_AHB_MODE, PHY_SELF_REF_EN
USB_IO_INPUT_SEL	USB_IO_INPUT_SEL
PERIPH_CLK_MUX_SEL_CR	SPI0_SCK_FAB_SEL, SPI1_SCK_FAB_SEL, TRACECLK_DIV2_SEL
WDOG_CR	WDOGENABLE, WDOGMODE
EDAC_IRQ_ENABLE_CR	All Bits
MSS_IRQ_ENABLE_CR	DDRB_INTERRUPT_EN, SW_INTERRUPT_EN, CC_INTERRUPT_EN
RTC_WAKEUP_CR	RTC_WAKEUP_M3_EN, RTC_WAKEUP_FAB_EN, RTC_WAKEUP_C_EN
MSSDDR_PLL_STATUS_LOW_CR	FACC_PLL_DIVR, FACC_PLL_DIVF, FACC_PLL_DIVQ, FACC_PLL_RANGE, FACC_PLL_LOCKWIN, FACC_PLL_LOCKCNT
MSSDDR_PLL_STATUS_HIGH_CR	FACC_PLL_BYPASS, FACC_PLL_MODE_1V2, FACC_PLL_MODE_3V3, FACC_PLL_FSE, FACC_PLL_PD, FACC_PLL_SSE, FACC_PLL_SSMD, FACC_PLL_SSMF
MSSDDR_FACC1_CR	DIVISOR_A, APB0_DIVISOR, APB1_DIVISOR, DDR_CLK_EN, M3_CLK_DIVISOR, FACC_GLMUX_SEL, FIC_0_DIVISOR. FIC_1_DIVISOR
IOMUXCELL_CONFIG	MSS_IOMUXSEL0, MSS_IOMUXSEL1, MSS_IOMUXSEL2, MSS_IOMUXSEL3, MSS_IOMUXSEL4UPPER, MSS_IOMUXSEL4MID, MSS_IOMUXSEL4LOWER, MSS_IOMUXSEL5MID, MSS_IOMUXSEL5LOWER

Application Impact

This impacts all SmartFusion2 devices in the 005 and 010 device densities. Libero v11.7 SP3 contains a new MSS Component (version 1.1.500) that adds capabilities to initialize register settings affected by this change. The new configurator allows all SYSREG bits to be set to a static user defined power-up value initialized from an SEU immune FPGA flash configuration bit. Typically, these registers are set once and never changed.

Action Required

During the design process, you can configure the components of the MSS using the MSS configurator in Libero. Specifically, the register locations in Table 1 must be set to a user defined default power up state using SEU immune FPGA flash configuration bits and must never be altered at run time. The new MSS configurator allows you to define the power-up state of each one of these register locations to your specific application requirements.

If you are using C code to initialize these registers on power-up, you must now use the MSS configurator to define the initialized value of these registers.

1. Go through the system builder flow and regenerate the system builder block.
2. Right-click the system builder block and select **Convert to SmartDesign** check box.
3. Open the converted SmartDesign block and check/modify the MSS configurator settings. Note that some of the register settings can only be changed in the MSS configurator.
4. Go through the Libero design flow and generate the new bitstream.
5. Update the devices with the new bitstream. You can use the remote in application programming (IAP) methodology to push the new bitstream to fielded systems.

You must generate a new bitstream. You can use the remote IAP methodology to push the new bitstreams to fielded systems. If your application requires these registers to be dynamically changed, call tech support for further assistance.

PCN 17005.2 Timing Model Adjustments for SmartFusion2 and IGLOO2 Devices

Change

For SmartFusion2 and IGLOO2 devices, there are small adjustments to the timing model.

1. Timing model adjustment for nets driving into the fabric a small additional timing delay has been added to more accurately model the timing arc Table 2 lists the worst-case additional timing delay by interface and device. Both nets and clocks are affected. Interfaces affected are,
    a. SERDES to Fabric Nets
    b. FDDR/MDDR to Fabric Nets
    c. MSS to Fabric Nets
    d. User I/O to Fabric Nets
    e. Fabric Nets to User I/O
    f. CCC divider Timing Model change for SmartFusion2 and IGLOO2 devices
2. When the divider in the CCC block is used, the algorithm used to calculate external hold time has been updated to ensure that maximum delay is utilized along the entire clock path from the input pin to the clock input of a flip flop. Previously, the delay from the input pin through the CCC was incorrectly using a minimum delay, resulting in skewed external hold time. Both Y and GL outputs are impacted.
3. Timing arcs for SmartFusion2 Fabric to MSS interrupts and Embedded Trace Macrocell
4. For SmartFusion2 timing arcs for interrupts to the Cortex-M3 sourced from the FPGA fabric have been updated. In addition, timing arcs for the Cortex-M3 Embedded Trace Macrocell (ETM) have been added.

Table 2. Worst-Case Delays

	additional delay in ps, -1 speed grade, C temp 85 °C						
Interface	5	10	25	50	60	90	150
fic_0	561	140	129	481	49	103	120
fic_1				234			117
fic_2	433	70	75	126	68	88	82
smc_fic	83	82	80	132	40	385	92
mss_misc	486	189	146	234	134	116	94
Fddr				198			41
Xaui		378	567	295	181	386	478
Pcie		404	682	318	180	415	584
Epcs		377	567	92	177	397	387
I/Os to Fabric	158	156	137	217	216	239	280
Fabric to I/Os	389	378	331	401	361	373	430

	additional delay in ps, -1 speed grade, I temp 100 °C						
Interface	5	10	25	50	60	90	150
fic_0	567	142	130	486	50	104	121
fic_1				237			118
fic_2	438	71	76	127	69	89	83
smc_fic	84	83	81	133	40	389	93
mss_misc	491	191	148	237	136	117	95
Fddr				200			41
Xaui		382	573	298	183	390	483
Pcie		409	690	322	182	420	591
Epcs		381	573	93	179	401	391
I/Os to Fabric	159	158	138	220	218	241	283
Fabric to I/Os	393	382	335	405	365	377	434

	additional delay in ps, -1 speed grade, M/T2 temp 125 °C						
Interface	5	10	25	50	60	90	150
fic_0	581	145	134	498	51	107	124
fic_1				242			121
fic_2	449	73	78	131	70	91	85

smc_fic	86	85	83	137	41	399	95
mss_misc	504	196	151	242	139	120	97
Fddr				205			42
Xaui		392	588	306	188	400	495
Pcie		419	707	330	187	430	605
Epcs		391	588	95	183	411	401
I/Os to Fabric	163	162	142	225	223	247	290
Fabric to I/Os	403	391	343	415	374	387	445

	additional delay in ps, -1 speed grade, T1 temp 135 °C						
Interface	5	10	25	50	60	90	150
fic_0	584	146	134	500	51	107	125
fic_1				243			122
fic_2	450	73	78	131	71	92	85
smc_fic	86	85	83	137	42	401	96
mss_misc	506	197	152	243	139	121	98
Fddr				206			43
Xaui		393	590	307	188	402	497
Pcie		420	710	331	187	432	608
Epcs		392	590	96	184	413	403
I/Os to Fabric	164	162	142	226	224	248	291
Fabric to I/Os	405	393	344	417	375	388	447

Action Required

You should open your designs with Libero v11.7 SP3 and re-run the timing analysis. If there are no timing violations, no action is required. If new timing violations exist, the following options can be used to resolve them:

- Re-run place-and-route
- Re-run place-and-route with high effort
- Run place-and-route with multi-pass
- Adjust timing constraints or use chip planner to floorplan the affected interfaces

If timing violations still occur, call tech support at the number listed below for further assistance.

PCN 17005.3 PLL Lock Window Default Settings

Change

If the reference divider for the PLL is 2 or less, and if you use the wrong PPM settings, the PLL comes into and out of lock. This applies to the fabric PLLs.

For all the SmartFusion2 and IGLOO2 devices, the default lock window for the PLL has changed when using the internal RC oscillators as the PLL reference clock. This accommodates the larger jitter associated with using the on-chip RC's as a PLL source.

- Using the 50 MHz RC oscillator, you should use the 32,000 ppm setting.
- Using the 1 MHz RC oscillator, you should use the 64,000 ppm setting.

Application Impact

This impacts all the SmartFusion2 and IGLOO2 devices when using the internal RC oscillator as the reference clock for the PLL.

Action Required

For new designs if you use the RC (1 or 50 MHz) as a source for the PLL, the appropriate PPM settings must be used.

CAN 17005.1 Certain I/Os during Programming are not Tri-stated

Change

User I/Os such as SPI_0_SS4, SPI_0_SS5, SPI_0_SS6, and SPI_0_SS7 on SmartFusion2 and MSIO14PB2, MSIO14NB2, MSIO15PB2, and MSIO15NB2 on IGLOO2 drive to a logic level 1 during IAP, auto programming, auto update, and programming recovery operations. Note that these I/Os are not bonded out in all die/packages, and that 005 and 010 device densities are not affected.

Action Required

Check if these I/Os are creating contention during programming operations.

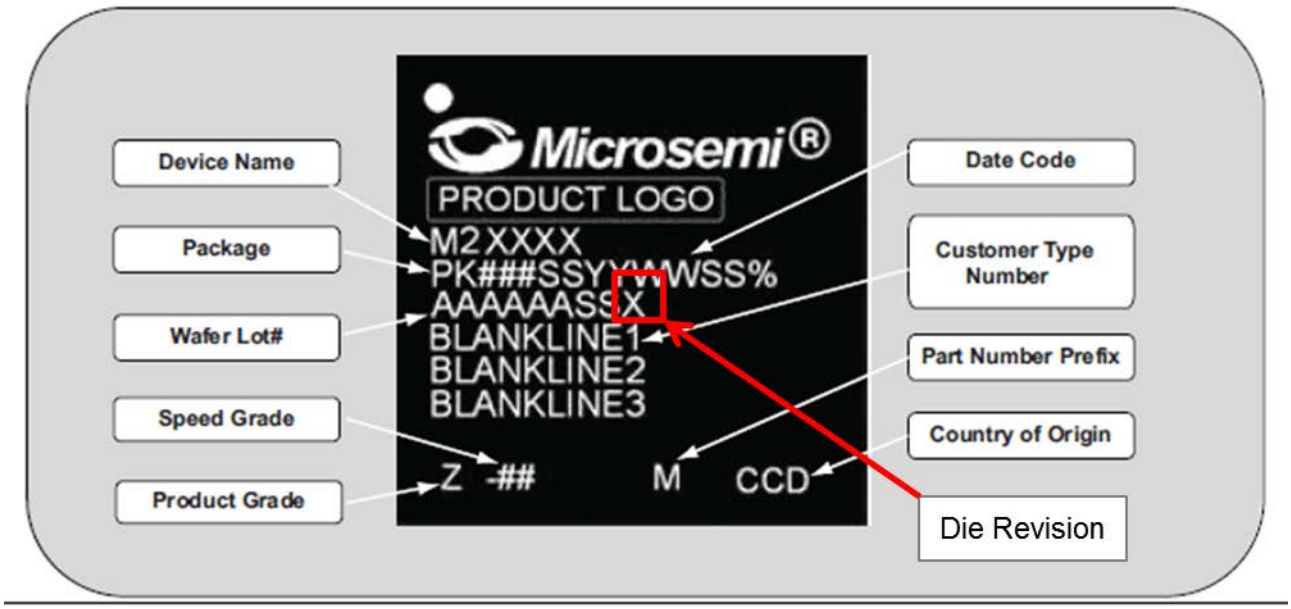
CAN 17005.2 Reserved eNVM Page

Change

In both SmartFusion2 and IGLOO2 050 device densities, for die revisions 0 and 1, you can write to eNVM pages at addresses 0x6003FC80-0x6003FFFF. This area is reserved for storing the device certificate and digest information. Die revision 2 and above prevent the user from overwriting the device certificate and digest information. Firmware drivers and documentation have been updated to indicate proper usage.

In both SmartFusion2 and IGLOO2 005 and 010 device densities, for die revisions 0, you can write to eNVM pages at addresses 0x6003FC80-0x6003FFFF. This area is reserved for storing the device certificate and digest information. Die revision 1 and above prevent the user from overwriting the device certificate and digest information. Firmware drivers and documentation have been updated to indicate proper usage.

The following figure illustrates the part marking specification for determining the die revision.



Application Impact

If you started your design on the affected die revision for the 005, 010, or 050 devices and subsequently purchased a new version, then the user's firmware will return an error when trying to write to the specific eNVM pages as the once previously available eNVM page is now used to store the device certificate.

Action Required

If you use eNVM at addresses, 0x6003FC80-0x6003FFFF, on the affected 005, 010, or 050 dies, you must move your data to another region in eNVM. You need to use the latest firmware drivers for writing to the eNVM.

CAN 17005.3 Proper Flash*Freeze Usage

Change

New guidelines to properly enter and exit Flash*Freeze have been published.

Action Required

See the new low power design guidelines at UG0444: SmartFusion2 and IGLOO2 Low Power Design User Guide.

CAN 17005.4 Programming Revision 0 090 and 150 Devices with Libero v11.7

Change

Using revision 0 of M2S090 or M2S150 devices, you must program the eNVM block independently from the FPGA fabric in Libero v11.6 or older. In Libero v11.7, eNVM only programming is not available for die revision 0.

Action Required

Contact Microsemi SoC Technical Support, if you want to program the eNVM block independently in revision 0 of M2S090 and M2S150 devices using Libero v11.7.

CAN 17005.5 New PUF Power-Up Timing Affects Auto-Update Programming Time

Change

As a result of decreasing the PUF power-up time, a side effect is observed. The auto-update programming time is reduced by 900 ms.

Action Required

None

CAN 17005.6 I/O Glitch during Power-Down

Change

During power-down, a glitch may appear on MSIO and MSIOD I/Os for any SmartFusion2 or IGLOO2 devices.

Application Impact

This glitch may be high enough for a receiver on a separate power domain with a different power-down characteristic to view the glitch as a valid signal for a short period of time.

Action Required

See the board design guidelines at AC393: Board Design Guidelines for SmartFusion2 SoC and IGLOO2 FPGAs Application Note for workarounds.

CAN 17005.7 SSN Analyzer uses 0 ns as the Default

Microsemi previously defined SSOs as any outputs that transition in phase within a 1 ns window of each other. The current SSN analyzer uses a worst case 0 ns as the default window between I/O's switching. Currently, the tool does not offer a typical (1 ns) SSN analysis; it is expected in an upcoming release.

CAN 17005.8 SerDes IBIS-AMI Model does not Support Programmable Transmit Amplitude

The SERDES IBIS-AMI model does not support the programmable transmit amplitude parameter. Changes to this parameter in the AMI model have no impact on the simulation. The AMI model transmit amplitude always produces a 1200 mV value.

Products Affected by this Change: PCN17005 notifies the changes and their affected parts of all SmartFusion2 and IGLOO2 devices. See the spreadsheet that lists all the affected SmartFusion2 and IGLOO2 devices: PCN17005:_SmartFusion2_and_IGLOO2_Affected_Devices List

Contact Information: Microsemi SoC Marketing

If you have any questions, please contact Microsemi's SoC Technical Support at soc_tech@microsemi.com.

Regards,

Microsemi Corporation

Any projected dates in this PCN are based on the most current product information at the time this PCN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Microsemi Sales Office, the factory contact shown above, or your local distributor.

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