TEXAS INSTRUMENTS

LMP90100, LMP90099, LMP90098, LMP90097

SNAS510S – JANUARY 2011 – REVISED JANUARY 2016

LMP90100 and LMP9009x Sensor AFE System: Multichannel, Low-Power, 24-Bit Sensor AFE With True Continuous Background Calibration

1 Features

- 24-Bit, Low-Power Sigma-Delta ADC
- True Continuous Background Calibration at all Gains
- In-Place System Calibration Using Expected Value Programming
- Low-Noise Programmable Gain (1x to 128x)
- Continuous Background Open / Short and Out-of-Range Sensor Diagnostics
- 8 Output Data Rates (ODR) With Single-Cycle Settling
- 2 Matched Excitation Current Sources From 100 µA to 1000 µA (LMP90100/LMP90098)
- 4-DIFF / 7-SE Inputs (LMP90100/LMP90099)
- 2-DIFF / 4-SE Inputs (LMP90098/LMP90097)
- 7 General-Purpose Input/Output Pins
- Chopper-Stabilized Buffer for Low Offset
- SPI 4/3-wire With CRC Data Link Error Detection
- 50-Hz to 60-Hz Line Rejection at ODR ≤13.42 SPS
- Independent Gain and ODR Selection per Channel
- Supported by WEBENCH® Sensor AFE Designer
- Automatic Channel Sequencer
- **Key Specifications**
  - ENOB/NFR Up to 21.5/19 Bits
  - Offset Error (Typical) 8.4 nV
  - Gain Error (Typical) 7 ppm
  - Total Noise < 10 µV-rms
  - Integral Nonlinearity (INL Maximum) ± 15 ppm of FSR
  - Output Data Rates (ODR) 1.6775 - 214.65 SPS
  - Analog Voltage, VA 2.85 to 5.5 V
  - Operating Temp Range –40°C to 125°C
  - 28-Pin HTSSOP Exposed Pad

2 Applications

- Temperature and Pressure Transmitters
- Strain Gauge Interface
- Industrial Process Control

3 Description

The LMP90xxx is a highly integrated, multichannel, low-power, 24-bit Sensor AFEs. The devices features a precision, 24-bit Sigma-Delta analog-to-digital converter (ADC) with a low-noise programmable gain amplifier and a fully differential high-impedance analog input multiplexer. A true continuous background calibration feature allows calibration at all gains and output data rates without interrupting the signal path. The background calibration feature essentially eliminates gain and offset errors across temperature and time, providing measurement accuracy without sacrificing speed and power consumption.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMP90097	HTSSOP (28)	9.70 mm x 4.40 mm
LMP90098		
LMP90099		
LMP90100		

(1) For all available packages, see the orderable addendum at the end of the datasheet.
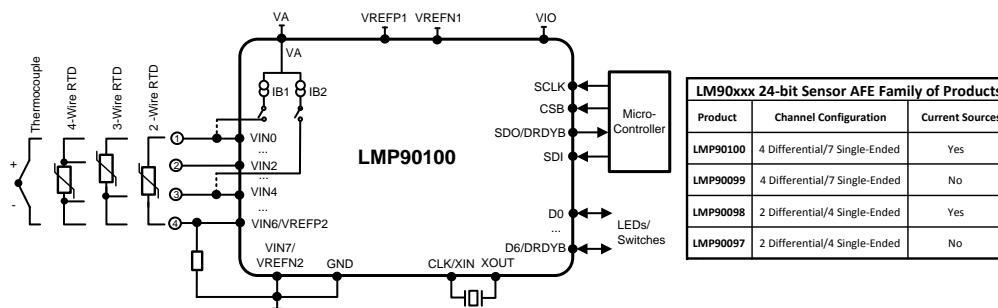
4 Typical Application Schematic

LM90xxx 24-bit Sensor AFE Family of Products		
Product	**Channel Configuration**	**Current Sources**
LMP90100	4 Differential/7 Single-Ended	Yes
LMP90099	4 Differential/7 Single-Ended	No
LMP90098	2 Differential/4 Single-Ended	Yes
LMP90097	2 Differential/4 Single-Ended	No

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision R (January 2015) to Revision S	Page
• Changed Buffer Enable/Disable.	54
• Changed BUF_EN = 1 to 0.	56

Changes from Revision Q (December 2014) to Revision R	Page
• Added SDO Timing Requirements back in.	12

Changes from Revision P (March 2013) to Revision Q	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Added footnote to INL, GE, and Crosstalk specifications.	6
• Changed t_{DOD1} specification to 27ns	12
• Added sentence to the end of the Reset and Restart section	32
• Deleted CH_STS from Compute the CRC... sentence	40

| Changes from Revision O (March 2013) to Revision P	Page
• Changed layout of National Data Sheet to TI format	48

6 Description (continued)

Another feature of the LMP90100/LMP90099/LMP90098/LMP90097 is continuous background sensor diagnostics, allowing the detection of open and short-circuit conditions and out-of-range signals, without requiring user intervention, resulting in enhanced system reliability.

Two sets of independent external reference voltage pins allow multiple ratiometric measurements. In addition, two matched programmable current sources are available in the LMP90100/LMP90098 to excite external sensors such as resistive temperature detectors and bridge sensors. Furthermore, seven GPIO pins are provided for interfacing to external LEDs and switches to simplify control across an isolation barrier.

Collectively, these features make the LMP90100/LMP90099/LMP90098/LMP90097 complete analog front-ends for low-power, precision sensor applications such as temperature, pressure, strain gauge, and industrial process control. The LMP90100/LMP90099/LMP90098/LMP90097 are ensured over the extended temperature range of -40°C to +125°C and are available in a 28-pin HTSSOP package with an exposed pad.

7 Pin Configuration and Functions

HTSSOP (PWP0028A) PACKAGE
28 PINS
TOP VIEW
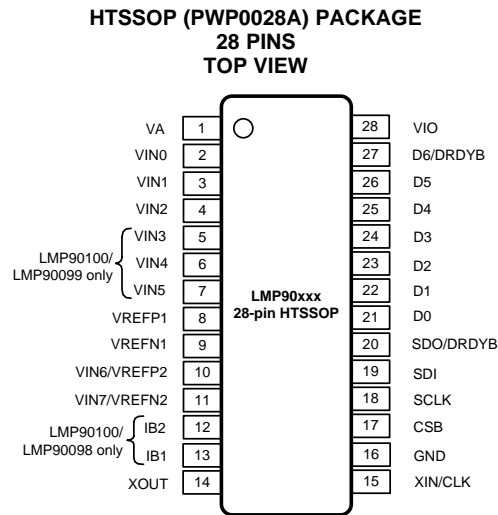
See below for specific information regarding options LMP90099, LMP90098, and LMP90097.

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
VA	1	Analog Supply	Analog power supply pin
VIN0 to VIN2	2 to 4	Analog Input	Analog input pins
VIN3 to VIN5	5 to 7 (LMP90100, LMP90099 only)	Analog Input	Analog input pins
VIN3 to VIN5	5 - 7 (LMP90098, LMP90097 only)	No Connect	No connect: must be left unconnected
VREFP1	8	Analog Input	Positive reference input
VREFN1	9	Analog Input	Negative reference input
VIN6 / VREFP2	10	Analog Input	Analog input pin or VREFP2 input
VIN7 / VREFN2	11	Analog Input	Analog input pin or VREFN2 input
IB2, IB1	12 to 13 (LMP90100, LMP90098 only)	Analog Output	Excitation current sources for external RTDs
IB2, IB1	12 - 13 (LMP90099, LMP90097 only)	No Connect	No connect: must be left unconnected
XOUT	14	Analog Output	External crystal oscillator connection
XIN / CLK	15	Analog Input	External crystal oscillator connection or external clock input
GND	16	Ground	Power supply ground
CSB	17	Digital Input	Chip select bar
SCLK	18	Digital Input	Serial clock
SDI	19	Digital Input	Serial data input
SDO / DRDYB	20	Digital Output	Serial data output and data ready bar
D0 to D5	21 to 26	Digital IO	General purpose input/output (GPIO) pins
D6 / DRDYB	27	Digital IO	General purpose input/output pin or data ready bar
VIO	28	Digital Supply	Digital input/output supply pin
Thermal Pad	—	—	You can leave this thermal pad floating.

8 Specifications

8.1 Absolute Maximum Ratings

See [1] [2] [3].

		MIN	MAX	UNIT
V_A	Analog Supply Voltage	-0.3	6.0	V
V_{IO}	Digital I/O Supply Voltage	-0.3	6.0	V
V_{REF}	Reference Voltage	-0.3	VA+0.3	V
	Voltage on Any Analog Input Pin to GND [4]	-0.3	VA+0.3	V
	Voltage on Any Digital Input PIN to GND [4]	-0.3	VIO+0.3	V
	Voltage on SDO [4]	-0.3	VIO+0.3	V
	Input Current at Any Pin [4]		5	mA
	Output Current Source or Sink by SDO		3	mA
	Total Package Input and Output Current		20	mA
T_{JMAX}	Junction Temperature		150	°C
T_{stg}	Storage Temperature	−65	150	°C

(1) All voltages are measured with respect to GND, unless otherwise specified
(2) *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. *Recommended Operating Conditions* indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics* . The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) For soldering specifications: see product folder at www.ti.com and SNOA549.
(4) When the input voltage (VIN) exceeds the power supply (VIN < GND or VIN > VA), the current at that pin must be limited to 5mA and VIN has to be within the Absolute Maximum Rating for that pin. The 20 mA package input current rating limits the number of pins that can safely exceed the power supplies with current flow to four pins.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1250	
		Machine Model (MM)	+200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_A	Analog Supply Voltage	2.85	5.5	V
V_{IO}	Digital I/O Supply Voltage	2.7	5.5	V
V_{IN}	Full Scale Input Range		$\pm V_{REF}$ / PGA	V
V_{REF}	Reference Voltage	0.5	V_A	V
	Temperature Range for Electrical Characteristics	$T_{MIN} = -40$	$T_{MAX} = 125$	°C
T_A	Operating Temperature Range	−40	125	°C

8.4 Thermal Information

THERMAL METRIC[1]	LMP90100, LMP9009x	UNIT
	PWP	
	28 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance [2]	41	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$ AND θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A) / \theta_{JA}$.

8.5 Electrical Characteristics

Unless otherwise noted, the key for the condition is (VA = VIO = VREF) / ODR (SPS) / buffer / calibration / gain. The typical values apply for T_A = 25°C.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
n	Resolution				24		Bits
ENOB / NFR	Effective Number of Bits and Noise Free Resolution	3V / all / ON / OFF / all. Shorted input.			Table 1		Bits
		5V / all / ON / OFF / all. Shorted input.			Table 3		Bits
ODR	Output Data Rates			1.6675	Table 1	214.6	SPS
	Gain	FGA × PGA		1	Table 1	128	
INL	Integral Non-Linearity[1]	3V / 214.65 / ON / ON / 1		-15	± 7	+15	ppm
		3V & 5V / 214.65 / ON / ON / 16			± 15		ppm
	Total Noise	3V / all / ON / ON / all. Shorted input.			Table 2		µV
		5V / all / ON / OFF / all. Shorted input.			Table 4		µV
OE	Offset Error	3V & 5V / all / ON or OFF / ON / all			Below Noise Floor (rms)		µV
		3V / 214.65 / ON / ON / 1			1.22	9.52	µV
		3V / 214.65 / ON / ON / 128			0.00838	0.70	µV
		5V / 214.65 / ON / ON / 1			1.79	8.25	µV
		5V / 214.65 / ON / ON / 128			0.0112	0.63	µV
	Offset Drift Over Temp[1]	3V & 5V / 214.65 / ON or OFF / OFF / 1-8			100		nV/°C
		3V & 5V / 214.65 / ON / ON / 1-8			3		nV/°C
		3V & 5V / 214.65 / ON / OFF / 16			25		nV/°C
		3V & 5V / 214.65 / ON / ON / 16			0.4		nV/°C
		3V & 5V / 214.65 / ON / OFF / 128			6		nV/°C
		3V & 5V / 214.65 / ON / ON / 128			0.125		nV/°C
	Offset Drift over Time [1]	5V / 214.65 / ON / OFF / 1, T_A = 150°C			2360		nV / 1000 hours
		5V / 214.65 / ON / ON / 1, T_A = 150°C			100		nV / 1000 hours
GE	Gain Error[1]	3V & 5V / 214.65 / ON / ON / 1	25°C		7		ppm
			Full Range	-80		80	
		3V & 5V / 13.42 / ON / ON / 16			50		ppm
		3V & 5V / 13.42 / ON / ON / 64			50		ppm
		3V & 5V / 13.42 / ON / ON / 128			100		ppm
	Gain Drift over Temp [1]	3V & 5V / 214.65 / ON / ON / all			0.5		ppm/°C
	Gain Drift over Time [1]	5V / 214.65 / ON / OFF / 1, T_A = 150°C			5.9		ppm / 1000 hours
		5V / 214.65 / ON / ON / 1, T_A = 150°C			1.6		ppm / 1000 hours
CONVERTER'S CHARACTERISTIC							
CMRR	Input Common Mode Rejection Ratio	DC, 3V / 214.65 / ON / ON / 1	25°C		117		dB
			Full Range	70			
		DC, 5V / 214.65 / OFF / OFF / 1	25°C		120		dB
			Full Range	90			
		50/60 Hz, 5V / 214.65 / OFF / OFF / 1			117		dB
	Reference Common Mode Rejection	VREF = 2.5V			101		dB

(1) This parameter is specified by design and/or characterization and is not tested in production

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Electrical Characteristics (continued)

Unless otherwise noted, the key for the condition is (VA = VIO = VREF) / ODR (SPS) / buffer / calibration / gain. The typical values apply for $T_A = 25°C$.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
PSRR	Power Supply Rejection Ratio	DC, 3V / 214.65 / ON / ON / 1		75	115		dB
		DC, 5V / 214.65 / ON / ON / 1			112		dB
NMRR	Normal Mode Rejection Ratio [1]	47 Hz to 63 Hz, 5V / 13.42 / OFF / OFF / 1	25°C				dB
			Full Range	78			
	Cross-talk [1]	3V / 214.65 / OFF / OFF / 1	25°C		136		dB
			Full Range	95			
		5V / 214.65 / OFF / OFF / 1	25°C		143		dB
			Full Range	95			
POWER SUPPLY CHARACTERISTICS							
VA	Analog Supply Voltage			2.85	3.0	5.5	V
VIO	Digital Supply Voltage			2.7	3.3	5.5	V
IVA	Analog Supply Current	3V / 13.42 / OFF / OFF / 1, ext. CLK	25°C		400		µA
			Full Range			500	
		5V / 13.42 / OFF / OFF / 1, ext. CLK	25°C		464		µA
			Full Range			555	
		3V / 13.42 / ON / OFF / 64, ext. CLK	25°C		600		µA
			Full Range			700	
		5V / 13.42 / ON / OFF / 64, ext. CLK	25°C		690		µA
			Full Range			800	
		3V / 214.65 / ON / OFF / 64, int. CLK	25°C		1547		µA
			Full Range			1700	
		5V / 214.65 / ON / OFF / 64, int. CLK	25°C		1760		µA
			Full Range			2000	
		3V / 214.65 / OFF / OFF / 1, int. CLK	25°C		826		µA
			Full Range			1000	
		5V / 214.65 / OFF / OFF / 1, int. CLK	25°C		941		µA
			Full Range			1100	
		Standby, 3V , int. CLK			3	10	µA
		Standby, 3V , ext. CLK			257		µA
		Standby, 5V, int. CLK			5	15	µA
		Standby, 3V, ext. CLK			300		µA
		Power-down, 3 V, int/ext CLK	25°C		2.6		µA
			Full Range			5	
		Power-down, 5 V, int/ext CLK	25°C		4.6		µA
			Full Range			9	
REFERENCE INPUT							
VREFP	Positive Reference			VREFN + 0.5		VA	V
VREFN	Negative Reference			GND		VREFP - 0.5	V
VREF	Differential Reference	VREF = VREFP - VREFN		0.5		VA	V
ZREF	Reference Impedance	3 V / 13.42 / OFF / OFF / 1			10		MΩ
IREF	Reference Input	3 V / 13.42 / ON or OFF / ON or OFF / all			±2		µA
CREFP	Capacitance of the Positive Reference	See [1], gain = 1			6		pF

Electrical Characteristics (continued)

Unless otherwise noted, the key for the condition is (VA = VIO = VREF) / ODR (SPS) / buffer / calibration / gain. The typical values apply for T_A = 25°C.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
CREFN	Capacitance of the Negative Reference	See [1], gain = 1			6		pF
ILREF	Reference Leakage Current	Power-down			1		nA
ANALOG INPUT							
VINP	Positive Input	Gain = 1-8, buffer ON		GND + 0.1		VA - 0.1	V
		Gain = 16 - 128, buffer ON		GND + 0.4		VA - 1.5	V
		Gain = 1-8, buffer OFF		GND		VA	V
VINN	Negative Input	Gain = 1-8, buffer ON		GND + 0.1		VA - 0.1	V
		Gain = 16 - 128, buffer ON		GND + 0.4		VA - 1.5	V
		Gain = 1-8, buffer OFF		GND		VA	V
VIN	Differential Input	VIN = VINP - VINN			±VREF / PGA		
ZIN	Differential Input Impedance	ODR = 13.42 SPS			15.4		MΩ
CINP	Capacitance of the Positive Input	5V / 214.65 / OFF / OFF / 1			4		pF
CINN	Capacitance of the Negative Input	5V / 214.65 / OFF / OFF / 1			4		pF
IIN	Input Leakage Current	3V & 5V / 13.42 / ON / OFF / 1-8			500		pA
		3V & 5V / 13.42 / ON / OFF / 16 - 128			100		pA
DIGITAL INPUT CHARACTERISTICS at VA = VIO = VREF = 3.0V							
VIH	Logical "1" Input Voltage			0.7 x VIO			V
VIL	Logical "0" Input Voltage					0.3 x VIO	V
IIL	Digital Input Leakage Current			-10		+10	µA
VHYST	Digital Input Hysteresis				0.1 x VIO		V
DIGITAL OUTPUT CHARACTERISTICS at VA = VIO = VREF = 3.0V							
VOH	Logical "1" Output Voltage	Source 300 µA		2.6			V
VOL	Logical "0" Output Voltage	Sink 300 µA				0.4	V
IOZH, IOZL	Tri-state Leakage Current			-10		10	µA
COUT	Tri-state Capacitance	See [1]			5		pF
EXCITATION CURRENT SOURCES CHARACTERISTICS (LMP90100/LMP90098 only)							
IB1, IB2	Excitation Current Source Output				0, 100, 200, 300, 400, 500, 600, 700, 800, 900, 1000		µA
	IB1/IB2 Tolerance	VA = VREF = 3 V	25°C		2.5%		
			Full Range	-7%		7%	
		VA = VREF = 5 V	25°C		0.2%		
			Full Range	-3.5%		3.5%	
	IB1/IB2 Output Compliance Range	VA = 3.0 V & 5.0 V, IB1/IB2 = 100 µA to 1000 µA			VA - 0.8		V
	IB1/IB2 Regulation	VA = 5.0 V, IB1/IB2 = 100 µA to 1000 µA			0.07		% / V

Electrical Characteristics (continued)

Unless otherwise noted, the key for the condition is (VA = VIO = VREF) / ODR (SPS) / buffer / calibration / gain. The typical values apply for T_A = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IBTC	IB1/IB2 Drift	VA = 3.0 V			95		ppm/°C
		VA = 5.0 V			60		ppm/°C
IBMT	IB1/IB2 Matching	3 V and 5 V / 214.65 / OFF / OFF / 1, IB1/IB2 = 100 µA	25°C		0.34%		
			Full Range			1.53%	
		3 V and 5 V / 214.65 / OFF / OFF / 1, IB1/IB2 = 200 µA	25°C		0.22%		
			Full Range			1%	
		3V & 5V / 214.65 / OFF / OFF / 1, IB1/IB2 = 300 µA	25°C		0.2%		
			Full Range			0.85%	
		3 V and 5 V / 214.65 / OFF / OFF / 1, IB1/IB2 = 400 µA	25°C		0.15%		
			Full Range			0.8%	
		3 V and 5 V / 214.65 / OFF / OFF / 1, IB1/IB2 = 500 µA	25°C		0.14%		
			Full Range			0.7%	
		3 V and 5 V / 214.65 / OFF / OFF / 1, IB1/IB2 = 600 µA	25°C		0.13%		
			Full Range			0.7%	
		3 V and 5 V / 214.65 / OFF / OFF / 1, IB1/IB2 = 700 µA	25°C		0.075%		
			Full Range			0.65%	
		3 V and 5 V / 214.65 / OFF / OFF / 1, IB1/IB2 = 800 µA	25°C		0.085%		
			Full Range			0.6%	
		3 V and 5 V / 214.65 / OFF / OFF / 1, IB1/IB2 = 900 µA	25°C		0.11%		
			Full Range			0.55%	
		3 V and 5 V / 214.65 / OFF / OFF / 1, IB1/IB2 = 1000 µA	25°C		0.11%		
			Full Range			0.45%	
IBMTC	IB1/IB2 Matching Drift	VA = 3.0 V and 5.0 V, IB1/IB2 = 100 µA to 1000 µA			2		ppm/°C
INTERNAL/EXTERNAL CLK							
CLKIN	Internal Clock Frequency				893		kHz
CLKEXT	External Clock Frequency	See [(1)]		1.8	3.5717	7.2	MHz
	External Crystal Frequency	Input Low Voltage			0		V
		Input High Voltage			1		V
		Frequency		1.8	3.5717	7.2	MHz
		Start-up time			7		ms
SCLK	Serial Clock					10	MHz

Table 1. ENOB (Noise Free Resolution) vs. Sampling Rate and Gain at VA = VIO = VREF = 3 V

ODR (SPS)	Gain of the ADC							
	1	2	4	8	16	32	64	128
1.6775	20.5 (18)	20.5 (18)	19.5 (17)	19 (16.5)	20.5 (18)	19.5 (17)	19 (16.5)	18 (15.5)
3.355	20 (17.5)	20 (17.5)	19 (16.5)	18.5 (16)	20 (17.5)	19 (16.5)	18.5 (16)	17 (14.5)
6.71	19.5 (17)	19.5 (17)	18.5 (16)	18 (15.5)	19.5 (17)	18.5 (16)	17.5 (15)	17 (14.5)
13.42	19 (16.5)	18.5 (16)	18 (15.5)	17.5 (15)	19 (16.5)	18 (15.5)	17.5 (15)	16.5 (14)
26.83125	20.5 (18)	20 (17.5)	19.5 (17)	19 (16.5)	20 (17.5)	19 (16.5)	18 (15.5)	17.5 (15)
53.6625	20 (17.5)	19.5 (17)	19 (16.5)	18.5 (16)	19.5 (17)	18.5 (16)	17.5 (15)	17 (14.5)
107.325	19.5 (17)	19 (16.5)	18.5 (16)	18 (15.5)	19 (16.5)	18 (15.5)	17 (14.5)	16.5 (14)
214.65	19 (16.5)	18.5 (16)	18 (15.5)	17.5 (15)	18.5 (16)	17.5 (15)	17 (14.5)	16 (13.5)

Table 2. RMS Noise (µV) vs. Sampling Rate and Gain at VA = VIO = VREF = 3 V

ODR (SPS)	Gain of the ADC							
	1	2	4	8	16	32	64	128
1.6775	3.08	1.90	1.53	1.27	0.23	0.21	0.15	0.14
3.355	4.56	2.70	2.21	1.67	0.34	0.27	0.24	0.26
6.71	6.15	4.10	3.16	2.39	0.51	0.40	0.37	0.35
13.42	8.60	5.85	4.29	3.64	0.67	0.54	0.51	0.49
26.83125	3.35	2.24	1.65	1.33	0.33	0.27	0.26	0.25
53.6625	4.81	3.11	2.37	1.90	0.44	0.39	0.37	0.36
107.325	6.74	4.51	3.38	2.66	0.63	0.54	0.52	0.49
214.65	9.52	6.37	4.72	3.79	0.90	0.79	0.72	0.70

Table 3. ENOB (Noise Free Resolution) vs. Sampling Rate and Gain at VA = VIO = VREF = 5 V

SPS	Gain of the ADC							
	1	2	4	8	16	32	64	128
1.6775	21.5 (19)	21.5 (19)	20.5 (18)	20 (17.5)	21 (18.5)	20.5 (18)	19.5 (17)	18.5 (16)
3.355	21 (18.5)	21 (18.5)	20 (17.5)	19.5 (17)	20.5 (18)	20 (17.5)	19 (16.5)	18 (15.5)
6.71	20.5 (18)	20 (17.5)	19.5 (17)	19 (16.5)	20 (17.5)	19.5 (17)	19 (16.5)	17.5 (15)
13.42	20 (17.5)	19.5 (17)	19 (16.5)	18.5 (16)	20 (17.5)	19 (16.5)	18 (15.5)	17.5 (15)
26.83125	21.5 (19)	21 (18.5)	20.5 (18)	20 (17.5)	21 (18.5)	20 (17.5)	19.5 (17)	18 (15.5)
53.6625	21 (18.5)	20.5 (18)	20 (17.5)	19.5 (17)	20.5 (18)	19.5 (17)	18.5 (16)	17.5 (15)
107.325	20.5 (18)	20 (17.5)	19.5 (17)	19 (16.5)	20 (17.5)	19 (16.5)	18 (15.5)	17 (14.5)
214.65	20 (17.5)	19.5 (17)	19 (16.5)	18.5 (16)	19.5 (17)	18.5 (16)	17.5 (15)	16.5 (14)

Table 4. RMS Noise (µV) vs. Sampling Rate and Gain at VA = VIO = VREF = 5 V

SPS	Gain of the ADC							
	1	2	4	8	16	32	64	128
1.6775	2.68	1.65	1.24	1.00	0.22	0.19	0.17	0.16
3.355	3.86	2.36	1.78	1.47	0.34	0.27	0.22	0.22
6.71	5.23	3.49	2.47	2.09	0.44	0.34	0.30	0.32
13.42	7.94	5.01	3.74	2.94	0.61	0.50	0.45	0.43
26.83125	2.90	1.86	1.34	1.08	0.29	0.24	0.23	0.23
53.6625	4.11	2.60	1.90	1.50	0.39	0.35	0.32	0.31
107.325	5.74	3.72	2.72	2.11	0.56	0.48	0.46	0.44
214.65	8.25	5.31	3.82	2.97	0.79	0.68	0.64	0.63

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

8.6 SPI Timing Requirements

Unless otherwise noted, specified limits apply for VA = VIO = 3.0 V.

		MIN	NOM	MAX	UNIT
f_{SCLK}				10	MHz
t_{CH}	SCLK High time	$0.4 / f_{SCLK}$			ns
t_{CL}	SCLK Low time	$0.4 / f_{SCLK}$			ns
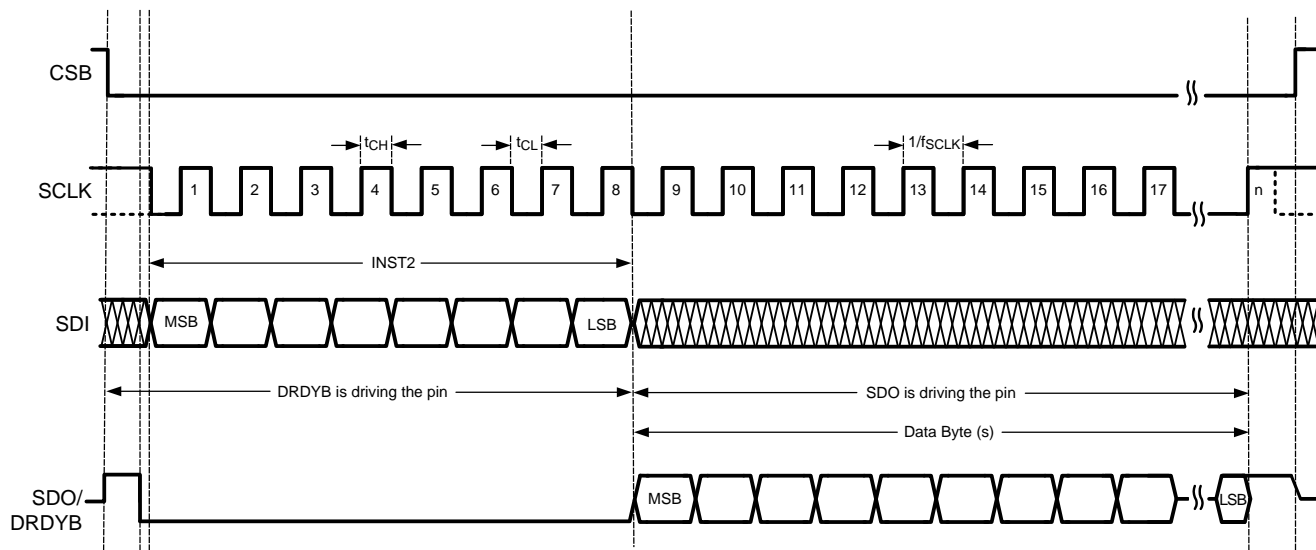
Figure 1. SPI Timing Diagram

8.7 CBS Setup and Hold Timing Requirements

Unless otherwise noted, specified limits apply for VA = VIO = 3.0 V.

		MIN	NOM	MAX	UNIT
t_{CSSU}	CSB Setup time prior to an SCLK rising edge	5			ns
t_{CSH}	CSB Hold time after the last rising edge of SCLK	6			ns
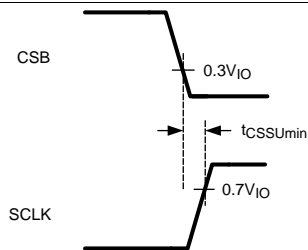
Figure 2. CBS Setup Timing
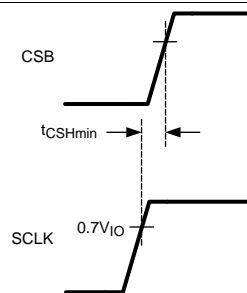
Figure 3. CSB Hold Timing

8.8 SCLK and SDI Timing Requirements

Unless otherwise noted, specified limits apply for VA = VIO = 3.0 V.

		MIN	NOM	MAX	UNIT
t_{CLKR}	SCLK Rise time		1.15		ns
t_{CLKF}	SCLK Fall time		1.15		ns
t_{DISU}	SDI Setup time prior to an SCLK rising edge	5			ns
t_{DIH}	SDI Hold time after an SCLK rising edge	6			ns
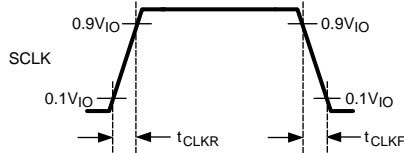
Figure 4. SCLK Rise and Fall Time
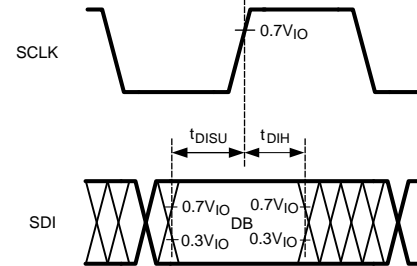
Figure 5. SDI Setup and Hold Time

8.9 SDO Timing Requirements

Unless otherwise noted, specified limits apply for VA = VIO = 3.0 V.

		MIN	NOM	MAX	UNIT
t_{DOA}	SDO Access time after a SCLK falling edge			35	ns
t_{DOH}	SDO Hold time after a SCLK falling edge	5			ns
t_{DOD1}	SDO Disable time after the rising edge of CSB			27	ns
t_{DOD2}	SDO Disable time after either edge of SCLK			27	ns
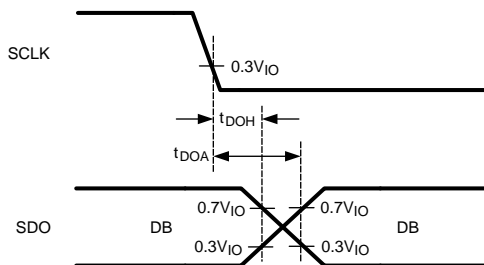
Figure 6. SDO and SCLK Timing
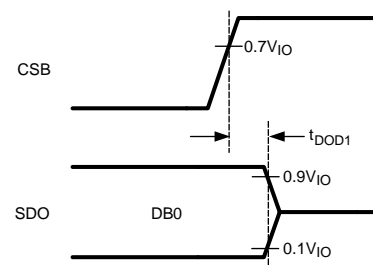
Figure 7. SDO and $\overline{CS}$ Timing
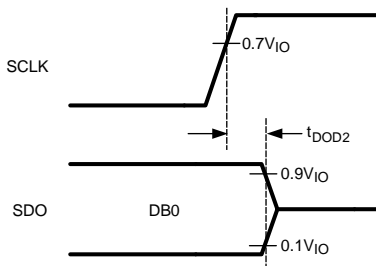
Figure 8. SDO Disable and SCLK Timing
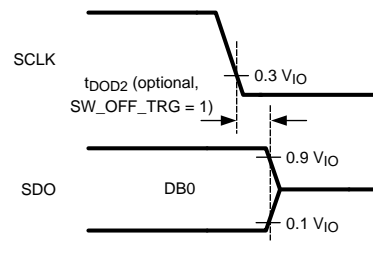
Figure 9. SDO Disable and SCLK Timing

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

8.10 SDO and DRDYB Timing Requirements

Unless otherwise noted, specified limits apply for VA = VIO = 3.0 V.

			MIN	NOM	MAX	UNIT
t_{DOE}	SDO Enable time from the falling edge of the 8th SCLK				35	ns
t_{DOR}	SDO Rise time	See [1]			7	ns
t_{DOF}	SDO Fall time	See [1]			7	ns
t_{DRDYB}	Data Ready Bar pulse at every 1/ODR second, see Figure 62	ODR ≤ 13.42 SPS			64	µs
		13.42 < ODR ≤ 214.65 SPS			4	

(1) This parameter is specified by design and/or characterization and is not tested in production
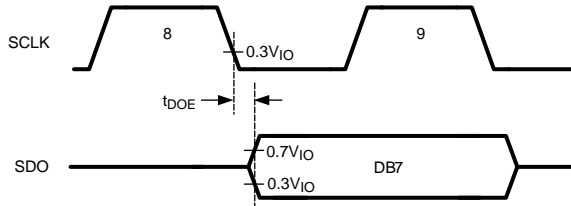
Figure 10. SDO and SCLK Enable Timing
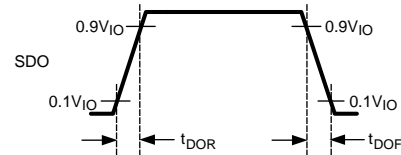
Figure 11. SDO Rise and Fall Timing

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

8.11 Typical Characteristics

Unless otherwise noted, specified limits apply for VA = VIO = VREF = 3.0 V. The maximum and minimum values apply for T_A = T_{MIN} to T_{MAX}; the typical values apply for T_A = 25°C.
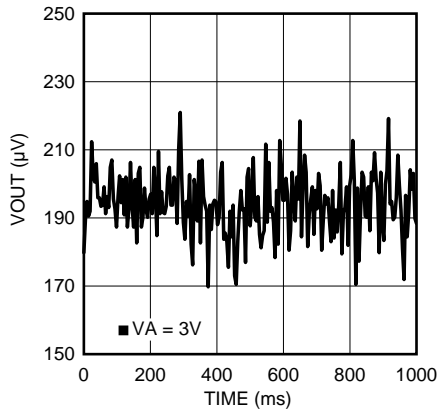
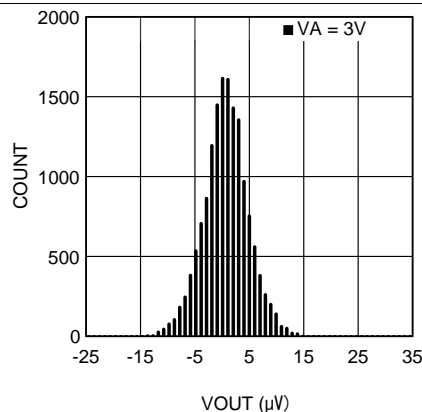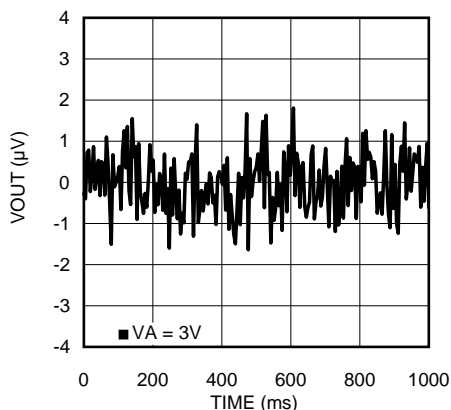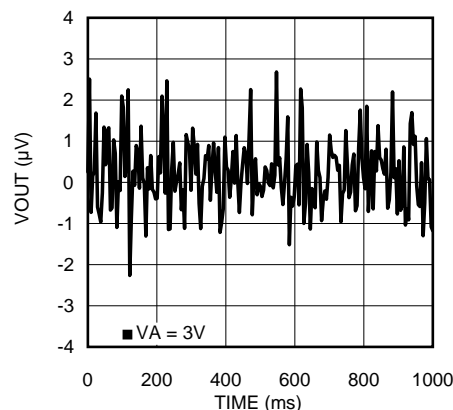**Figure 12. Noise Measurement Without Calibration at Gain = 1**
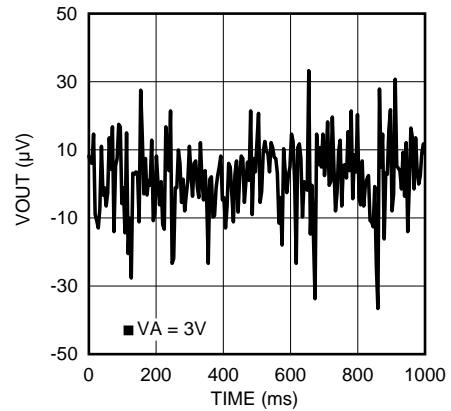
Figure 13. Noise Measurement With Calibration at Gain = 1
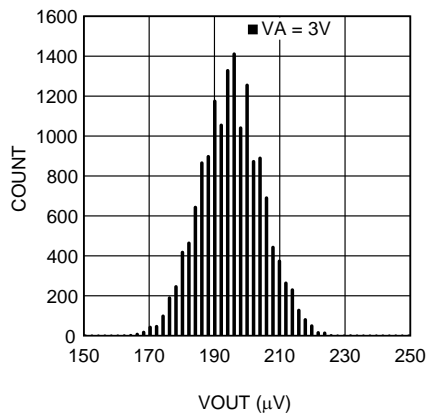
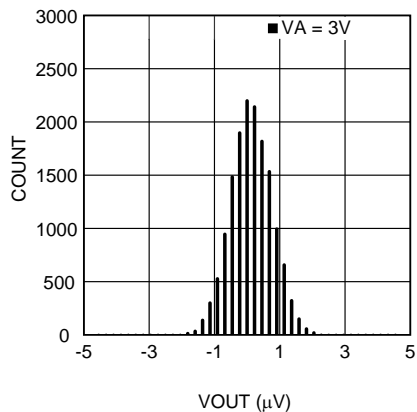
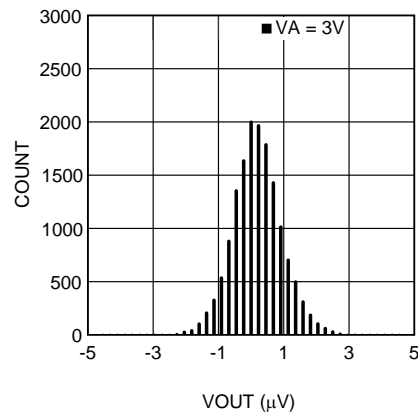**Figure 14. Histogram Without Calibration at Gain = 1**
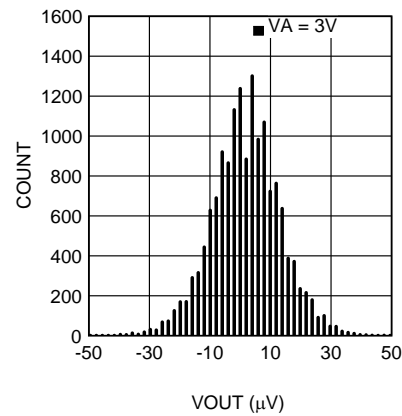
Figure 15. Histogram With Calibration at Gain = 1
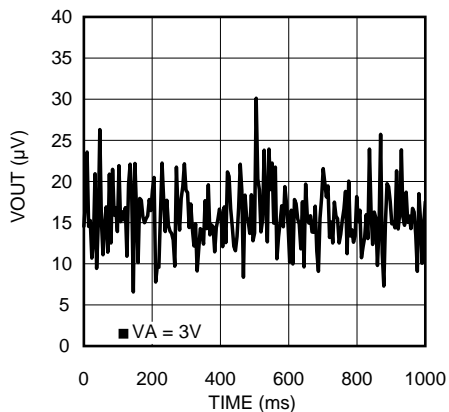
Figure 16. Noise Measurement Without Calibration at Gain = 8
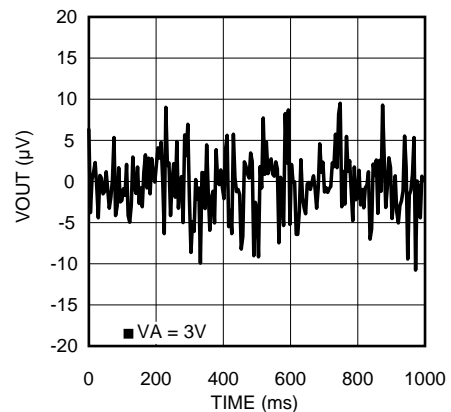
Figure 17. Noise Measurement With Calibration at Gain = 8

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Typical Characteristics (continued)

Unless otherwise noted, specified limits apply for VA = VIO = VREF = 3.0 V. The maximum and minimum values apply for T_A = T_{MIN} to T_{MAX}; the typical values apply for T_A = 25°C.
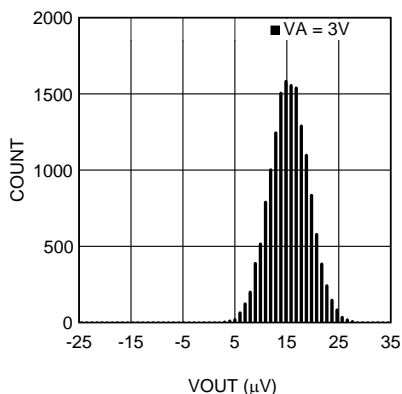
Figure 18. Histogram Without Calibration at Gain = 8

Figure 19. Histogram With Calibration at Gain = 8

Figure 20. Noise Measurement Without Calibration at Gain = 128

Figure 21. Noise Measurement With Calibration at Gain = 128

Figure 22. Histogram Without Calibration at Gain = 128

Figure 23. Histogram With Calibration at Gain = 128

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Typical Characteristics (continued)

Unless otherwise noted, specified limits apply for VA = VIO = VREF = 3.0 V. The maximum and minimum values apply for T_A = T_{MIN} to T_{MAX}; the typical values apply for T_A = 25°C.
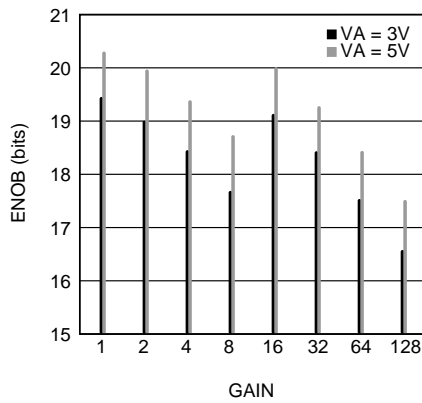
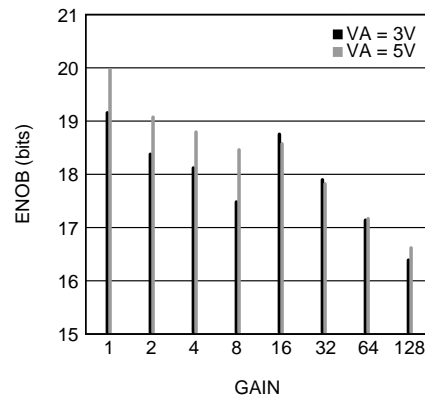**Figure 24. ENOB vs. Gain Without Calibration at ODR = 13.42 SPS**

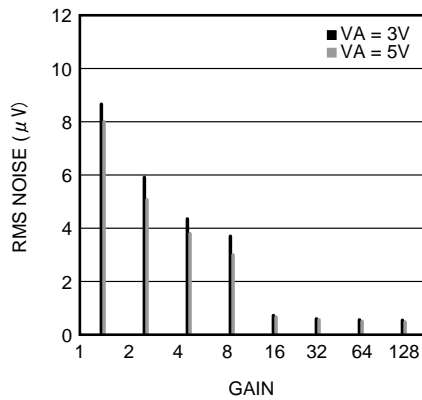**Figure 25. ENOB vs. Gain With Calibration at ODR = 13.42 SPS**

Figure 26. Noise vs. Gain Without Calibration at ODR = 13.42 SPS
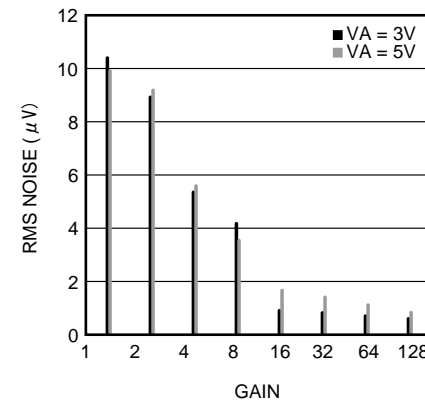

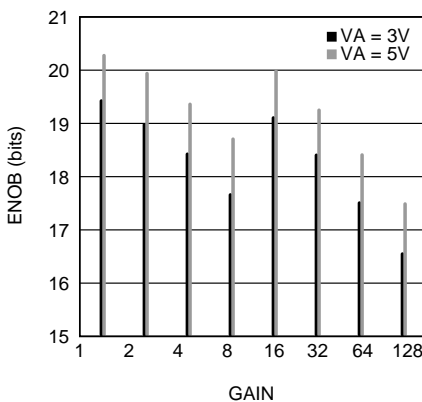**Figure 27. Noise vs. Gain With Calibration at ODR = 13.42 SPS**

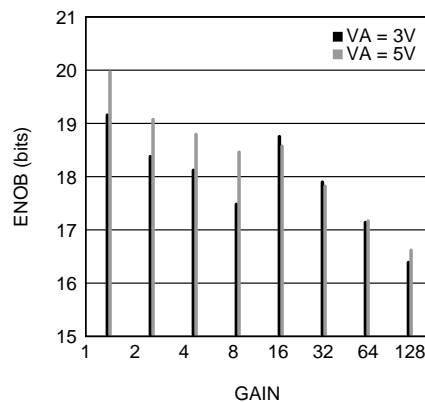**Figure 28. ENOB vs. Gain Without Calibration at ODR = 214.65 SPS**

Figure 29. ENOB vs. Gain With Calibration at ODR = 214.65 SPS

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Typical Characteristics (continued)

Unless otherwise noted, specified limits apply for VA = VIO = VREF = 3.0 V. The maximum and minimum values apply for T_A = T_{MIN} to T_{MAX}; the typical values apply for T_A = 25°C.
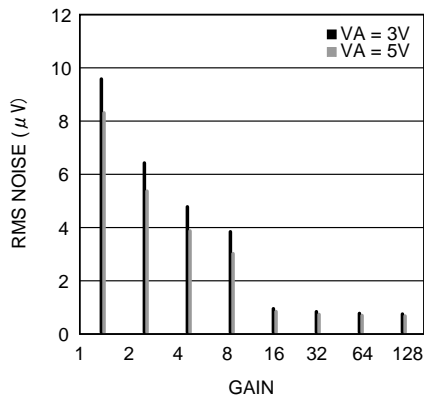

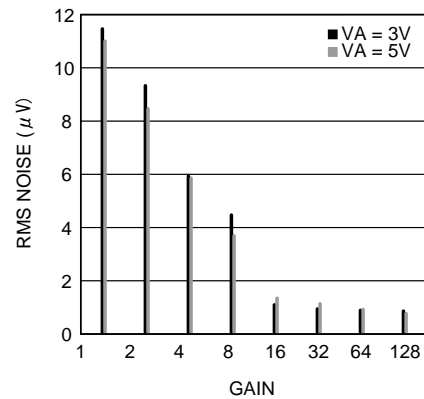**Figure 30. Noise vs. Gain Without Calibration at ODR = 214.65 SPS**

Figure 31. Noise vs. Gain With Calibration at ODR = 214.65 SPS

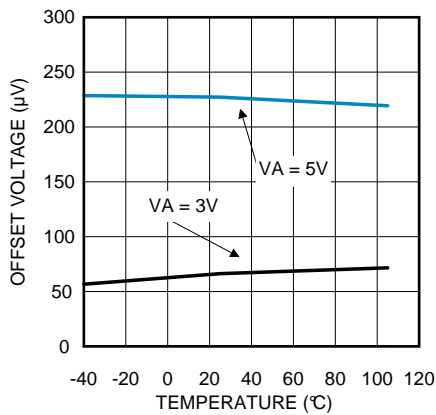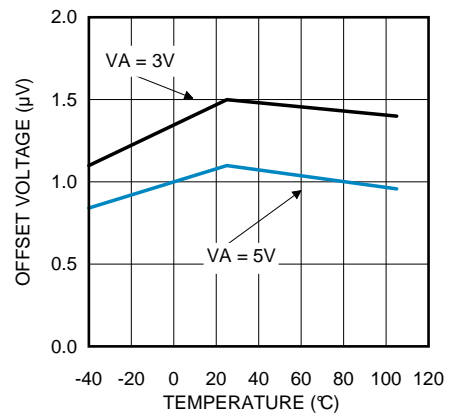**Figure 32. Offset Error vs. Temperature Without Calibration at Gain = 1**

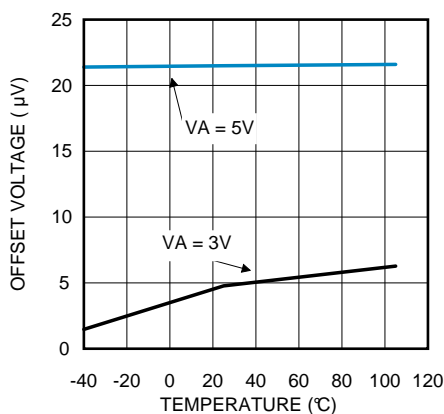**Figure 33. Offset Error vs. Temperature With Calibration at Gain = 1**

Figure 34. Offset Error vs. Temperature Without Calibration at Gain = 8

Figure 35. Offset Error vs. Temperature With Calibration at Gain = 8

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Typical Characteristics (continued)

Unless otherwise noted, specified limits apply for VA = VIO = VREF = 3.0 V. The maximum and minimum values apply for T_A = T_{MIN} to T_{MAX}; the typical values apply for T_A = 25°C.
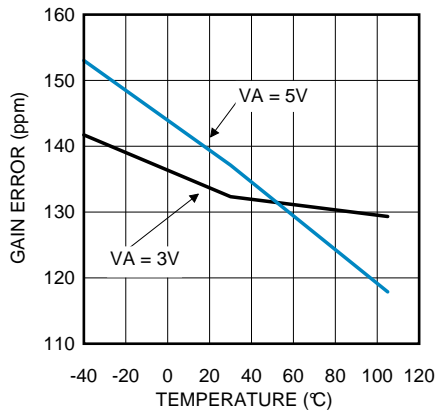
Figure 36. Gain Error vs. Temperature Without Calibration at Gain = 1
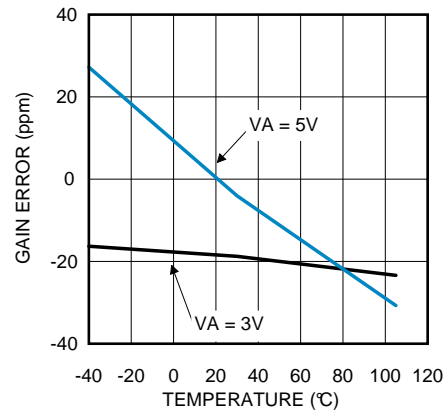
Figure 37. Gain Error vs. Temperature With Calibration at Gain = 1
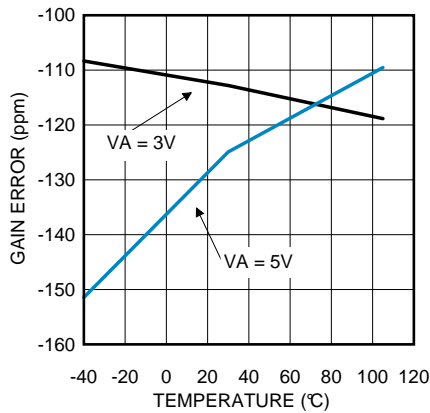
Figure 38. Gain Error vs. Temperature Without Calibration at Gain = 8
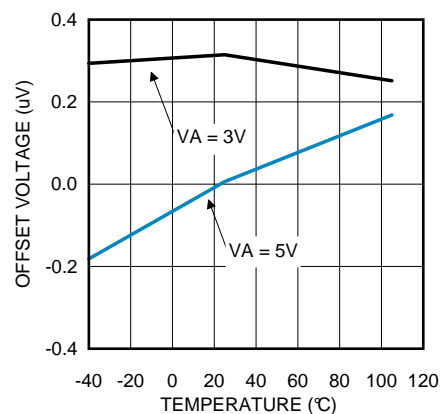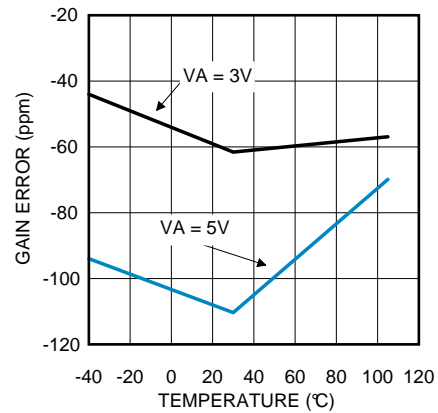

Figure 39. Gain Error vs. Temperature With Calibration at Gain = 8
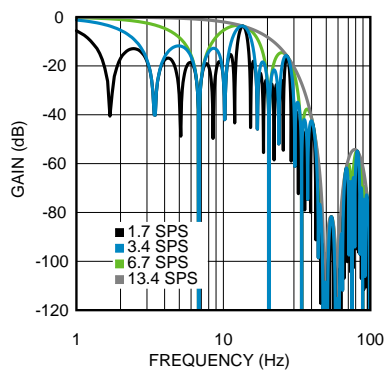
Figure 40. Digital Filter Frequency Response
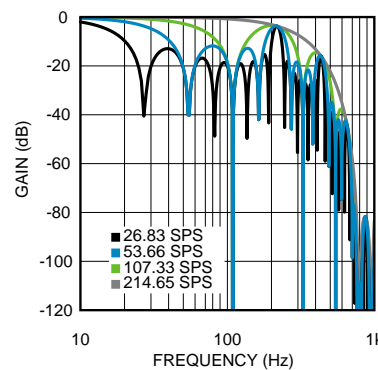
Figure 41. Digital Filter Frequency Response

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Typical Characteristics (continued)

Unless otherwise noted, specified limits apply for VA = VIO = VREF = 3.0 V. The maximum and minimum values apply for T_A = T_{MIN} to T_{MAX}; the typical values apply for T_A = 25°C.


Figure 42. INL at Gain = 1
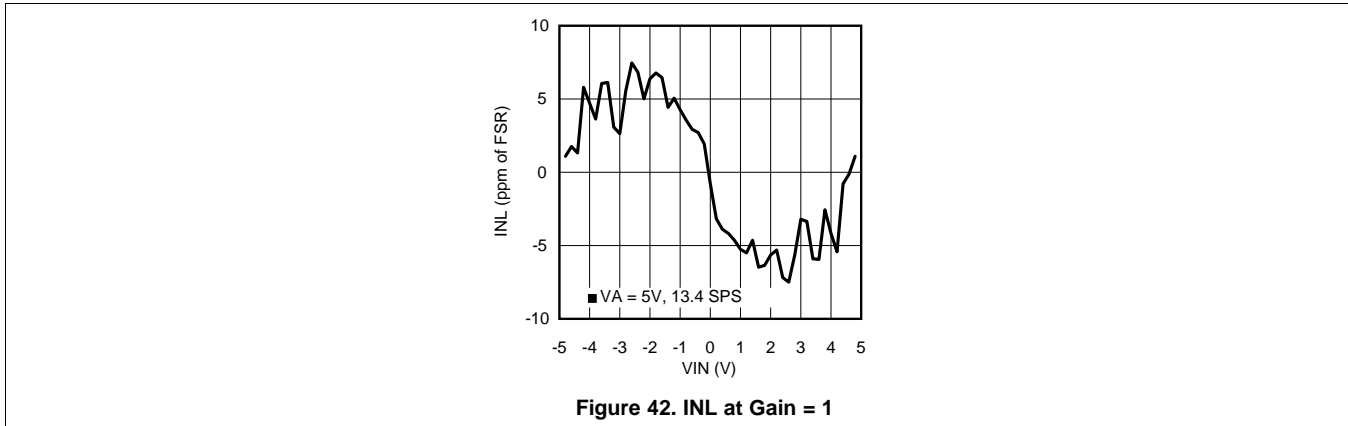
9 Detailed Description

9.1 Overview

The LMP90xxx is a low-power 24-Bit ΣΔ ADC with 4 fully differential / 7 single-ended analog channels for the LMP90100/LMP90099 and 2 full differential / 4 single-ended for the LMP90098/LMP90097. Its serial data output is two's complement format. The output data rate (ODR) ranges from 1.6775 SPS to 214.65 SPS.

The serial communication for LMP90xxx is SPI, a synchronous serial interface that operates using 4 pins: chip select bar (CSB), serial clock (SCLK), serial data in (SDI), and serial data out / data ready bar (SDO/DRYDYB).

True continuous built-in offset and gain background calibration is also available to improve measurement accuracy. Unlike other ADCs, the LMP90xxx's background calibration can run without heavily impacting the input signal. This unique technique allows for positive as well as negative gain calibration and is available at all gain settings.

The registers can be found in *Programming*, and a detailed description of the LMP90xxx are provided in the following sections.

9.2 Functional Block Diagram
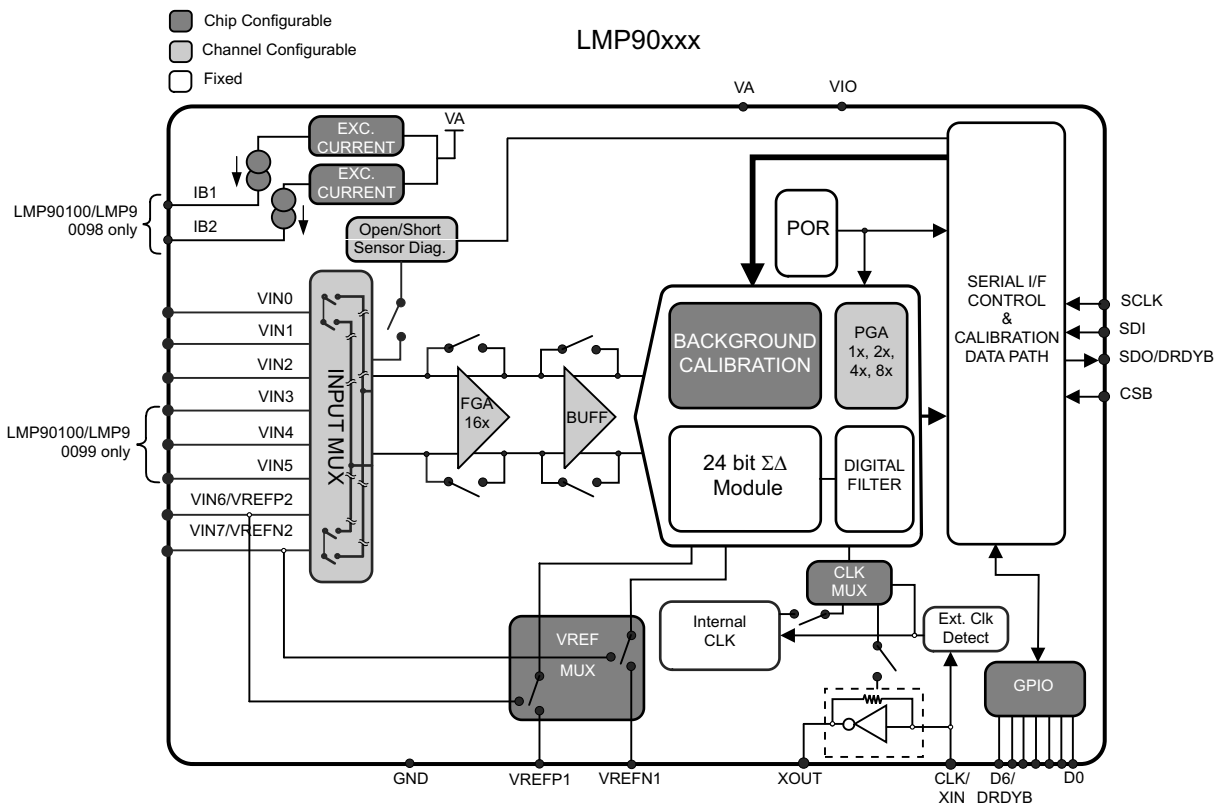
9.3 Feature Description

9.3.1 True Continuous Background Calibration

The LMP90100/LMP90099/LMP90098/LMP90097 feature a 24 bit ΣΔ core with continuous background calibration to compensate for gain and offset errors in the ADC, virtually eliminating any drift with time and temperature. The calibration is performed in the background without user or ADC input interruption, making it unique in the industry and eliminating down time associated with field calibration required with other solutions. Having this continuous calibration improves performance over the entire life span of the end product.

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Feature Description (continued)

9.3.2 Continuous Background Sensor Diagnostics

Sensor diagnostics are also performed in the background, without interfering with signal path performance, allowing the detection of sensor shorts, opens, and out-of-range signals, which vastly improves system reliability. In addition, the fully flexible input multiplexer described below allows any input pin to be connected to any ADC input channel providing additional sensor path diagnostic capability.

9.3.3 Flexible Input MUX Channels

The flexible input MUX allows interfacing to a wide range of sensors such as thermocouples, RTDs, thermistors, and bridge sensors. The LMP90100/LMP90099's multiplexer supports 4 differential channels while the LMP90098/LMP90097 supports 2. Each effective input voltage that is digitized is VIN = VINx – VINy, where x and y are any input. In addition, the input multiplexer of the LMP90100/LMP90099 also supports 7 single-ended channels (LMP90098/LMP90097 supports 4), where the common ground is any one of the inputs.

9.3.4 Programmable Gain Amplifiers (FGA and PGA)

The LMP90100/LMP90099/LMP90098/LMP90097 contain an internal 16x fixed gain amplifier (FGA) and a 1x, 2x, 4x, or 8x programmable gain amplifier (PGA). This allows accurate gain settings of 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x through configuration of internal registers. Having an internal amplifier eliminates the need for external amplifiers that are costly, space consuming, and difficult to calibrate.

9.3.5 Excitation Current Sources (IB1 and IB2) - LMP90100/LMP90098

Two matched internal excitation currents, IB1 and IB2, can be used for sourcing currents to a variety of sensors. The current range is from 100 µA to 1000 µA in steps of 100 µA.

9.3.6 Signal Path

9.3.6.1 Reference Input (VREF)

The differential reference voltage VREF (VREFP – VREFN) sets the range for VIN.

The muxed VREF allows the user to choose between VREF1 or VREF2 for each channel. This selection can be made by programming the VREF_SEL bit in the CHx_INPUTCN registers (CHx_INPUTCN: VREF_SEL). The default mode is VREF1. If VREF2 is used, then VIN6 and VIN7 cannot be used as inputs because they share the same pin.

Refer to VREF for VREF applications information.

9.3.6.2 Flexible Input MUX (VIN)

The LMP90xxx provides a flexible input MUX as shown in Figure 43. The input that is digitized is VIN = VINP – VINN; where VINP and VINN can be any available input.

The digitized input is also known as a channel, where CH = VIN = VINP – VINN. Thus, there are a maximum of 4 differential channels: CH0, CH1, CH2, and CH3 for the LMP90100/LMP90099. The LMP90098/LMP90097 has a maximum of 2 differential channels: CH0 and CH1 because it does not have access to the VIN3, VIN4, and VIN5 pins.

The LMP90xxx can also be configured single-endedly, where the common ground is any one of the inputs. There are a maximum of 7 single-ended channels: CH0, CH1, CH2, CH3, CH4, CH5, and CH6 for the LMP90100/LMP90099 and 4: CH0, CH1, CH2, CH3 for the LMP90098/LMP90097.

The input MUX can be programmed in the CHx_INPUTCN registers. For example on the LMP90100, to program CH0 = VIN = VIN4 – VIN1, go to the CH0_INPUTCN register and set:

1. VINP = 0x4

2. VINN = 0x1

Feature Description (continued)

* VIN3, VIN4, VIN5 are only available for LMP90100 and LMP90099
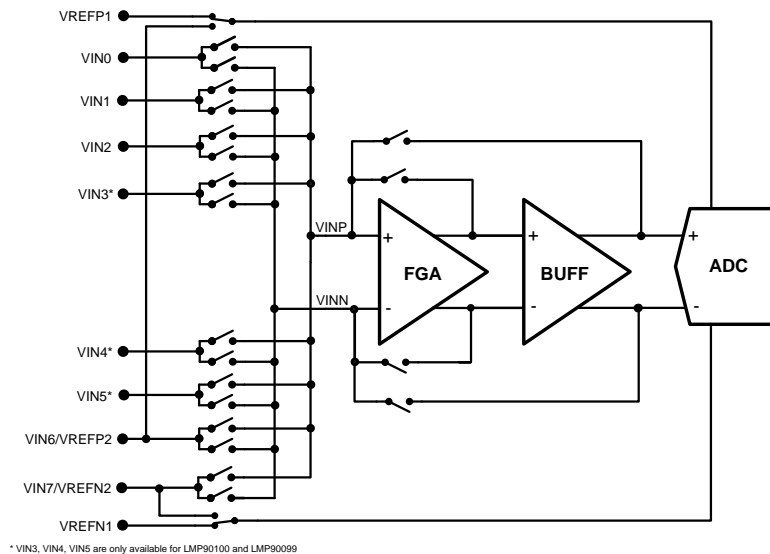
Figure 43. Simplified VIN Circuitry

9.3.6.3 Selectable Gains (FGA and PGA)

The LMP90xxx provides two types of gain amplifiers: a fixed gain amplifier (FGA) and a programmable gain amplifier (PGA). FGA has a fixed gain of 16x or it can be bypassed, while the PGA has programmable gain settings of 1x, 2x, 4x, or 8x.

Total gain is defined as FGA x PGA. Thus, LMP90xxx provides gain settings of 1x, 2x, 4x, 8x, 16x, 32x, 64x, or 128x with true continuous background calibration.

The gain is channel specific, which means that one channel can have one gain, while another channel can have the same or a different gain.

The gain can be selected by programming the CHx_CONFIG: GAIN_SEL bits.

9.3.6.4 Buffer (BUFF)

There is an internal unity gain buffer that can be included or excluded from the signal path. Including the buffer provides a high input impedance but increases the power consumption.

When gain ≥ 16, the buffer is automatically included in the signal path. When gain < 16, including or excluding the buffer from the signal path can be done by programming the CHX_CONFIG: BUF_EN bit.

9.3.6.5 Internal/External CLK Selection

LMP90xxx allows two clock options: internal CLK or external CLK (crystal (XTAL) or clock source).

There is an "External Clock Detection" mode, which detects the external XTAL if it is connected to XOUT and XIN. When operating in this mode, the LMP90xxx shuts off the internal clock to reduce power consumption. Below is a flow chart to help set the appropriate clock registers.

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Feature Description (continued)
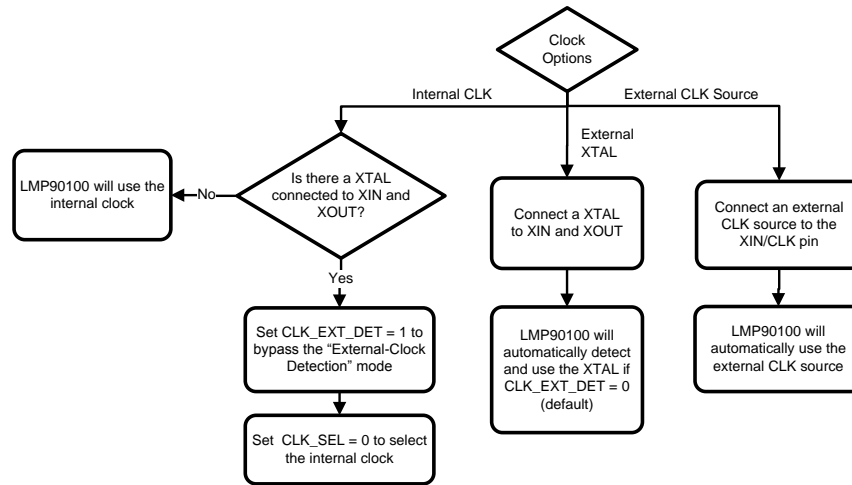
Figure 44. CLK Register Settings

The recommended value for the external CLK is discussed in the next sections.

9.3.6.6 Programmable ODRs

If using the internal CLK or external CLK of 3.5717 MHz, then the output date rates (ODR) can be selected (using the ODR_SEL bit) as:

1. 13.42/8 = 1.6775 SPS

2. 13.42/4 = 3.355 SPS

3. 13.42/2 = 6.71SPS

4. 13.42 SPS

5. 214.65/8 = 26.83125 SPS

6. 214.65/4 = 53.6625 SPS

7. 214.65/2 = 107.325 SPS

8. 214.65 SPS (default)

If the internal CLK is not being used and the external CLK is not 3.5717 MHz, then the ODR will be different. If this is the case, use the equation below to calculate the new ODR values.

$$\text{ODR\_Base1} = (\text{CLK}_{\text{EXT}}) / (266,240) \tag{1}$$
$$\text{ODR\_Base2} = (\text{CLK}_{\text{EXT}}) / (16,640) \tag{2}$$
$$\text{ODR1} = (\text{ODR\_Base1}) / n$$

where

- $n = 1,2,4,8$ (3)

$$\text{ODR2} = (\text{ODR\_Base2}) / n$$

where

- $n = 1,2,4,8$ (4)

For example, a 3.6864 MHz XTAL or external clock has the following ODR values:

$$\text{ODR\_Base1} = (3.6864 \text{ MHz}) / (266,240) = 13.85 \text{ SPS} \tag{5}$$
$$\text{ODR\_Base2} = (3.6864 \text{ MHz}) / (16,640) = 221.54 \text{ SPS} \tag{6}$$
$$\text{ODR1} = (13.85 \text{ SPS}) / n = 13.85, 6.92, 3.46, 1.73 \text{ SPS} \tag{7}$$

Feature Description (continued)

ODR2 = (221.54 SPS) / n = 221.54, 110.77, 55.38, 27.69 SPS   (8)

The ODR is channel specific, which means that one channel can have one ODR, while another channel can have the same or a different ODR.

Note that these ODRs are meant for a single channel conversion; the ODR needs to be divided by n for n channels scanning. For example, if the ADC were running at 214.65 SPS and four channels are being scanned, then the ODR per channel would be 214.65/4 = 53.6625 SPS.

9.3.6.7 Digital Filter

The LMP90xxx has a fourth order rotated sinc filter that is used to configure various ODRs and to reject power supply frequencies of 50Hz and 60Hz. The 50/60 Hz rejection is only effective when the device is operating at ODR ≤ 13.42 SPS. If the internal CLK or the external CLK of 3.5717 MHz is used, then the LMP90xxx will have the frequency response shown in Figure 45 to Figure 49.

Figure 45. Digital Filter Response, 1.6775 SPS and 3.355 SPS

Figure 46. Digital Filter Response, 6.71 SPS and 13.42 SPS

Figure 47. Digital Filter Response at 13.42 SPS

Figure 48. Digital Filter Response, 26.83125 SPS and 53.6625 SPS

Figure 49. Digital Filter Response 107.325 SPS and 214.65 SPS

Figure 50. Digital Filter Response for a 3.5717 MHz versus 3.6864 MHz XTAL
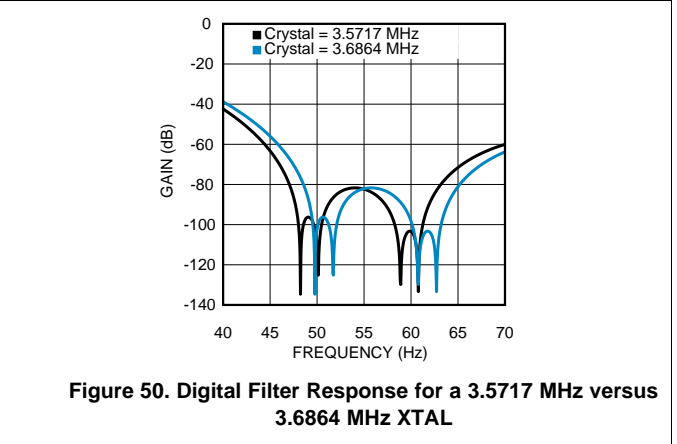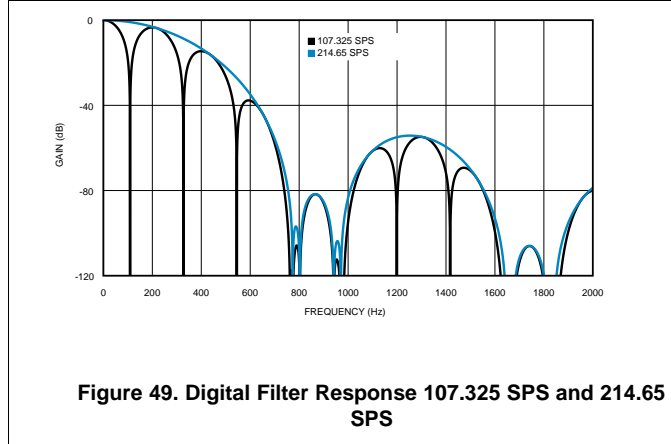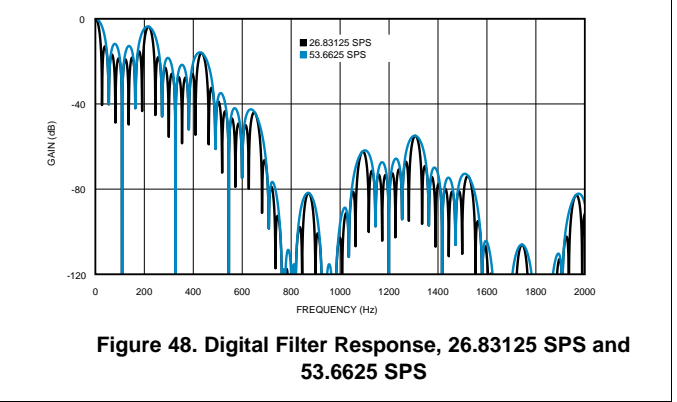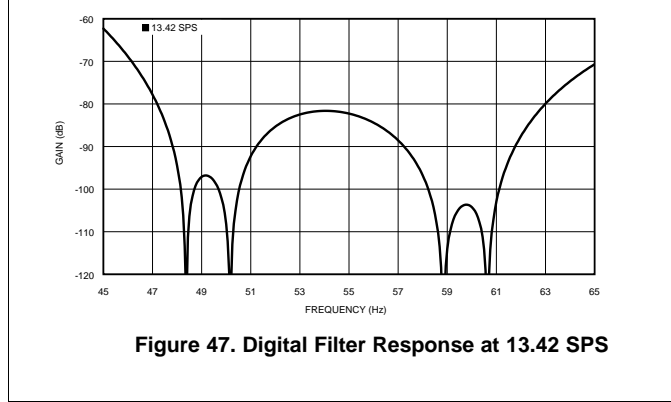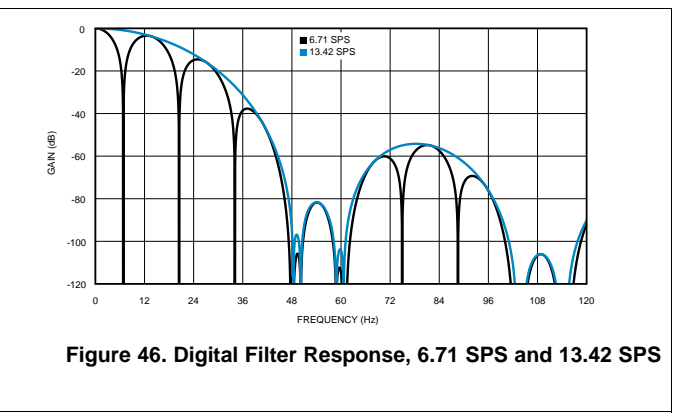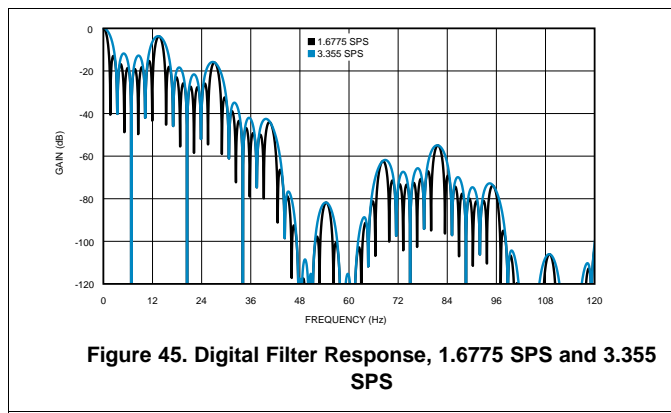
Feature Description (continued)

If the internal CLK is not being used and the external CLK is not 3.5717 MHz, then the filter response would be the same as the response shown in Figure 49, but the frequency will change according to the equation:

$$f_{NEW} = [(CLK_{EXT}) / 256] \times (f_{OLD} / 13.952k) \tag{9}$$

Using Equation 9, an example of the filter response for a 3.5717 MHz XTAL versus a 3.6864 MHz XTAL can be seen in Figure 50.

9.3.6.8 GPIO (D0–D6)

Pins D0-D6 are general-purpose input/output (GPIO) pins that can be used to control external LEDs or switches. Only a high or low value can be sourced to or read from each pin.

Figure 51 shows a flow chart how these GPIOs can be programmed.
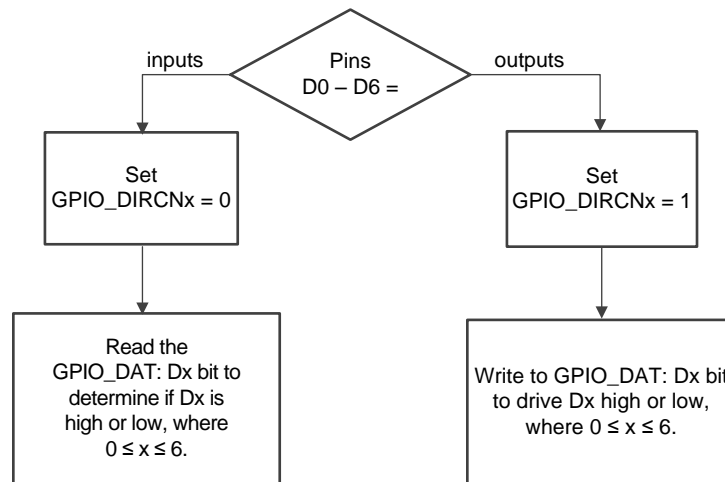
Figure 51. GPIO Register Settings

9.3.7 Calibration

As seen in Figure 52, there are two types of calibration: background calibration and system calibration. These calibrations are further described in the next sections.
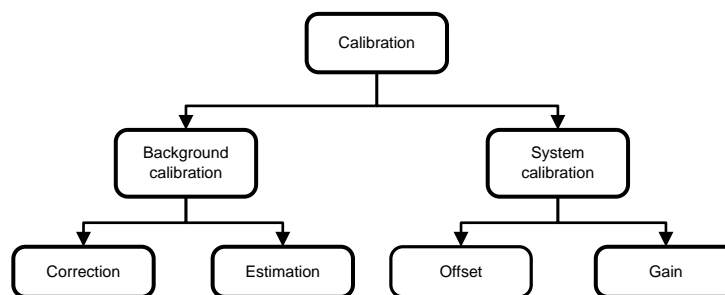
Figure 52. Types of Calibration

9.3.7.1 Background Calibration

Background calibration is the process of continuously determining and applying the offset and gain calibration coefficients to the output codes to minimize the LMP90xxx's offset and gain errors. Background calibration is a feature built into the LMP90xxx and is automatically done by the hardware without interrupting the input signal.

Four differential channels, CH0-CH3, each with its own gain and ODRs, can be calibrated to improve the accuracy.

Feature Description (continued)

9.3.7.1.1 Types of Background Calibration

Figure 52 also shows that there are two types of background calibration:

1. Type 1: Correction - the process of continuously determining and applying the offset and gain calibration coefficients to the output codes to minimize the LMP90xxx's offset and gain errors.
    – This method keeps track of changes in the LMP90xxx's gain and offset errors due to changes in the operating condition such as voltage, temperature, or time.
2. Type 2: Estimation - the process of determining and continuously applying the last known offset and gain calibration coefficients to the output codes to minimize the LMP90xxx's offset and gain errors.
    – The last known offset or gain calibration coefficients can come from two sources. The first source is the default coefficient which is pre-determined and burnt in the device's non-volatile memory. The second source is from a previous calibration run of Type 1: Correction.

The benefits of using type 2 calibration are a higher throughput, lower power consumption, and slightly better noise. The exact savings would depend on the number of channels being scanned, and the ODR and gain of each channel.

9.3.7.1.2 Using Background Calibration

There are four modes of background calibration, which can be programmed using the BGCALCN bits. They are as follows:

1. BgcalMode0: Background Calibration OFF
2. BgcalMode1: Offset Correction / Gain Estimation
3. BgcalMode2: Offset Correction / Gain Correction
    – Follow Figure 53 to set other appropriate registers when using this mode.
4. BgcalMode3: Offset Estimation / Gain Estimation

Figure 53. BgcalMode2 Register Settings

If operating in BgcalMode2, four channels (with the same ODR) are being converted, and FGA_BGCAL = 0 (default), then the ODR is reduced by:

1. 0.19% of 1.6775 SPS
2. 0.39% of 3.355 SPS
3. 0.78% of 6.71 SPS
4. 1.54% of 13.42 SPS
5. 3.03% of 26.83125 SPS
6. 5.88% of 53.6625 SPS

Feature Description (continued)

7. 11.11% of 107.325 SPS

8. 20% of 214.65 SPS

9.3.7.2 System Calibration

The LMP90xxx provides some unique features to support easy system offset and system gain calibrations.

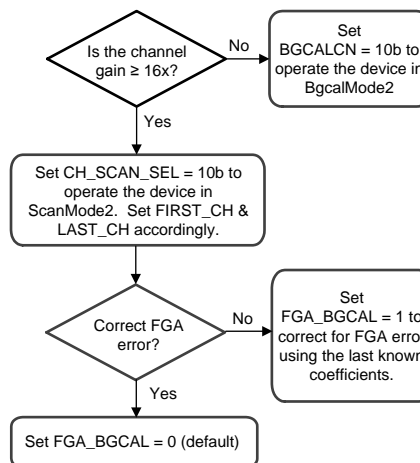The System Calibration Offset Registers (CHx_SCAL_OFFSET) hold the System Calibration Offset Coefficients in 24-bit, two's complement binary format. The System Calibration Gain Registers (CHx_SCAL_GAIN) hold the System Calibration Gain Coefficient in 24-bit, 1.23, unsigned, fixed-point binary format. For each channel, the System Calibration Offset coefficient is subtracted from the conversion result prior to the division by the System Calibration Gain Coefficient.

A data-flow diagram of these coefficients can be seen in Figure 54.
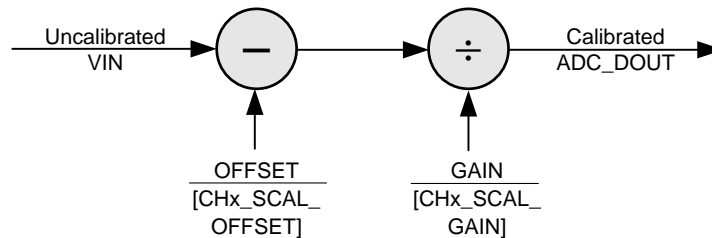
Figure 54. System Calibration Data-Flow Diagram

There are four distinct sets of System Calibration Offset and System Calibration Gain Registers for use with CH0-CH3. CH4-CH6 reuse the registers of CH0-CH2, respectively.

The LMP90xxx provides two system calibration modes that automatically fill the Offset and Gain coefficients for each channel. These modes are the System Calibration Offset Coefficient Determination mode and the System Calibration Gain Coefficient Determination mode. The System Calibration Offset Coefficient Determination mode must be entered prior to the System Calibration Gain Coefficient Determination mode, for each channel.

The system zero-scale condition is a system input condition (sensor loading) for which zero (0x00_0000) system-calibrated output code is desired. It may not, however, cause a zero input voltage at the input of the ADC.

The system reference-scale condition is usually the system full-scale condition in which the system's input (or sensor's loading) would be full-scale and the desired system-calibrated output code would be 0x80_0000 (unsigned 24-bit binary). However, system full-scale condition need not cause full-scale input voltage at the input of the ADC.

The system reference-scale condition is not restricted to just the system full-scale condition. In fact, it can be any arbitrary fraction of full-scale (up to 1.25 times) and the desired system-calibrated output code can be any appropriate value (up to 0xA00000). The CHx_SCAL_GAIN register must be written with the desired system-calibrated output code (default:0x800000) before entering the System Calibration Gain Coefficient Determination mode. This helps in in-place system calibration.

Below are the detailed procedures for using the System Calibration Offset Coefficient Determination and System Calibration Gain Coefficient Determination modes.

9.3.7.2.1 System Calibration Offset Coefficient Determination Mode

1. Apply system zero-scale condition to the channel (CH0/CH1/CH2/CH3).
2. Enter the System Calibration Offset Coefficient Determination mode by programming 0x1 in the SCALCN register.
3. LMP90xxx starts a fresh conversion at the selected output data rate for the selected channel. At the end of the conversion, the CHx_SCAL_OFFSET register is filled-in with the System Calibration Offset coefficient.
4. The System Calibration Offset Coefficient Determination mode is automatically exited.
5. The computed calibration coefficient is accurate only to the effective resolution of the device and will probably contain some noise. The noise factor can be minimized by computing over many times, averaging

Feature Description (continued)

(externally) and putting the resultant value back into the register. Alternatively, select the output data rate to be 26.83 sps or 1.67 sps.

9.3.7.2.2 System Calibration Gain Coefficient Determination Mode

1. Repeat the System Calibration Offset Coefficient Determination mode to calibrate for the channel's system offset.
2. Apply the system reference-scale condition to the channel CH0/CH1/CH2/CH3.
3. In the CHx_SCAL_GAIN Register, program the expected (desired) system-calibrated output code for this condition in 24-bit unsigned format.
4. Enter the System Calibration Gain Coefficient Determination mode by programming 0x3 in the SCALCN register.
5. LMP90xxx starts a fresh conversion at the selected output data rate for the channel. At the end of the conversion, the CHx_SCAL_GAIN is filled-in (or overwritten) with the System Calibration Gain coefficient.
6. The System Calibration Gain Coefficient Determination mode is automatically exited.
7. The computed calibration coefficient is accurate only to the effective resolution of the device and will probably contain some noise. The noise factor can be minimized by computing over many times, averaging (externally) and putting the resultant value back into the register. Alternatively, select the output data rate to be 26.83 sps or 1.67 sps.

9.3.7.2.3 Post-Calibration Scaling

LMP90xxx allows scaling (multiplication and shifting) for the System Calibrated result. This eases downstream processing, if any. Multiplication is done using the System Calibration Scaling Coefficient in the CHx_SCAL_SCALING register and shifting is done using the System Calibration Bits Selector in the CHx_SCAL_BITS_SELECTOR register.

The System Calibration Bits Selector value should ideally be the logarithm (to the base 2) of the System Calibration Scaling Coefficient value.

There are four distinct sets of System Calibration Scaling and System Calibration Bits Selector Registers for use with Channels 0-3. Channels 4-6 reuse the registers of Channels 0-2, respectively.

A data-flow diagram of these coefficients can be seen in Figure 55
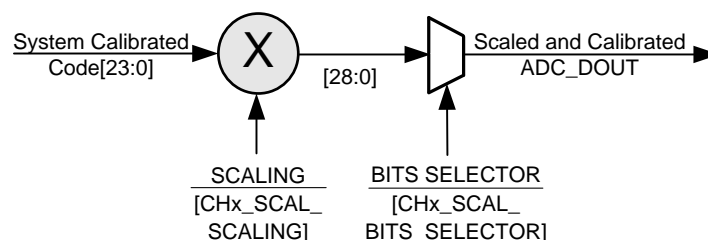
Figure 55. Post-calibration Scaling Data-Flow Diagram

9.3.8 Sensor Interface

LMP90100/LMP90098 contain two types of current sources: excitation currents (IB1 & IB2) and burnout currents. They are described in the next sections.

9.3.8.1 IB1 and IB2 - Excitation Currents

IB1 and IB2 can be used for providing currents to external sensors, such as RTDs or bridge sensors. 100µA to 1000µA, in steps of 100µA, can be sourced by programming the ADC_AUXCN: RTD_CUR_SEL bits.

Refer to *3-Wire RTD Using 2 Current Sources* to see how IB1 and IB2 can be used to source a 3-wire RTD.

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Feature Description (continued)

9.3.8.2 Burnout Currents

As shown in Figure 56, the LMP90xxx contains two internal 10 μA burnout current sources, one sourcing current from VA to VINP, and the other sinking current from VINN to ground. These currents are used for sensor diagnostics and can be enabled for each channel using the CHx_INPUTCN: BURNOUT_EN bit.
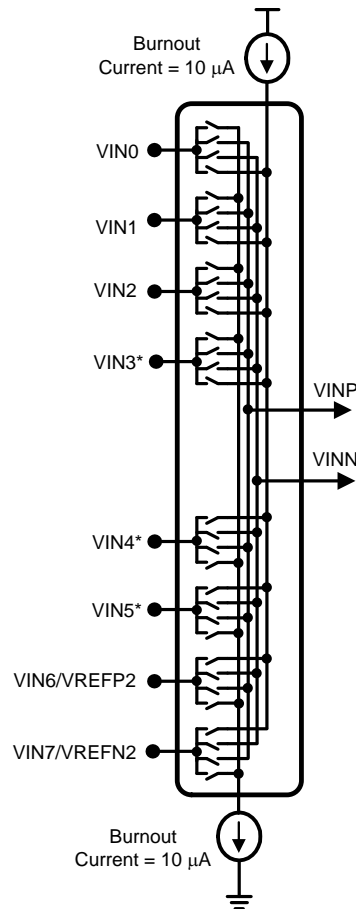
* VIN3, VIN4, VIN5 are only available for LMP90100 and LMP90099

Figure 56. Burnout Currents

9.3.8.2.1 Burnout Current Injection

Burnout currents are injected differently depending on the channel scan mode selected.

When BURNOUT_EN = 1 and the device is operating in ScanMode0, 1, or 2, the burnout currents are injected into all the channels for which the BURNOUT_EN bit is selected. This will cause problems and hence in this mode, more than one channel should not have its BURNOUT_EN bit selected. Also, the burnout current will interfere with the signal and introduce a fixed error depending on the particular external sensor.

When BURNOUT_EN = 1 and the device is operating in ScanMode3, burnout currents are injected into the last sampled channel on a cyclical basis (Figure 57). In this mode, burnout currents injection is truly done in the background without affecting the accuracy of the on-going conversion. Operating in this mode is recommended.

Feature Description (continued)
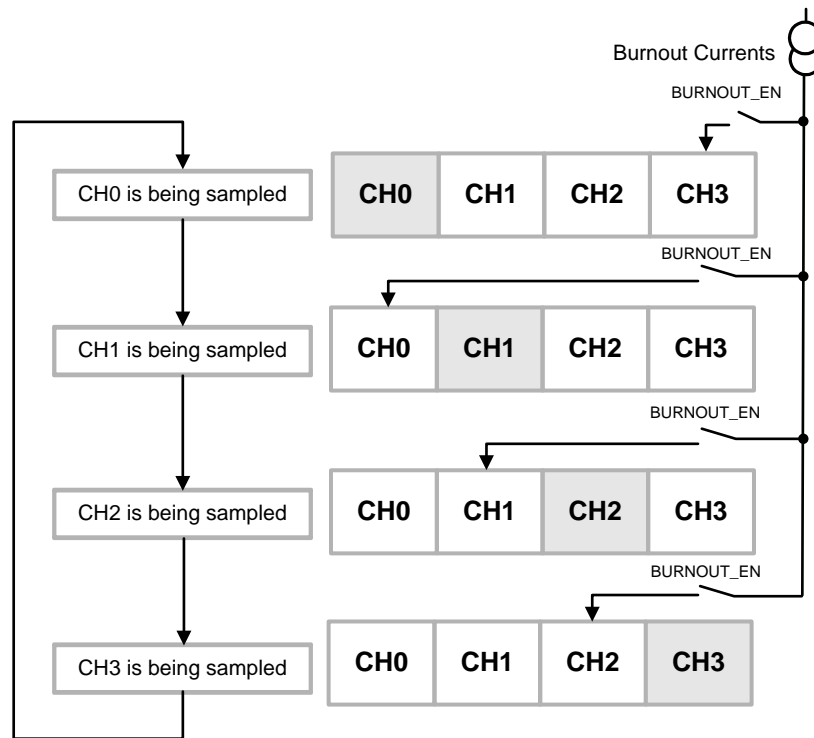
Figure 57. Burnout Currents Injection for ScanMode3

9.3.8.3 Sensor Diagnostic Flags

Burnout currents can be used to verify that an external sensor is still operational before attempting to make measurements on that channel. A non-operational sensor means that there is a possibility the connection between the sensor and the LMP90xxx is open circuited, short circuited, shorted to VA or GND, overloaded, or the reference may be absent. The sensor diagnostic flags diagram can be seen in Figure 58.
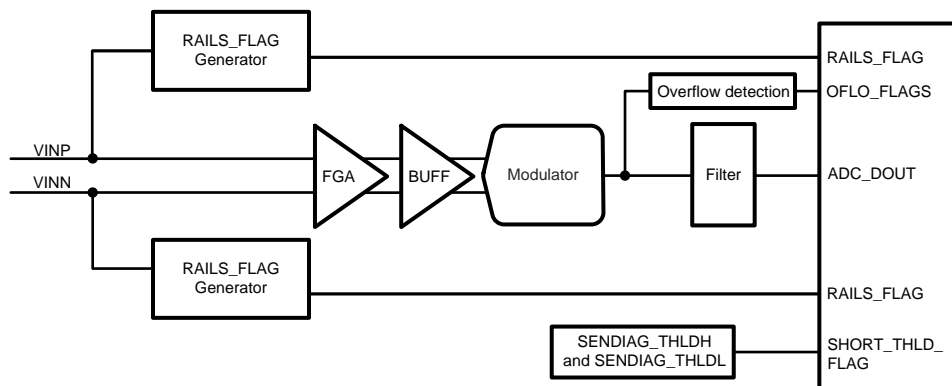
Figure 58. Sensor Diagnostic Flags Diagram

The sensor diagnostic flags are located in the SENDIAG_FLAGS register and are described in further details below.

Feature Description (continued)

9.3.8.3.1 SHORT_THLD_FLAG

The short circuit threshold flag is used to report a short-circuit condition. It is set when the output voltage (VOUT) is within the absolute Vthreshold. Vthreshold can be programmed using the 8-bit SENDIAG_THLDH register concatenated with the 8-bit SENDIAG_THLDL register.

For example, assume VREF = 5V, gain = 1, SENDIAG_THLDH = 0xFA, and SENDIAG_THLDL = 0x45. In this case, Dthreshold = 0xFA45 = 64069d, and Vthreshold can be calculated as:

$$Vthreshold = [(Dthreshold)(2)(VREF)] / [(Gain)(2^{24})] \tag{10}$$

$$Vthreshold = [(64069)(2)(5V)] / [(1)(2^{24})] \tag{11}$$

$$Vthreshold = 38.2 \text{ mV} \tag{12}$$

When (-38.2mV) ≤ VOUT ≤ (38.2mV), then SHORT_THLD_FLAG = 1; otherwise, SHORT_THLD_FLAG = 0.

9.3.8.3.2 RAILS_FLAG

The rails flag is used to detect if one of the sampled channels is within 50mV of the rails potential (VA or VSS). This can be further investigated to detect an open-circuit or short-circuit condition. If the sampled channel is near a rail, then RAILS_FLAG = 1; otherwise, RAILS_FLAG = 0.

9.3.8.3.3 POR_AFT_LST_RD:

If POR_AFT_LST_READ = 1, then there was a power-on reset because the last time the SENDIAG_FLAGS register was read. This flag's status is cleared when this bit is read, unless this bit is set again on account of another power-on-reset event in the intervening period.

9.3.8.3.4 OFLO_FLAGS

OFLO_FLAGS is used to indicate whether the modulator is over-ranged or under-ranged. The following conditions are possible:

1. OFLO_FLAGS = 0x0: Normal Operation
2. OFLO_FLAGS = 0x1: The differential input is more than (±VREF/Gain) but is not more than ±(1.3*VREF/Gain) to cause a modulator over-range.
3. OFLO_FLAGS = 0x2: The modulator was over-ranged towards +VREF/Gain.
4. OFLO_FLAGS = 0x3: The modulator was over-ranged towards −VREF/Gain.

The condition of OFLO_FLAGS = 10b or 11b can be used in conjunction with the RAILS_FLAG to determine the fault condition.

9.3.8.3.5 SAMPLED_CH

These three bits show the channel number for which the ADC_DOUT and SENDIAG_FLAGS are available. This does not necessarily indicate the current channel under conversion because the conversion frame and computation of results from the channels are pipelined. That is, while the conversion is going on for a particular channel, the results for the previous conversion (of the same or a different channel) are available.

9.3.9 RESET and RESTART

Writing 0xC3 to the REG_AND_CNV_RST field will reset the conversion and most of the programmable registers to their default values. The only registers that will not be reset are the System Calibration Registers (CHx_SCAL_OFFSET, CHx_SCAL_GAIN) and the DT_AVAIL_B bit.

If it is desirable to reset the System Calibration Coefficient Registers, then set RESET_SYSCAL = 1 before writing 0xC3 to REG_AND_CNV_RST. If the device is operating in the "System Calibration Offset/Gain Coefficient Determination" mode (SCALCN register), then write REG_AND_CNV_RST = 0xC3 twice to get out of this mode.

After a register reset, any on-going conversions will be aborted and restarted. If the device is in the power-down state, then a register reset will bring it out of the power-down state.

To restart a conversion, write 1 to the RESTART bit. This bit can be used to synchronize the conversion to an external event.

Feature Description (continued)

After a restart conversion, the first sample is not valid. To restart with a valid first sample, issue a stand-by command followed by an active command.

9.4 Device Functional Modes

9.4.1 Power Management

The device can be placed in Active, Power-Down, or Stand-By state.

In Power-Down, the ADC is not converting data, contents of the registers are unaffected, and there is a drastic power reduction. In Stand-By, the ADC is not converting data, but the power is only slightly reduced so that the device can quickly transition into the active state if desired.

These states can be selected using the PWRCN register. When written, PWRCN brings the device into the Active, Power-Down, or Stand-By state. When read, PWRCN indicates the state of the device.

The read value would confirm the write value after a small latency (approximately 15 µs with the internal CLK). It may be appropriate to wait for this latency to confirm the state change. Requests not adhering to this latency requirement may be rejected.

It is not possible to make a direct transition from the power-down state to the stand-by state. This state diagram is shown in Figure 59.
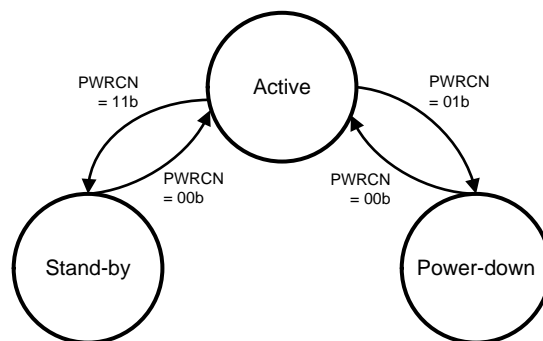
Figure 59. Active, Power-Down, Stand-by State Diagram

9.4.2 Channels Scan Mode

There are four scan modes. These scan modes are selected using the CH_SCAN: CH_SCAN_SEL bit. The first scanned channel is FIRST_CH, and the last scanned channel is LAST_CH; they are both located in the CH_SCAN register.

The CH_SCAN register is double buffered. That is, user inputs are stored in a slave buffer until the start of the next conversion during which time they are transferred to the master buffer. Once the slave buffer is written, subsequent updates are disregarded until a transfer to the master buffer happens. Hence, it may be appropriate to check the CH_SCAN_NRDY bit before programming the CH_SCAN register.

9.4.2.1 ScanMode0: Single-Channel Continuous Conversion

LMP90xxx continuously converts the selected FIRST_CH.

Do not operate in this scan mode if gain ≥ 16 and the LMP90xxx is running in background calibration modes BgcalMode1 or BgcalMode2. If this is the case, then it is more suitable to operate the device in ScanMode2 instead.

9.4.2.2 ScanMode1: Multiple-Channels Single Scan

LMP90xxx converts one or more channels starting from FIRST_CH to LAST_CH, and then enters the stand-by state.

Device Functional Modes (continued)

9.4.2.3 ScanMode2: Multiple-Channels Continuous Scan

LMP90xxx continuously converts one or more channels starting from FIRST_CH to LAST_CH, and then it repeats this process.

9.4.2.4 ScanMode3: Multiple-Channels Continuous Scan with Burnout Currents

This mode is the same as ScanMode2 except that the burnout current is provided in a serially scanned fashion (injected in a channel after it has undergone a conversion). Thus it avoids burnout current injection from interfering with the conversion result for the channel.

The sensor diagnostic burnout currents are available for all four scan modes. The burnout current is further gated by the BURNOUT_EN bit for each channel. ScanMode3 is the only mode that scans multiple channels while injecting burnout currents without interfering with the signal. This is described in details in *Burnout Currents*.

9.5 Programming

9.5.1 General Rules

1. If written to, RESERVED bits must be written to only 0 unless otherwise indicated.
2. Read back value of RESERVED bits and registers is unspecified and should be discarded.
3. Recommended values must be programmed and forbidden values must not be programmed where they are indicated in order to avoid unexpected results.
4. If written to, registers indicated as Reserved must have the indicated default value as shown in the *Register Maps*. Any other value can cause unexpected results.

9.5.2 Serial Digital Interface

A synchronous 4-wire serial peripheral interface (SPI) provides access to the internal registers of LMP90xxx via CSB, SCLK, SDI, SDO/DRDYB.

9.5.3 Register Address (ADDR)

All registers are memory-mapped. A register address (ADDR) is composed of an upper register address (URA) and lower register address (LRA) as shown in Table 5. For example, ADDR 0x3A has URA=0x3 and LRA=0xA.

Table 5. ADDR Map

Bit	[6:4]	[3:0]
Name	URA	LRA

9.5.4 Register Read/Write Protocol

Figure 60 shows the protocol how to write to or read from a register.

Transaction 1 sets up the upper register address (URA) where the user wants to start the register-write or register-read.

Transaction 2 sets the lower register address (LRA) and includes the Data Byte(s), which contains the incoming data from the master or outgoing data from the LMP90xxx.

Examples of register-reads or register-writes can be found in *Register Read/Write Examples*.

Transaction 1 – URA Setup – necessary only when the previous URA is different than the desired URA.

←——————— Instruction Byte 1 (INST1) ———————→	←——————— Upper Address Byte (UAB) ———————→	
[7:0]	[7:3]	[2:0]
RA/WAB	0x0	Upper Register Address (URA)

R/WB = Read/Write Address
0x10: Write Address
0x90: Read Address

Transaction 2 – Data Access

←——————— Instruction Byte 2 (INST2) ———————→				←——————— Data Byte (s) ———————→
7	[6:5]	4	[3:0]	[N:0]
R/WB	SZ	0	Lower Register Address (LRA)	Data Byte (s)

R/WB = Read/Write Data
0: Write Data
1: Read Data

SZ = Size
0x0: 1 byte
0x1: 2 bytes
0x2: 3 bytes
0x3: Streaming – 3+ bytes until CSB is de-asserted
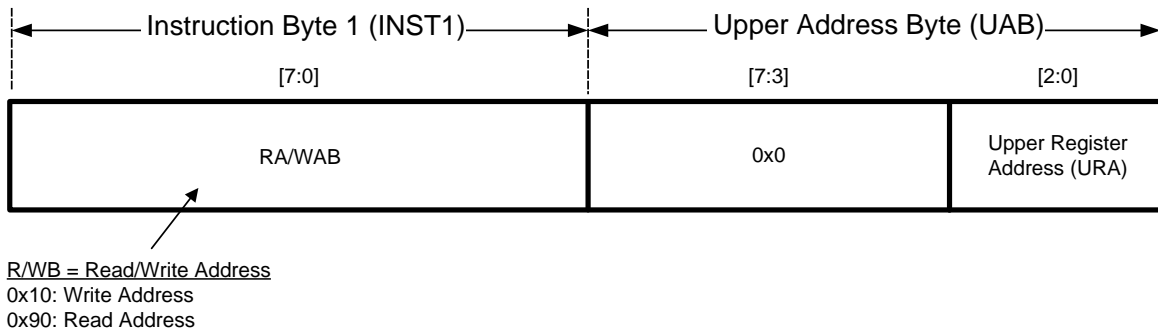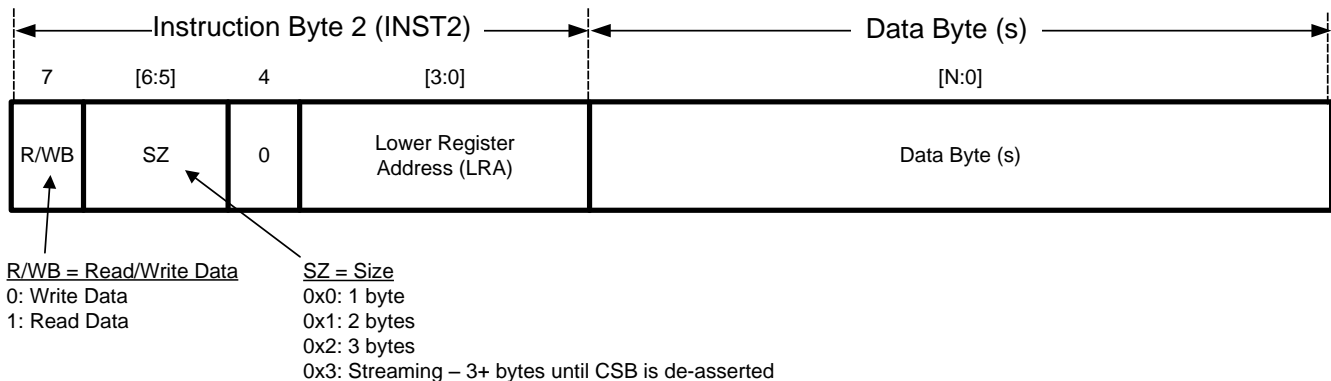
Figure 60. Register Read / Write Protocol

9.5.5 Streaming

When writing/reading 3+ bytes, the user must operate the device in Normal Streaming mode or Controlled Streaming mode. In the Normal Streaming mode, which is the default mode, data runs continuously starting from ADDR until CSB deasserts. This mode is especially useful when programming all the configuration registers in a single transaction. See *Normal Streaming Example* for an example of the Normal Streaming mode.

In the Controlled Streaming mode, data runs continuously starting from ADDR until the data has run through all (STRM_RANGE + 1) registers. For example, if the starting ADDR is 0x1C, STRM_RANGE = 5, then data will be written to or read from the following ADDRs: 0x1C, 0x1D, 0x1E, 0x1F, 0x20, 0x21. Once the data reaches ADDR 0x21, LMP90xxx will wrap back to ADDR 0x1C and repeat this process until CSB deasserts. See *Controlled Streaming Example* for an example of the Controlled Streaming mode.

If streaming reaches ADDR 0x7F, then it will wrap back to ADDR 0x00. Furthermore, reading back the Upper Register Address after streaming will report the Upper Register Address at the start of streaming, not the Upper Register Address at the end of streaming.

To stream, write 0x3 to INST2's SZ bits as seen in *Figure 60*. To select the stream type, program the SPI_STREAMCN: STRM_TYPE bit. The STRM_RANGE can also be programmed in the same register.

9.5.6 CSB - Chip Select Bar

An SPI transaction begins when the master asserts (active low) CSB and ends when the master deasserts (active high) CSB. Each transaction might be separated by a subsequent one with a CSB deassertion, but this is optional. Once CSB is asserted, it must not pulse (deassert and assert again) during a (desired) transaction.

CSB can be grounded in systems where LMP90xxx is the only SPI slave. This frees the software from handling the CSB. Care has to be taken to avoid any false edge on SCLK, and while operating in this mode, the streaming transaction should not be used because exiting from this mode can only be done through a CSB deassertion.

9.5.7 SPI Reset

SPI Reset resets the SPI-Protocol State Machine by monitoring the SDI for at least 73 consecutive 1's at each SCLK rising edge. After an SPI Reset, SDI is monitored for a possible Write Instruction at each SCLK rising edge.

SPI Reset will reset the Upper Address Register (URA) to 0, but the register contents are not reset.

By default, SPI reset is disabled, but it can be enabled by writing 0x01 to SPI Reset Register (ADDR 0x02).

9.5.8 DRDYB - Data Ready Bar

DRDYB is a signal generated by the LMP90xxx that indicates a fresh conversion data is available in the ADC_DOUT registers.

DRDYB is automatically asserted every (1/ODR) second and deasserts when ADC_DOUT is completely read out (LSB of ADC_DOUTL) (Figure 61).
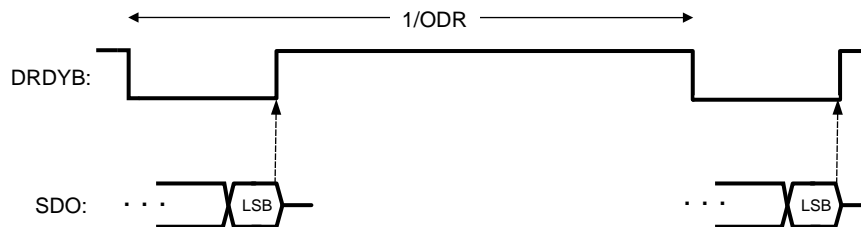
Figure 61. DRDYB Behavior for a Complete ADC_DOUT Reading

If ADC_DOUT is not completely read out (Figure 62) or is not read out at all, but a new ADC_DOUT is available, then DRDYB will automatically pulse for t_{DRDYB} second. The value for t_{DRDYB} can be found in *Timing Diagrams.*

Figure 62. DRDYB Behavior for an ADC_DOUT not Read

If ADC_DOUT is being read, while the new ADC_DOUT becomes available, then the ADC_DOUT that is being read is still valid (Figure 63). DRDYB will be deasserted at the LSB of the data being read, but a consecutive read on the ADC_DOUT register will fetch the newly converted data available.

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*
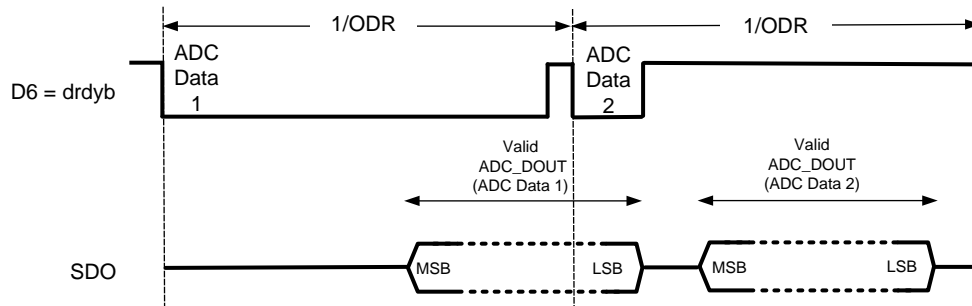
Figure 63. DRDYB Behavior for an Incomplete ADC_DOUT Reading

DRDYB can also be accessed via registers using the DT_AVAIL_B bit. This bit indicates when fresh conversion data is available in the ADC_DOUT registers. If new conversion data is available, then DT_AVAIL_B = 0; otherwise, DT_AVAIL_B = 1.

As opposed to the DRDYB signal, a complete reading for DT_AVAIL_B occurs when the MSB of ADC_DOUTH is read out. This bit cannot be reset even if REG_AND_CNV_RST = 0xC3.

9.5.9 DRDYB Case1: Combining SDO/DRDYB with SDO_DRDYB_DRIVER = 0x00
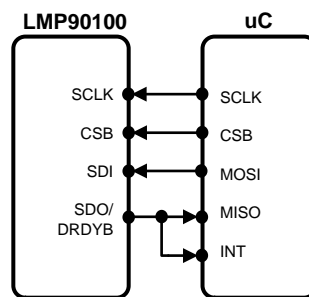
Figure 64. DRDYB Case1 Connection Diagram

As shown in Figure 64, the DRDYB signal and SDO can be multiplexed on the same pin as their functions are mostly complementary. In fact, this is the default mode for the SDO/DRDYB pin.

Figure 65 shows a timing protocol for DRDYB Case1. In this case, start by asserting CSB first to monitor a DRDYB assertion. When the DRDYB signal asserts, begin writing the Instruction Bytes (INST1, UAB, INST2) to read from or write to registers. Note that INST1 and UAB are omitted from the figure below because this transaction is only required if a new UAB needs to be implemented.

While the CSB is asserted, DRDYB is driving the SDO/DRDYB pin unless the device is reading data, in which case, SDO will be driving the pin. If CSB is deasserted, then the SDO/DRDYB pin is High-Z.
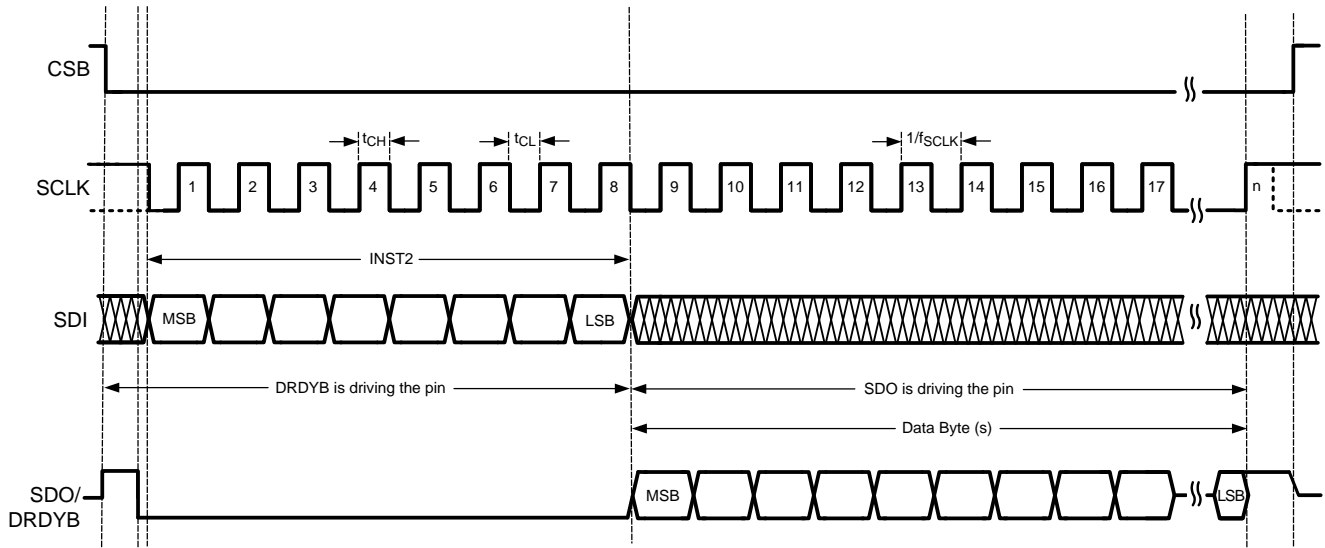
Figure 65. Timing Protocol for DRDYB Case1

9.5.10 DRDYB Case2: Combining SDO/DRDYB with SDO_DRDYB_DRIVER = 0x03

SDO/DRDYB can be made independent of CSB by setting SDO_DRDYB_DRIVER = 0x03 in the SPI Handshake Control register. In this case, DRDYB will drive the pin unless the device is reading data, independent of the state of CSB. SDO will drive the pin when CSB is asserted and the device is reading data.

With this scheme, one can use SDO/DRDYB as a true interrupt source, independent of the state of CSB. But this scheme can only be used when the LMP900xx is the only device connected to the master's SPI bus because the SDO/DRDYB pin will be DRDYB even when CSB is deasserted.

The timing protocol for this case can be seen in Figure 66. When DRDYB asserts, assert CSB to start the SPI transaction and begin writing the Instruction Bytes (INST1, UAB, INST2) to read from or write to registers.
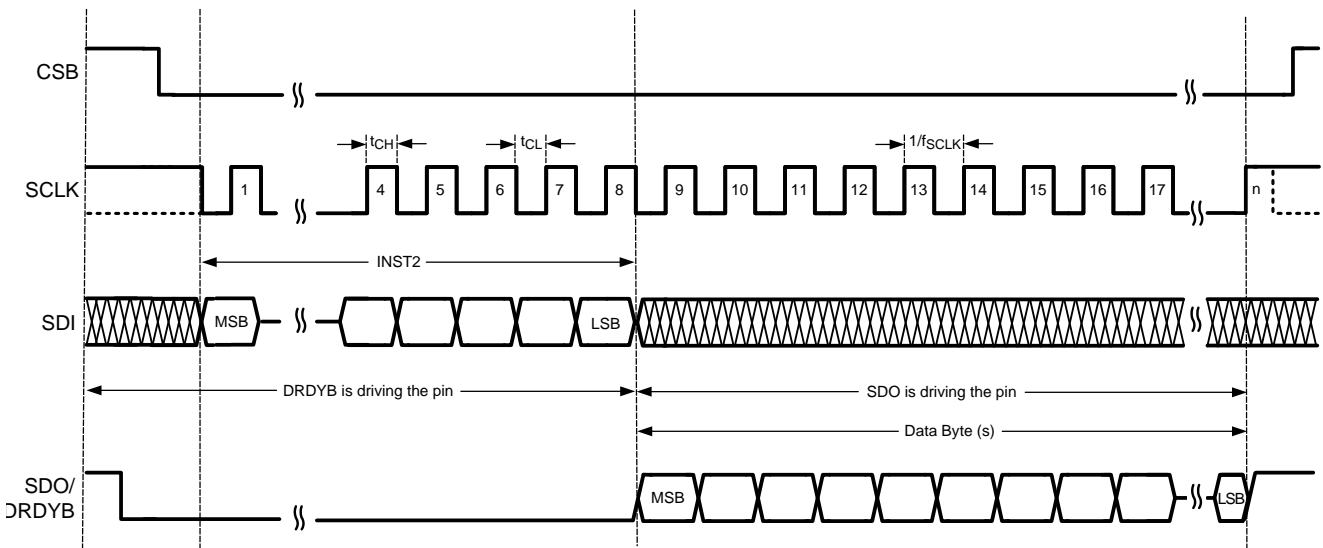
Figure 66. Timing Protocol for DRDYB Case2

9.5.11 DRDYB Case3: Routing DRDYB to D6
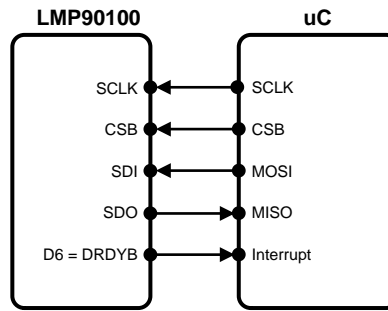
Figure 67. DRDYB Case3 Connection Diagram

The DRDYB signal can be routed to pin D6 by setting SPI_DRDYB_D6 high and SDO_DRDYB_DRIVER to 0x4. This is the behavior for DrdybCase3 as shown in Figure 67.

The timing protocol for this case can be seen in Figure 68. Because DRDYB is separated from SDO, it can be monitored using the interrupt or polling method. If polled, the DRDYB signal needs to be polled faster than t_{DRDYB} to detect a DRDYB assertion. When DRDYB asserts, assert CSB to start the SPI transaction and begin writing the Instruction Bytes (INST1, UAB, INST2) to read from or write to registers.
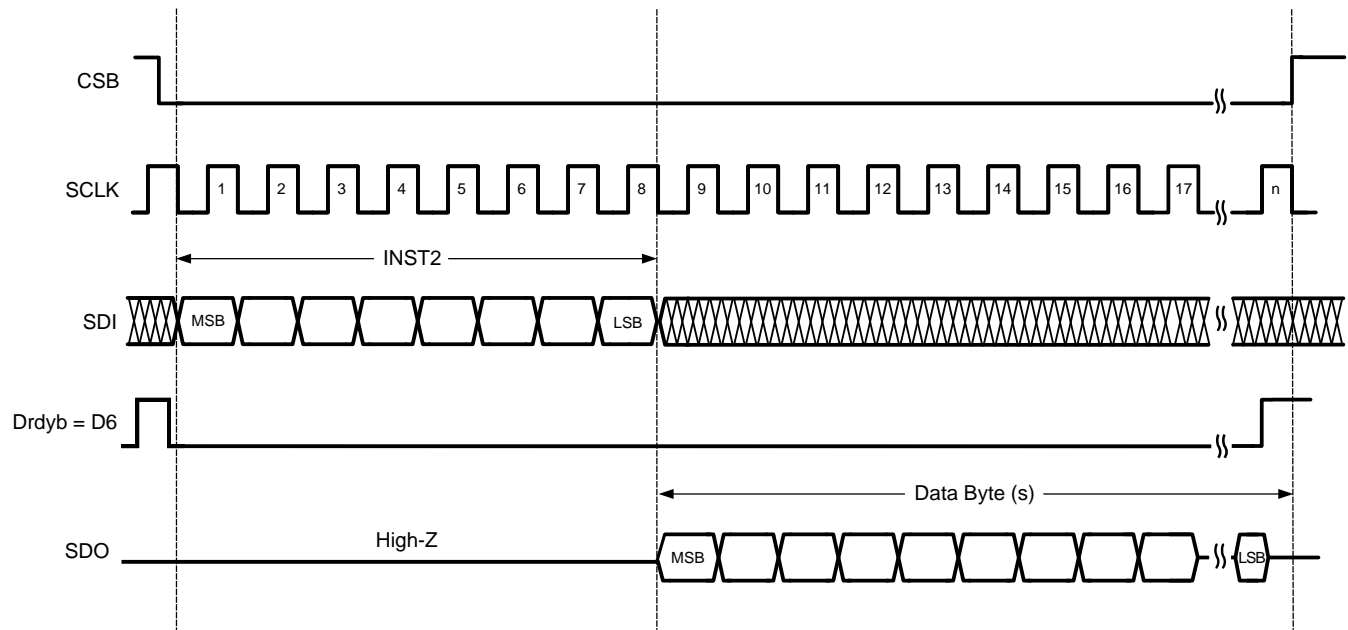
Figure 68. Timing Protocol for DRDYB Case3

9.5.12 Data Only Read Transaction

In a data only read transaction, one can directly access the data byte(s) as soon as the CSB is asserted without having to send any instruction byte. This is useful as it brings down the latency as well as the overhead associated with the instruction byte (as well as the Upper Address Byte, if any).

In order to use the data only transaction, the device must be placed in the data first mode. The following table lists transaction formats for placing the device in and out of the data first mode and reading the mode status.

Table 6. Data First Mode Transactions

	Bit[7]	Bits[6:5]	Bit[4]	Bits[3:0]	Data Bytes
Enable Data First Mode Instruction	1	11	1	1010	None
Disable Data First Mode Instruction	1	11	1	1011	None
Read Mode Status Transaction	1	00	1	1111	One

Note that while being in the data first mode, once the data bytes in the data only read transaction are sent out, the device is ready to start on any normal (non-data-only) transaction including the Disable Data First Mode Instruction. The current status of the data first mode (enabled/disabled status) can be read back using the Read Mode Status Transaction. This transaction consists of the Read Mode Status Instruction followed by a single data byte (driven by the device). The data first mode status is available on bit [1] of this data byte.

The data only read transaction allows reading up to eight consecutive registers, starting from any start address. Usually, the start address will be the address of the most significant byte of conversion data, but it could just as well be any other address. The start address and number of bytes to be read during the data only read transaction can be programmed using the DATA_ONLY_1 AND DATA_ONLY_2 registers respectively.

The upper register address is unaffected by a data only read transaction. That is, it retains its setting even after encountering a data only transaction. The data only transaction uses its own address (including the upper address) from the DATA_ONLY_1 register. When in the data first mode, the SCLK must stop high before entering the Data Only Read Transaction; this transaction should be completed before the next scheduled DRDYB deassertion.

9.5.13 Cyclic Redundancy Check (CRC)

CRC can be used to ensure integrity of data read from LMP90xxx. To enable CRC, set EN_CRC high. Once CRC is enabled, the CRC value is calculated and stored in SPI_CRC_DAT so that the master device can periodically read for data comparison. Conveniently, the SPI_CRC_DAT register address is located next to the ADC_DOUT register address so that the CRC value can be easily read as part of the data set. The CRC is automatically reset when CSB or DRDYB is deasserted.

The CRC polynomial is $x^8 + x^5 + x^4 + 1$. The reset value of the SPI_CRC_DAT register is zero, and the final value is ones-complemented before it is sent out. Note that CRC computation only includes the bits sent out on SDO and does not include the bits of the SPI_CRC_DAT itself; thus it is okay to read SPI_CRC_DAT repeatedly.

The DRDYB signal normally deasserts (active high) every 1/ODR second or when the LSB of ADC_DOUTL is read. However, this behavior can be changed so that DRDYB deassertion can occur after SPI_CRC_DAT is read, but not later than normal DRDYB deassertion which occurs at every 1/ODR seconds. This is done by setting bit DRDYB_AFT_CRC high.

The timing protocol for CRC can be found in Figure 69.
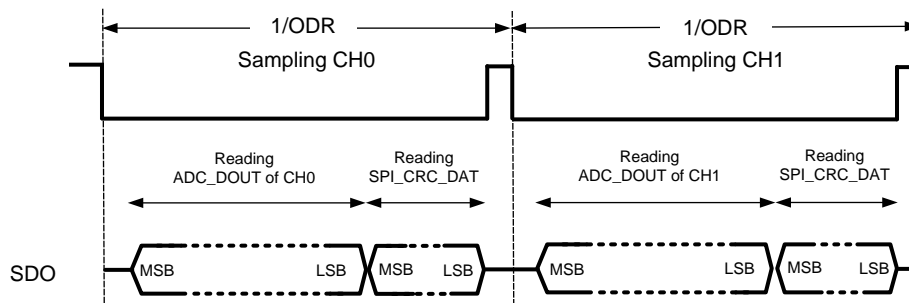
Figure 69. Timing Protocol for Reading SPI_CRC_DAT

If SPI_CRC_DAT read extends beyond the normal DRDYB deassertion at every 1/ODR seconds, then CRC_RST has to be set in the SPI Data Ready Bar Control Register. This is done to avoid a CRC reset at the DRDYB deassertion. Timing protocol for reading CRC with CRC_RST set is shown in Figure 70.
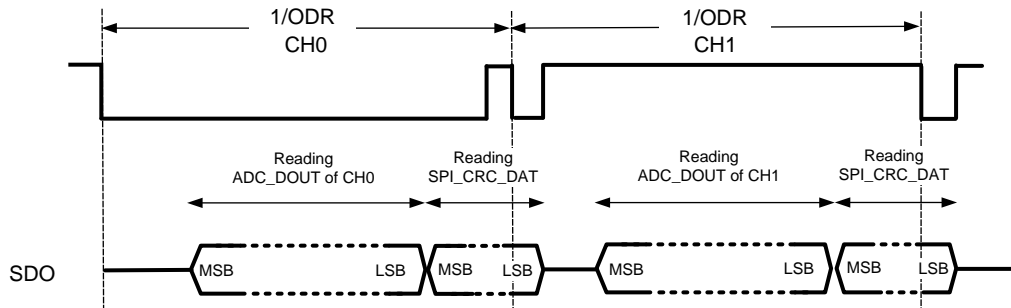
Figure 70. Timing Protocol for Reading SPI_CRC_DAT Beyond Normal DRDYB Deassertion at Every 1/ODR seconds

Follow the steps below to enable CRC:

1. Set SPI_CRC_CN = 1 (register 0x13, bit 4) to enable CRC.
2. Set DRDYB_AFT_CRC = 1 (register 0x13, bit 2) to dessert the DRDYB after CRC.
3. Compute the CRC externally, which should include ADC_DOUTH, ADC_DOUTM , and ADC_DOUTL.
4. Collect the data and verify the reported CRC matches with the computed CRC (step above).

9.5.14 Register Read/Write Examples

9.5.14.1 Writing To Register Examples

Using the register read/write protocol shown in Figure 60, the following example shows how to write three data bytes starting at register address (ADDR) 0x1F. After the last byte has been written to ADDR 0x21, deassert CSB to end the register-write.
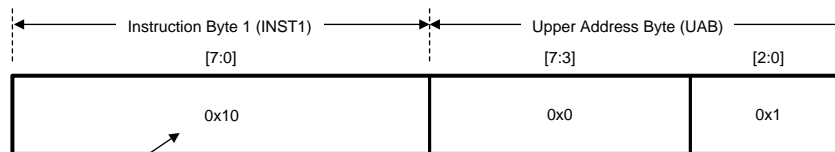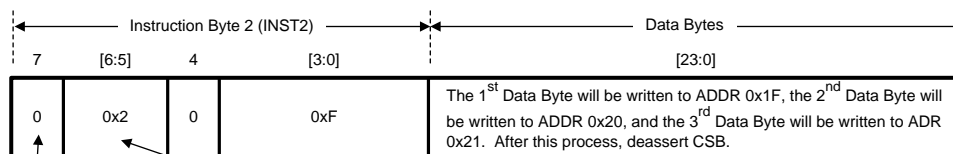
Figure 71. Register-Write Example 1

The next example shows how to write one data byte to ADDR 0x12. Because the URA for this example is the same as the last example, transaction 1 can be omitted.

Transaction 2 – Data Access

R/WB = Read/Write Data
0: Write Data
1: Read Data

SZ = Size
0x0: 1 byte
0x1: 2 bytes
0x2: 3 bytes
0x3: Streaming – 3+ bytes until CSB is de-asserted
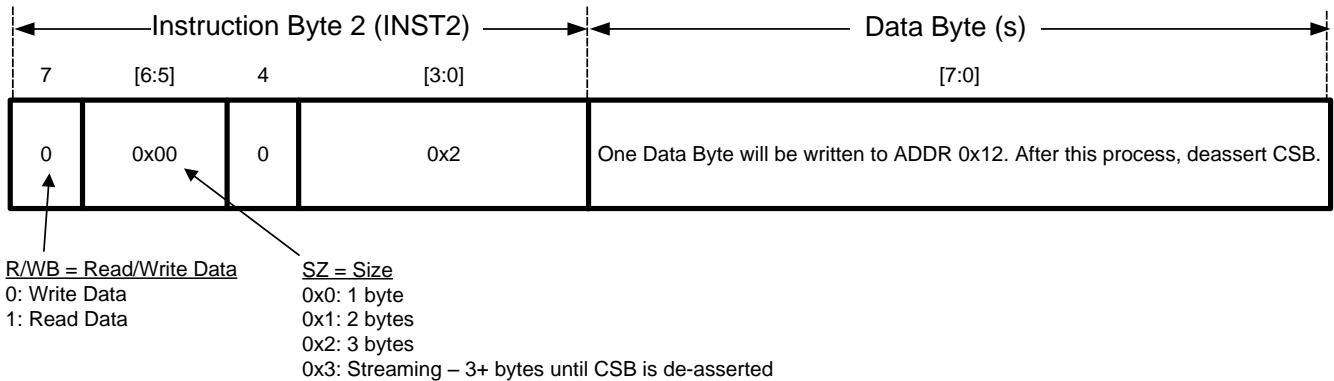
Figure 72. Register-Write Example 2

9.5.14.2 Reading From Register Example

The following example shows how to read two bytes. The first byte will be read from starting ADDR 0x24, and the second byte will be read from ADDR 0x25.

Transaction 1 – URA Setup – necessary only when the previous URA is different than the desired URA.

R/WB = Read/Write Address
0x10: Write Address
0x90: Read Address

Transaction 2 – Data Access

R/WB = Read/Write Data
0: Write Data
1: Read Data

SZ = Size
0x0: 1 byte
0x1: 2 bytes
0x2: 3 bytes
0x3: Streaming – 3+ bytes until CSB is de-asserted
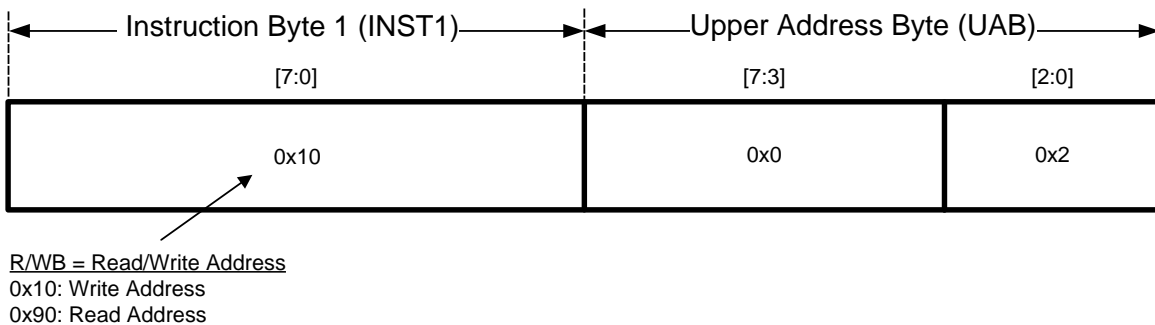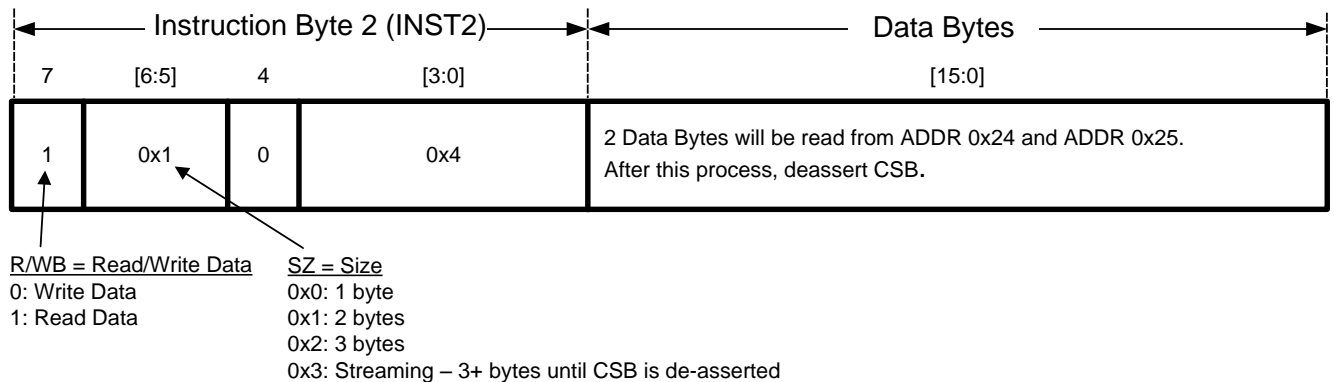
Figure 73. Register-Read Example

9.5.15 Streaming Examples

9.5.15.1 Normal Streaming Example

This example shows how to write six data bytes starting at ADDR 0x28 using the Normal Streaming mode. Because the default STRM_TYPE is the Normal Streaming mode, setting up the SPI_STREAMCN register can be omitted.

Transaction 1 – URA Setup – necessary only when the previous URA is different than the desired URA.

Instruction Byte 1 (INST1)	Upper Address Byte (UAB)	
[7:0]	[7:3]	[2:0]
0x10	0x0	0x2

R/WB = Read/Write Address
0x10: Write Address
0x90: Read Address

Transaction 2 – Data Access

Instruction Byte 2 (INST2)				Data Bytes
7	[6:5]	4	[3:0]	[47:0]
0	0x3	0	0x8	The 1st Data Byte will be written to ADDR 0x28, the 2nd Data Byte will be written to ADDR 0x29, etc. The last and 6th Data Byte will be written to ADDR 0x2D. After this process, deassert CSB.
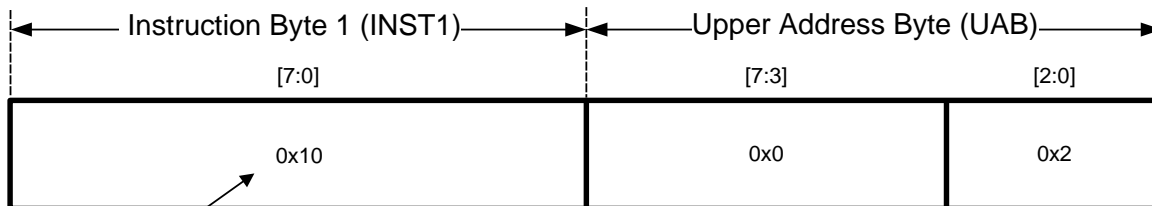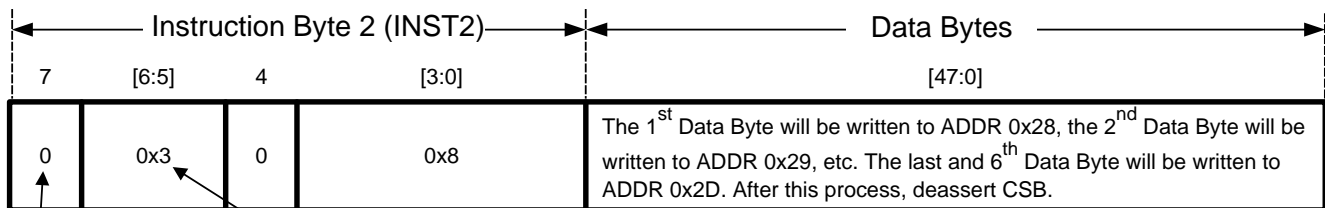
R/WB = Read/Write Data
0: Write Data
1: Read Data

SZ = Size
0x0: 1 byte
0x1: 2 bytes
0x2: 3 bytes
0x3: Streaming – 3+ bytes until CSB is de-asserted

Figure 74. Normal Streaming Example

9.5.15.2 Controlled Streaming Example

This example shows how to read the 24-bit conversion data (ADC_DOUT) four times using the Controlled Streaming mode. The ADC_DOUT registers consist of ADC_DOUTH at ADDR 0x1A, ADC_DOUTM at ADDR 0x1B, and ADC_DOUTL at ADDR 0x1C.

The first step (Figure 75) sets up the SPI_STREAMCN register. This step enters the Controlled Streaming mode by setting STRM_TYPE high in ADDR 0x03. Because three registers (ADDR 0x1A - 0x1C) need to be read, the STRM_RANGE is 2.

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Transaction 1 – URA Setup – necessary only when the previous URA is different than the desired URA.
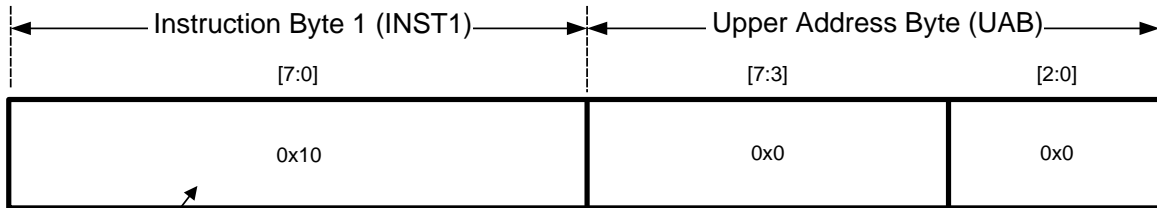
R/WB = Read/Write Address
0x10: Write Address
0x90: Read Address

Transaction 2 – Data Access
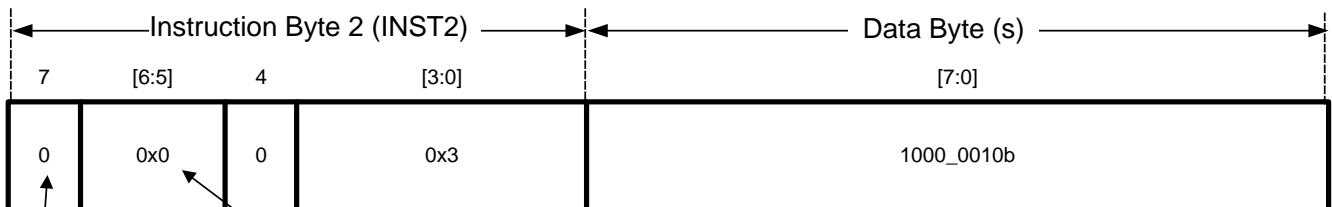
R/WB = Read/Write Data
0: Write Data
1: Read Data

SZ = Size
0x0: 1 byte
0x1: 2 bytes
0x2: 3 bytes
0x3: Streaming – 3+ bytes until CSB is de-asserted

Figure 75. Setting up SPI_STREAMCN

The next step shows how to perform the Controlled Streaming mode so that the master device will read ADC_DOUT from ADDR 0x1A, 0x1B, 0x1C, then wrap back to ADDR 0x1A, and repeat this process for four times. After this process, deassert CSB to end the Controlled Streaming mode.

Transaction 1 – URA Setup – necessary only when the previous URA is different than the desired URA.

←——————— Instruction Byte 1 (INST1) ———————→	←——————— Upper Address Byte (UAB) ———————→	
[7:0]	[7:3]	[2:0]
0x10	0x0	0x1

R/WB = Read/Write Address
0x10: Write Address
0x90: Read Address

Transaction 2 – Data Access

←———— Instruction Byte 2 (INST2) ————→				←———————— Data Byte (s) ————————→
7	[6:5]	4	[3:0]	[95:0]
1	0x3	0	0xA	Read ADC_DOUTH, ADC_DOUTM, and ADC_DOUTL four times. After this process, deassert CSB.
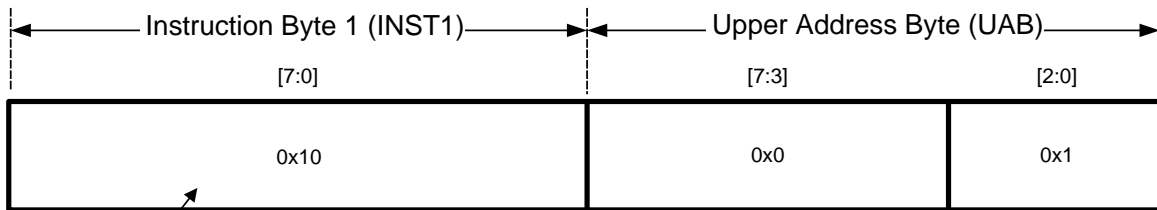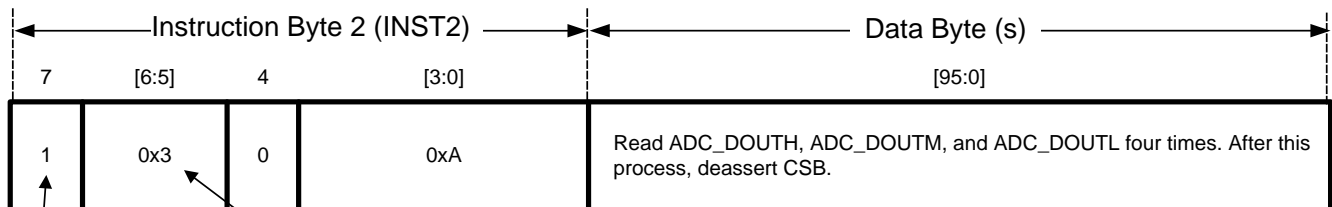
R/WB = Read/Write Data
0: Write Data
1: Read Data

SZ = Size
0x0: 1 byte
0x1: 2 bytes
0x2: 3 bytes
0x3: Streaming – 3+ bytes until CSB is de-asserted

Figure 76. Controlled Streaming Example

9.6 Register Maps

| Register Name		ADDR (URA & LRA)	Type	Default
RESETCN	Reset Control	0x00	WO	-
SPI_HANDSHAKECN	SPI Handshake Control	0x01	R/W	0x00
SPI_RESET	SPI Reset Control	0x02	R/W	0x00
SPI_STREAMCN	SPI Stream Control	0x03	R/W	0x00
Reserved	-	0x04 - 0x07	-	0x00
PWRCN	Power Mode Control and Status	0x08	RO & WO	0x00
DATA_ONLY_1	Data Only Read Control 1	0x09	R/W	0x1A
DATA_ONLY_2	Data Only Read Control 2	0x0A	R/W	0x02
ADC_RESTART	ADC Restart Conversion	0x0B	WO	-
Reserved	-	0x0C - 0x0D	-	0x00
GPIO_DIRCN	GPIO Direction Control	0x0E	R/W	0x00
GPIO_DAT	GPIO Data	0x0F	RO & WO	-
BGCALCN	Background Calibration Control	0x10	R/W	0x00
SPI_DRDYBCN	SPI Data Ready Bar Control	0x11	R/W	0x03
ADC_AUXCN	ADC Auxiliary Control	0x12	R/W	0x00
SPI_CRC_CN	CRC Control	0x13	R/W	0x02
SENDIAG_THLD	Sensor Diagnostic Threshold 1,0	0x14 - 0x15	R/W	0x0000
Reserved	-	0x16	-	0x00
SCALCN	System Calibration Control	0x17	R/W	0x00
ADC_DONE	ADC Data Available	0x18	RO	-
SENDIAG_FLAGS	Sensor Diagnostic Flags	0x19	RO	-
ADC_DOUT	Conversion Data 2,1,0	0x1A - 0x1C	RO	-
SPI_CRC_DAT	CRC Data	0x1D	RO & WO	-
CHANNEL CONFIGURATION REGISTERS (CH4 to CH6 for LMP90100/LMP9099 only)				
CH_STS	Channel Status	0x1E	RO	0x00
CH_SCAN	Channel Scan Mode	0x1F	R/W	0x30
CH0_INPUTCN	CH0 Input Control	0x20	R/W	0x01
CH0_CONFIG	CH0 Configuration	0x21	R/W	0x70
CH1_INPUTCN	CH1 Input Control	0X22	R/W	0x13
CH1_CONFIG	CH1 Configuration	0x23	R/W	0x70
CH2_INPUTCN	CH2 Input Control	0x24	R/W	0x25
CH2_CONFIG	CH2 Configuration	0x25	R/W	0x70
CH3_INPUTCN	CH3 Input Control	0x26	R/W	0x37
CH3_CONFIG	CH3 Configuration	0x27	R/W	0x70
CH4_INPUTCN	CH4 Input Control	0x28	R/W	0x01
CH4_CONFIG	CH4 Configuration	0x29	R/W	0x70
CH5_INPUTCN	CH5 Input Control	0x2A	R/W	0x13
CH5_CONFIG	CH5 Configuration	0x2B	R/W	0x70
CH6_INPUTCN	CH6 Input Control	0x2C	R/W	0x25
CH6_CONFIG	CH6 Configuration	0x2D	R/W	0x70
Reserved	-	0x2E - 0x2F	-	0x00
SYSTEM CALIBRATION REGISTERS				
CH0_SCAL_OFFSET	CH0 System Calibration Offset Coefficients	0x30 - 0x32	R/W	0x00_0000
CH0_SCAL_GAIN	CH0 System Calibration Gain Coefficients	0x33 - 0x35	R/W	0x80_0000
CH0_SCAL_SCALING	CH0 System Calibration Scaling Coefficients	0x36	R/W	0x01

Register Maps (continued)

Register Name		ADDR (URA & LRA)	Type	Default
CH0_SCAL_BITS_SELECTOR	CH0 System Calibration Bits Selector	0x37	R/W	0x00
CH1_SCAL_OFFSET	CH1 System Calibration Offset Coefficients	0x38 - 0x3A	R/W	0x00_0000
CH1_SCAL_GAIN	CH1 System Calibration Gain Coefficient	0x3B - 0x3D	R/W	0x80_0000
CH1_SCAL_SCALING	CH1 System Calibration Scaling Coefficients	0x3E	R/W	0x01
CH1_SCAL_BITS_SELECTOR	CH1 System Calibration Bits Selector	0x3F	R/W	0x00
CH2_SCAL_OFFSET	CH2 System Calibration Offset Coefficients	0x40 - 0x42	R/W	0x00_0000
CH2_SCAL_GAIN	CH2 System Calibration Gain Coefficient	0x43 - 0x45	R/W	0x80_0000
CH2_SCAL_SCALING	CH2 System Calibration Scaling Coefficients	0x46	R/W	0x01
CH2_SCAL_BITS_SELECTOR	CH2 System Calibration Bits Selector	0x47	R/W	0x00
CH3_SCAL_OFFSET	CH3 System Calibration Offset Coefficients	0x48 - 0x4A	R/W	0x00_0000
CH3_SCAL_GAIN	CH3 System Calibration Gain Coefficient	0x4B - 0x4D	R/W	0x80_0000
CH3_SCAL_SCALING	CH3 System Calibration Scaling Coefficients	0x4E	R/W	0x01
CH3_SCAL_BITS_SELECTOR	CH3 System Calibration Bits Selector	0x4F	R/W	0x00
Reserved	-	0x50 - 0x7F	-	0x00

Table 7. RESETCN: Reset Control (Address 0x00)

Bit	Bit Symbol	Bit Description
[7:0]	REG_AND_CNV_ RST	Register and Conversion Reset **0xC3:** Register and conversion reset **Others:** Neglected

Table 8. SPI_HANDSHAKECN: SPI Handshake Control (Address 0x01)

Bit	Bit Symbol	Bit Description			
[7:4]	Reserved	-			
[3:1]	SDO_DRDYB_ DRIVER	SDO/DRDYB Driver – sets who is driving the SDO/DRYB pin			
			Whenever CSB is Asserted and the Device is Reading ADC_DOUT	Whenever CSB is Asserted and the Device is Not Reading ADC_DOUT	CSB is Deasserted
		0x0 (default)	SDO is driving	DRDYB is driving	High-Z
		0x3	SDO is driving	DRDYB is driving	DRDYB is driving
		0x4	SDO is driving	High-Z	High-Z
		Others	Forbidden		
0	SW_OFF_TRG	Switch-off trigger - refers to the switching of the output drive from the slave to the master. **0 (default):** SDO will be high-Z after the last (16th, 24th, 32nd, etc) rising edge of SCLK. This option allows time for the slave to transfer control back to the master at the end of the frame. **1:** SDO's high-Z is postponed to the subsequent falling edge following the last (16th, 24th, 32nd, etc) rising edge of SCLK. This option provides additional hold time for the last bit, DB0, in non-streaming read transfers.			

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Table 9. SPI_RESET: SPI Reset Control (Address 0x02)

Bit	Bit Symbol	Bit Description
[0]	SPI_ RST	SPI Reset Enable **0x0 (default):** SPI Reset Disabled **0x1:** SPI Reset Enabled Note: Once Written, The contents of this register are sticky. That is, the content of this register cannot be changed with subsequent write. However, a Register reset clears the register as well as the sticky status.

Table 10. SPI_STREAMCN: SPI Streaming Control (Address 0x03)

Bit	Bit Symbol	Bit Description
7	STRM_TYPE	Stream type **0 (default):** Normal Streaming mode **1:** Controlled Streaming mode
[6:0]	STRM_ RANGE	Stream range – selects Range for Controlled Streaming mode **Default:** 0x00

Table 11. PWRCN: Power Mode Control and Status (Address 0x08)

Bit	Bit Symbol	Bit Description
[7:2]	Reserved	-
[1:0]	PWRCN	Power Control Write Only – power down mode control **0x0:** Active Mode **0x1:** Power-down Mode **0x3:** Stand-by Mode Read Only – the present mode is: **0x0 (default):** Active Mode **0x1:** Power-down Mode **0x3:** Stand-by Mode

Table 12. DATA_ONLY_1: Data Only Read Control 1 (Address 0x09)

Bit	Bit Symbol	Bit Description
7	Reserved	-
[6:0]	DATA_ONLY_ADR	Start address for the Data Only Read Transaction **Default:** 0x1A Please refer to the description of DT_ONLY_SZ in DATA_ONLY_2 register.

Table 13. DATA_ONLY_2: Data Only Read Control 2 (Address 0x0A)

Bit	Bit Symbol	Bit Description
[7:3]	Reserved	-
[2:0]	DATA_ONLY_SZ	Number of bytes to be read out in Data Only mode. A value of 0x0 means read one byte and 0x7 means read 8 bytes. **Default:** 0x2

Table 14. ADC_RESTART: ADC Restart Conversion (Address 0x0B)

Bit	Bit Symbol	Bit Description
[7:1]	Reserved	-
0	RESTART	Restart conversion **1**: Restart conversion.

Table 15. GPIO_DIRCN: GPIO Direction (Address 0x0E)

Bit	Bit Symbol	Bit Description
7	Reserved	-
x	GPIO_DIRCNx	GPIO direction control – these bits are used to control the direction of each General Purpose Input/Outputs (GPIO) pins D0 - D6. **0 (default):** Dx is an Input **1:** Dx is an Output where 0 ≤ x ≤ 6. For example, writing a 1 to bit 6 means D6 is an Output. Note: If D6 is used for DRDYB, then it cannot be used for GPIO.

Table 16. GPIO_DAT: GPIO Data (Address 0x0F)

Bit	Bit Symbol	Bit Description
7	Reserved	-
x	Dx	Write Only - when GPIO_DIRCNx = 0 0: Dx is LO 1: Dx is HI Read Only - when GPIO_DIRCNx = 1 0: Dx driven LO 1: Dx driven HI where 0 ≤ x ≤ 6. For example, writing a 0 to bit 4 means D4 is LO. It is okay to Read the GPIOs that are configured as outputs and write to GPIOs that are configured as inputs. Reading the GPIOs that are outputs would return the current value on those GPIOs, and writing to the GPIOs that are inputs are neglected

Table 17. BGCALCN: Background Calibration Control (Address 0x10)

Bit	Bit Symbol	Bit Description
[7:2]	Reserved	-
[1:0]	BGCALN	Background calibration control – selects scheme for continuous background calibration. **0x0 (default):** BgcalMode0: Background Calibration OFF **0x1:** BgcalMode1: Offset Correction / Gain Estimation **0x2:** BgcalMode2: Offset Correction / Gain Correction **0x3:** BgcalMode3: Offset Estimation / Gain Estimation

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Table 18. SPI_DRDYBCN: SPI Data Ready Bar Control (Address 0x11)

Bit	Bit Symbol	Bit Description
7	SPI_DRDYB_D6	Enable DRDYB on D6 **0 (default):** D6 is a GPIO **1:** D6 = DRDYB signal
6	Reserved	-
5	CRC_RST	CRC Reset **0 (default):** Enable CRC reset on DRDYB deassertion **1:** Disable CRC reset on DRDYB deassertion
4	Reserved	-
3	FGA_BGCAL	Gain background calibration **0 (default):** Correct FGA gain error. This is useful only if the device is operating in BgcalMode2 and ScanMode2 or ScanMode3. **1:** Correct FGA gain error using the last known coefficients.
[2:0]	Reserved	Default - 0x3 (do not change this value)

Table 19. ADC_AUXCN: ADC Auxiliary Control (Address 0x12)

Bit	Bit Symbol	Bit Description
7	Reserved	-
6	RESET_SYSCAL	The System Calibration registers (CHx_SCAL_OFFSET and CHx_SCAL_GAIN) are: **0 (default):** preserved even when "REG_AND_CNV_ RST" = 0xC3. **1:** reset by setting "REG_AND_CNV_ RST" = 0xC3.
5	CLK_EXT_DET	External clock detection **0 (default):** "External Clock Detection" is operational **1:** "External-Clock Detection" is bypassed
4	CLK_SEL	Clock select – only valid if CLK_EXT_DET = 1 **0 (default):** Selects internal clock **1:** Selects external clock
[3:0]	RTD_CUR_SEL (LMP90100 and LMP90098 only)	Selects RTD Current as follows: **0x0 (default):** 0 µA **0x1:** 100 µA **0x2:** 200 µA **0x3:** 300 µA **0x4:** 400 µA **0x5:** 500 µA **0x6:** 600 µA **0x7**: 700 µA **0x8:** 800 µA **0x9:** 900 µA **0xA:** 1000 µA

Table 20. SPI_CRC_CN: CRC Control (Address 0x13)

Bit	Bit Symbol	Bit Description
[7:5]	Reserved	-
4	EN_CRC	Enable CRC **0 (default):** Disable CRC **1:** Enable CRC
3	Reserved	Default - 0x0 (do not change this value)
2	DRDYB_AFT_CRC	DRDYB After CRC **0 (default):** DRDYB is deasserted (active high) after ADC_DOUTL is read. **1:** DRDYB is deasserted after SPI_CRC_DAT (which follows ADC_DOUTL), is read.
[1:0]	Reserved	-

Table 21. SENDIAG_THLD: Sensor Diagnostic Threshold (Address 0x14 to 0x15)

Address	Name	Register Description
0x14	SENDIAG_THLDH	Sensor Diagnostic threshold [15:8]
0x15	SENDIAG_THLDL	Sensor Diagnostic threshold [7:0]

Table 22. SCALCN: System Calibration Control (Address 0x17)

Bit	Bit Symbol	Bit Description
[7:2]	Reserved	-
[1:0]	SCALCN	System Calibration Control When written, set SCALCN to: **0x0 (default):** Normal Mode **0x1:** "System Calibration Offset Coefficient Determination" mode **0x2:** "System Calibration Gain Coefficient Determination" mode **0x3:** Reserved When read, this bit indicates the system calibration mode is in: **0x0:** Normal Mode **0x1:** "System Calibration Offset Coefficient Determination" mode **0x2:** "System Calibration Gain Coefficient Determination" mode **0x3:** Reserved Note: when read, this bit will indicate the current System Calibration status. Because this coefficient determination mode will only take 1 conversion cycle, reading this register will only return 0x00, unless this register is read within 1 conversion window.

Table 23. ADC_DONE: ADC Data Available (Address 0x18)

Bit	Bit Symbol	Bit Description
[7:0]	DT_AVAIL_B	Data Available – indicates if new conversion data is available **0x00 − 0xFE:** Available **0xFF:** Not available

Table 24. SENDIAG_FLAGS: Sensor Diagnostic Flags (Address 0x19)

Bit	Bit Symbol	Bit Description
7	SHORT_THLD_ FLAG	Short Circuit Threshold Flag = 1 when the absolute value of VOUT is within the absolute threshold voltage set by SENDIAG_THLDH and SENDIAG_THLDL.
6	RAILS_FLAG	Rails Flag = 1 when at least one of the inputs is near rail (VA or GND).
5	POR_AFT_LST_RD	Power-on-reset after last read = 1 when there was a power-on-reset event because the last time the SENDIAG_FLAGS register was read.
[4:3]	OFLO_FLAGS	Overflow flags **0x0:** Normal operation **0x1:** The modulator was not overranged, but ADC_DOUT got clamped to 0x7f_ffff (positive fullscale) or 0x80_0000 (negative full scale) **0x2:** The modulator was over-ranged (VIN > 1.3*VREF/GAIN) **0x3:** The modulator was over-ranged (VIN < -1.3*VREF/GAIN)
[2:0]	SAMPLED_CH	Channel Number – the sampled channel for ADC_DOUT and SENDIAG_FLAGS.

Table 25. ADC_DOUT: 24-Bit Conversion Data (Two's Complement) (Address 0x1A - 0x1C)

Address	Name	Register Description
0x1A	ADC_DOUTH	ADC Conversion Data [23:16]
0x1B	ADC_DOUTM	ADC Conversion Data [15:8]
0x1C	ADC_DOUTL	ADC Conversion Data [7:0]

Note: Repeat reads of these registers are allowed as long as such reads are spaced apart by at least 72 µs.

Table 26. SPI_CRC_DAT: CRC Data (Address 0x1D)

Bit	Bit Symbol	Bit Description
[7:0]	CRC_DAT	CRC Data When written, this register reset CRC: **Any Value:** Reset CRC When read, this register indicates the CRC data.

Table 27. CH_STS: Channel Status (Address 0x1E)

Bit	Bit Symbol	Bit Description
[7:2]	Reserved	-
1	CH_SCAN_NRDY	Channel Scan Not Ready – indicates if it is okay to program CH_SCAN 0: Update not pending, CH_SCAN register is okay to program 1: Update pending, CH_SCAN register is not ready to be programmed
0	INV_OR_RPT_RD_STS	Invalid or Repeated Read Status 0: ADC_DOUT just read was valid and hitherto unread 1: ADC_DOUT just read was either invalid (not ready) or there was a repeated read.

Table 28. CH_SCAN: Channel Scan Mode (Address 0x1F)

Bit	Bit Symbol	Bit Description
[7:6]	CH_SCAN_SEL	Channel Scan Select **0x0 (default):** ScanMode0: Single-Channel Continuous Conversion **0x1:** ScanMode1: One or more channels Single Scan **0x2:** ScanMode2: One or more channels Continuous Scan **0x3**: ScanMode3: One or more channels Continuous Scan with Burnout Currents
[5:3]	LAST_CH (CH4 to CH6 for LMP90100 and LMP90099 only)	Last channel for conversion **0x0:** CH0 **0x1:** CH1 **0x2:** CH2 **0x3:** CH3 **0x4:** CH4 **0x5:** CH5 **0x6 (default):** CH6 Note: LAST_CH cannot be smaller than FIRST_CH. For example, if LAST_CH = CH5, then FIRST_CH cannot be CH6. If 0x7 is written it is ignored.
[2:0]	FIRST_CH (CH4 to CH6 for LMP90100 and LMP90099 only)	Starting channel for conversion **0x0 (default):** CH0 **0x1:** CH1 **0x2:** CH2 **0x3:** CH3 **0x4:** CH4 **0x5:** CH5 **0x6:** CH6 Note: FIRST_CH cannot be greater than LAST_CH. For example, if FIRST_CH = CH1, then LAST_CH cannot be CH0. If 0x7 is written it is ignored.

Note: While writing to the CH_SCAN register, if 0x7 is written to FIRST_CH or LAST_CH the write to the entire CH_SCAN register is ignored.

Table 29. CHx_INPUTCN: Channel Input Control (CH4 to CH6 for LMP90100/LMP9099 Only)[1]

Bit	Bit Symbol	Bit Description
7	BURNOUT_EN	Enable sensor diagnostic **0 (default):** Disable Sensor Diagnostics current injection for this Channel **1:** Enable Sensor Diagnostics current injection for this Channel
6	VREF_SEL	Select the reference 0 (Default): Select VREFP1 and VREFN1 1: Select VREFP2 and VREFN2
[5:3]	VINP	Positive input select **0x0:** VIN0 **0x1:** VIN1 **0x2:** VIN2 **0x3:** VIN3 (LMP90100/LMP90099 only) **0x4:** VIN4 (LMP90100/LMP90099 only) **0x5:** VIN5 (LMP90100/LMP90099 only) **0x6:** VIN6 **0x7:** VIN7 Note: to see the default values for each channel, refer to the table below.
[2:0]	VINN	Negative input select **0x0:** VIN0 **0x1:** VIN1 **0x2:** VIN2 **0x3:** VIN3 (LMP90100/LMP90099 only) **0x4:** VIN4 (LMP90100/LMP90099 only) **0x5:** VIN5 (LMP90100/LMP90099 only) **0x6:** VIN6 **0x7:** VIN7 Note: to see the default values for each channel, refer to the table below.

(1) Register Address (hex):
    (a) CH0: 0x20
    (b) CH1: 0X22
    (c) CH2: 0x24
    (d) CH3: 0x26
    (e) CH4: 0x28
    (f) CH5: 0x2A
    (g) CH6: 0x2C

Table 30. Default VINx for CH0 to CH6

	VINP	VINN
CH0	VIN0	VIN1
CH1	VIN2	VIN3 (LMP90100/LMP90099 only)
CH2	VIN4 (LMP90100/LMP90099 only)	VIN5 (LMP90100/LMP90099 only)
CH3	VIN6	VIN7
CH4 (LMP90100/LMP90099 only)	VIN0	VIN1
CH5 (LMP90100/LMP90099 only)	VIN2	VIN3
CH6 (LMP90100/LMP90099 only)	VIN4	VIN5

Table 31. CHx_CONFIG: Channel Configuration (CH4 to CH6 LMP90100/LMP90099 Only)[1]

Bit	Bit Symbol	Bit Description
7	Reserved	-
[6:4]	ODR_SEL	ODR Select **0x0:** 13.42 / 8 = 1.6775 SPS **0x1:** 13.42 / 4 = 3.355 SPS **0x2:** 13.42 / 2 = 6.71 SPS **0x3:** 13.42 SPS **0x4:** 214.65 / 8 = 26.83125 SPS **0x5:** 214.65 / 4 = 53.6625 SPS **0x6:** 214.65 / 2 = 107.325 SPS **0x7(default):** 214.65 SPS
[3:1]	GAIN_SEL	Gain Select **0x0 (default):** 1 (FGA OFF) **0x1:** 2 (FGA OFF) **0x2:** 4 (FGA OFF) **0x3:** 8 (FGA OFF) **0x4:** 16 (FGA ON) **0x5:** 32 (FGA ON) **0x6:** 64 (FGA ON) **0x7:** 128 (FGA ON)
0	BUF_EN	Enable/Disable the buffer **0 (default):** Exclude the buffer in the signal path **1:** Include the buffer from the signal path Note: When gain ≥ 16, the buffer is automatically included in the signal path irrespective of this bit.

(1) Register Address (hex):
    (a) CH0: 0x21
    (b) CH1: 0x23
    (c) CH2: 0x25
    (d) CH3: 0x27
    (e) CH4: 0x29
    (f) CH5: 0x2B
    (g) CH6: 0x2D

Table 32. CHX_SCAL_OFFSET: CH0 to CH3 System Calibration Offset Registers (Two's Complement)

ADDR				NAME	DESCRIPTION
CH0	CH1	CH2	CH3		
0x30	0x38	0x40	0x48	CHx_SCAL_OFFSETH	System Calibration Offset Coefficient Data [23:16]
0x31	0x39	0x41	0x49	CHx_SCAL_OFFSETM	System Calibration Offset Coefficient Data [15:8]
0x32	0x3A	0x42	0x4A	CHx_SCAL_OFFSETL	System Calibration Offset Coefficient Data[7:0]

Table 33. CHX_SCAL_GAIN: CH0 to CH3 System Calibration Gain Registers (Fixed Point 1.23 Format)

ADDR				NAME	DESCRIPTION
CH0	CH1	CH2	CH3		
0x33	0x3B	0x43	0x4B	CHx_SCAL_GAINH	System Calibration Gain Coefficient Data [23:16]
0x34	0x3C	0x44	0x4C	CHx_SCAL_GAINM	System Calibration Gain Coefficient Data [15:8]
0x35	0x3D	0x45	0x4D	CHx_SCAL_GAINL	System Calibration Gain Coefficient Data[7:0]

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Table 34. CHX_SCAL_SCALING: CH0 to CH3 System Calibration Scaling Coefficient Registers

ADDR				NAME	DESCRIPTION
CH0	CH1	CH2	CH3		
0x36	0x3E	0x46	0x4E	CHx_SCAL_SCALING	System Calibration Scaling Coefficient Data [5:0]

Table 35. CHX_SCAL_BITS_SELECTOR: CH0 to CH3 System Calibration Bits Selector Registers

ADDR				NAME	DESCRIPTION
CH0	CH1	CH2	CH3		
0x37	0x3F	0x47	0x4F	CHx_SCAL_BITS_SELECTOR	System Calibration Bits Selection Data [2:0]

10 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The LMP90100/LMP90099/LMP90098/LMP90097 are highly integrated, multi-channel, low power 24-bit Sensor AFEs. The devices features a precision, 24-bit Sigma Delta Analog-to-Digital Converter (ADC) with a low-noise programmable gain amplifier and a fully differential high impedance analog input multiplexer. A true continuous background calibration feature allows calibration at all gains and output data rates without interrupting the signal path. The background calibration feature essentially eliminates gain and offset errors across temperature and time, providing measurement accuracy without sacrificing speed and power consumption.

10.1.1 Quick Start

This section shows step-by-step instructions to configure the LMP90xxx to perform a simple DC reading from CH0.

1. Apply VA = VIO = VREFP1 = 5V, and ground VREFN1
2. Apply VINP = ¾VREF and VINN = ¼VREF for CH0. Thus, set CH0 = VIN = VINP - VINN = ½VREF (CH0_INPUTCN register)
3. Set gain = 1 (CH0_CONFIG: GAIN_SEL = 0x0)
4. Exclude the buffer from the signal path (CH0_CONFIG: BUF_EN = 0)
5. Set the background to BgcalMode2 (BGCALCN = 0x2)
6. Select VREF1 (CH0_INPUTCN: VREF_SEL = 0)
7. To use the internal CLK, set CLK_EXT_DET = 1 and CLK_SEL = 0.
8. Follow the register read/write protocol (Figure 60) to capture ADC_DOUT from CH0.

10.1.2 ADC_DOUT Calculation

The output code of the LMP90xxx can be calculated as:

$$\text{ADC\_DOUT} = \pm \left(\frac{(\text{VINP} - \text{VINN}) \times \text{GAIN}}{\text{VREFP} - \text{VREFN}} \right) \times \left(2^{23} \right)$$

Equation 1 — Output Code (13)

ADC_DOUT is in 24−bit two's complement binary format. The largest positive value is 0x7F_FFFF while the largest negative value is 0x80_0000. In case of an over range the value is automatically clamped to one of these two values.

Figure 77 shows the theoretical output code, ADC_DOUT, vs. analog input voltage, VIN, using the equation above.
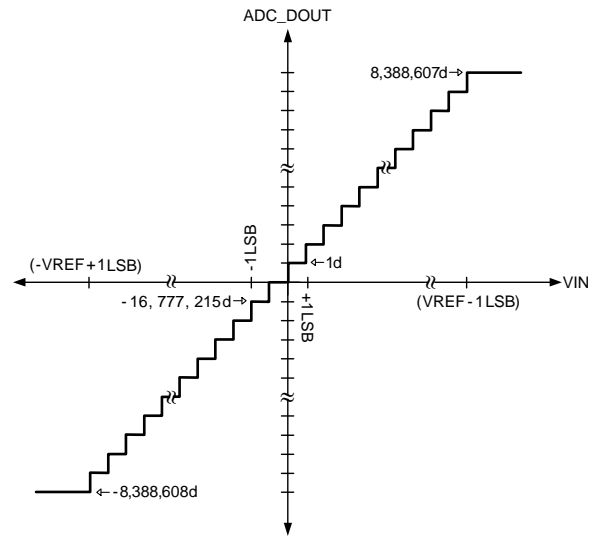
Application Information (continued)

Figure 77. ADC_DOUT vs. VIN of a 24-Bit Resolution (VREF = 5.5V, Gain = 1).

10.2 Typical Applications
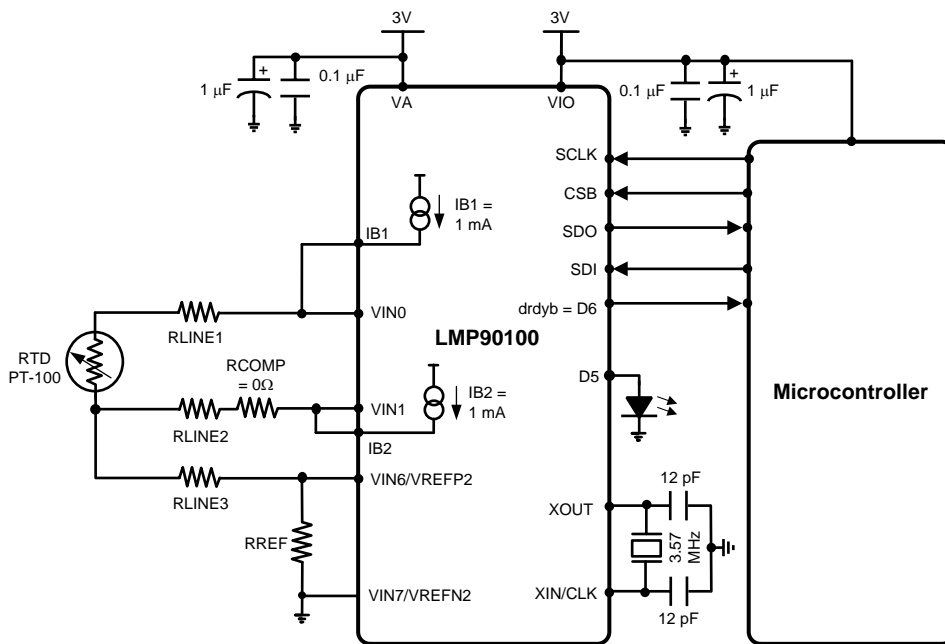
10.2.1 3-Wire RTD Using 2 Current Sources

Figure 78. Topology 1: 3-Wire RTD Using 2 Current Sources

10.2.1.1 Design Requirements

- VA = 3V
- VIO = 3V
- 3-Wire RTD using 2 current sources

Typical Applications (continued)

10.2.1.2 Detailed Design Procedure

Figure 78 shows the first topology for a 3-wire resistive temperature detector (RTD) application. Topology 1 uses two excitation current sources, IB1 and IB2, to create a differential voltage across VIN0 and VIN1. As a result of using both IB1 and IB2, only one channel (VIN0-VIN1) needs to be measured. As shown in Equation 14, the equation for this channel is IB1 x (RTD – RCOMP) assuming that RLINE1 = RLINE2. Equation 14 is the VIN equation for Topology 1.

VIN0 = IB1 (RLINE1 + RTD) + (IB1 + IB2) (RLINE3 + RREF)
VIN1 = IB2 (RLINE2 + RCOMP) + (IB1 + IB2) (RLINE3 + RREF)
If RLINE1 = RLINE2, then:
VIN = (VIN0 - VIN1) = IB1 (RTD - RCOMP)

(14)

The PT-100 changes linearly from 100Ω at 0°C to 146.07Ω at 120°C. If desired, choose a suitable compensating resistor (RCOMP) so that VIN can be virtually 0V at any desirable temperature. For example, if RCOMP = 100Ω, then at 0°C, VIN = 0V and thus a higher gain can be used.

The advantage of this circuit is its ratiometric configuration, where VREF = (IB1 + IB2) x (RREF). Equation 15 shows that a ratiometric configuration eliminates IB1 and IB2 from the output equation, thus increasing the overall performance. Equation 15 is for ADC_DOUT showing IB1 and IB2 eimination.

$$ADC\_DOUT = \frac{VIN(Gain)}{2VREF}(2^n)$$

$$ADC\_DOUT = \frac{[IB1(RTD - RCOMP)Gain]}{2(IB1+IB2)RREF}(2^n)$$

$$ADC\_DOUT = \frac{[(RTD - RCOMP)Gain]}{2(2)RREF}(2^n)$$

(15)

10.2.1.3 Application Curve
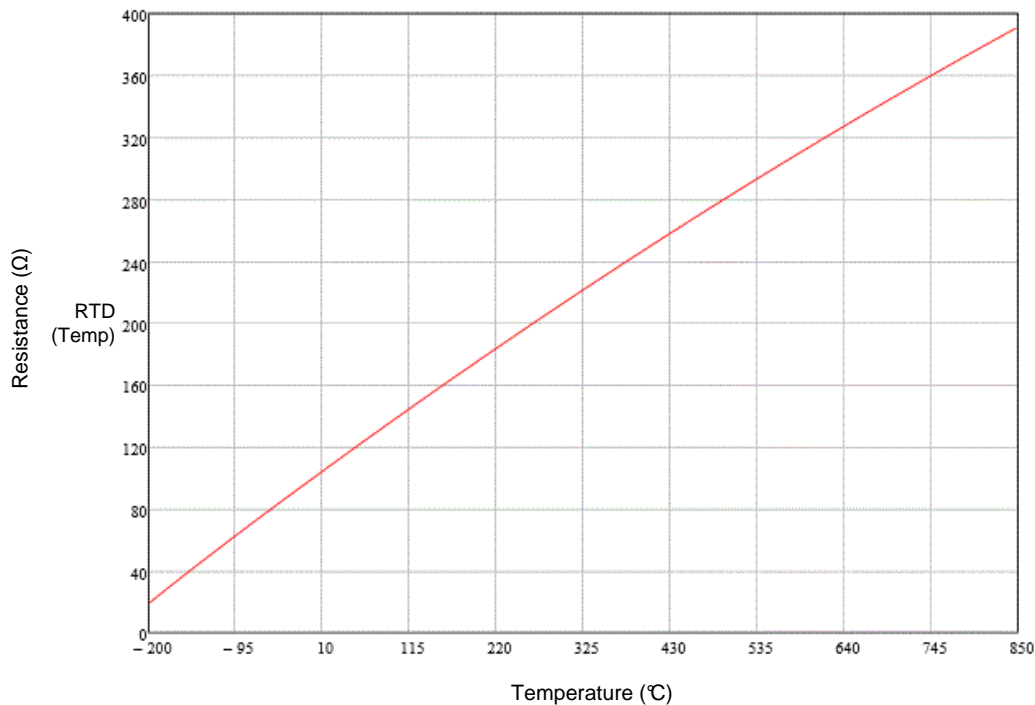
Figure 79. PT-100 RTD Resistance from –200°C to 850°C

Typical Applications (continued)

10.2.2 3-Wire RTD Using 1 Current Source
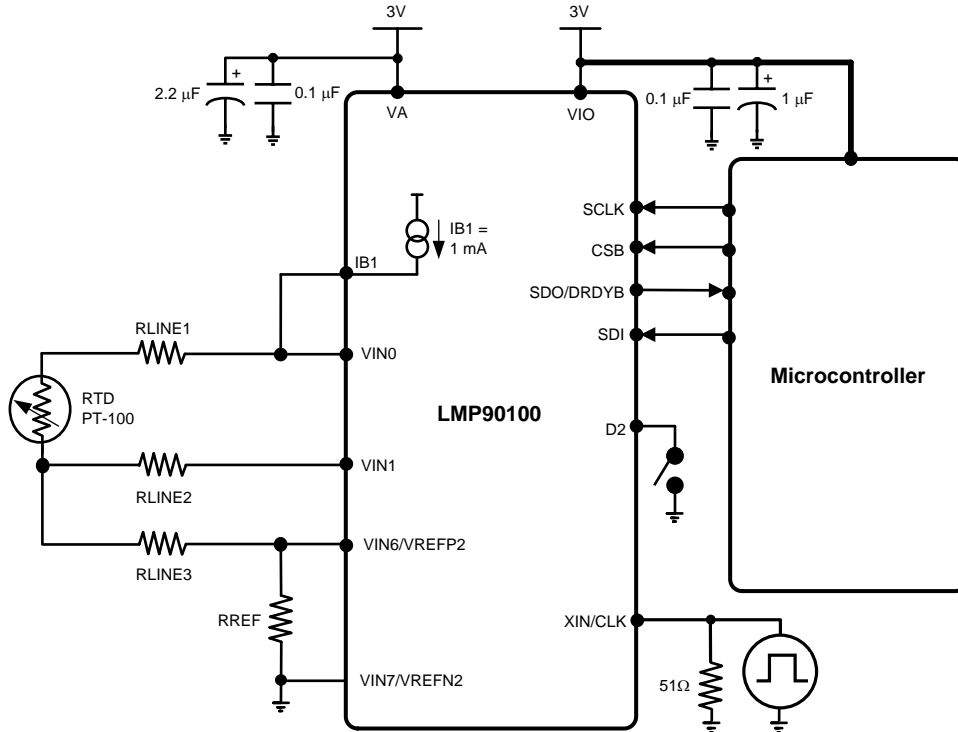
Figure 80. Topology 2: 3-Wire RTD Using 1 Current Source

10.2.2.1 Design Requirements

- VA = 3V
- VIO = 3V
- 3-Wire RTD using 1 current source

10.2.2.2 Detailed Design Procedure

Figure 80 shows the second topology for a 3-wire RTD application. Topology 2 shows the same connection as topology 1, but without IB2. Although this topology eliminates a current source, it requires two channel measurements as shown in Equation 4.

VIN0 = IB1 (RLINE1 + RTD + RLINE3 + RREF)
VIN1 = IB1 (RLINE3 + RREF)
VIN6 = IB1 (RREF)

CH0 = VIN0 - VIN1 = IB1 (RLINE1 + RTD)
CH1 = VIN1 - VIN6 = IB1 (RLINE3)

Assume RLINE1 = RLINE3, thus:
CH0 - CH1 = IB1 (RTD)

Equation 4 — VIN Equation for Topology 2   (16)

Typical Applications (continued)

10.2.2.3 Application Curve
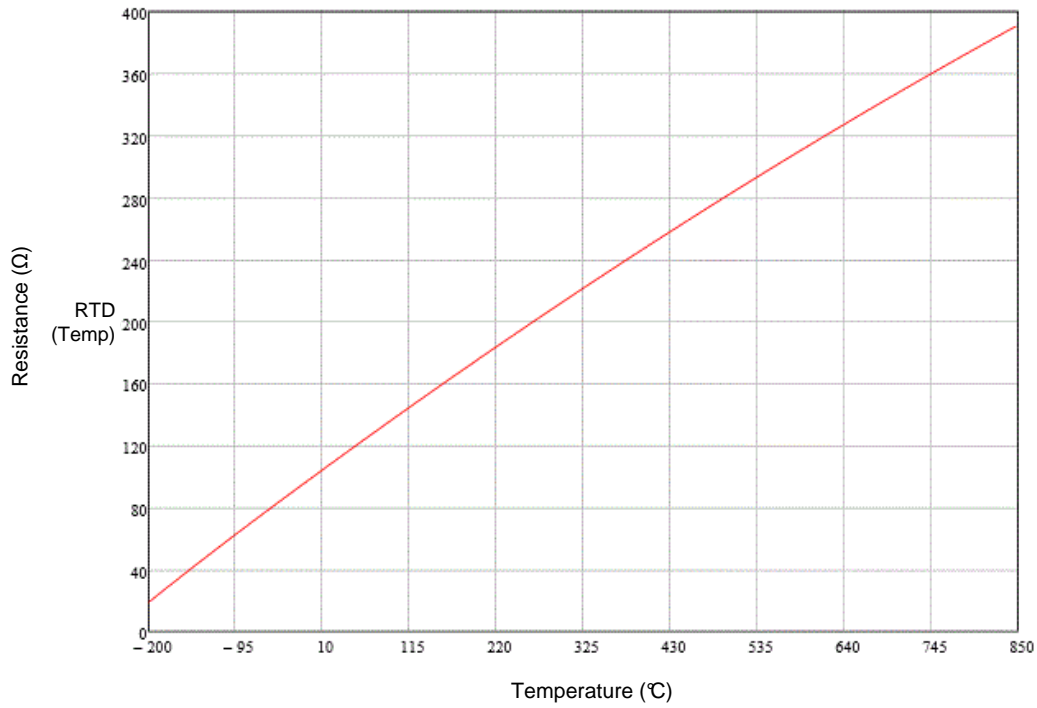
Figure 81. PT-100 RTD Resistance from –200°C to 850°C

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Typical Applications (continued)

10.2.3 Thermocouple with Cold Junction Compensation
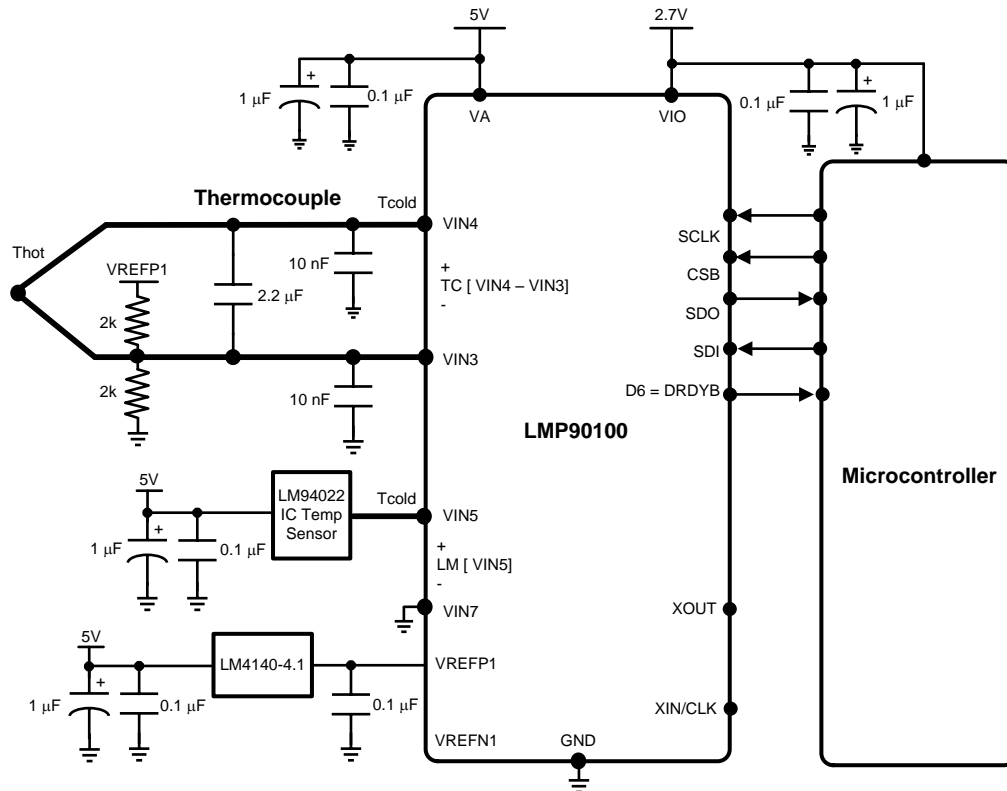
Figure 82. Thermocouple With CJC

10.2.3.1 Design Requirements

- VA = 5V
- VIO = 2.7V
- Thermocouple with Cold Junction Compensation

10.2.3.2 Detailed Design Procedure

The LMP90xxx is also ideal for thermocouple temperature applications. Thermocouples have several advantages that make them popular in many industrial and medical applications. Compare to RTDs, thermistors, and IC sensors, thermocouples are the most rugged, least expensive, and can operate over the largest temperature range.

A thermocouple is a sensor whose junction generates a differential voltage, VIN, that is relative to the temperature difference (Thot – Tcold). Thot is also known as the measuring junction or "hot" junction, which is placed at the measured environment. Tcold is also known as the reference or "cold" junction, which is placed at the measuring system environment.

Because a thermocouple can only measure a temperature difference, it does not have the ability to measure absolute temperature. To determine the absolute temperature of the measured environment (Thot), a technique known as cold junction compensation (CJC) must be used.

In a CJC technique, the "cold" junction temperature, Tcold, is sensed by using an IC temperature sensor, such as the LM94022. The temperature sensor should be placed within close proximity of the reference junction and should have an isothermal connection to the board to minimize any potential temperature gradients.

Once Tcold is obtained, use a standard thermocouple look-up-table to find its equivalent voltage. Next, measure the differential thermocouple voltage and add the equivalent cold junction voltage. Lastly, convert the resulting voltage to temperature using a standard thermocouple look-up-table.

Product Folder Links: *LMP90100 LMP90099 LMP90098 LMP90097*

Typical Applications (continued)

For example, assume Tcold = 20°C. The equivalent voltage from a type K thermocouple look-up-table is 0.798 mV. Next, add the measured differential thermocouple voltage to the Tcold equivalent voltage. For example, if the thermocouple voltage is 4.096 mV, the total would be 0.798 mV + 4.096 mV = 4.894 mV. Referring to the type K thermocouple table gives a temperature of 119.37°C for 4.894 mV.

10.2.4 Application Curve
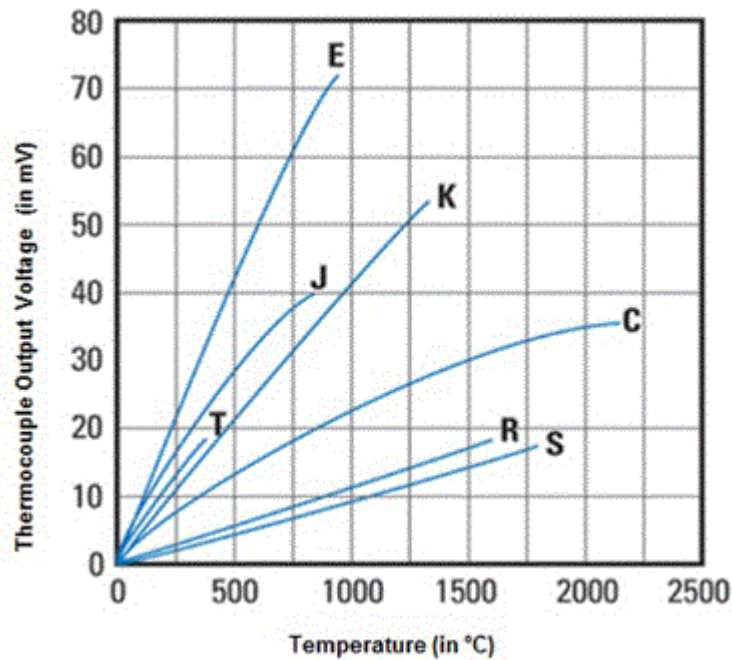
Figure 83. Thermocouple Output as Function of Temperature

11 Power Supply Recommendations

11.1 VA and VIO

Any ADC architecture is sensitive to spikes on the analog voltage, VA, digital input/output voltage, VIO, and ground pins. These spikes may originate from switching power supplies, digital logic, high power devices, and other sources. To diminish these spikes, the LMP90xxx's VA and VIO pins should be clean and well bypassed. A 0.1 µF ceramic bypass capacitor and a 1 µF tantalum capacitor should be used to bypass the LMP90xxx supplies, with the 0.1 µF capacitor placed as close to the LMP90xxx as possible.

Because the LMP90xxx has both external VA and VIO pins, the user has two options on how to connect these pins. The first option is to tie VA and VIO together and power them with the same power supply. This is the most cost effective way of powering the LMP90xxx but is also the least ideal because noise from VIO can couple into VA and negatively affect performance. The second option involves powering VA and VIO with separate power supplies. These supply voltages can have the same amplitude or they can be different.

11.2 VREF

Operation with VREF below VA is also possible with slightly diminished performance. As VREF is reduced, the range of acceptable analog input voltages is also reduced. Reducing the value of VREF also reduces the size of the LSB. When the LSB size goes below the noise floor of the LMP90xxx, the noise will span an increasing number of codes and performance will degrade. For optimal performance, VREF should be the same as VA and sourced with a clean source that is bypassed with a ceramic capacitor value of 0.1 µF and a tantalum capacitor of 10 µF.

LMP90xxx also allows ratiometric connection for noise immunity reasons. A ratiometric connection is when the ADC's VREFP and VREFN are used to excite the input device's (i.e. a bridge sensor) voltage references. This type of connection severely attenuates any VREF ripple seen the ADC output, and is thus strongly recommended.

12 Layout

12.1 Layout Guidelines

1. Follow the guidelines in the *Power Supply Recommendations* section.
2. Keep analog traces away from digital traces.
3. Never run an analog and digital trace parallel to each other.
4. If a digital and analog need to cross each other cross them at a 90° angle.
5. Use a solid ground plane under the LMP90100.

12.2 Layout Example

The example layout in Figure 84 is for the Typical Application, 3-Wire RTD Using 2 Current Sources shown in Figure 78.
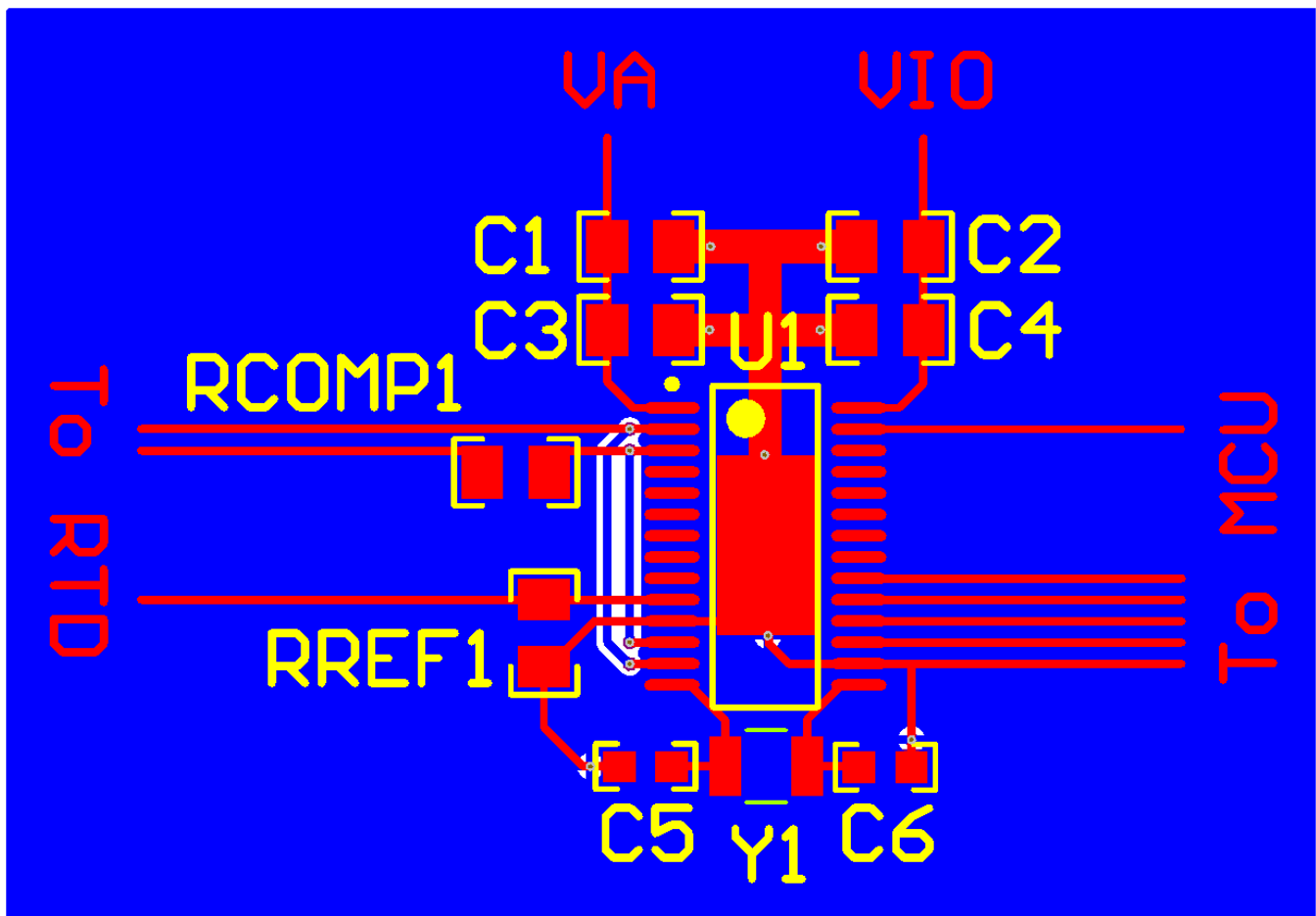

Figure 84. LMP90xxx Sample Layout

13 Device and Documentation Support

13.1 Device Support

13.1.1 Device Nomenclature

13.1.1.1 Specific Definitions

CMRR = 20 LOG(ΔCommon Input / ΔOutput Offset)

COMMON MODE REJECTION RATIO is a measure of how well in-phase signals common to both input pins are rejected. To calculate CMRR, the change in output offset is measured while the common mode input voltage is changed.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) – says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits. LMP90xxx's ENOB is a DC ENOB spec, not the dynamic ENOB that is measured using FFT and SINAD. Its equation is as follows:

$$ENOB = \log_2\left(\frac{2 \times VREF/Gain}{RMS\ Noise}\right)$$

(17)

GAIN ERROR is the deviation from the ideal slope of the transfer function.

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The end point fit method is used. INL for this product is specified over a limited range, per the Electrical Tables.

NEGATIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions to negative full scale and (-VREF + 1LSB).

NEGATIVE GAIN ERROR is the difference between the negative full-scale error and the offset error divided by (VREF / Gain).

NOISE FREE RESOLUTION is a method of specifying the number of bits for a converter with noise.

$$NFR = \log_2\left(\frac{2 \times VREF/Gain}{Peak\text{-}to\text{-}Peak\ Noise}\right)$$

(18)

ODR Output Data Rate.

OFFSET ERROR is the difference between the differential input voltage at which the output code transitions from code 0000h to 0001h and 1 LSB.

POSITIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions to positive full scale and (VREF – 1LSB).

POSITIVE GAIN ERROR is the difference between the positive full-scale error and the offset error divided by (VREF / Gain).

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well a change in the analog supply voltage is rejected. PSRR is calculated from the ratio of the change in offset error for a given change in supply voltage, expressed in dB.

PSRR = 20 LOG (ΔVA / ΔOutput Offset)

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 36. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LMP90100	Click here	Click here	Click here	Click here	Click here
LMP90099	Click here	Click here	Click here	Click here	Click here
LMP90098	Click here	Click here	Click here	Click here	Click here
LMP90097	Click here	Click here	Click here	Click here	Click here

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.6 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMP90097MH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90097 MH	Samples
LMP90097MHE/NOPB	ACTIVE	HTSSOP	PWP	28	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90097 MH	Samples
LMP90097MHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90097 MH	Samples
LMP90098MH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90098 MH	Samples
LMP90098MHE/NOPB	ACTIVE	HTSSOP	PWP	28	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90098 MH	Samples
LMP90098MHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90098 MH	Samples
LMP90099MH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90099 MH	Samples
LMP90099MHE/NOPB	ACTIVE	HTSSOP	PWP	28	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90099 MH	Samples
LMP90099MHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90099 MH	Samples
LMP90100MH/NOPB	ACTIVE	HTSSOP	PWP	28	48	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90100 MH	Samples
LMP90100MHE/NOPB	ACTIVE	HTSSOP	PWP	28	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90100 MH	Samples
LMP90100MHX/NOPB	ACTIVE	HTSSOP	PWP	28	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	LMP90100 MH	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Reel Width (W1)

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMP90097MHE/NOPB	HTSSOP	PWP	28	250	178.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LMP90097MHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LMP90098MHE/NOPB	HTSSOP	PWP	28	250	178.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LMP90098MHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LMP90099MHE/NOPB	HTSSOP	PWP	28	250	178.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LMP90099MHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LMP90100MHE/NOPB	HTSSOP	PWP	28	250	178.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1
LMP90100MHX/NOPB	HTSSOP	PWP	28	2500	330.0	16.4	6.8	10.2	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMP90097MHE/NOPB	HTSSOP	PWP	28	250	210.0	185.0	35.0
LMP90097MHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	38.0
LMP90098MHE/NOPB	HTSSOP	PWP	28	250	210.0	185.0	35.0
LMP90098MHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	38.0
LMP90099MHE/NOPB	HTSSOP	PWP	28	250	210.0	185.0	35.0
LMP90099MHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	38.0
LMP90100MHE/NOPB	HTSSOP	PWP	28	250	210.0	185.0	35.0
LMP90100MHX/NOPB	HTSSOP	PWP	28	2500	367.0	367.0	38.0

6.6
6.2 TYP

A

PIN 1 ID
AREA

1   28

26X 0.65

2X
8.45

9.8
9.6
NOTE 3

14   15

28X 0.30
0.19

⊕ 0.1 Ⓜ C A Ⓢ B Ⓢ

B

4.5
4.3
NOTE 4

C

SEATING PLANE

⌓ 0.1 C

1.1 MAX

SEE DETAIL A

0.20
0.09 TYP

3.15
2.75

5.65
5.25

THERMAL
PAD

0.25

GAGE PLANE

0° - 8°

0.7
0.5

(1)

0.10
0.02

DETAIL A
TYPICAL
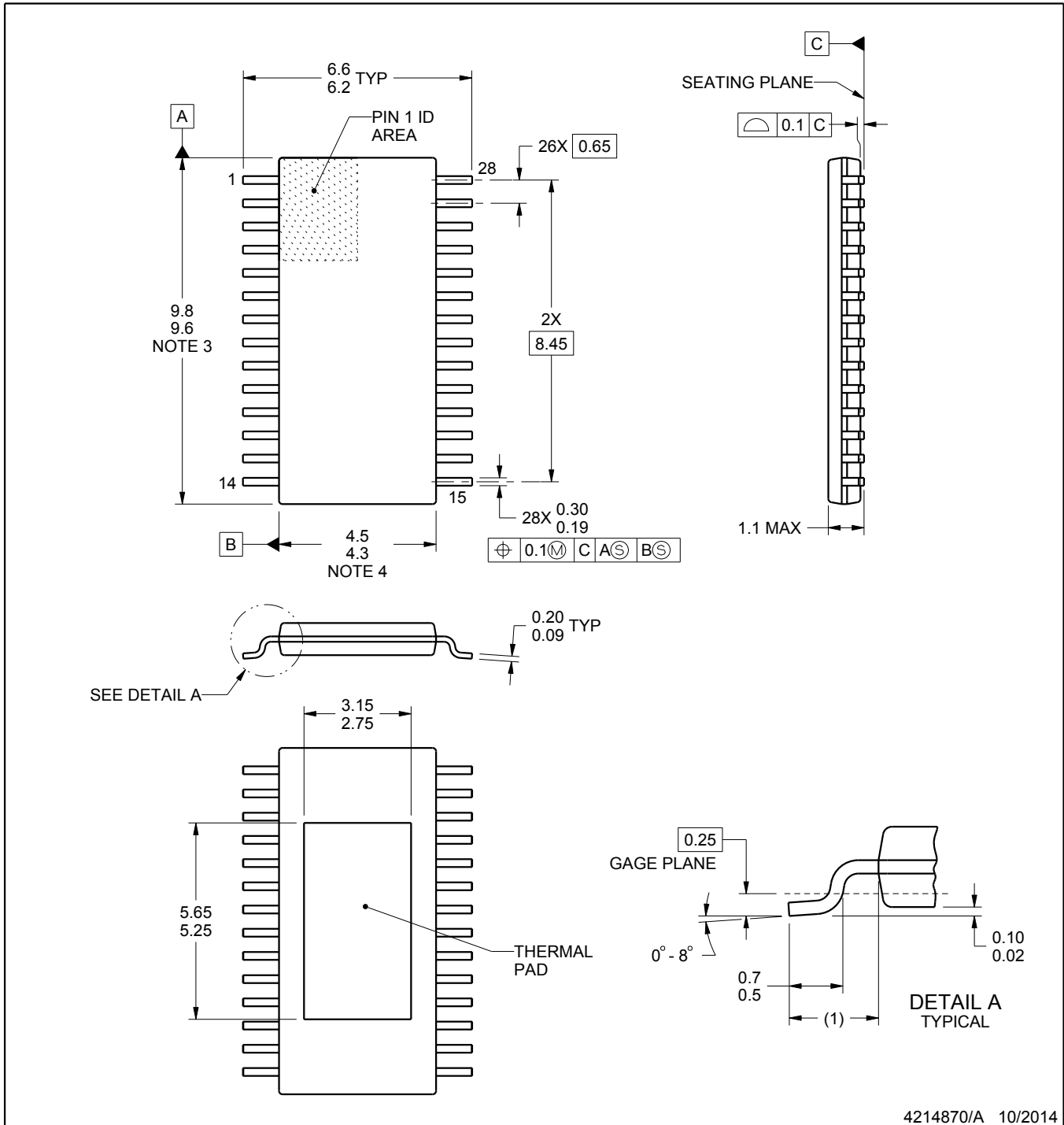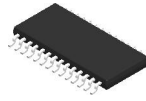
4214870/A   10/2014

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MO-153, variation AET.

LAND PATTERN EXAMPLE
SCALE:6X

(3.4) NOTE 9

(3) SOLDER MASK OPENING

SOLDER MASK DEFINED PAD

28X (1.5)

28X (0.45)

1

26X (0.65)

SYMM ℄

(1.3) TYP

14

SEE DETAILS

(0.65) TYP

(5.8)

28

(5.5) SOLDER MASK OPENING

(9.7)

(1.3)

SYMM ℄

(Ø 0.2) TYP VIA

METAL COVERED BY SOLDER MASK

15

IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE

28X (0.45)

28X (1.3)

(0.9) TYP

(6.1)

HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

SOLDER MASK DETAILS

SOLDER MASK OPENING — METAL

0.05 MAX ALL AROUND

NON SOLDER MASK DEFINED

METAL UNDER SOLDER MASK — SOLDER MASK OPENING

0.05 MIN ALL AROUND

SOLDER MASK DEFINED
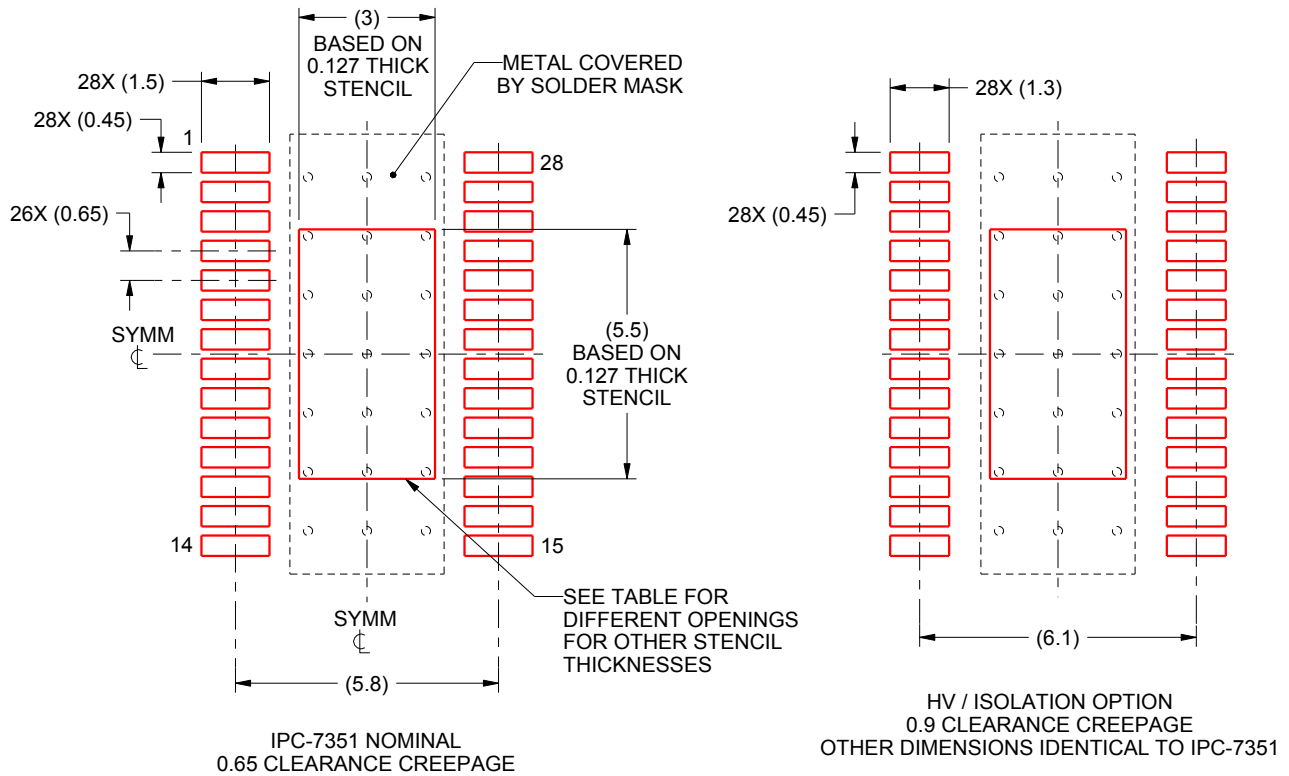
4214870/A   10/2014

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

PWP0028A

PowerPAD™ - 1.1 mm max height

(3)
BASED ON
0.127 THICK
STENCIL

METAL COVERED
BY SOLDER MASK

28X (1.5)

28X (0.45)

1

26X (0.65)

28

SYMM

(5.5)
BASED ON
0.127 THICK
STENCIL

14

15

SEE TABLE FOR
DIFFERENT OPENINGS
FOR OTHER STENCIL
THICKNESSES

SYMM

(5.8)

IPC-7351 NOMINAL
0.65 CLEARANCE CREEPAGE

28X (1.3)

28X (0.45)

(6.1)

HV / ISOLATION OPTION
0.9 CLEARANCE CREEPAGE
OTHER DIMENSIONS IDENTICAL TO IPC-7351

SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE AREA
SCALE:6X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.55 X 6.37
0.127	3.0 X 5.5 (SHOWN)
0.152	2.88 X 5.16
0.178	2.66 X 4.77

4214870/A   10/2014

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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