SPECIFICATIONS

CUSTOMER : _____

MODEL NO. : GFTO024KD240320

VERSION : C

DATE : 2023.03.03

CERTIFICATION : ROHS

Customer Sign	Approved By	Prepared By	Prepared By
	GIFAR 2023.03.03 Sidney	GIFAR 2023.03.03 Roger	GIFAR 2023.03.03 Hazel

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Revision Record

Data(y/m/d)	Ver.	Description	page
2021.01.05	A	New	
2021.01.21	B	New Sample(客戶承認)	
2023.03.03	C	更新公司抬頭認證圖示	

CONTENTS

1.SPECIFICATIONS

1.1 Features

Main LCD Panel

Item	Standard Value
Display Type	240 * (R 、G、B) * 320 Dots
LCD Type	a-Si TFT , Normally white TN mode , Transmissive
Screen size(Inch)	2.4 (Diagonal)
Gray Scale Inversion Direction	12 O'clock
Color configuration	R.G.B. vertical stripe
Interface	8080MCU, SPI, RGB interface
Other(controller / driver IC)	ILI9341

1.2 Mechanical Specifications

Item	Standard Value	Unit
Outline Dimension	42.72 (W) * 60.26 (L) * 2.5(H)	mm
Active Area	36.72 (W) * 48.96 (L)	mm

Note : For detailed information please refer to LCM drawing

1.3 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit
Logic Supply Voltage	IOVCC	-	-0.3	+4.6	V
Analog Supply Voltage	VCC	-	-0.3	+4.6	V
Input Voltage	VIN	-	-0.3	IOVCC+0.3	V
Operating Temperature	T_{OP}	Note 1	-20	+70	°C
Storage Temperature	T_{ST}	Note 2	-30	+80	°C
Storage Humidity	H_D	Ta ≦ 60 °C	10	90	%RH

The absolute maximum rating values of this product are not allowed to be exceeded at any times. Should a module be used with any of the absolute maximum ratings exceeded, the characteristics of the module may not be recovered, or in an extreme case, the module may be permanently destroyed.
Note 1：Ts is the temperature of panel's surface.
Note 2：Ta is the ambient temperature of samples.

1.4 DC Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage1	VCC / IOVCC		-	3.0	-	V
Input High Voltage	VIH		0.7* IOVCC		IOVCC	V
Input Low Voltage	VIL		GND		0.3* IOVCC	V
Output High Voltage	VOH	IOH=-1.0 mA	0.8* IOVCC		IOVCC	V
Output Low Voltage	VOL	IOL=+1.0mA	GND		0.2* IOVCC	V
Supply Current	Icc	VCC=IOVCC =3.3V		8	14	mA

Note1 : ICC contains the current of the IOVCC & VCC

1.5 Optical Characteristics

TFT LCD Panel VDD = 3.3V, Ta=25°C

Item		Symbol	Condition	Min.	Typ.	Max.	unit	
Response time		Tr + Tf	-	-	30	45	ms	Note2
Viewing angle	Top	θY+	CR ≥ 10	-	60	-	Deg.	Note4
	Bottom	θY-		-	60	-		
	Left	θX-		-	60	-		
	Right	θX+		-	60	-		
Contrast ratio		CR	-	500	600	-	-	Note3
Color of CIE Coordinate (With B/L)	White	X	IF=40mA	0.23	0.28	0.33	-	Note1
		Y		0.25	0.30	0.35		
	Red	X		0.55	0.60	0.65		
		Y		0.29	0.34	0.39		
	Green	X		0.30	0.35	0.40		
		Y		0.55	0.60	0.65		
	Blue	X		0.10	0.15	0.20		
		Y		0.01	0.03	0.11		
Average Brightness Pattern = white display (With B/L)		IV	IF=40mA	-	320	-	cd/m^2	Note1
Uniformity (With B/L)		△B	-	80	-	-	%	Note1

Note1:

1：△B=B(min) / B(max) × 100%

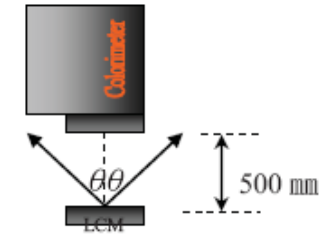
2：Measurement Condition for Optical Characteristics:

a：Environment: 25℃±5℃ / 60±20%R.H，no wind，dark room below 10 Lux at typical lamp current and typical operating frequency.

b：Measurement Distance: 500 ± 50 ㎜ ，(θ= 0°)

c：Equipment: TOPCON BM-7 fast，(field 1°)，after 10 minutes operation.

d：The uncertainty of the C.I.E coordinate measurement ±0.01，Average Brightness ± 4%

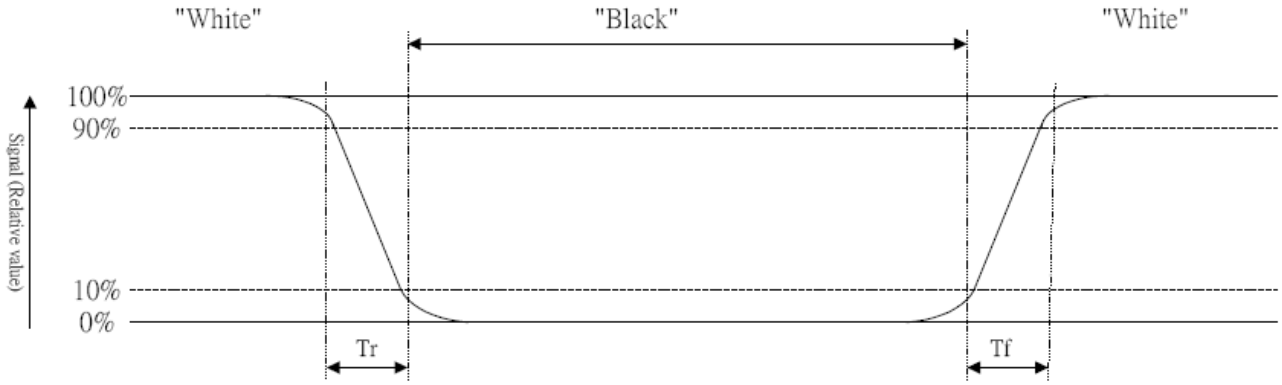


Colorimeter=BM-7 fast

Note2: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of Amplitudes.

Refer to figure as below:



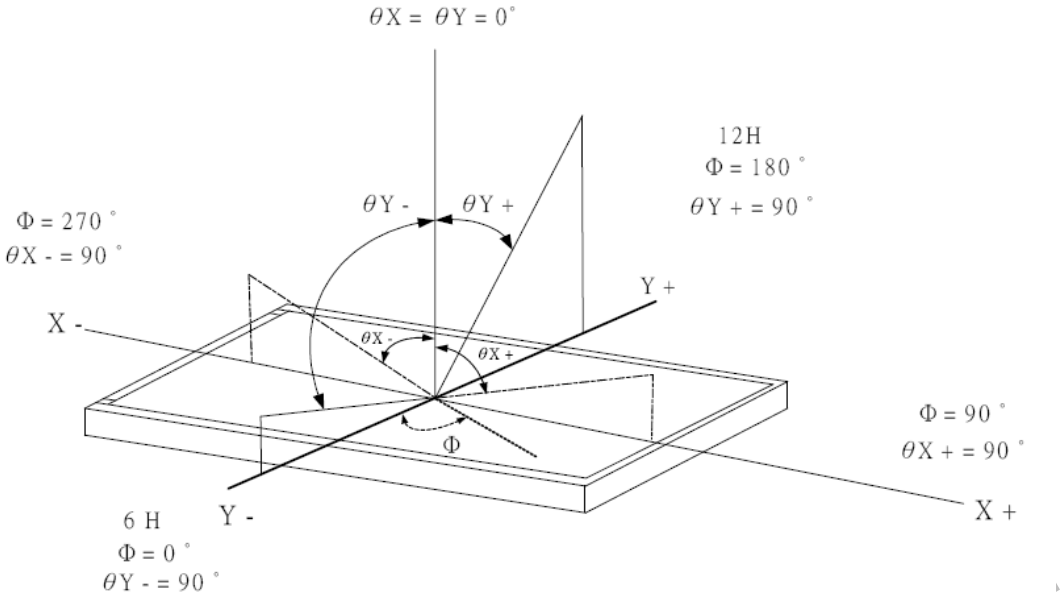
Note3: Definition of contrast ratio:

Contrast ratio is calculated with the following formula

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note4: Definition of viewing angle:

Refer to figure as below:



1.6 Backlight Characteristics

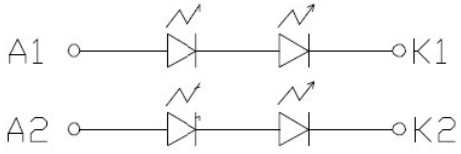
Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward Current	IF	Ta =25℃	-	60	mA
Reverse Voltage	VR	Ta =25℃	-	7	V
Power dissipation	Pd	Ta =25℃	-	420	mW

Electrical / Optical Characteristics

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage	VF	IF=40mA	5.6	6.7	7.0	V
Color of CIE Coordinate (without LCD & T/P)	X		0.25	0.28	0.31	-
	Y		0.25	0.28	0.31	
Color	White					

B/L Internal Circuit Diagram



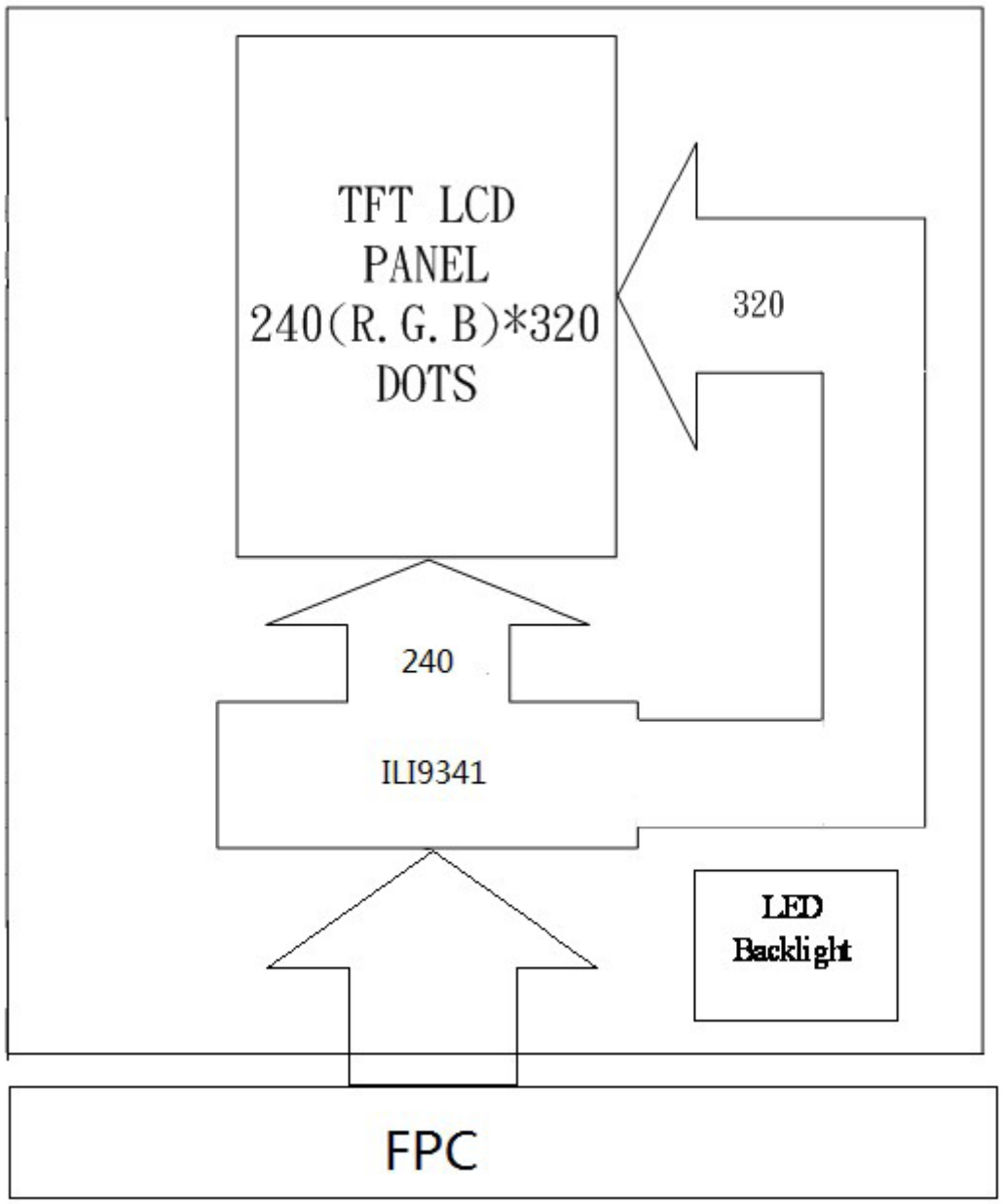
IF=20mA*2 ,Vf=6.6V

Other Description

Item	Conditions	Description
Life Time	Ta =25℃ IF= 40mA	20000 hrs

2. MODULE STRUCTURE

2.1 Block Diagram



2.2 Interface Pin Description

Pin No.	Symbol	Function
1	VCI	System power supply.
2	IOVCC	I/O Power supply.
3	IM0	Note 1
4	IM1	
5	IM2	
6	IM3	
7	RESET	Reset signal input terminal, active at "L".
8	VSYNC	Vertical sync signal in RGB I/F.
9	HSYNC	Horizontal sync signal in RGB I/F.
10	DOTCLK	Pixel clock signal in RGB I/F.
11	ENABLE	Data Enable signal in RGB I/F mode
12	DB17	16-bit/pixel: D[17:13]=R[4:0], D[11:6]=G[5:0] and D[5:1]=B[4:0]; Connect D0 and D12 pins to GND.
13	DB16	
14	DB15	
15	DB14	
16	DB13	
17	DB12	
18	DB11	
19	DB10	
20	DB9	
21	DB8	
22	DB7	
23	DB6	
24	DB5	
25	DB4	
26	DB3	
27	DB2	
28	DB1	16-bit/pixel: D[17:13]=R[4:0], D[11:6]=G[5:0] and D[5:1]=B[4:0]; Connect D0 and D12 pins to GND.
29	DB0	
30	SDO	Serial output signal. The data is outputted on the falling edge of the SCL signal.
31	SDI	Serial data input signal in SPI I/F. If not used, open this pin.
32	RD	Read signal in 80-system.
33	WR	Write signal in 80-system.

34	RS/SCL	This pin is used to select "Data or Command" in the parallel interface When DCX = '1', data is selected. When DCX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface.
35	CS(CSX)	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only.
36	GND(VSS)	Power ground.
37	LEDA	LED backlight anode.
38	LEDK1	LED backlight cathode.
39	LEDK2	LED backlight cathode.
40	NC	No Function
41	NC	
42	NC	
43	NC	
44	NC	
45	NC	

Note1:

IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pin in use	
					Register/Content	GRAM
0	0	0	0	80 MCU 8-bit bus interface Ⅰ	D[7:0]	D[7:0]
0	0	0	1	80 MCU 16-bit bus interface Ⅰ	D[7:0]	D[15:0]
0	0	1	0	80 MCU 9-bit bus interface Ⅰ	D[7:0]	D[8:0]
0	0	1	1	80 MCU 18-bit bus interface Ⅰ	D[7:0]	D[17:0]
0	1	0	1	3-wire 9-bit data serial interface Ⅰ	SDA: In/OUT	
0	1	1	0	4-wire 8-bit data serial interface Ⅰ	SDA: In/OUT	
1	0	0	0	80 MCU 16-bit bus interface Ⅱ	D[8:1]	D[17:10], D[8:1]
1	0	0	1	80 MCU 8-bit bus interface Ⅱ	D[17:10]	D[17:10]
1	0	1	0	80 MCU 18-bit bus interface Ⅱ	D[8:1]	D[17:0]
1	0	1	1	80 MCU 9-bit bus interface Ⅱ	D[17:10]	D[17:9]
1	1	0	1	3-wire 9-bit data serial interface Ⅱ	SDI: In SDO: Out	
1	1	1	0	4-wire 8-bit data serial interface Ⅱ	SDI: In SDO: Out	

2.2.1 Application Notes:

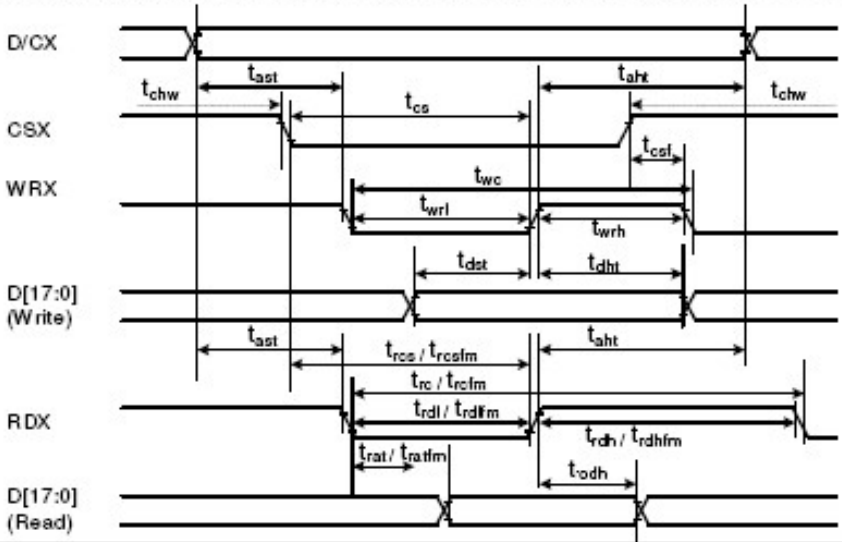
```
void Initial_Main(void)
{
    WriteCOM_Main(0xCB)
    WriteDAT_Main(0x39)
    WriteDAT_Main(0x2C)
    WriteDAT_Main(0x00)
    WriteDAT_Main(0x34)
    WriteDAT_Main(0x02)
    WriteCOM_Main(0xCF)
    WriteDAT_Main(0x00)
    WriteDAT_Main(0xD9)
    WriteDAT_Main(0x30)
    WriteCOM_Main(0xE8)
    WriteDAT_Main(0x85)
    WriteDAT_Main(0x00)
    WriteDAT_Main(0x78)
    WriteCOM_Main(0xEA)
    WriteDAT_Main(0x00)
    WriteDAT_Main(0x00)
    WriteCOM_Main(0xED)
    WriteDAT_Main(0x64)
    WriteDAT_Main(0x03)
    WriteDAT_Main(0x12)
    WriteDAT_Main(0x81)
    WriteCOM_Main(0xF6)
    WriteDAT_Main(0x01)
    WriteDAT_Main(0x00)
    WriteDAT_Main(0x06)
    WriteCOM_Main(0xB0)
    WriteDAT_Main(0x40)
    WriteCOM_Main(0x3A)
    WriteDAT_Main(0x55)
    WriteCOM_Main(0xF7)
    WriteDAT_Main(0x20)
    WriteCOM_Main(0xC0)
    WriteDAT_Main(0x21)
    WriteCOM_Main(0xC1)
    WriteDAT_Main(0x12)
```

```
WriteCOM_Main(0xC5)
WriteDAT_Main(0x32)
WriteDAT_Main(0x3C)
WriteCOM_Main(0xC7)
WriteDAT_Main(0Xa3)
WriteCOM_Main(0x36)
WriteDAT_Main(0x00)
WriteCOM_Main(0xB0)
WriteDAT_Main(0x40)
WriteCOM_Main(0xB1)
WriteDAT_Main(0x00)
WriteDAT_Main(0x1B)
WriteCOM_Main(0xB6)
WriteDAT_Main(0x0a)
WriteDAT_Main(0xa2)
WriteDAT_Main(0x27)
WriteDAT_Main(0x00)
WriteCOM_Main(0xF2)
WriteDAT_Main(0x00)
WriteCOM_Main(0x26)
WriteDAT_Main(0x01)
WriteCOM_Main(0xe0)          //set gamma
WriteDAT_Main(0x0F)
WriteDAT_Main(0x1C)
WriteDAT_Main(0x19)
WriteDAT_Main(0x08)
WriteDAT_Main(0x0B)
WriteDAT_Main(0x04)
WriteDAT_Main(0x4B)
WriteDAT_Main(0x64)
WriteDAT_Main(0x3E)
WriteDAT_Main(0x09)
WriteDAT_Main(0x15)
WriteDAT_Main(0x08)
WriteDAT_Main(0x16)
WriteDAT_Main(0x0D)
WriteDAT_Main(0x04)
WriteCOM_Main(0xe1)          //set gamma
WriteDAT_Main(0x00)
```

```
    WriteDAT_Main(0x1A)
    WriteDAT_Main(0x1E)
    WriteDAT_Main(0x03)
    WriteDAT_Main(0x0F)
    WriteDAT_Main(0x03)
    WriteDAT_Main(0x35)
    WriteDAT_Main(0x23)
    WriteDAT_Main(0x45)
    WriteDAT_Main(0x04)
    WriteDAT_Main(0x0C)
    WriteDAT_Main(0x0B)
    WriteDAT_Main(0x2B)
    WriteDAT_Main(0x2E)
    WriteDAT_Main(0x05)
    WriteCOM_Main(0x11)              //exit sleep
    Delay(120)
    WriteCOM_Main(0x29)              //Display on
}
```

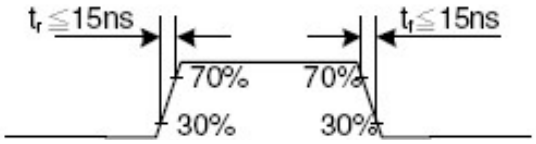
2.3 Timing Characteristics

Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- I system)

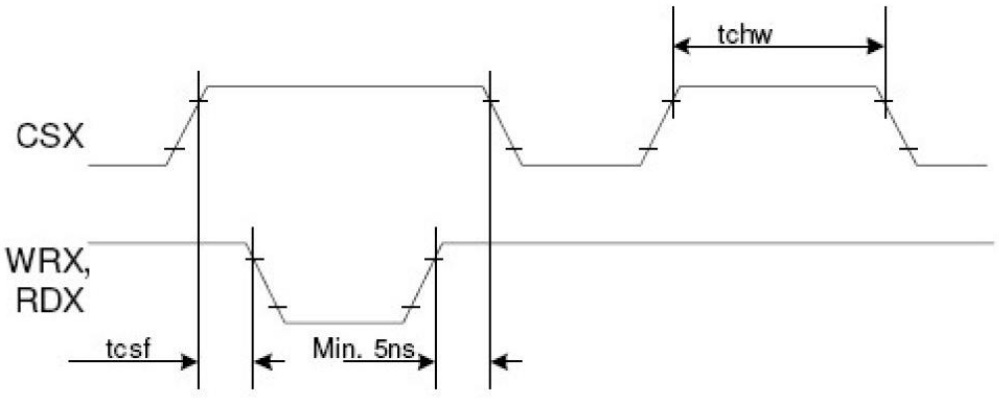


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[15:0], D[8:0], D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI= 1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

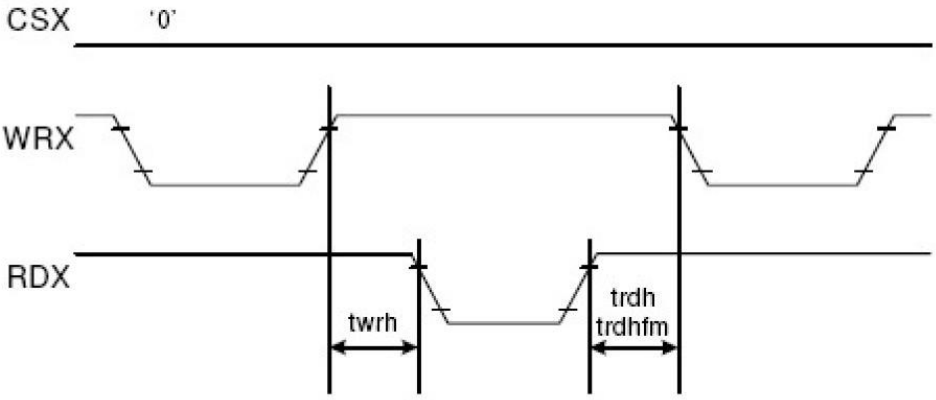


CSX timings :



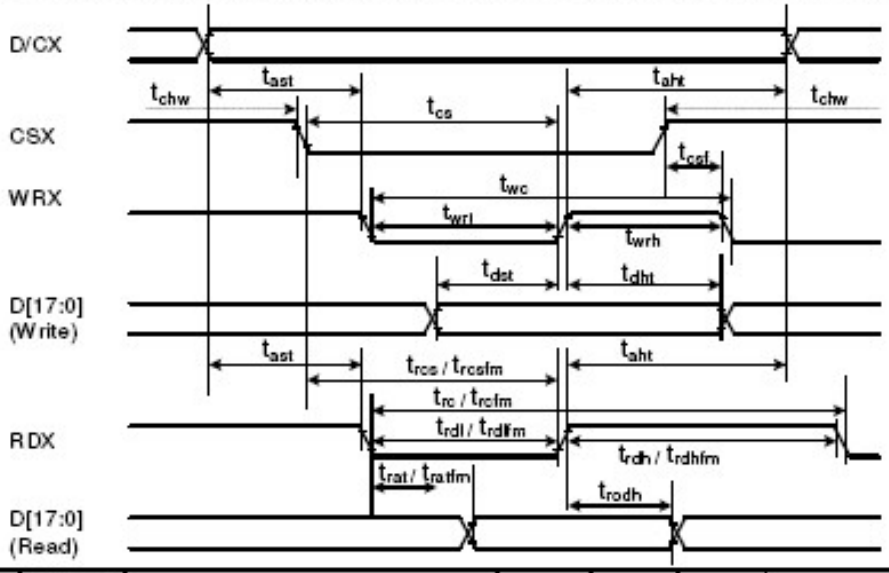
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



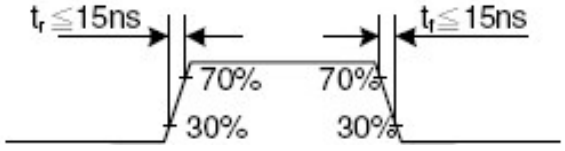
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Display Parallel 18/16/9/8-bit Interface Timing Characteristics(8080-Ⅱ system)

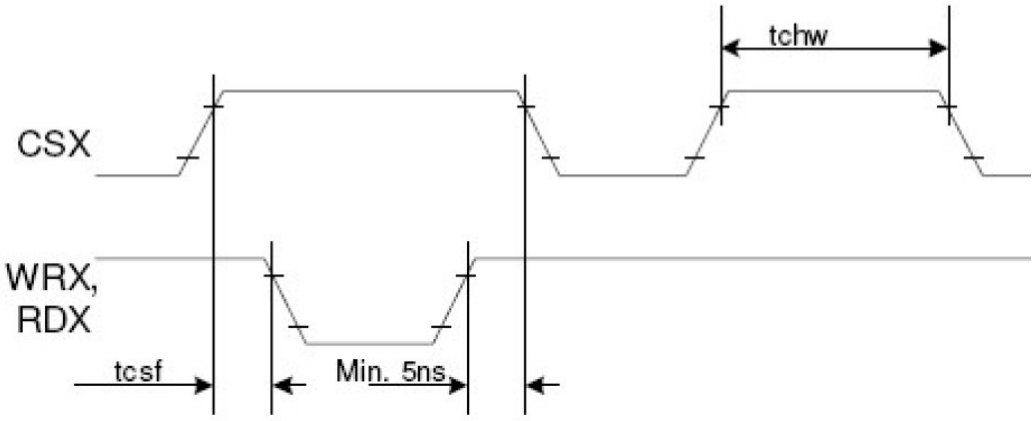


Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time (Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time (Write)	15	-	ns	
	trcs	Chip Select setup time (Read ID)	45	-	ns	
	trcsfm	Chip Select setup time (Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write cycle	66	-	ns	
	twrh	Write Control pulse H duration	15	-	ns	
	twrl	Write Control pulse L duration	15	-	ns	
RDX (FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration (FM)	90	-	ns	
	trdlfm	Read Control L duration (FM)	355	-	ns	
RDX (ID)	trc	Read cycle (ID)	160	-	ns	
	trdh	Read Control pulse H duration	90	-	ns	
	trdl	Read Control pulse L duration	45	-	ns	
D[17:0], D[17:10]&D[8:1], D[17:10], D[17:9]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V.

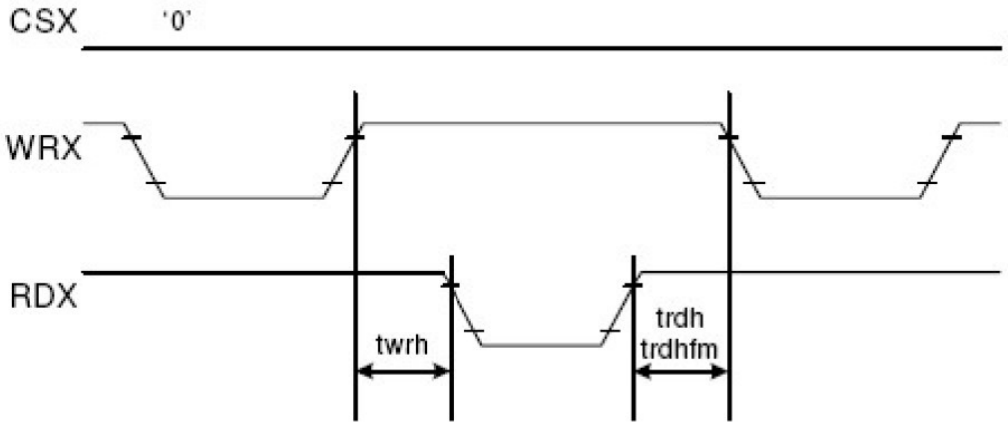


CSX timings :



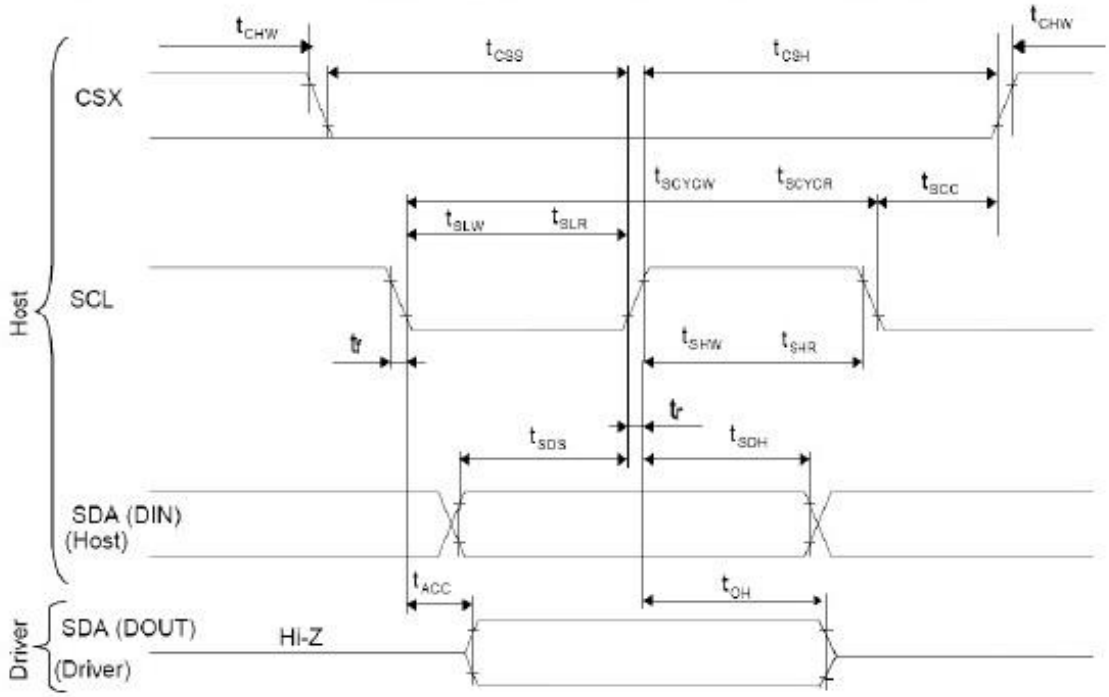
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



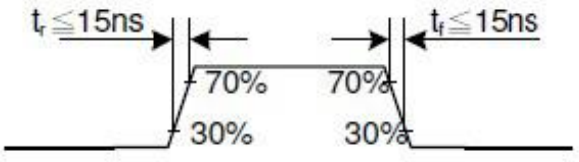
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Display Serial Interface Timing Characteristics (3-line SPI system)

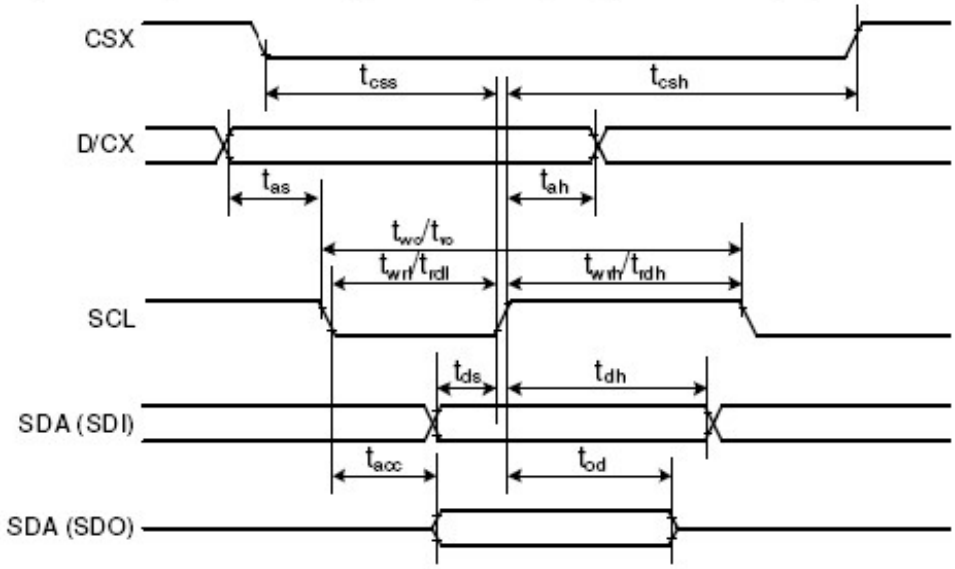


Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	100	-	ns	
	tshw	SCL "H" Pulse Width (Write)	40	-	ns	
	tslw	SCL "L" Pulse Width (Write)	40	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA / SDI (Input)	tsds	Data setup time (Write)	30	-	ns	
	tsdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	20	-	ns	
	tchw	CSX "H" Pulse Width	40	-	ns	
	tcss	CSX-SCL Time	60	-	ns	
	tcsh		65	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

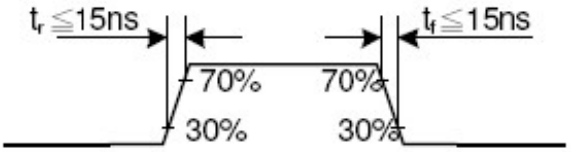


Display Serial Interface Timing Characteristics (4-line SPI system)

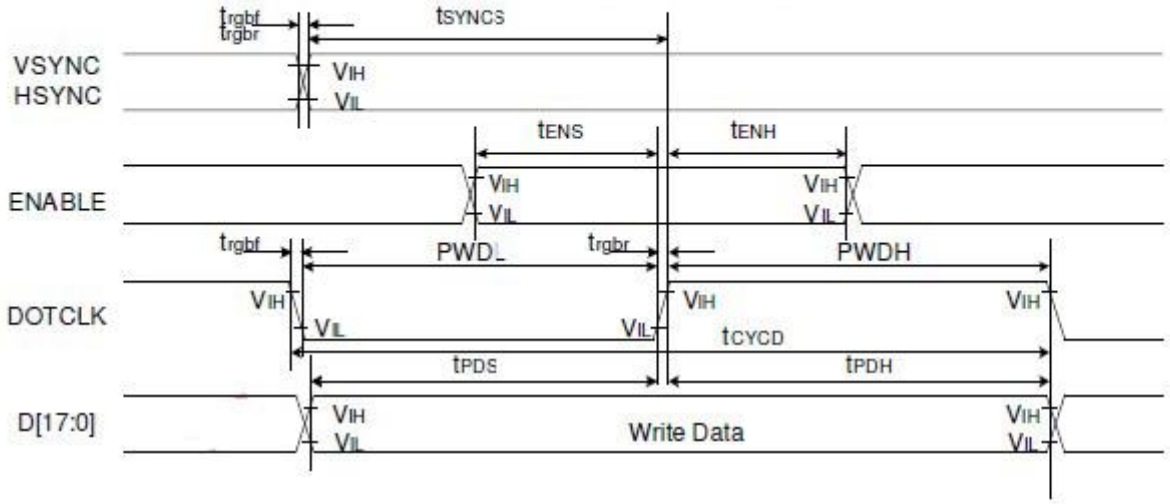


Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	40	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial clock cycle (Write)	100	-	ns	
	twrh	SCL "H" pulse width (Write)	40	-	ns	
	twrl	SCL "L" pulse width (Write)	40	-	ns	
	trc	Serial clock cycle (Read)	150	-	ns	
	trdh	SCL "H" pulse width (Read)	60	-	ns	
	trdl	SCL "L" pulse width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-		
	tah	D/CX hold time (Write / Read)	10	-		
SDA / SDI (Input)	tds	Data setup time (Write)	30	-	ns	
	tdh	Data hold time (Write)	30	-	ns	
SDA / SDO (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF
	tod	Output disable time (Read)	10	50	ns	For minimum CL=8pF

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

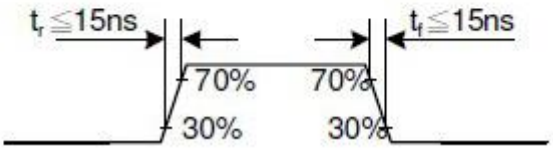


Parallel 18/16/6-bit RGB Interface Timing Characteristics

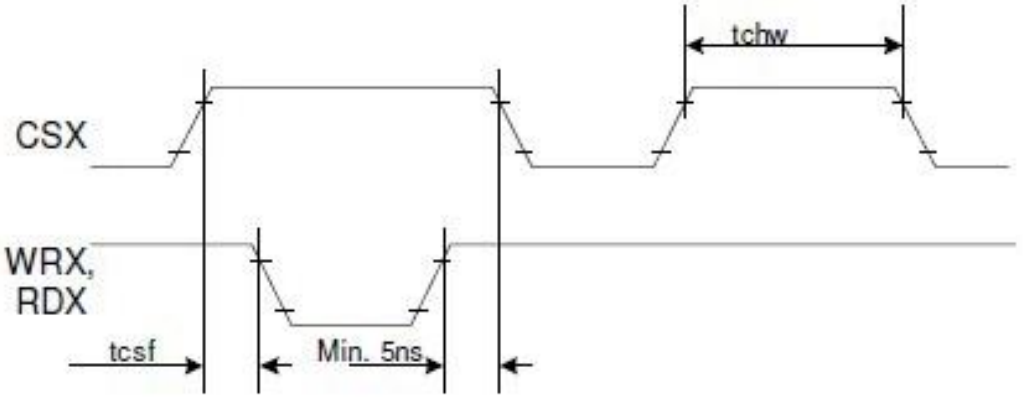


Signal	Symbol	Parameter	min	max	Unit	Description
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	18/16-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level period	15	-	ns	
	PWDL	DOTCLK low-level period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	
VSYNC / HSYNC	t_{SYNCS}	VSYNC/HSYNC setup time	15	-	ns	6-bit bus RGB interface mode
	t_{SYNCH}	VSYNC/HSYNC hold time	15	-	ns	
DE	t_{ENS}	DE setup time	15	-	ns	
	t_{ENH}	DE hold time	15	-	ns	
D[17:0]	t_{PDS}	Data setup time	15	-	ns	
	t_{PDH}	Data hold time	15	-	ns	
DOTCLK	PWDH	DOTCLK high-level pulse period	15	-	ns	
	PWDL	DOTCLK low-level pulse period	15	-	ns	
	t_{CYCD}	DOTCLK cycle time	100	-	ns	
	t_{rgbr} , t_{rgbf}	DOTCLK,HSYNC,VSYNC rise/fall time	-	15	ns	

Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V

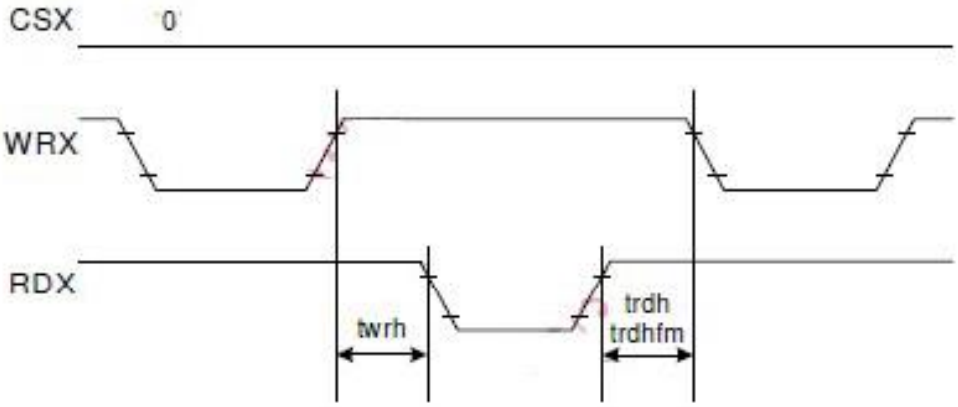


CSX timings :



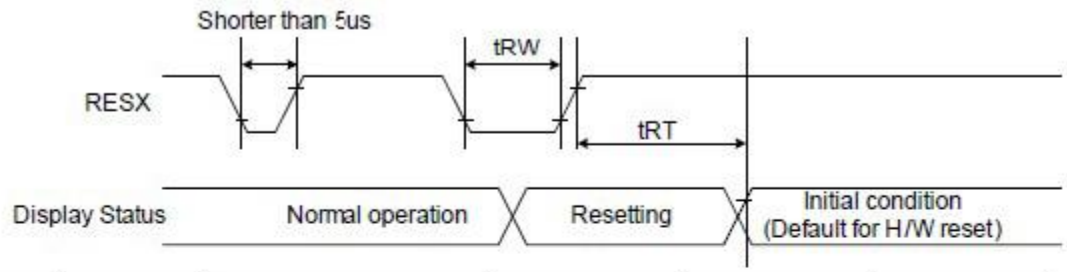
Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Reset Timing



Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5)	mS
				120 (note 1,6,7)	mS

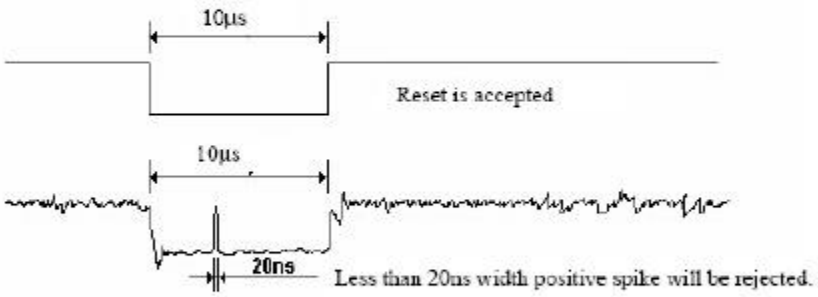
Note 1: The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NV memory to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

Note 2: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below: -

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

Note 3: During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) And then return to Default condition for Hardware Reset.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:



Note 5: When Reset applied during Sleep In Mode.

Note 6: When Reset applied during Sleep Out Mode.

Note 7: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

3. Inspection Specification

◆Scope ：The document shall be applied to TFT-LCD Module for less than 3.5″ (Ver.B01).

◆Inspection Standard：MIL-STD-105E Table Normal Inspection Single Sampling Level Ⅱ.

◆Equipment：Gauge、MIL-STD、Tester、Sample

◆Defect Level：Major Defect AQL： 0.4 ； Minor Defect AQL： 1.5

◆OUT Going Defect Level: Sampling.

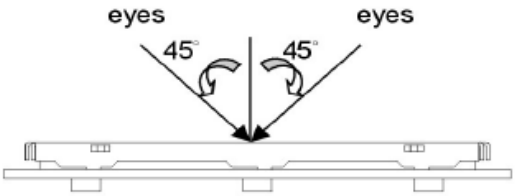
◆Standard of the product appearance test：

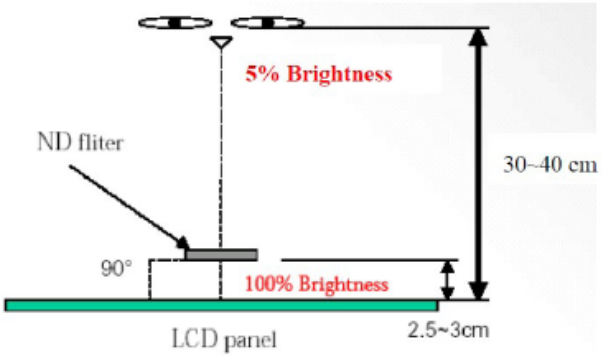
a. Manner of appearance test：

(1). The test best be under 20W×2 fluorescent light (about 300lux ～500lux)

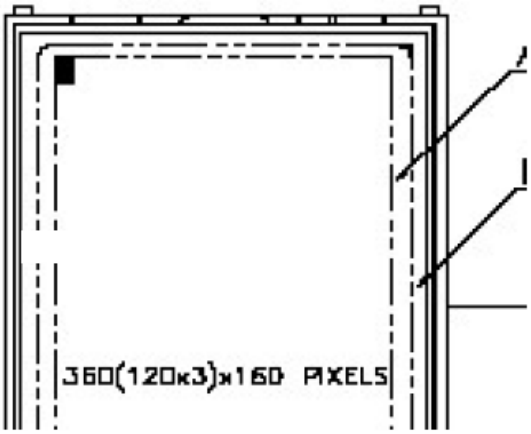
，and distance of view must be at 30~40 cm.

(2). The test direction is base on about around 45° of vertical line.





(3). Definition of area.



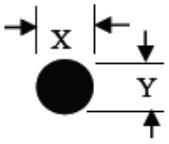
A area : viewing area

B area : Outside of viewing area

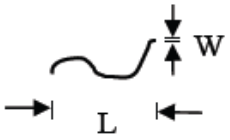
(4). Standard of inspection： (Unit：mm)

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

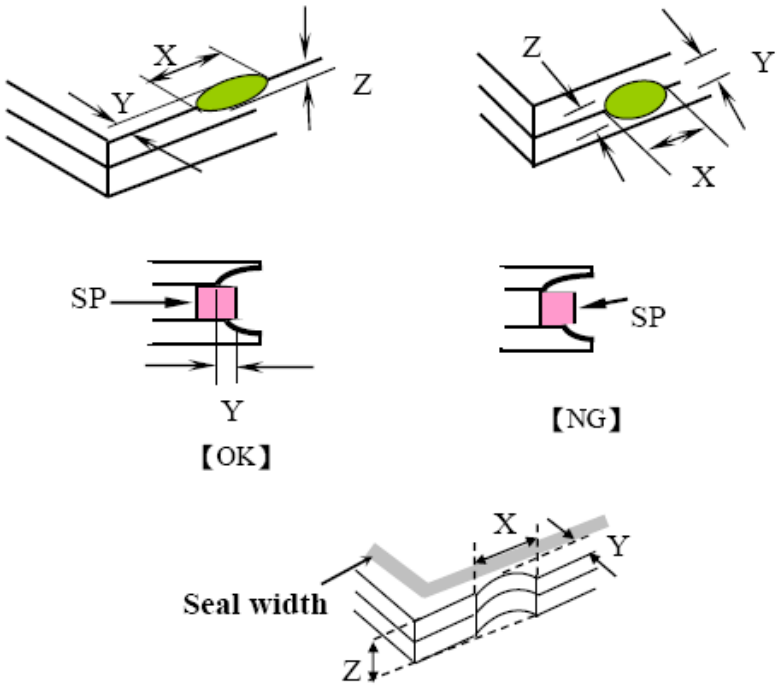
<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td>06</td><td>Black or white dot、scratch、contamination

Round type
 

Φ＝(x＋y) / 2

Line type
 
</td><td>6.1 Round type (Non-display or display) :
<table><tr><th rowspan="2">Dimension
(diameter : Φ)</th><th colspan="2">Acceptance (Q'ty)</th></tr><tr><th>A area</th><th>B area</th></tr><tr><td>Φ ≦ 0.15</td><td>Ignore</td><td rowspan="5">Ignore</td></tr><tr><td>0.15 ＜ Φ ≦ 0.20</td><td>2</td></tr><tr><td>0.20 ＜ Φ ≦ 0.30</td><td>2</td></tr><tr><td>Φ ＞ 0.30</td><td>0</td></tr><tr><td>Total</td><td>3</td></tr></table>6.2 Line type(Non-display or display) :
<table><tr><th colspan="2">Dimension</th><th colspan="2">Acceptance (Q'ty)</th></tr><tr><th>Length (L)</th><th>Width (W)</th><th>A area</th><th>B area</th></tr><tr><td>---</td><td>W ≦ 0.03</td><td>Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>L ≦5.0</td><td>0.03 ＜W ≦ 0.05</td><td>3</td></tr><tr><td>---</td><td>W ＞0.05</td><td>As round type</td></tr><tr><td colspan="2">Total</td><td>3</td></tr></table></td><td>Minor</td></tr>
<tr><td>07</td><td>Polarizer Bubble</td><td><table><tr><th rowspan="2">Dimension
(diameter : Φ)</th><th colspan="2">Acceptance (Q'ty)</th></tr><tr><th>A area</th><th>B area</th></tr><tr><td>Φ ≦ 0.20</td><td>Ignore</td><td rowspan="4">Ignore</td></tr><tr><td>0.20 ＜ Φ ≦ 0.50</td><td>3</td></tr><tr><td>Φ ＞ 0.50</td><td>0</td></tr><tr><td>Total</td><td>3</td></tr></table></td><td>Minor</td></tr>
</table>

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

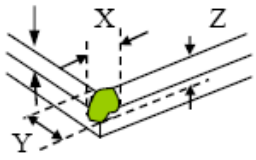
NO	Item	Criterion	Level
08	The crack of glass	Symbols : X : The length of crack　Y : The width of crack. Z : The thickness of crack　W : terminal length t : The thickness of glass　a : LCD side length 8.1 General glass chip : 8.1.1 Chip on panel surface and crack between panels: 	Minor

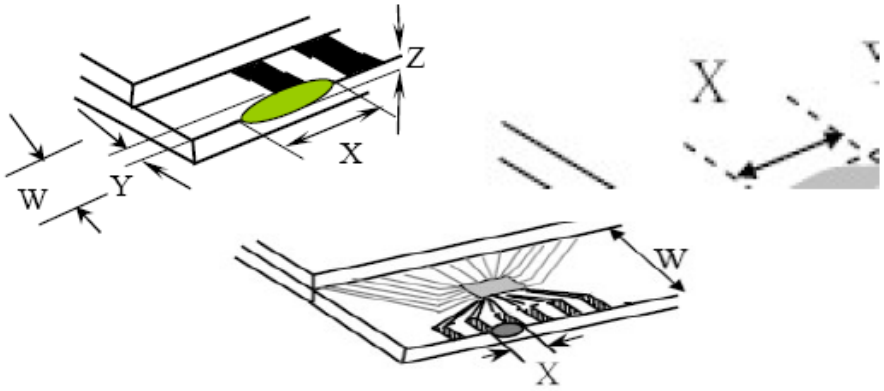
X	Y	Z
≦ a	Crack can't enter viewing area	≦1/2 t
≦ a	Crack can't exceed the half of SP width.	1/2 t < Z ≦2 t

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td rowspan="2">08</td><td rowspan="2">The crack of glass</td><td>
Symbols :

X : The length of crack　　Y : The width of crack.
Z : The thickness of crack　　W : terminal length
t : The thickness of glass　　a : LCD side length

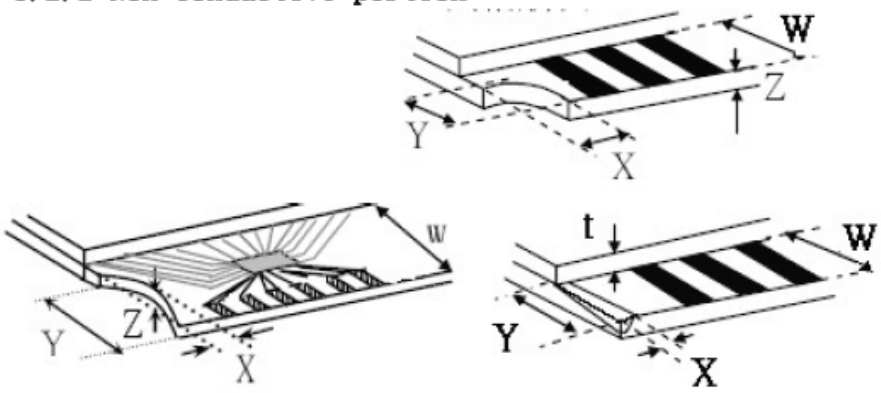
8.1.2 Corner crack :


<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≦1/5 a</td><td>Crack can't enter viewing area</td><td>Z ≦ 1/2 t</td></tr>
<tr><td>≦1/5 a</td><td>Crack can't exceed the half of SP width.</td><td>1/2 t < Z ≦ 2 t</td></tr>
</table>
</td><td rowspan="2">Minor</td></tr>
<tr><td>
8.2 Protrusion over terminal :
8.2.1 Chip on electrode pad :


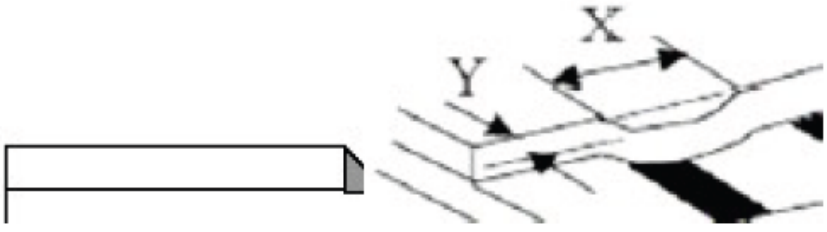
<table>
<tr><th></th><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>Front</td><td>≦ a</td><td>≦ 1/2 W</td><td>≦ t</td></tr>
<tr><td>Back</td><td>≦ a</td><td>≦ W</td><td>≦ 1/2 t</td></tr>
</table>
</td></tr>
</table>

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

<table>
<tr><th>NO</th><th>Item</th><th>Criterion</th><th>Level</th></tr>
<tr><td rowspan="2">08</td><td rowspan="2">The crack of glass</td><td>Symbols :

X : The length of crack Y : The width of crack.
Z : The thickness of crack W : terminal length
t : The thickness of glass a : LCD side length</td><td rowspan="2">Minor</td></tr>
<tr><td>8.2.2 Non-conductive portion :
 

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≦ 1/3 a</td><td>≦W</td><td>≦t</td></tr>
</table>
⊙ If the chipped area touches the ITO terminal, over 2/3 of
1. the ITO must remain and be inspected
according to electrode terminal specifications.

8.2.3 Glass remain :
 

<table>
<tr><th>X</th><th>Y</th><th>Z</th></tr>
<tr><td>≦ a</td><td>≦ 1/3 W</td><td>≦t</td></tr>
</table></td></tr>
</table>

◆Specification For TFT-LCD Module Less Than 3.5″ : (Ver.B01)

NO	Item	Criterion	Level
09	Backlight elements	9.1 Backlight can't work normally.	Major
		9.2 Backlight doesn't light or color is wrong.	Major
		9.3 Illumination source flickers when lit.	Major
10	General appearance	10.1 Pin type、quantity、dimension must match type in structure diagram.	Major
		10.2 No short circuits in components on PCB or FPC.	Major
		10.3 Parts on PCB or FPC must be: no wrong parts, missing parts or excess parts.	Major
		10.4 Product packaging must the same as specified on packaging specification sheet.	Minor
		10.5 The folding and peeled off in polarizer are not acceptable.	Minor
		10.6 The PCB or FPC between B/L assembled distance(PCB or FPC) is ≦1.5 mm.	Minor

4. RELIABILITY TEST

NO.	ITEM	CONDITION		STANDARD	NOTE
1	High Temp. Storage	80℃	120 hrs	Appearance Without defect	
2	Low Temp. Storage	-30℃	120 hrs	Appearance Without defect	
3	High Temp. & High Humi. Storage	40℃ 90% RH	120 hrs	Appearance Without defect	
4	High Temp. Operating Display	70℃	120 hrs	Appearance Without defect	
5	Low Temp. Operating Display	-20℃	120 hrs	Appearance Without defect	
6	Thermal Shock	-20℃, 30min. → 70℃,30min. ↑ (1cycle) ←		Appearance Without defect	10 cycles

** Dissipation current, contrast and display functions
** Polarizing filter deterioration, other appearance defects
** The function test shall be conducted after 4hours storage at the normal temperature and humidity after remove from the test chamber.

5. PRECAUTION RELATING PRODUCT HANDLING

5.1 SAFETY

5.1.1 If the LCD panel breaks , be careful not to get the liquid crystal to touch your skin.

5.1.2 If the liquid crystal touches your skin or clothes , please wash it off immediately by using soap and water.

5.2 HANDLING

5.2.1 Avoid any strong mechanical shock which can break the glass.

5.2.2 Avoid static electricity which can damage the CMOS LSI—When working with the module , be sure to ground your body and any electrical equipment you may be using.

5.2.3 Do not remove the panel or frame from the module.

5.2.4 The polarizing plate of the display is very fragile. So , please handle it very carefully, do not touch , push or rub the exposed polarizing with anything harder than an HB pencil lead (glass , tweezers , etc.)

5.2.5 Do not wipe the polarizing plate with a dry cloth , as it may easily scratch the surface of plate.

5.2.6 Do not touch the display area with bare hands , this will stain the display area.

5.2.7 Do not use ketonics solvent & aromatic solvent. Use with a soft cloth soaked with a cleaning naphtha solvent.

5.2.8 To control temperature and time of soldering is 320 ± 5°C and 3-5 sec.

5.2.9 To avoid liquid (include organic solvent) stained on LCM

5.3 STORAGE

5.3.1 Store the panel or module in a dark place where the temperature is 25°C ± 5°C and the humidity is below 65% RH.

5.3.2 Do not place the module near organics solvents or corrosive gases.

5.3.3 Do not crush , shake , or jolt the module.

5.4 TERMS OF WARRANTY

5.4.1 Applicable warrant period

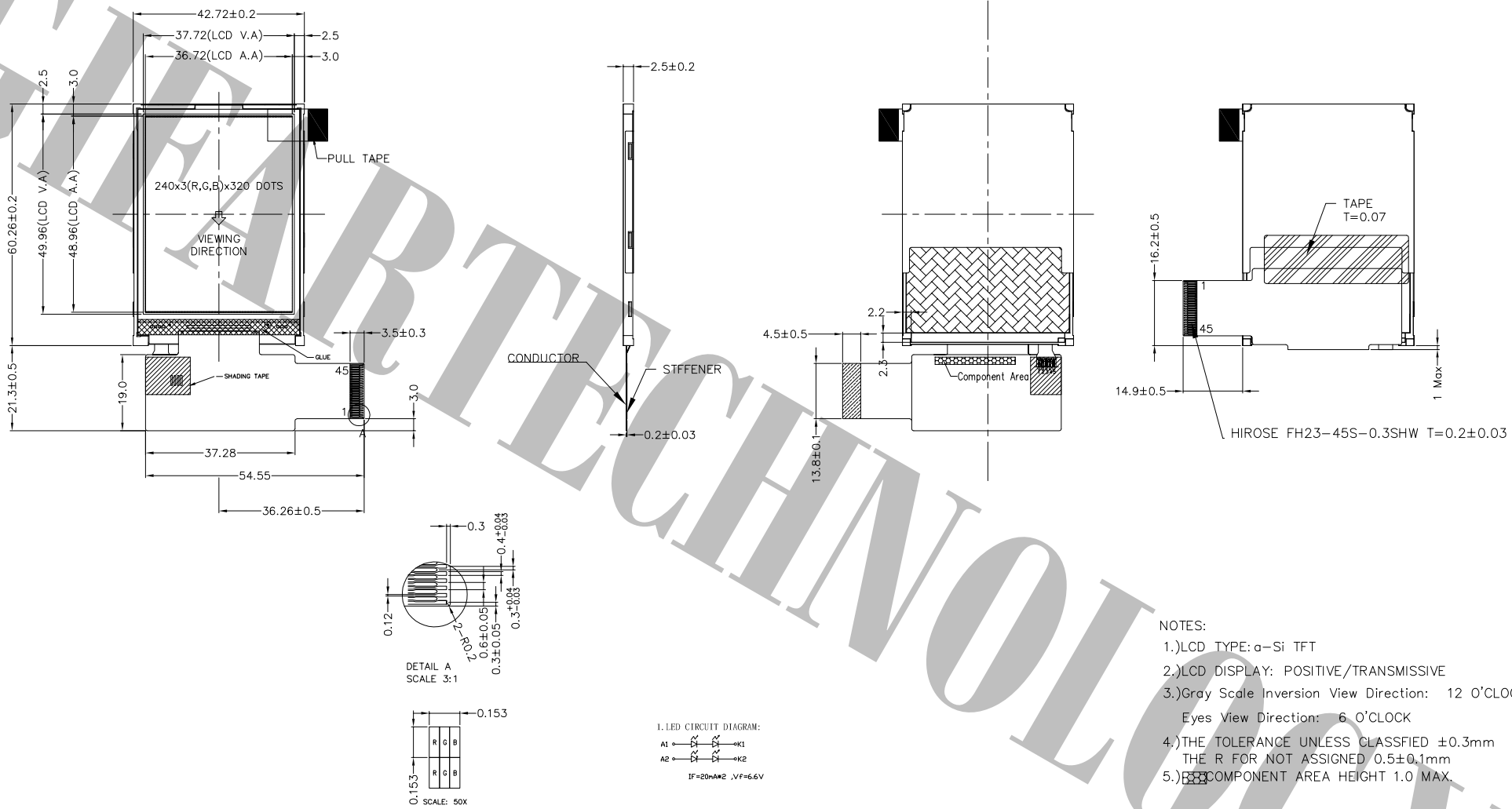
The period is within one year since the date of shipping out under normal using and storage conditions.

5.4.2 Unaccepted responsibility

This product has been manufactured to your company’s specification as a part for use in your company’s general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in nuclear power control equipment, aerospace equipment , fire and security systems or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required.

6. Appendix

RoHS



NOTES:

1.)LCD TYPE: a-Si TFT

2.)LCD DISPLAY: POSITIVE/TRANSMISSIVE

3.)Gray Scale Inversion View Direction: 12 O'CLOCK
Eyes View Direction: 6 O'CLOCK

4.)THE TOLERANCE UNLESS CLASSFIED ±0.3mm
THE R FOR NOT ASSIGNED 0.5±0.1mm

5.)COMPONENT AREA HEIGHT 1.0 MAX.

日期	版本	修改內容

晶發科技股份有限公司
GI FAR TECHNOLOGY CO., LTD

DATE	2020.10.21	REV	00	DRAWING NO.:	4M-2020092201
UNIT : mm SCALE : 1/1	Product : GFTO024KD240320				
	DRAWN: Hazel	CHECKED:	Sidney	PAGE:	1/1