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NTE74C14
Integrated Circuit
TTL– CMOS Hex Schmitt Trigger
14–Lead DIP

Description:

The NTE74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N– and P–channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} an V_{T-} show low variation with respect to temperature (typ. 0.0005V/°C at V_{CC} = 10V) and hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{CC}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features:

- Wide Supply Range: 3V to 15V
- High Noise Immunity: 0.7 V_{CC} (typ)
- Low Power TTL Compatibility: 0.4 V_{CC} (typ) 0.2 V_{CC} Guaranteed
- Hysteresis: 0.4 V_{CC} (typ) 0.2 V_{CC} Guaranteed

Absolute Maximum Ratings: (Note 1)

Voltage at Any Pin . . . . . –0.3V to V_{CC} +0.3V
Power Dissipation, P_D 700mW
Operating V_{CC} Range . . . . . 3V to 15V
Absolute Maximum V_{CC} 18V
Operating Temperature Range, T_A . . . . . –40° to +85°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. “Absolute Maximum Ratings” are those values beyond which th safety of the device cannot be guaranteed. Except for “Operating Temperature Range”, they are not meant to imply that the devices should be operated at these limits. The table of “Electrical Characteristics” provides conditions for actual device operation.

DC Electrical Characteristics: (T_A = −40° to +85°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CMOS to CMOS						
Positive Going Threshold Voltage	V_{T+}	V_{CC} = 5V	3.0	3.6	4.3	V
		V_{CC} = 10V	6.0	6.8	8.6	V
		V_{CC} = 15V	9.0	10.0	12.9	V
Negative Going Threshold Voltage	V_{T-}	V_{CC} = 5V	0.7	1.4	2.0	V
		V_{CC} = 10V	1.4	3.2	4.0	V
		V_{CC} = 15V	2.1	5.0	6.0	V
Hysteresis	V_{T+}–V_{T-}	V_{CC} = 5V	1.0	2.2	3.6	V
		V_{CC} = 10V	2.0	3.6	7.2	V
		V_{CC} = 15V	3.0	5.0	10.8	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 5V, I_O = −10µA	4.5	–	–	V
		V_{CC} = 10V, I_O = −10µA	9.0	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 5V, I_O = −10µA	–	–	0.5	V
		V_{CC} = 10V, I_O = −10µA	–	–	1.0	V
Logical “1” Input Current	$I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V	–	0.005	1.0	µA
Logical “0” Input Current	$I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V	–1.0	–0.005	–	µA
Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 0V/15V	–	0.05	15	µA
		V_{CC} = 5V, V_{IN} = 2.5V, Note 2	–	20	–	µA
		V_{CC} = 10V, V_{IN} = 5V, Note 2	–	200	–	µA
		V_{CC} = 15V, V_{IN} = 7.5V, Note 2	–	600	–	µA
CMOS/LPTTL Interface						
Logical “1” Input Voltage	$V_{IN(1)}$	V_{CC} = 5V	4.3	–	–	V
Logical “0” Input Voltage	$V_{IN(0)}$	V_{CC} = 5V	–	–	0.7	V
Logical “1” Output Voltage	$V_{OUT(1)}$	V_{CC} = 4.75V, I_O = −360µA	2.4	–	–	V
Logical “0” Output Voltage	$V_{OUT(0)}$	V_{CC} = 4.75V, I_O = 360µA	–	–	0.4	V
Output Drive (Short Circuit Current)						
Output Source Current (P−Channel)	I_{SOURCE}	V_{CC} = 5V, V_{OUT} = 0V, T_A = +25°C	–1.75	–3.3	–	mA
		V_{CC} = 10V, V_{OUT} = 0V, T_A = +25°C	–8.0	–15	–	mA
Output Sink Current (N−Channel)	I_{SINK}	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = +25°C	1.75	3.3	–	mA
		V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = +25°C	8.0	15	–	mA

Note 2. Only one of the six inputs is at 1/2 V_{CC}; the others are either at V_{CC} or GND.

AC Electrical Characteristics: (T_A = +25°, C_L = 50pF, Note 3 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time from Input to Output	t_{pd0}, t_{pd1}	V_{CC} = 5V	–	220	400	ns
		V_{CC} = 10V	–	80	200	ns
Input Capacitance	C_{IN}	Any Input (Note 4)	–	5.0	–	pF
Power Dissipation Capacitance	C_{PD}	Per Gate (Note 5)	–	45	–	pF

Note 3. AC Parameters are guaranteed by DC correlated testing.
Note 4. Capacitance is guaranteed by periodic testing.
Note 5. C_{PD} determines the no load AC power consumption of any CMOS device.

Pin Connection Diagram