FDMS8350LET40

MOSFET N-Channel POWERTRENCH®

40 V, 300 A, 0.85 mΩ

General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

Features

- Max $R_{DS(on)}$ = 0.85 mΩ at V_{GS} = 10 V, I_D = 47 A
- Max $R_{DS(on)}$ = 1.2 mΩ at V_{GS} = 4.5 V, I_D = 38 A
- Advanced Package and Silicon combination for Low $r_{DS(on)}$ and High Efficiency
- MSL1 Robust Package Design
- 100% UIL Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Primary DC−DC MOSFET
- Secondary Synchronous Rectifier
- Load Switch

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: Continuous (T_C = 25°C) (Note 5) Continuous T_C = 100°C (Note 5) Continuous, T_A = 25°C (Note 1a) Pulsed (Note 4)	300 212 49 1464	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	1176	mJ
P_D	Power Dissipation: T_C = 25°C T_A = 25°C (Note 1a)	 125 3.33	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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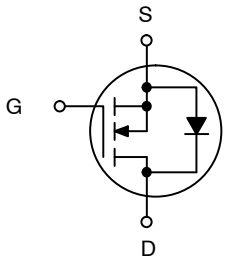
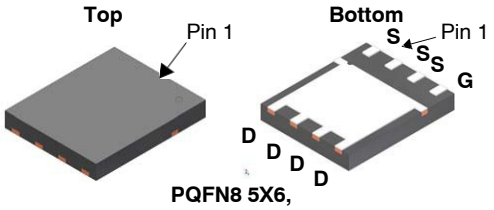
V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
40 V	0.85 mΩ @ 10 V	47 A
	1.2 mΩ @ 4.5 V	



N-CHANNEL MOSFET



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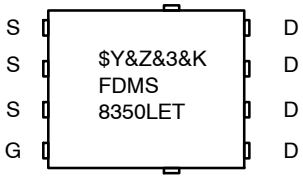
MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FDMS8350LET40	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		17		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.8	3.0	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		−6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 47 A		0.68	0.85	mΩ
		V_{GS} = 4.5 V, I_D = 38 A		0.96	1.2	
		V_{GS} = 10 V, I_D = 47 A, T_J = 150°C		1.1	1.4	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 47 A		247		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz		11850	16590	pF
C_{oss}	Output Capacitance			3430	4805	pF
C_{rss}	Reverse Transfer Capacitance			69	100	pF
R_g	Gate Resistance		0.1	1.2	2.4	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 20 V, I_D = 47 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		32	51	ns
t_r	Rise Time			19	34	ns
$t_{d(off)}$	Turn-Off Delay Time			74	118	ns
t_f	Fall Time			15	27	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V		156	219	nC
		V_{GS} = 0 V to 4.5 V		73	102	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 20 V, I_D = 47 A		33		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 20 V, I_D = 47 A		16		nC

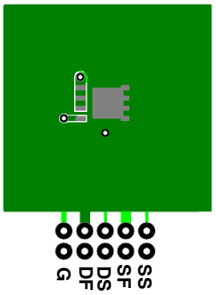
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.1 A (Note 2)		0.7	1.2	V
		V_{GS} = 0 V, I_S = 47 A (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	I_F = 47 A, di/dt = 100 A/μs		81	129	ns
Q_{rr}	Reverse Recovery Charge			82	131	nC

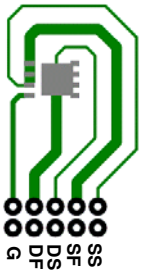
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

NOTES:



a) 45°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 115°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 1176 mJ is based on starting T_J = 25°C; L = 3 mH, I_{AS} = 28 A, V_{DD} = 40 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 87 A.
4. Pulsed Id please refer to Fig 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Quantity
FDMS8350LET40	FDMS8350LET	Power 56	13″	12 mm	3000 units

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

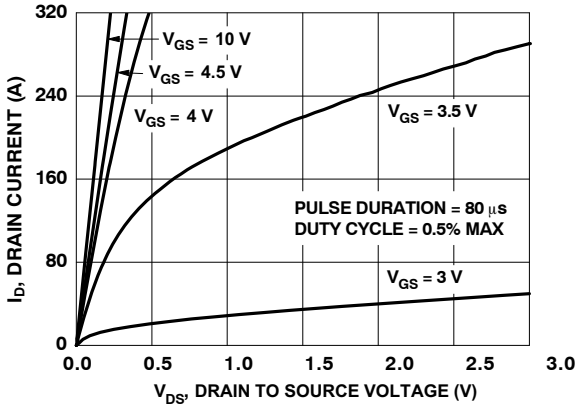


Figure 1. On−Region Characteristics

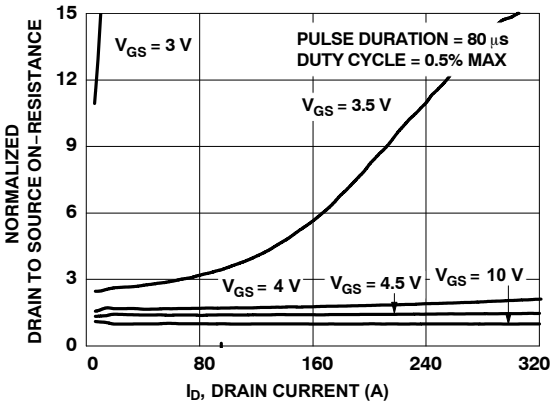


Figure 6. Normalized On−Resistance vs Drain Current and Gate Voltage

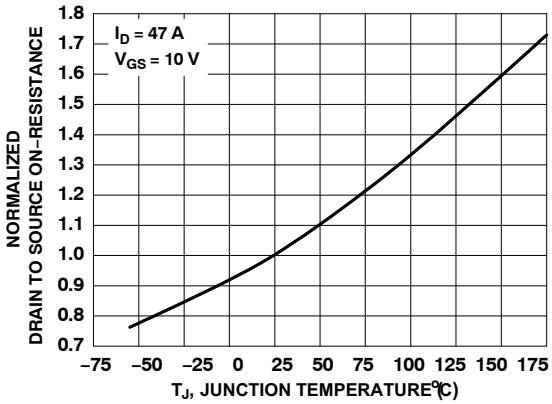


Figure 2. Normalized On−Resistance vs Junction Temperature

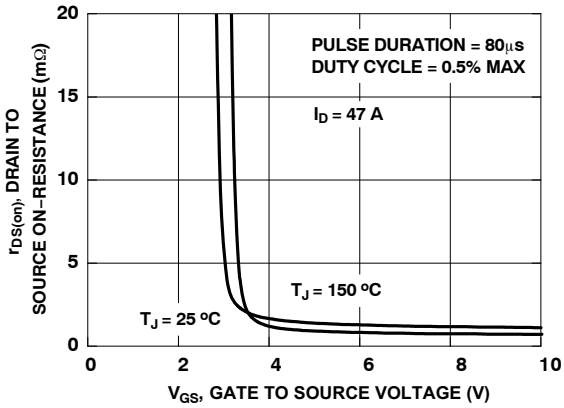


Figure 3. On−Resistance vs Gate to Source Voltage

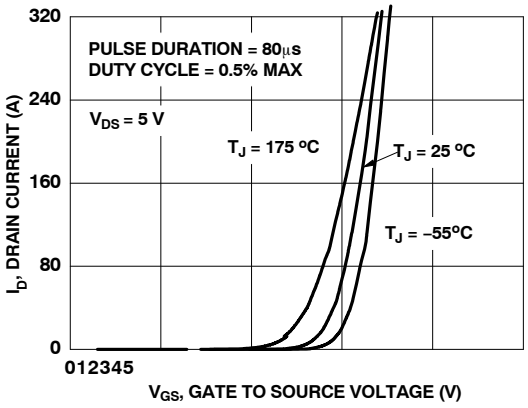


Figure 4. Transfer Characteristics

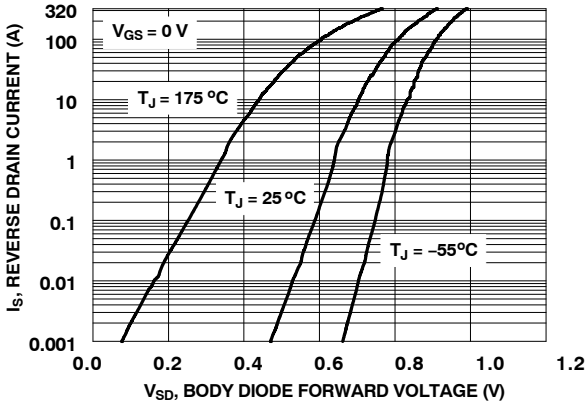


Figure 5. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

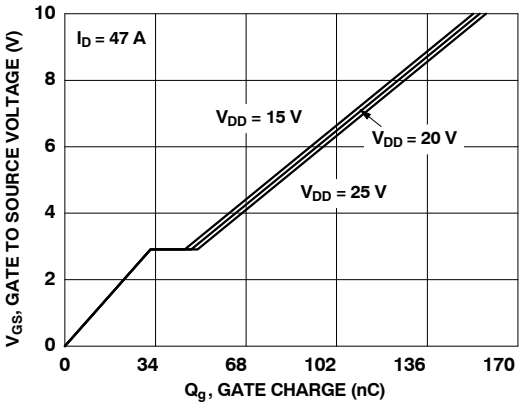


Figure 7. Gate Charge Characteristics

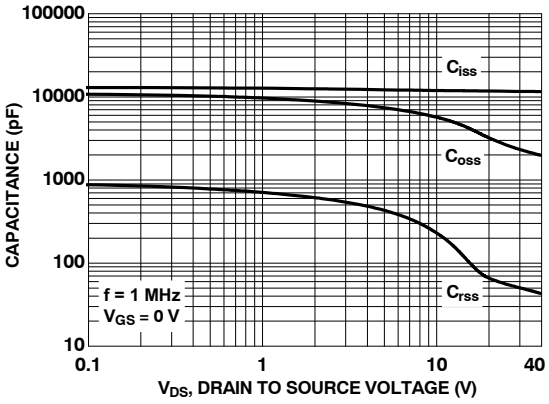


Figure 8. Capacitance vs Drain to Source Voltage

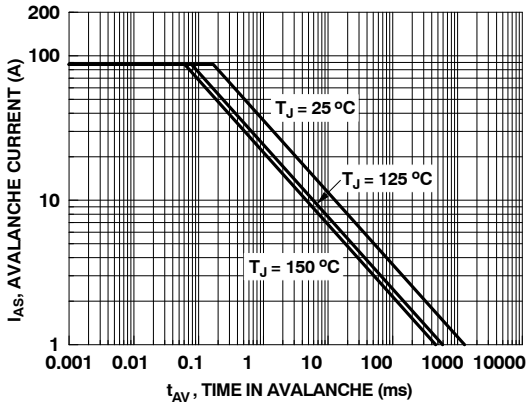


Figure 9. Unclamped Inductive Switching Capability

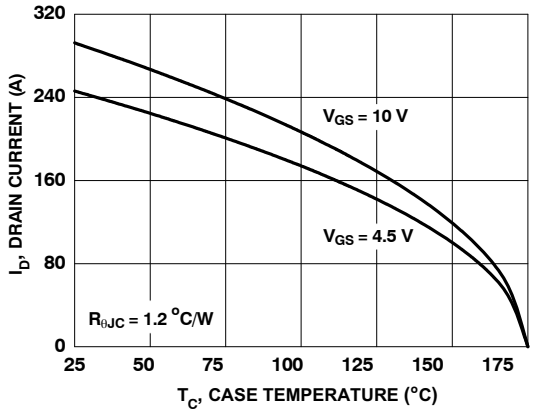


Figure 10. Maximum Continuous Drain Current vs Case Temperature

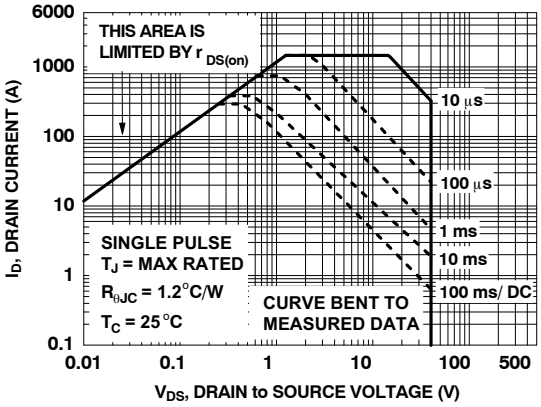


Figure 11. Forward Bias Safe Operating Area

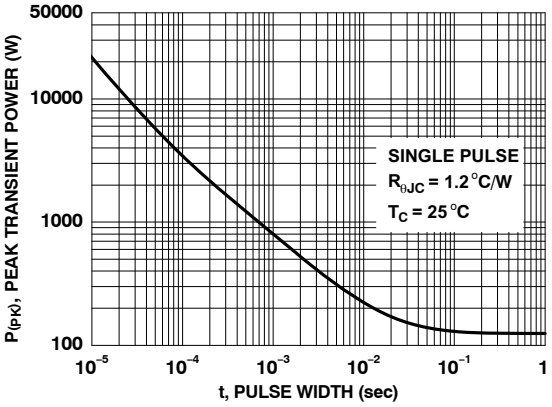


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

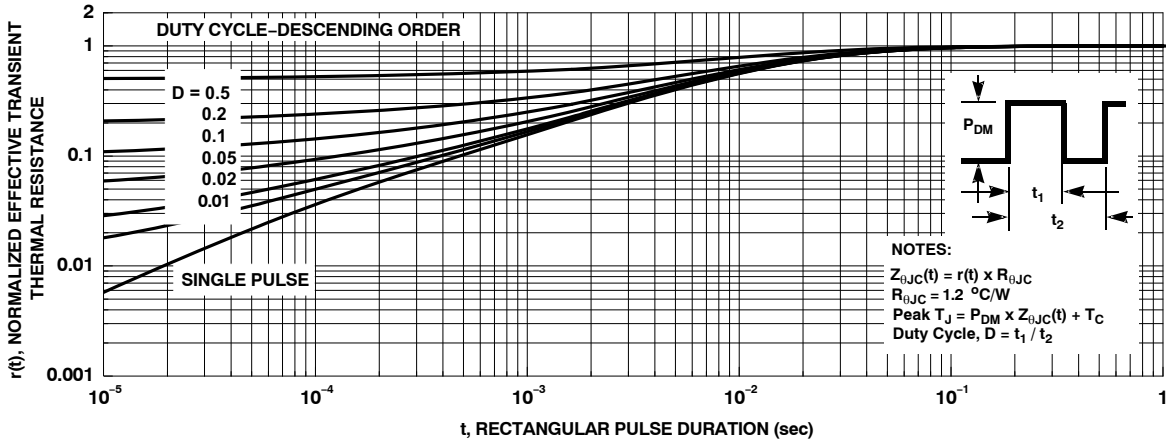
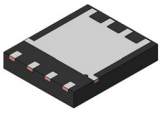


Figure 13. Junction−to−Case Transient Thermal Response Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



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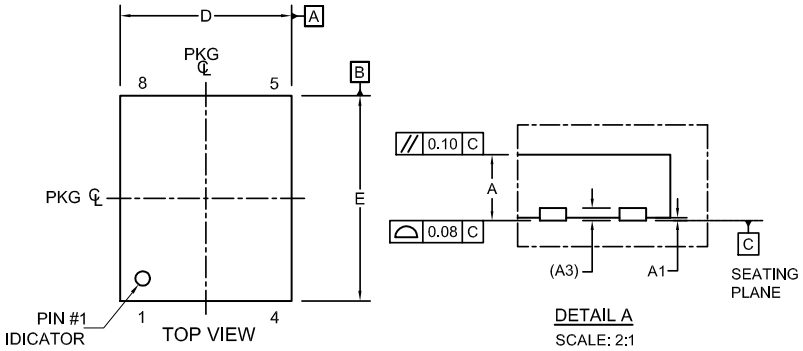
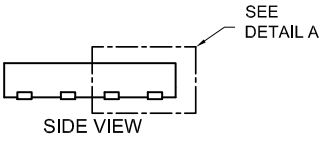
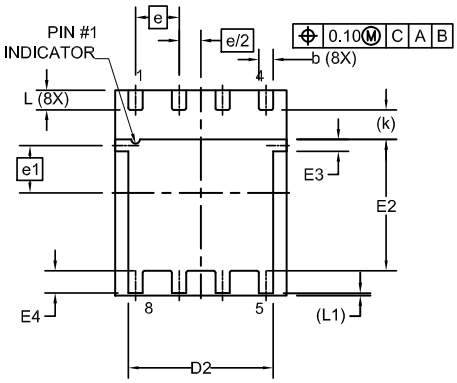
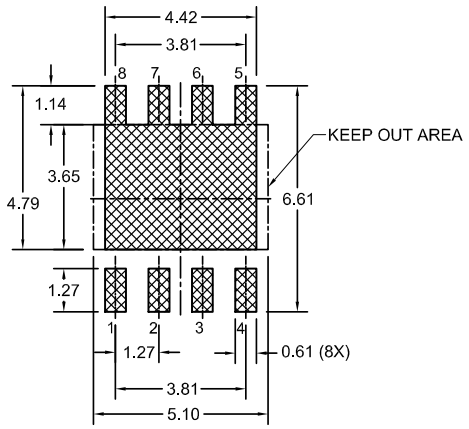


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.







LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3		0.20 REF	
b	0.37	0.42	0.47
D	4.90	5.00	5.10
D2	4.13	4.23	4.33
E	5.90	6.00	6.10
E2	3.74	3.84	3.94
E3	0.25	0.35	0.45
E4	0.60	0.70	0.80
e		1.27 BSC	
e/2		0.635 BSC	
e1		1.31 BSC	
k		0.86 REF	
L	0.47	0.57	0.67
L1		0.08REF	

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