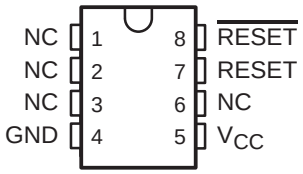
SLVS042D – JANUARY 1991 – REVISED JULY 1999

- **Power-On Reset Generator**
- **Automatic Reset Generation After Voltage Drop**
- **Precision Input Threshold Voltage . . . 4.55 V ±120 mV**
- **Low Standby Current . . . 20 μA**
- **Reset Outputs Defined When V_{CC} Exceeds 1 V**
- **True and Complementary Reset Outputs**
- **Wide Supply-Voltage Range . . . 1 V to 7 V**

D, P, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TL7759 is a supply-voltage supervisor designed for use as a reset controller in microcomputer and microprocessor systems. The supervisor monitors the supply voltage for undervoltage conditions. During power up, when the supply voltage, V_{CC}, attains a value approaching 1 V, the RESET and $\overline{\text{RESET}}$ outputs become active (high and low, respectively) to prevent undefined operation. If the supply voltage drops below the input threshold voltage level (V_{IT-}), the reset outputs go to the reset active state until the supply voltage has returned to its nominal value (see timing diagram).

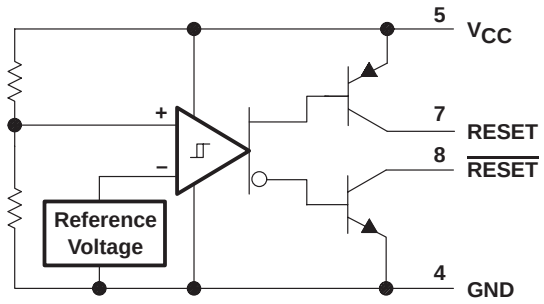
The TL7759C is characterized for operation from 0°C to 70°C.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES			CHIP FORM (Y)
	SMALL OUTLINE (D)	PLASTIC DIP (P)	SHRINK SMALL OUTLINE (PW)	
0°C to 70°C	TL7759CD	TL7759CP	TL7759CPW	TL7759Y

The D and PW packages are available taped and reeled. Add the suffix R to the device type (e.g., TL7759CDR). Chip forms are tested at 25°C.

functional block diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . . 20 V
Off-state output voltage range: $\overline{\text{RESET}}$ voltage . . . . . –0.3 V to 20 V
RESET voltage . . . . . –0.3 V to 20 V
Low-level output current, I_{OL} ($\overline{\text{RESET}}$) . . . . . 30 mA
High-level output current, I_{OH} (RESET) . . . . . –10 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): D package . . . . . 97°C/W
P package . . . . . 127°C/W
PW package . . . . . 149°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{CC}		1	7	V
Output voltage, V_O (see Note 4)	Transistor off $\overline{\text{RESET}}$ voltage		15	V
	Transistor off RESET voltage	0		
Low-level output current, I_{OL}	$\overline{\text{RESET}}$		24	mA
High-level output current, I_{OH}	RESET		–8	mA
Operating free-air temperature, T_A	TL7759C	0	70	°C

NOTE 4: RESET output must not be pulled down below GND potential.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL7759C MIN	TL7759C TYP‡	TL7759C MAX	UNIT
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	V_{CC} = 4.3 V	I_{OL} = 24 mA		0.4	0.8	V
V_{OH}	High-level output voltage	RESET		I_{OH} = –8 mA	V_{CC}–1			V
$V_{IT–}$	Input threshold voltage (negative-going V_{CC})		T_A = 25°C		4.43	4.55	4.67	V
			T_A = 0°C to 70°C		4.4		4.7	
V_{res}§	Power-up reset voltage		R_L = 2.2 kΩ	T_A = 25°C		0.8	1	V
				T_A = 0°C to 70°C			1.2	
V_{hys}¶	Hysteresis at V_{CC} input		T_A = 25°C		40	50	60	mV
			T_A = 0°C to 70°C		30		70	
I_{OH}	High-level output current	$\overline{\text{RESET}}$	V_{CC} = 7 V, See Figure 1	V_{OH} = 15 V			1	µA
I_{OL}	Low-level output current	RESET		V_{OL} = 0 V			–1	µA
I_{CC}	Supply current		No load	V_{CC} = 4.3 V		1400	2000	µA
				V_{CC} = 5.5 V			40	

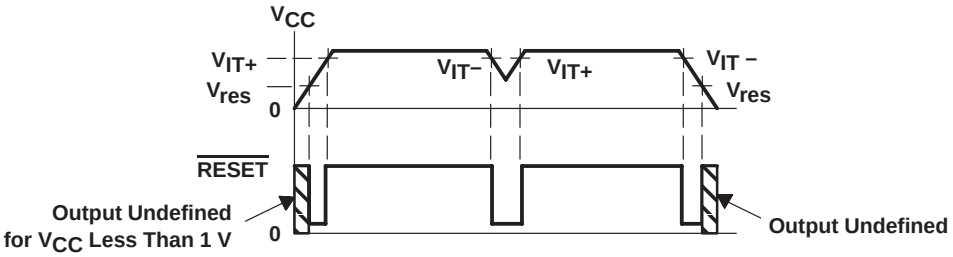
‡ Typical values are at T_A = 25°C.
§ This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active, V_{CC} slew rate ≤ 5 V/µs.
¶ This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, $V_{IT–}$.

electrical characteristics, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS		TL7759Y			UNIT
					MIN	TYP	MAX	
V_{OL}	Low-level output voltage	$\overline{\text{RESET}}$	V_{CC} = 4.3 V,	I_{OL} = 24 mA		0.4		V
V_{IT-}	Input threshold voltage (negative-going V_{CC})					4.55		V
V_{res}†	Power-up reset voltage		R_L = 2.2 kΩ			0.8		V
V_{hys}‡	Hysteresis at V_{CC} input					50		mV
I_{CC}	Supply current		V_{CC} = 4.3 V,	No load		1400		µA

† This is the lowest voltage at which $\overline{\text{RESET}}$ becomes active, V_{CC} slew rate ≤ 5 V/µs.
‡ This is the difference between positive-going input threshold voltage, V_{IT+}, and negative-going input threshold voltage, V_{IT-}.

timing diagram



switching characteristics at T_A = 25°C (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TL7759C		UNIT
					MIN	MAX	
t_{PLH}	Propagation delay time, low-to high-level output	V_{CC}	RESET	See Figures 2 and 3§		5	µs
t_{PHL}	Propagation delay time, high-to low-level output	V_{CC}	$\overline{\text{RESET}}$	See Figures 2 and 4		5	µs
t_r	Rise time		$\overline{\text{RESET}}$	See Figures 2 and 4§		1	µs
t_f	Fall time		$\overline{\text{RESET}}$	See Figures 2 and 4		1	µs
$t_{w(min)}$	Minimum pulse duration	V_{CC}	$\overline{\text{RESET}}$	See Figures 2 and 4	5		µs

§ V_{CC} slew rate ≤ 5 V/µs

PARAMETER MEASUREMENT INFORMATION

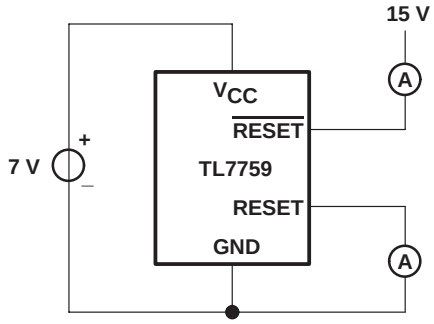
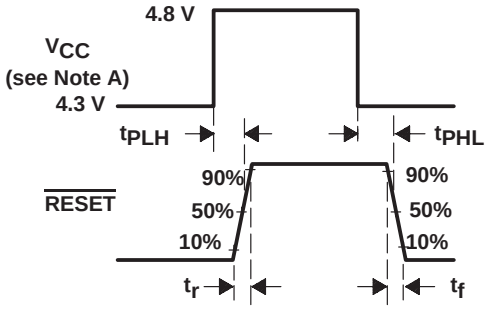
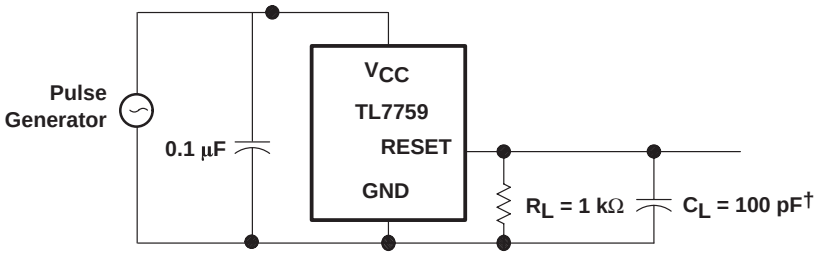


Figure 1. Test Circuit for Output Leakage Current



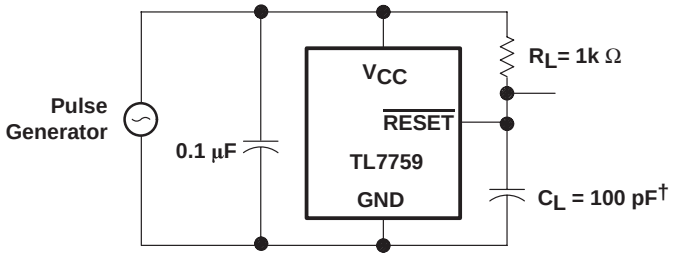
NOTE A: V_{CC} slew rate ≤ 5 V/μs.

Figure 2. Switching Diagram



† C_L Includes jig and probe capacitance.

Figure 3. Test Circuit for RESET Output Switching Characteristics



† C_L Includes jig and probe capacitance.

Figure 4. Test Circuit for $\overline{\text{RESET}}$ Output Switching Characteristics

APPLICATION INFORMATION

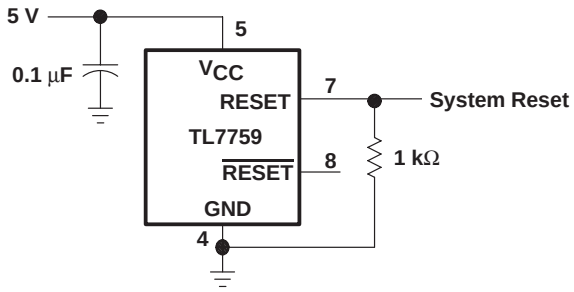


Figure 5. Power-Supply System Reset Generation

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL7759CD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7759C	Samples
TL7759CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7759C	Samples
TL7759CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL7759CP	Samples
TL7759CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T7759	Samples
TL7759CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T7759C	Samples
TL7759CPWRE4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T7759C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

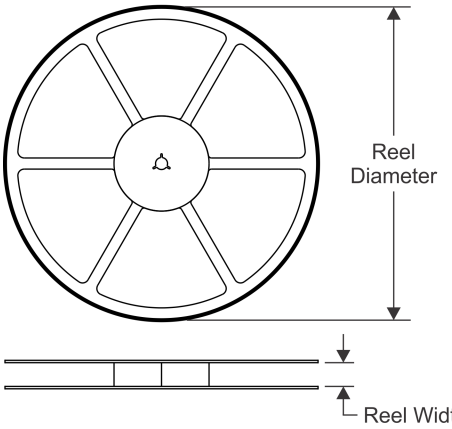
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

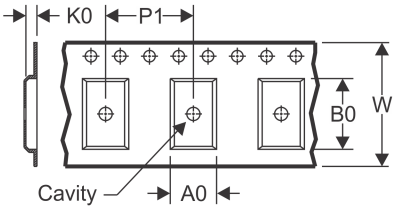
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

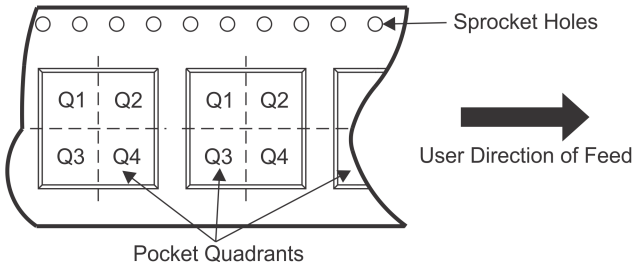


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

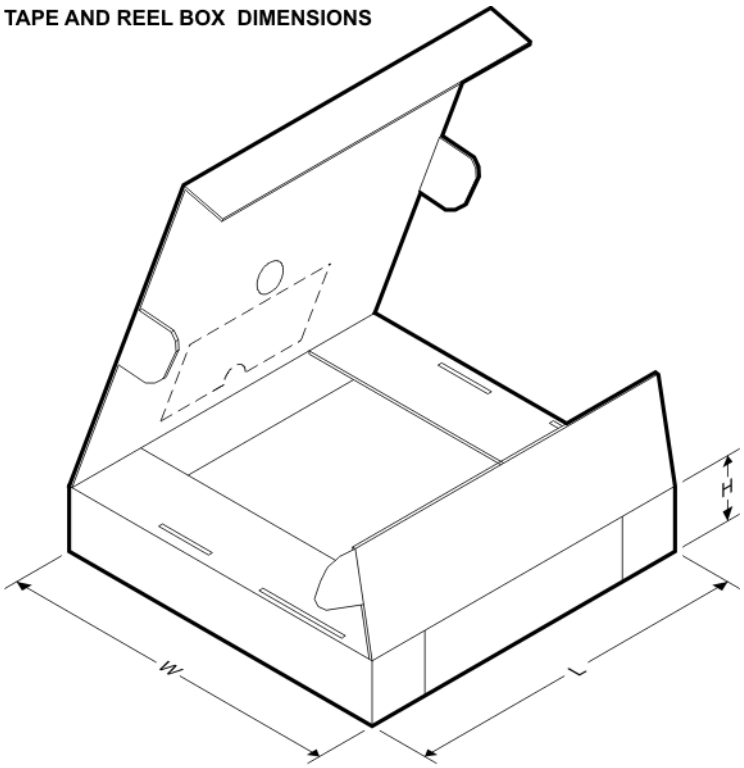
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

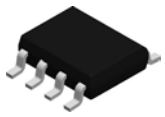
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7759CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL7759CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL7759CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL7759CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL7759CPSR	SO	PS	8	2000	853.0	449.0	35.0
TL7759CPWR	TSSOP	PW	8	2000	853.0	449.0	35.0

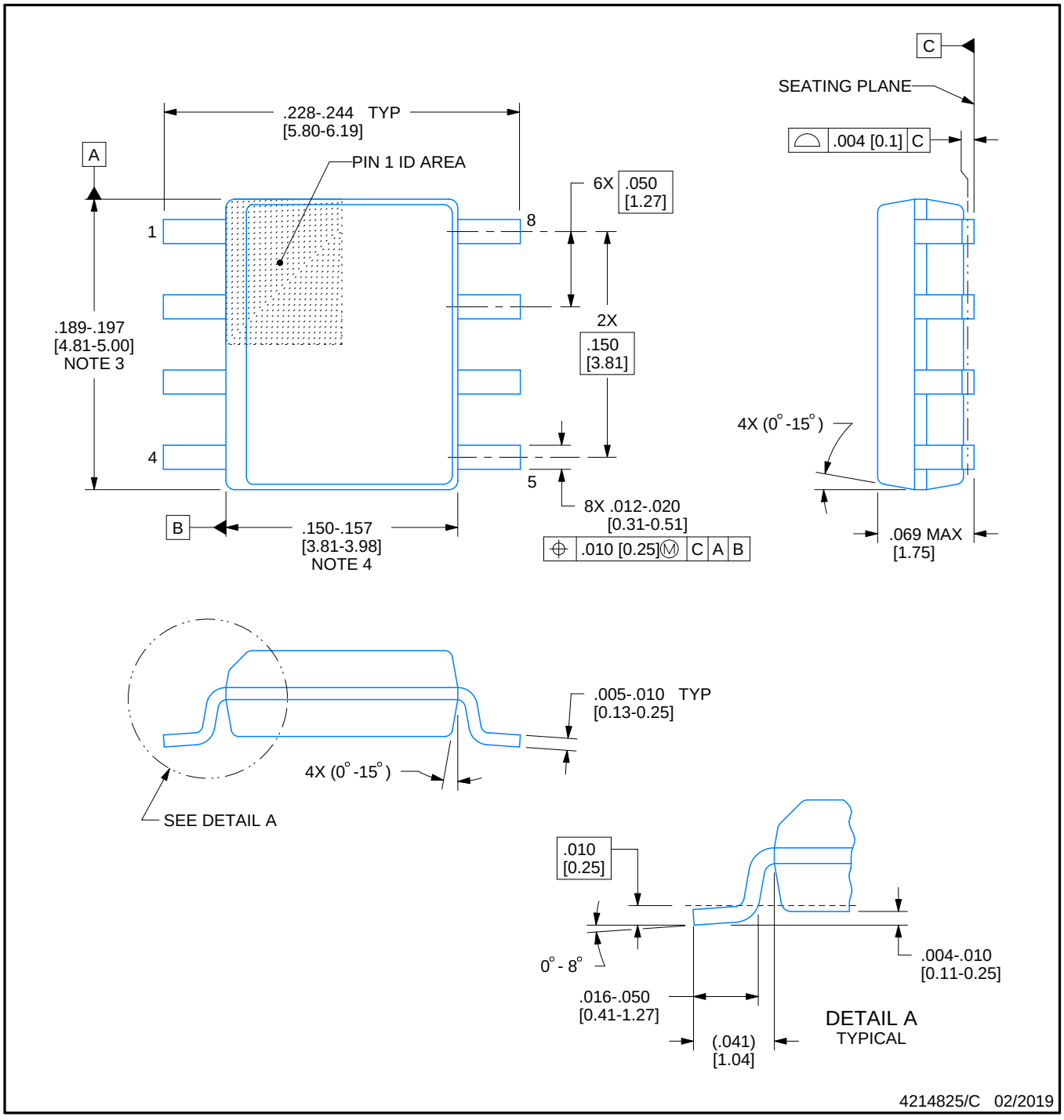


PACKAGE OUTLINE

D0008A

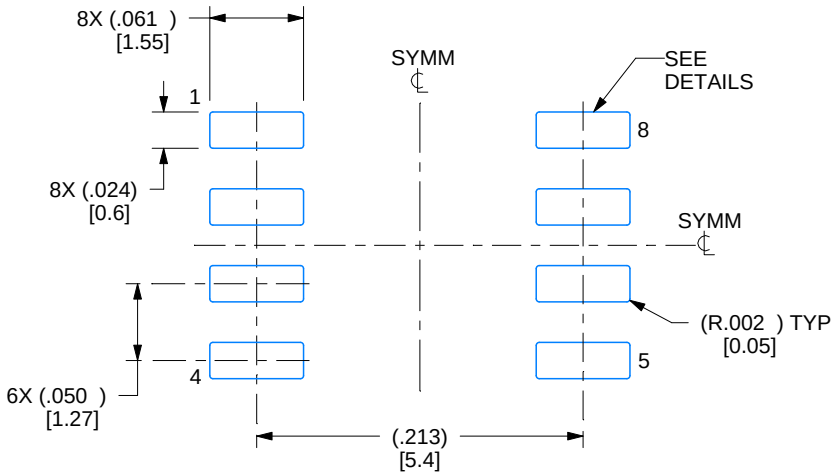
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

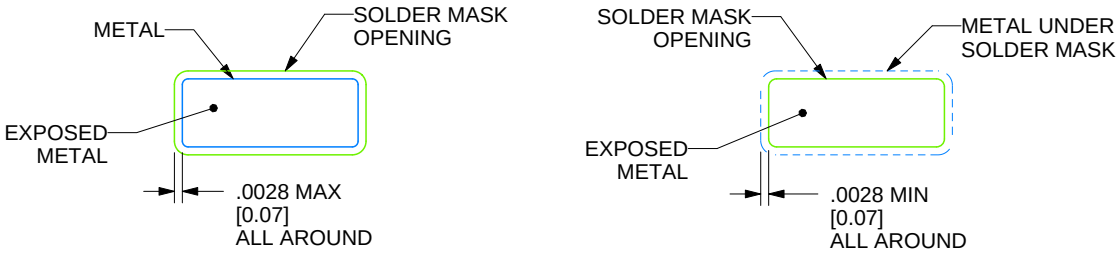


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

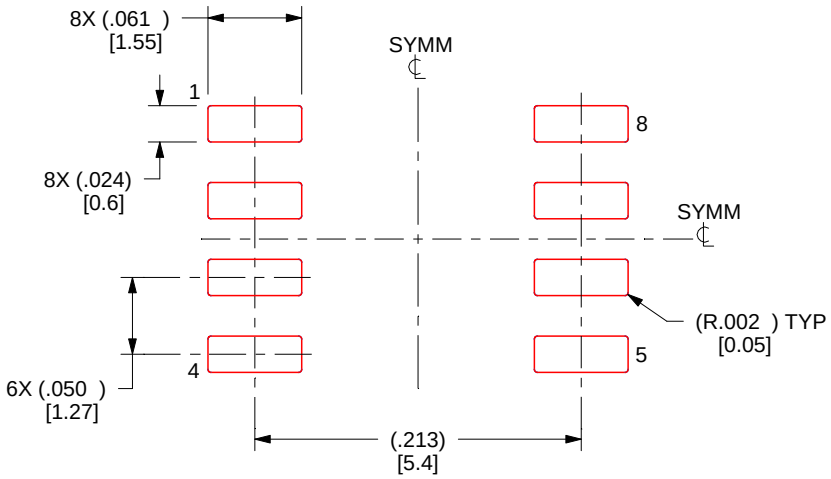
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

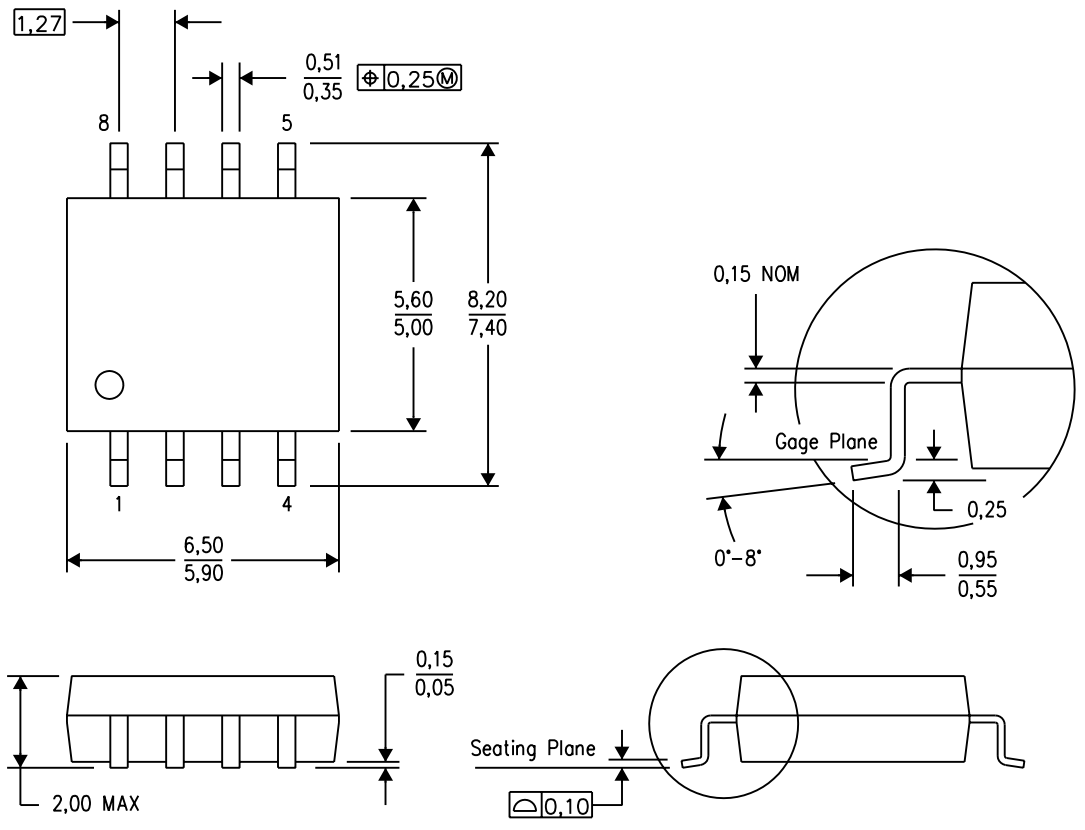
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

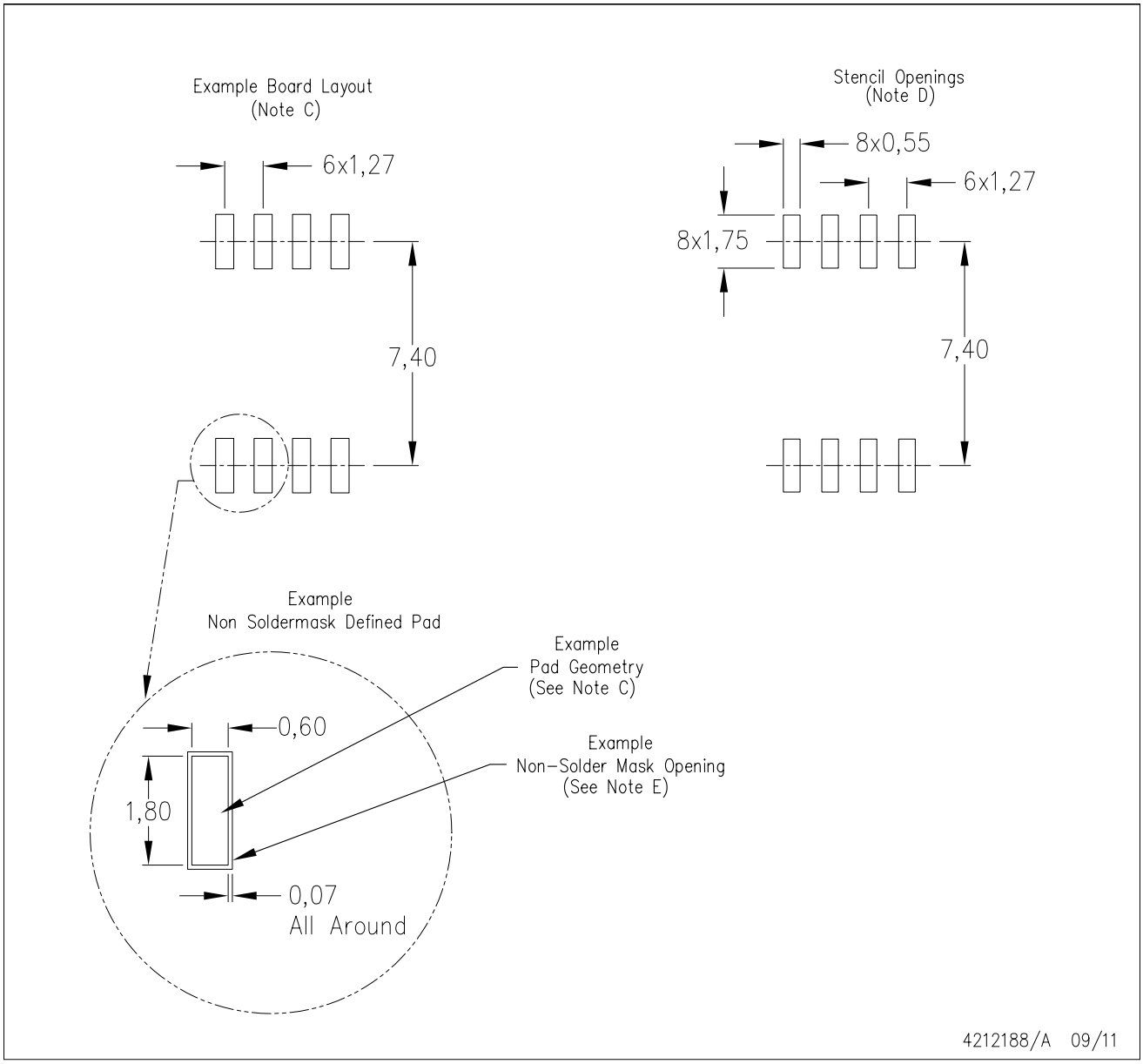
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

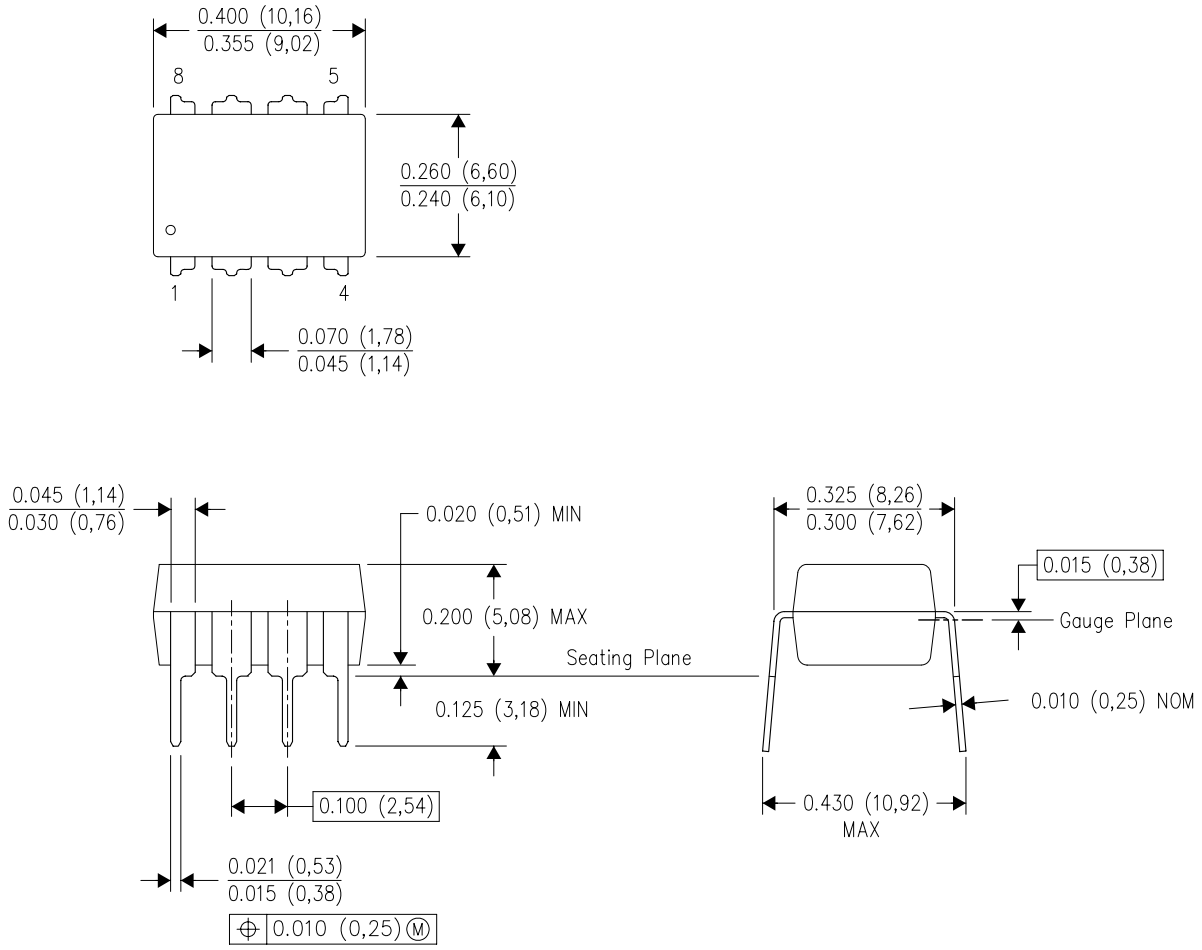
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



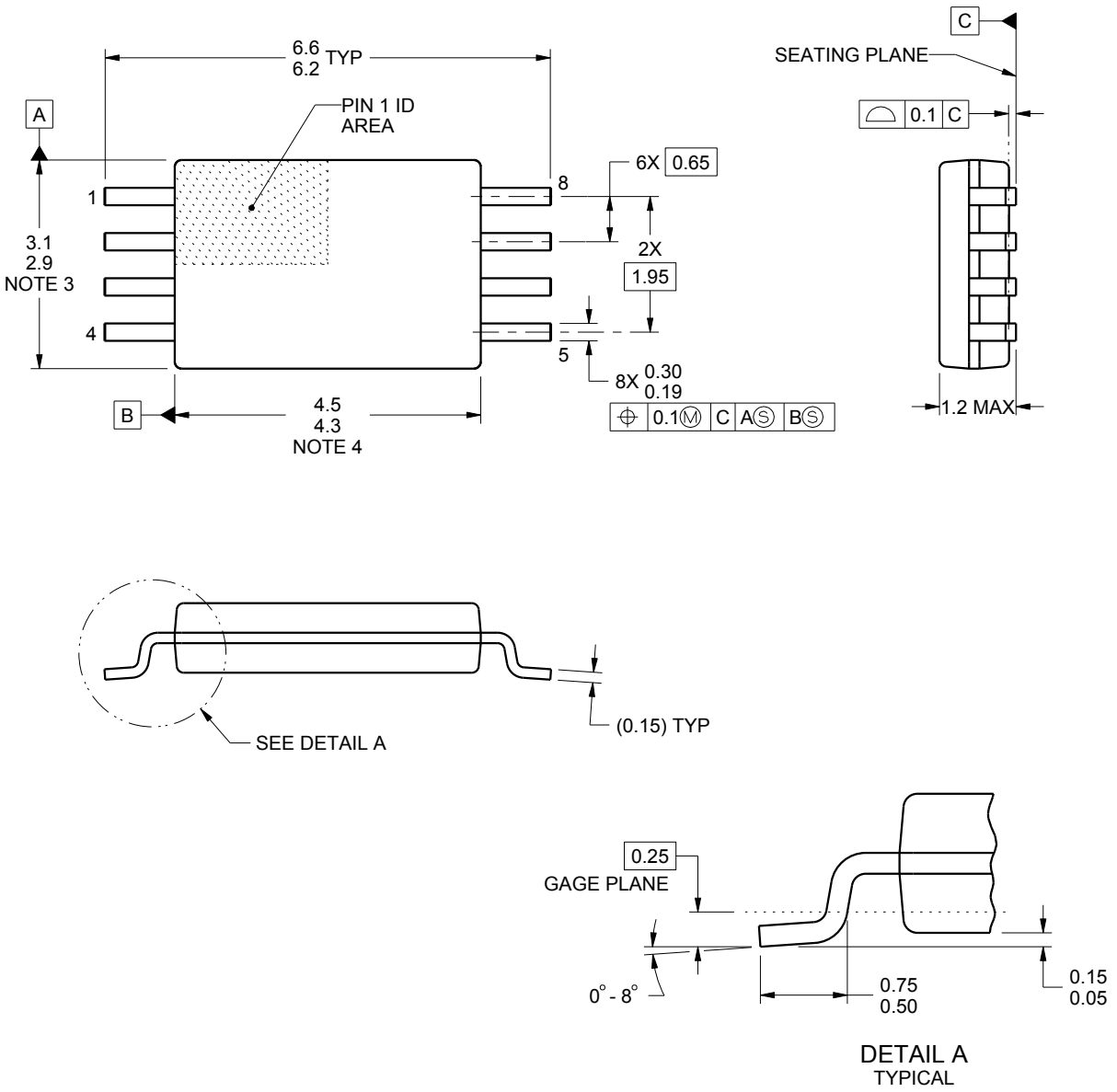
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

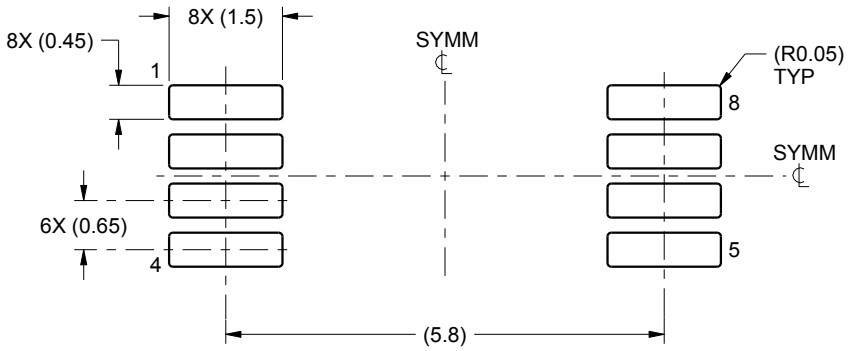
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

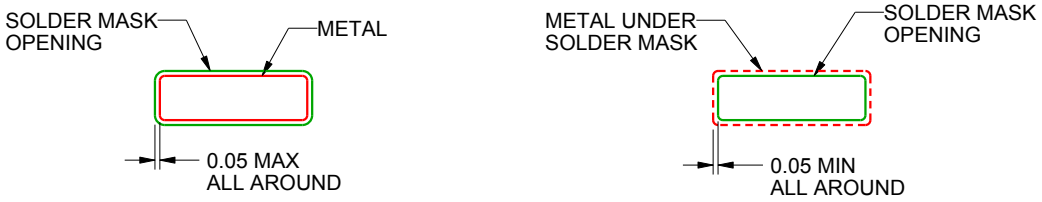


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

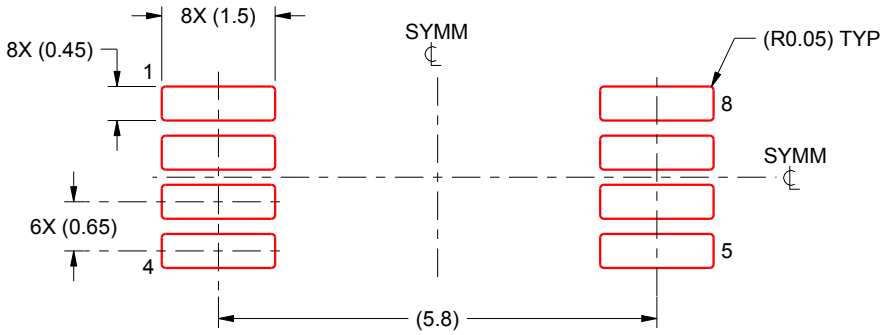


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265