

U_B12
B12.SchDoc

U_B13
B13.SchDoc

U_B14
B14.SchDoc

U_B15
B15.SchDoc

U_B16
B16.SchDoc

U_B34
B34.SchDoc

U_FPGA-MGT
FPGA-MGT.SchDoc

U_FPGA-CFG
FPGA-CFG.SchDoc

U_FPGA-MISC
FPGA-MISC.SchDoc

U_FPGA-PWR
FPGA-PWR.SchDoc

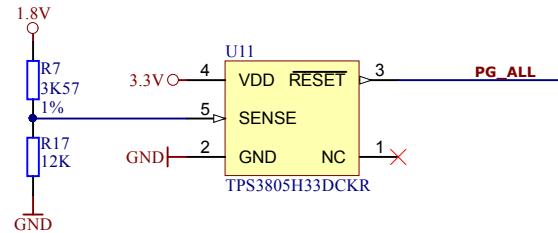
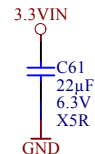
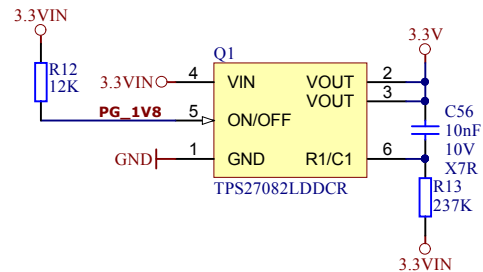
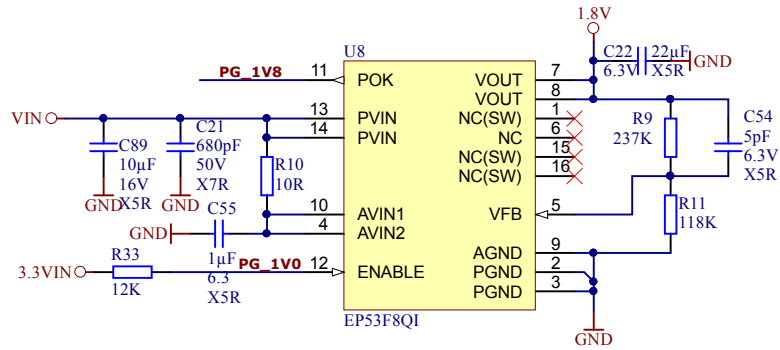
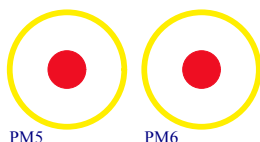
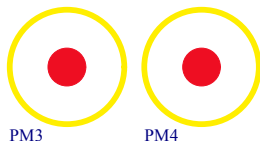
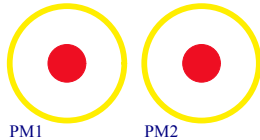
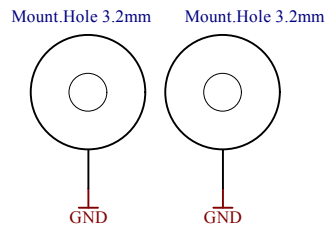
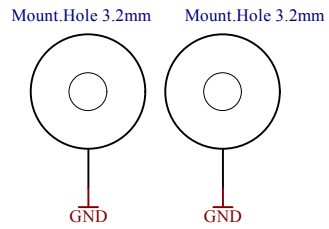
U_PWR1
PWR1.SchDoc

U_PWR2
PWR2.SchDoc

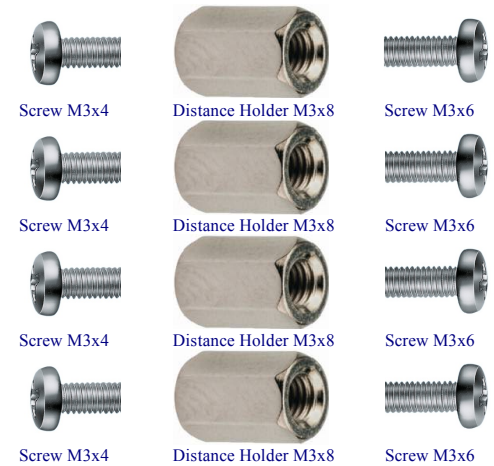
U_Clock
Clock.SchDoc

U_B2B-Connectors
B2B-Connectors.SchDoc

U_B33
B33.SchDoc



Top of Board

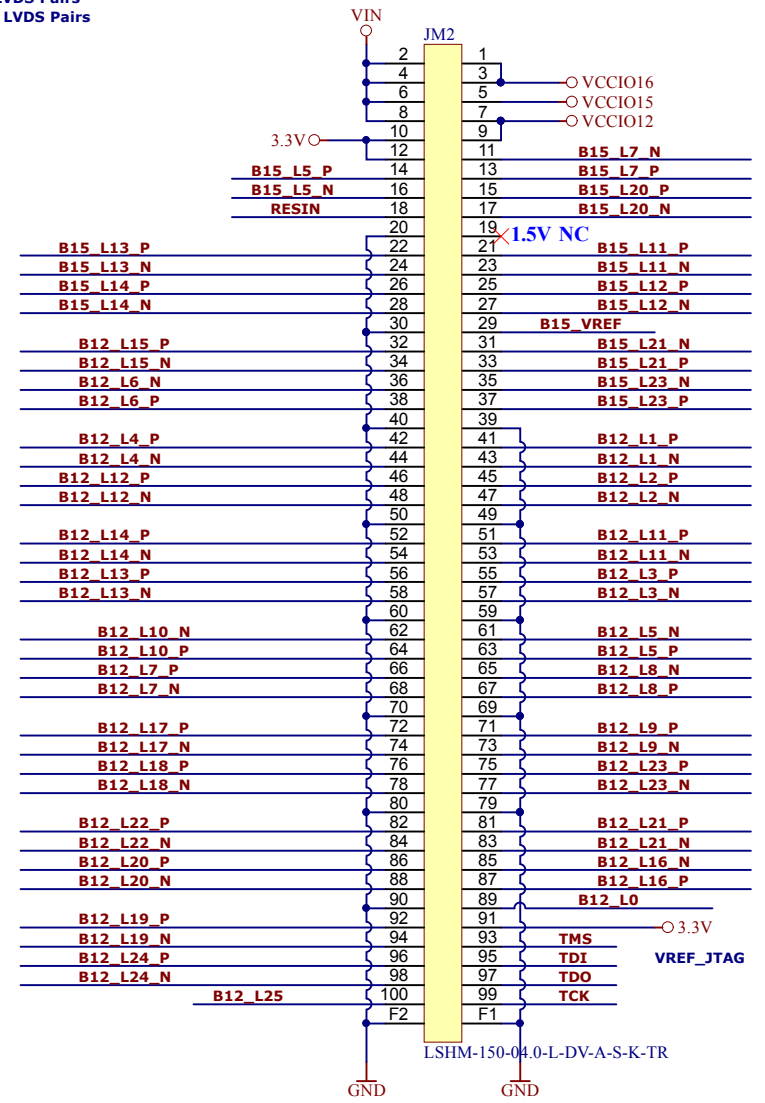
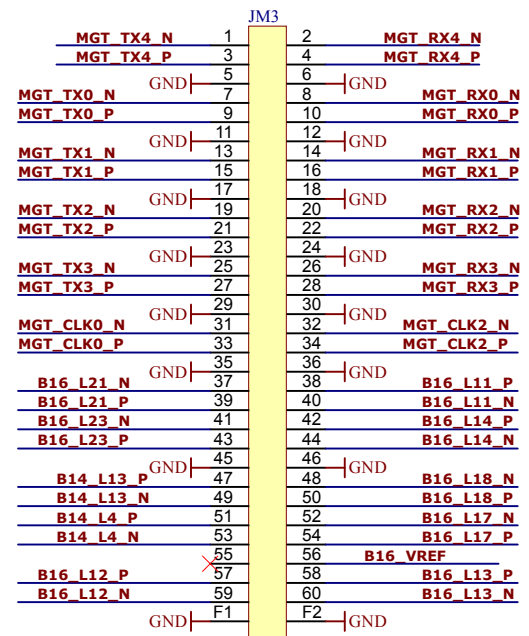
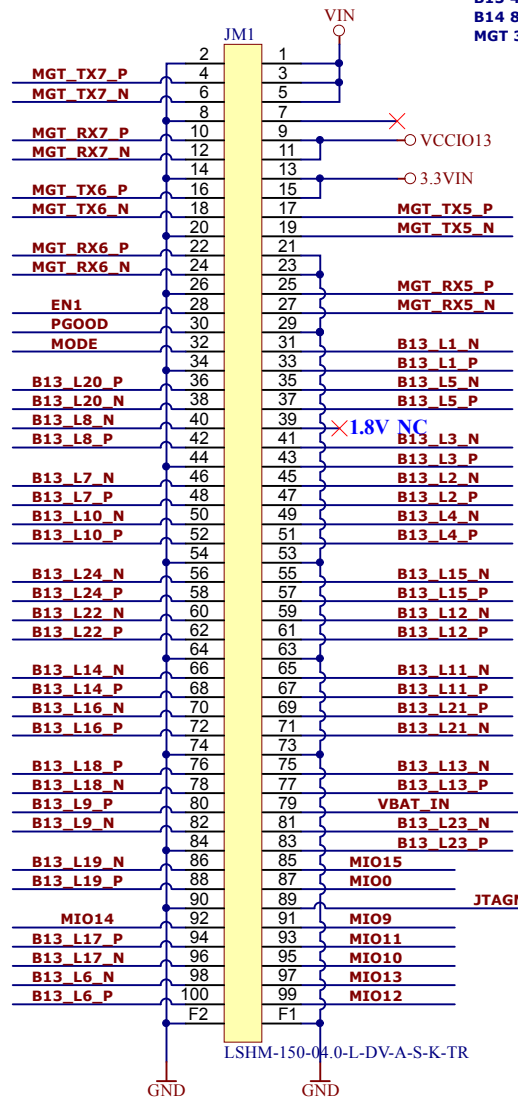


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B13 48 IO, 24 LVDS Pairs
B14 8 IO, 3.3V
MGT 3 Lanes

B16 16 IO, 8 LVDS Pairs
MGT 4 + 1 Lanes
B14 4 IO, 3.3V

B15 18 IO, 9 LVDS Pairs
B12 48 IO, 24 LVDS Pairs
B12 2 IO



TE0720 Compatibility

MIO0 8 pins => 8 IO B14
 USB D+,D-, vbusen,otg_id => 4 IO B14
 SGMII => MGT
 MIO1(SDCARD) => MGT
 ETH MD1 => MGT
 B34 => B16, MGT
 B35 => B13
 B13 => B12
 B33 => B15

Clock Capable I/O
 All pins named
 Bxx_H_X
 Bxx_I_X
 Bxx_O_X
 Bxx_T_X
 Bxx_C_X
 Bxx_D_X
 Bxx_E_X
 Bxx_F_X
 Bxx_G_X
 Bxx_H_X
 Bxx_I_X
 Bxx_J_X
 Bxx_K_X
 Bxx_L_X
 Bxx_M_X
 Bxx_N_X
 Bxx_O_X
 Bxx_P_X
 Bxx_Q_X
 Bxx_R_X
 Bxx_S_X
 Bxx_T_X
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 Bxx_X_X
 Bxx_Y_X
 Bxx_Z_X
 Are Clock Capable I/O's

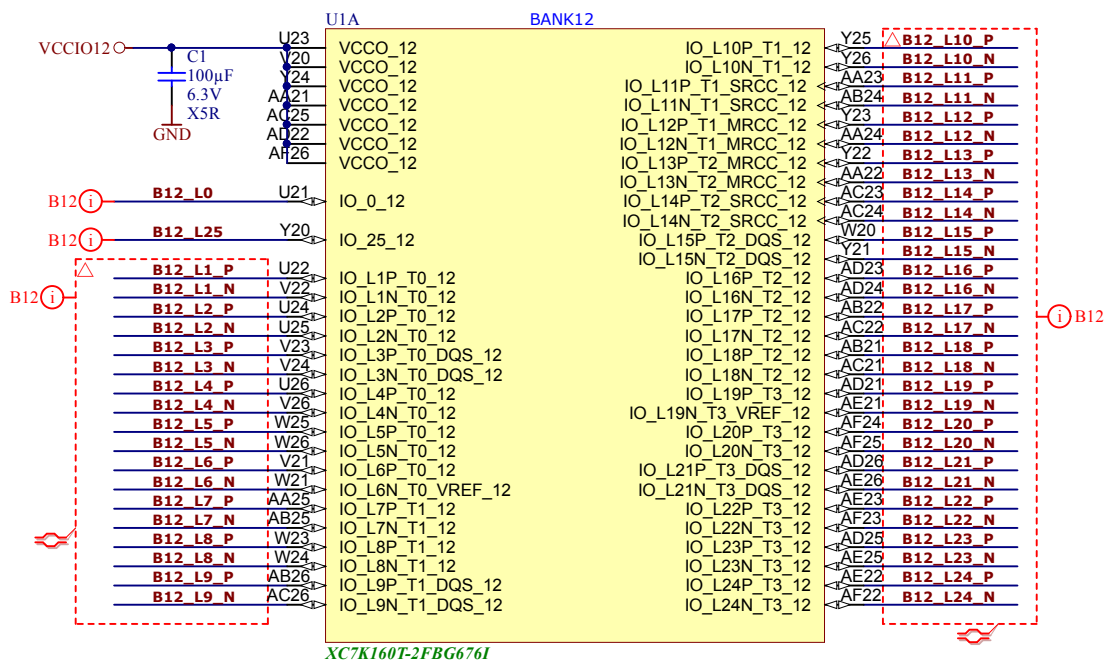


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B12_FIXED (i) △

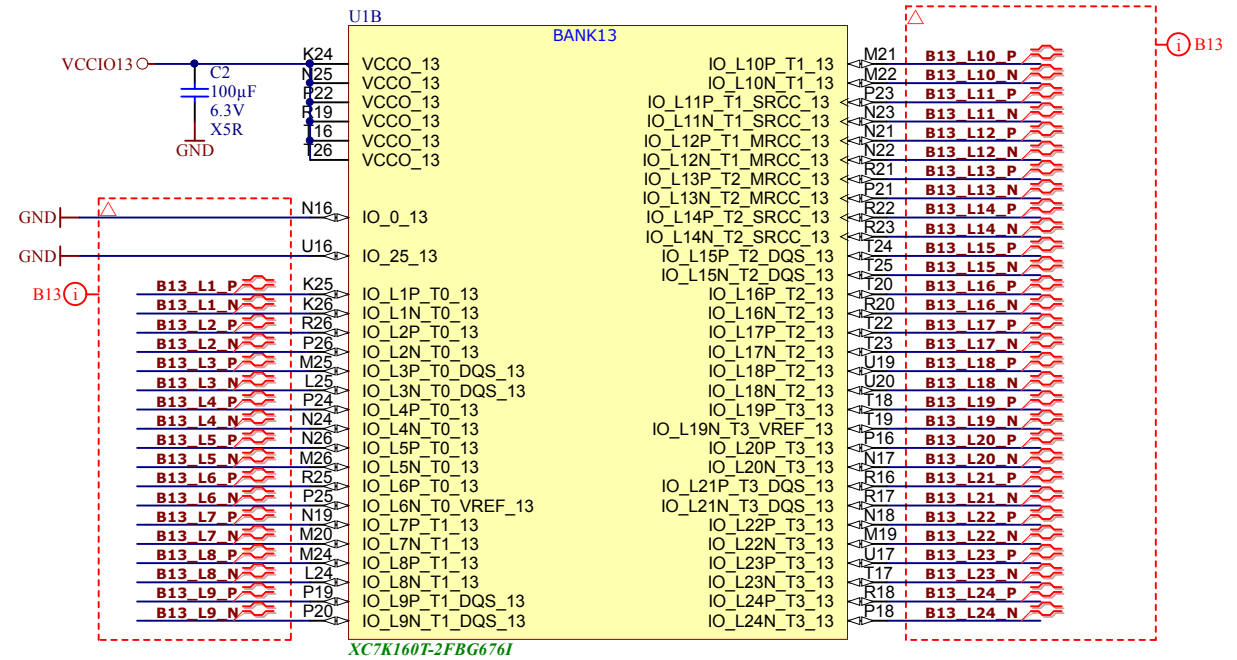
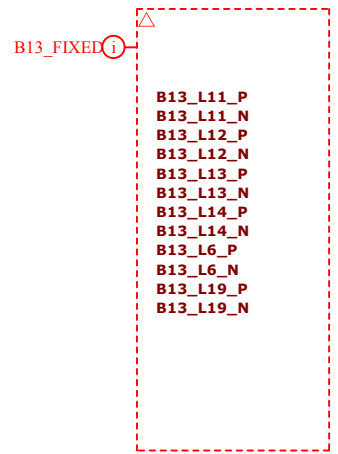

B12 L11 P
B12 L11 N
B12 L12 P
B12 L12 N
B12 L13 P
B12 L13 N
B12 L14 P
B12 L14 N
B12 L19 P
B12 L19 N
B12 L6 P
B12 L6 N

K70T version does not have this bank!



XC7K160T-2FBG676I

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Filename: B13.SchDoc		

1

2

3

4

A

A

B

B

C

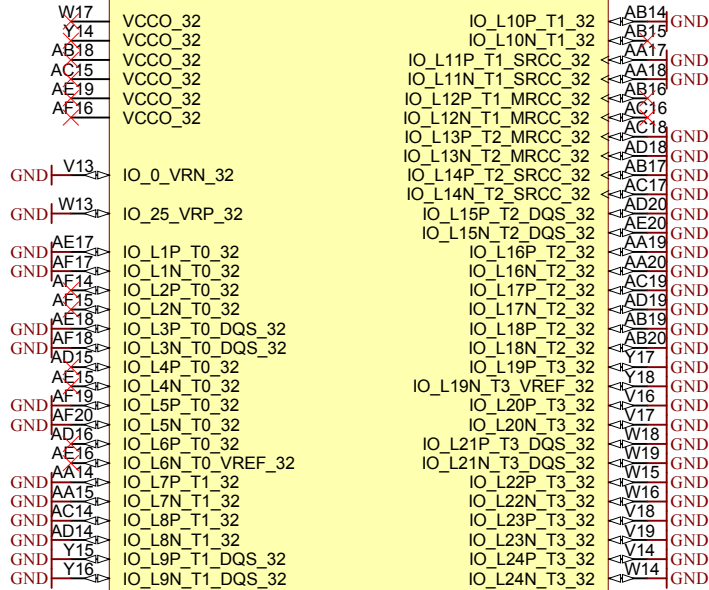
C

D

D

UIF

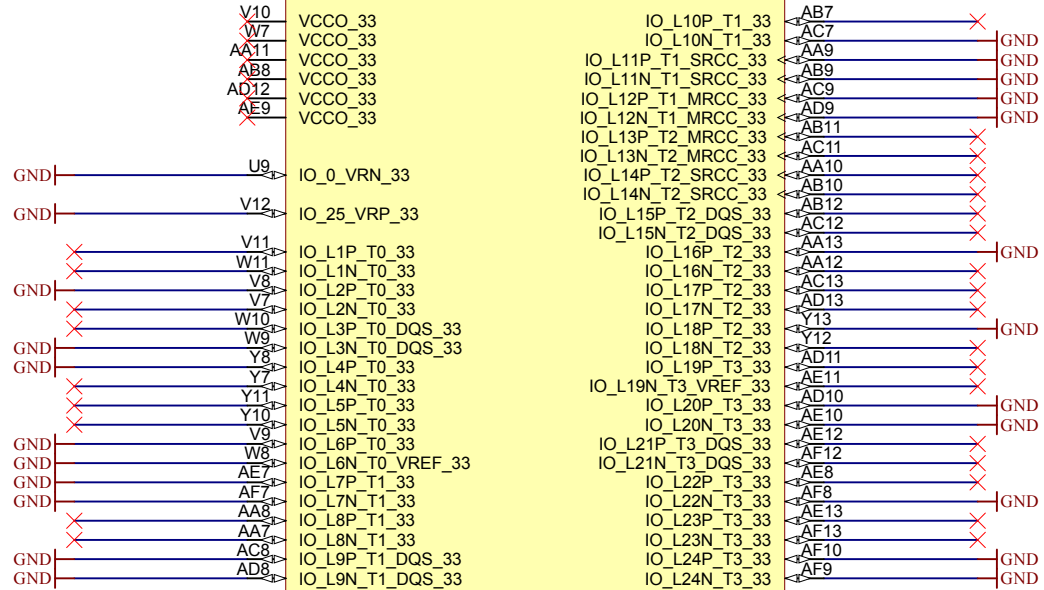
BANK32



XC7K160T-2FBG676I

UIG

BANK33



XC7K160T-2FBG676I



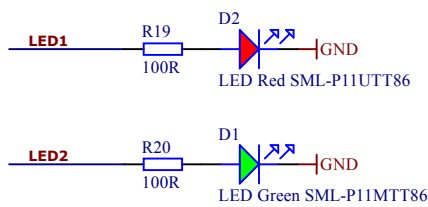
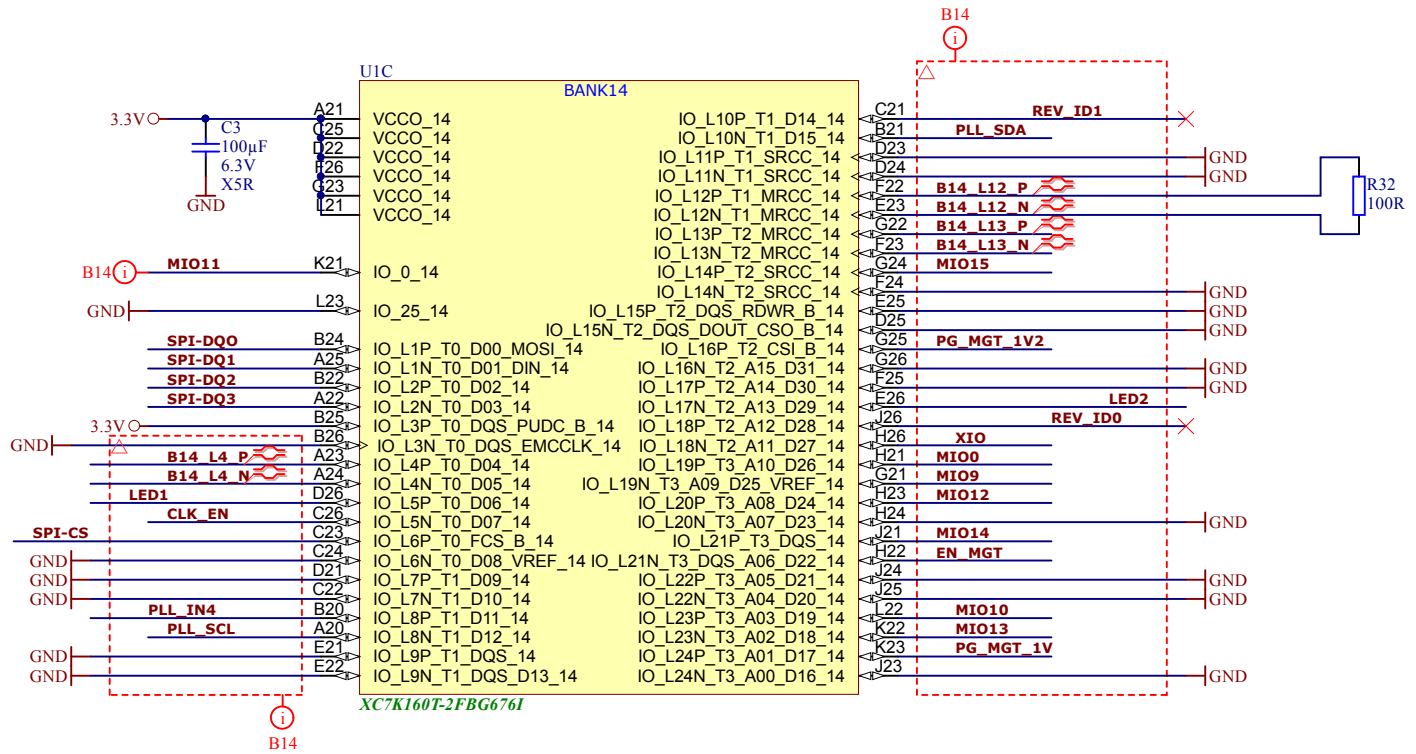
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Filename: B33.SchDoc		

1

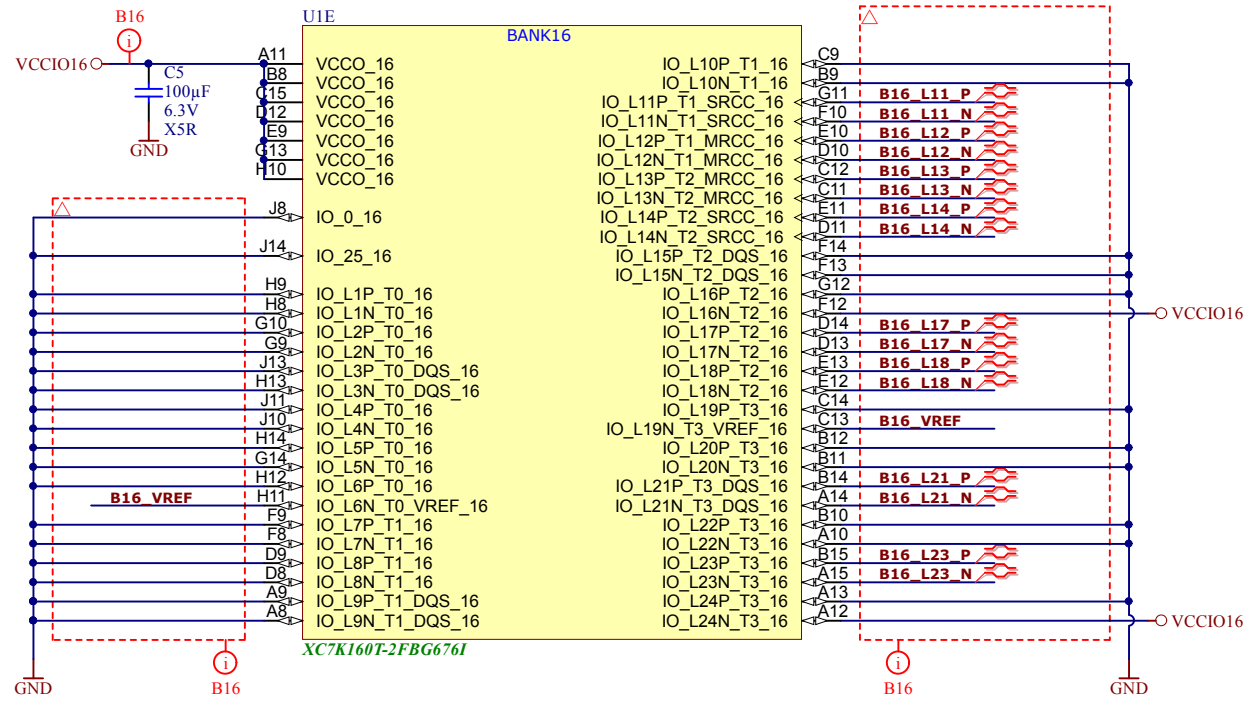
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3

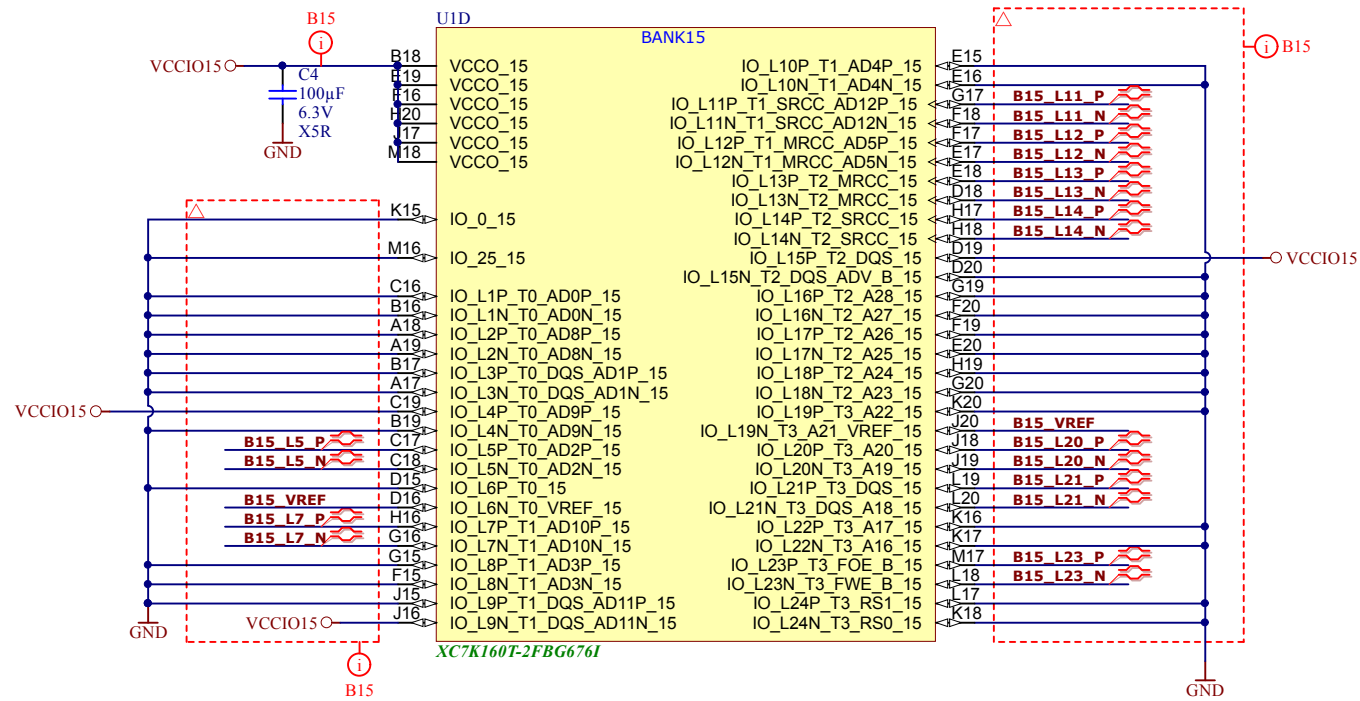
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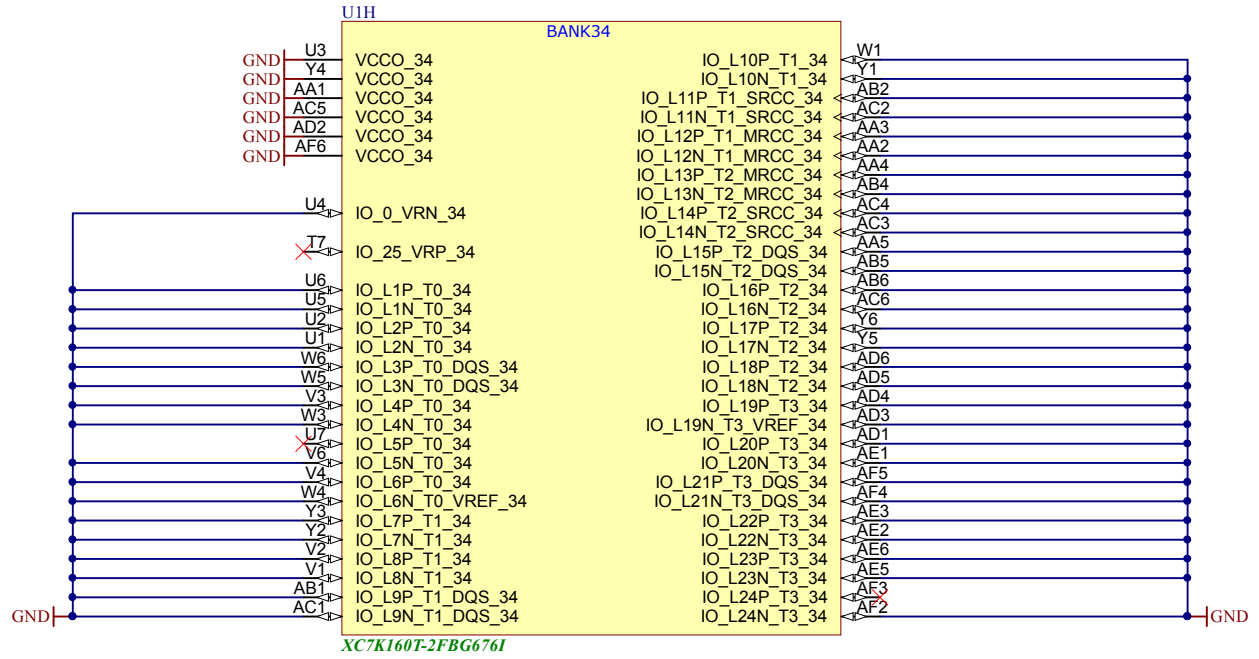
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Date: 2013-11-06		Copyright: 2013 Trenz Electronic GmbH	
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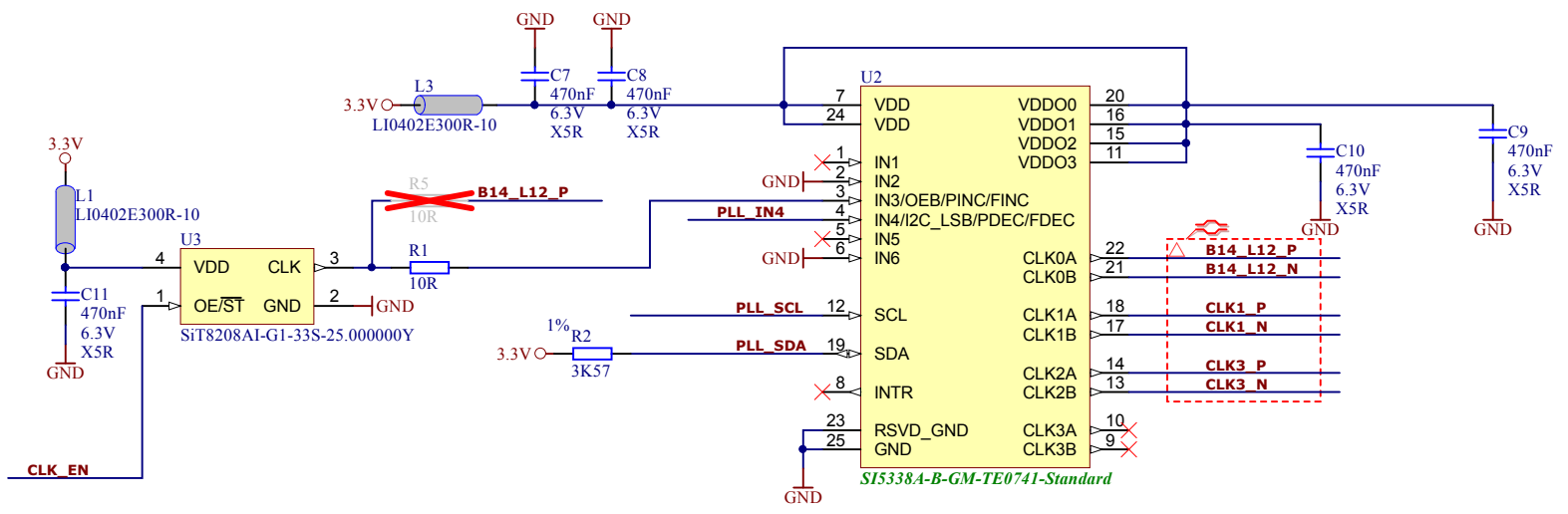
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	Date: 2013-11-06	Copyright: 2013 Trenz Electronic GmbH	Page 6 of 15
	Filename: B16.SchDoc		




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Filename: B15.SchDoc		

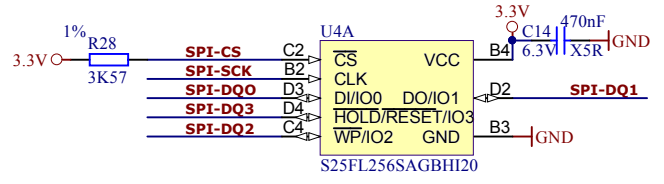
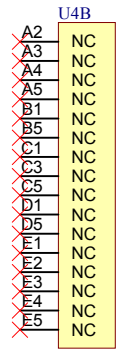
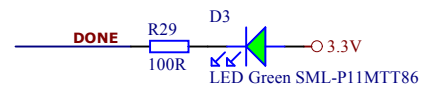
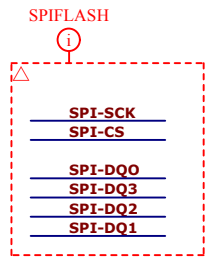
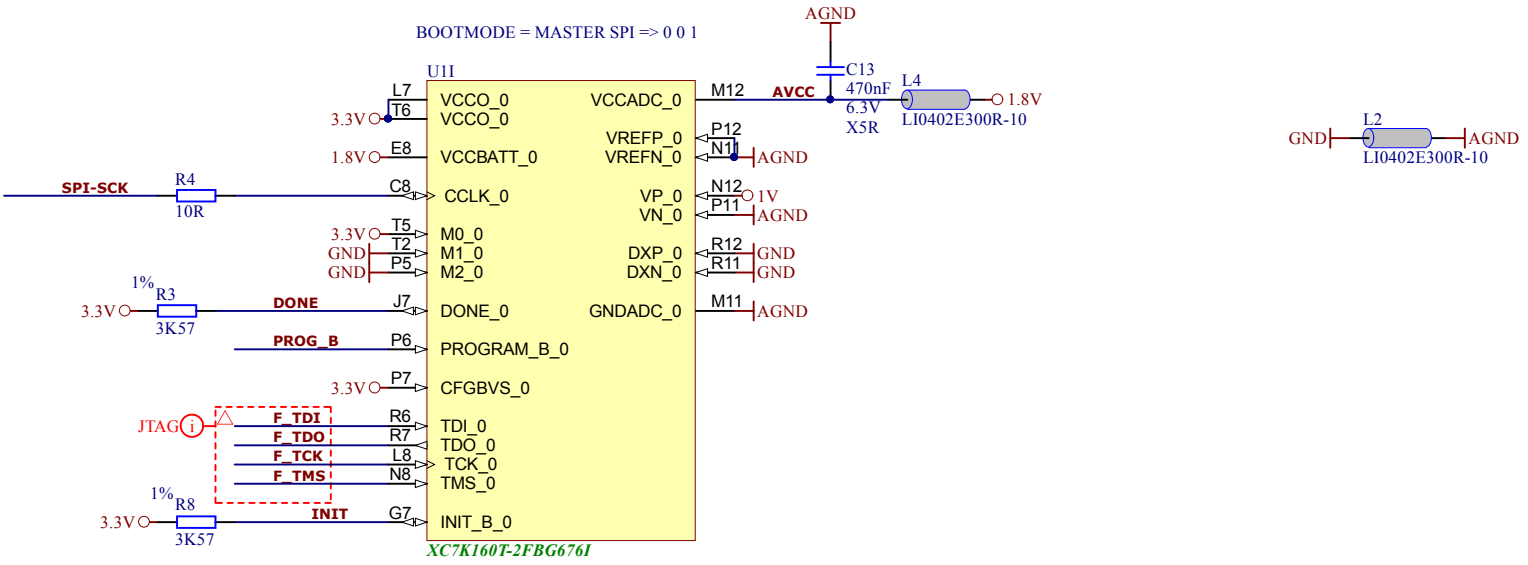


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Filename: B34.SchDoc		

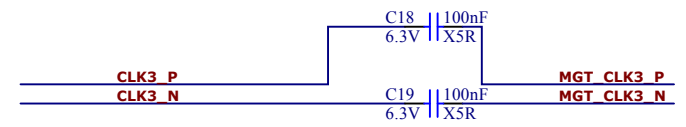
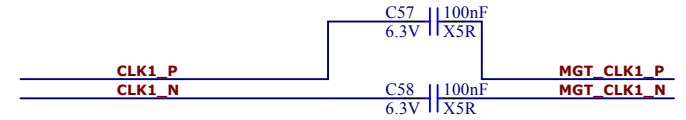
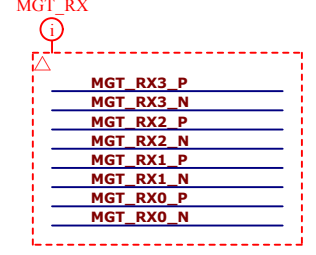
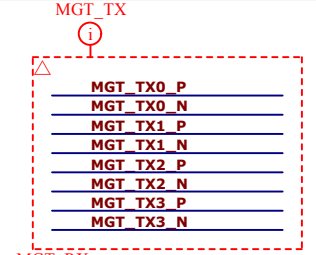
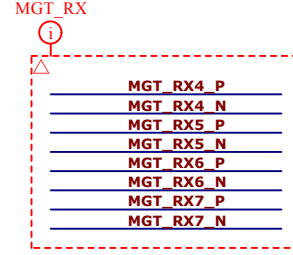
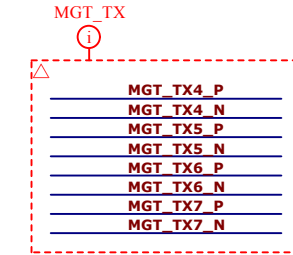
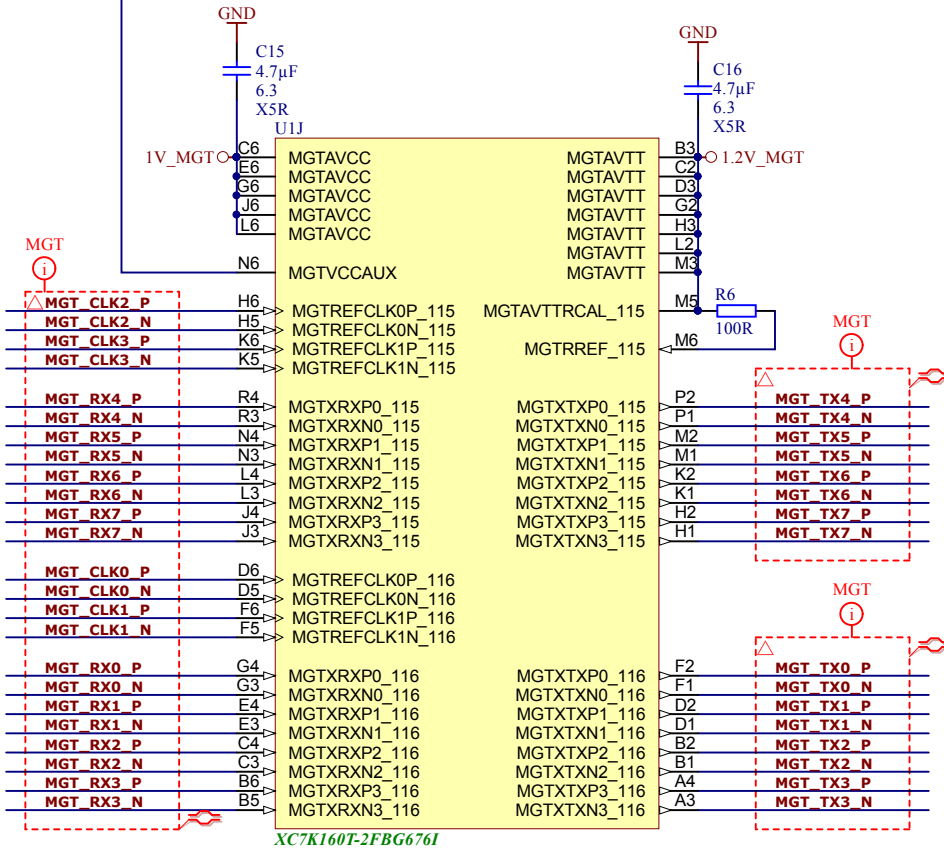
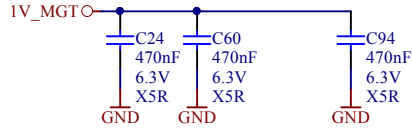
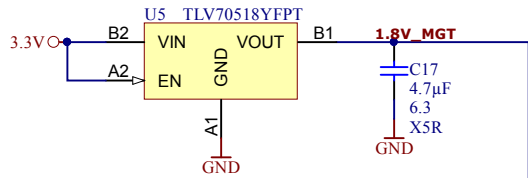


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Filename: Clock.SchDoc			

BOOTMODE = MASTER SPI => 0 0 1

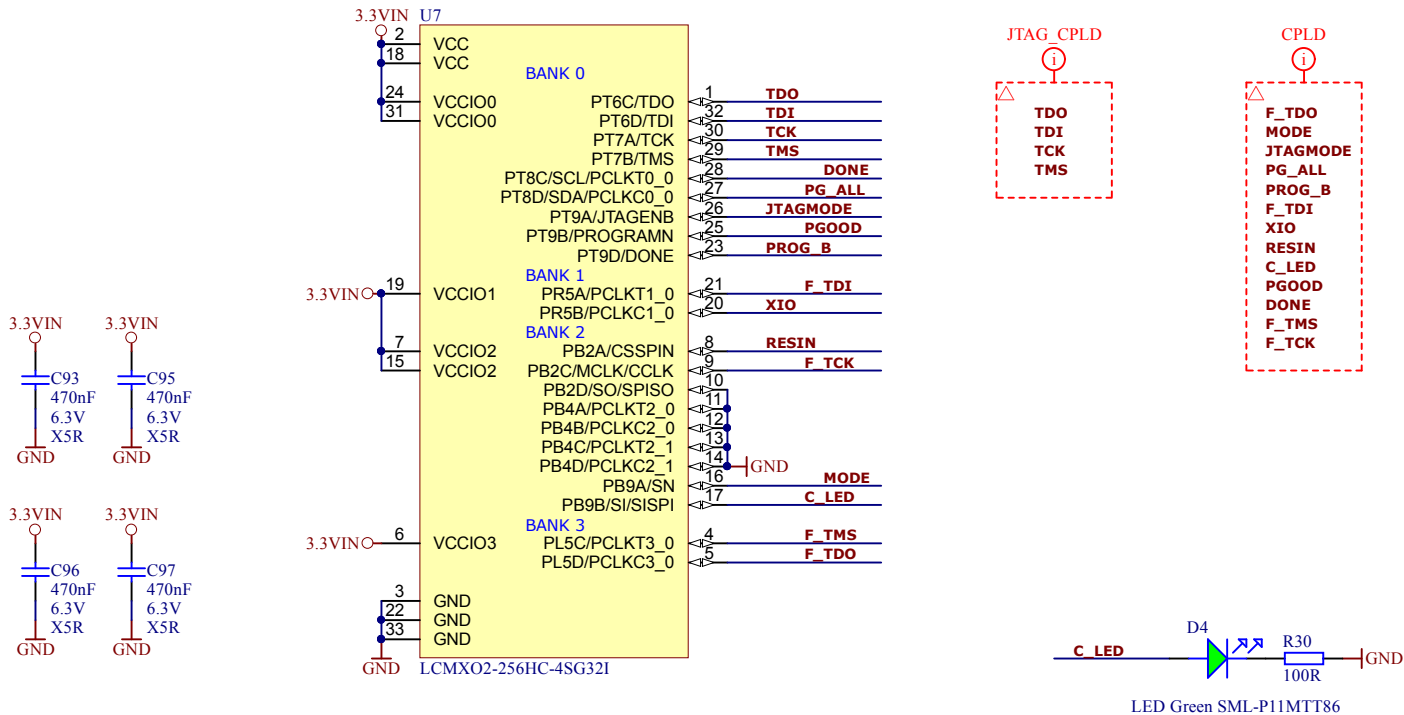


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1

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3

4

A

A

B

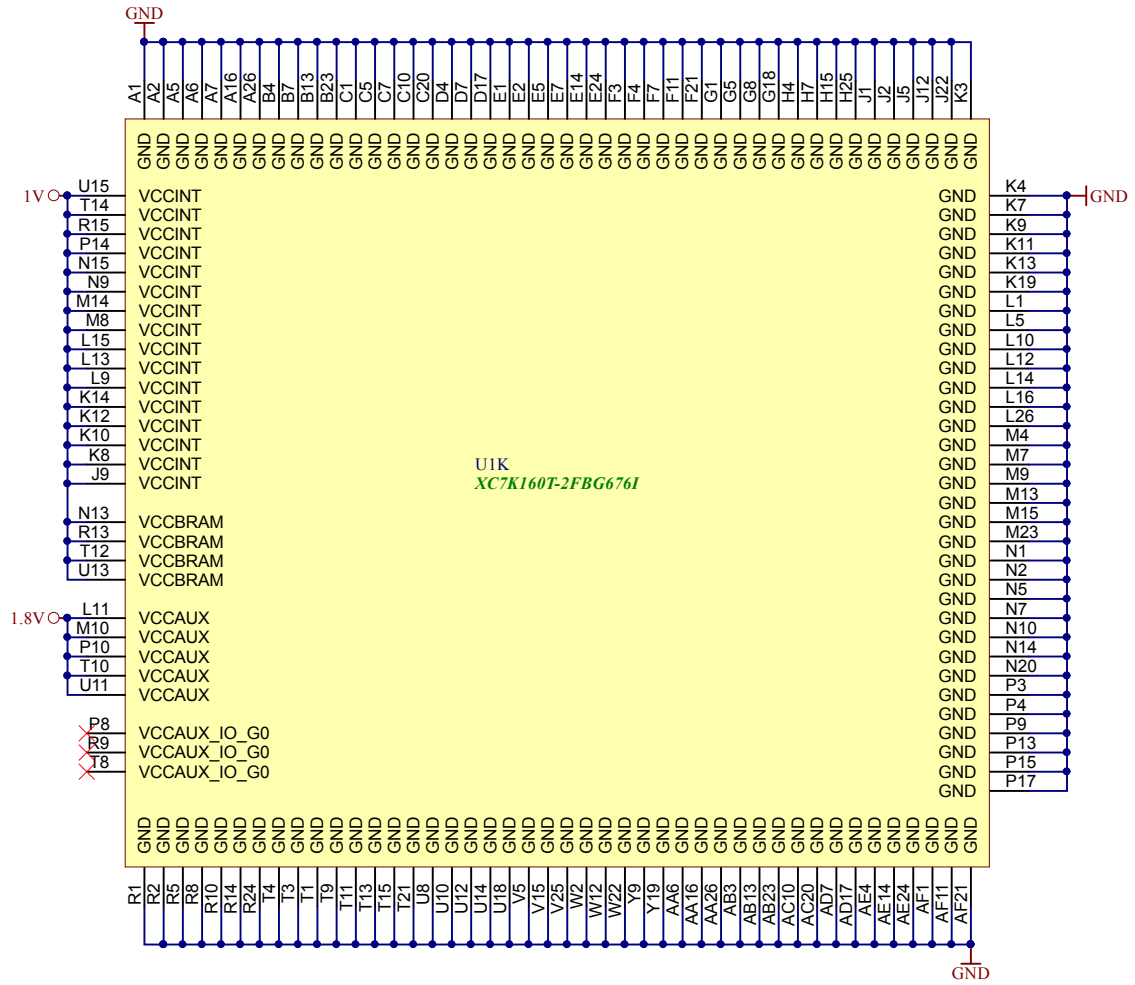
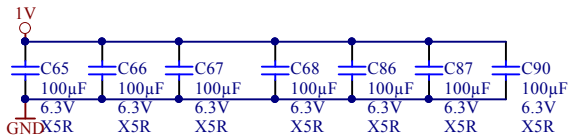
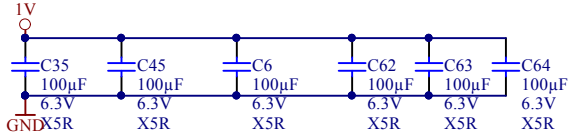
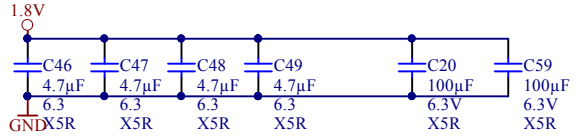
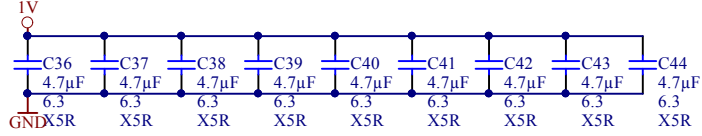
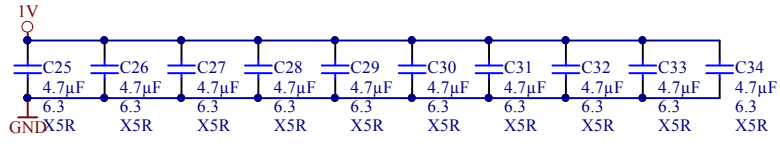
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C

C

D

D



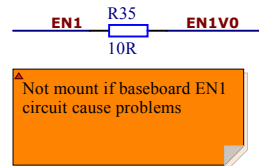
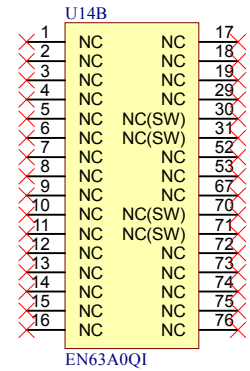
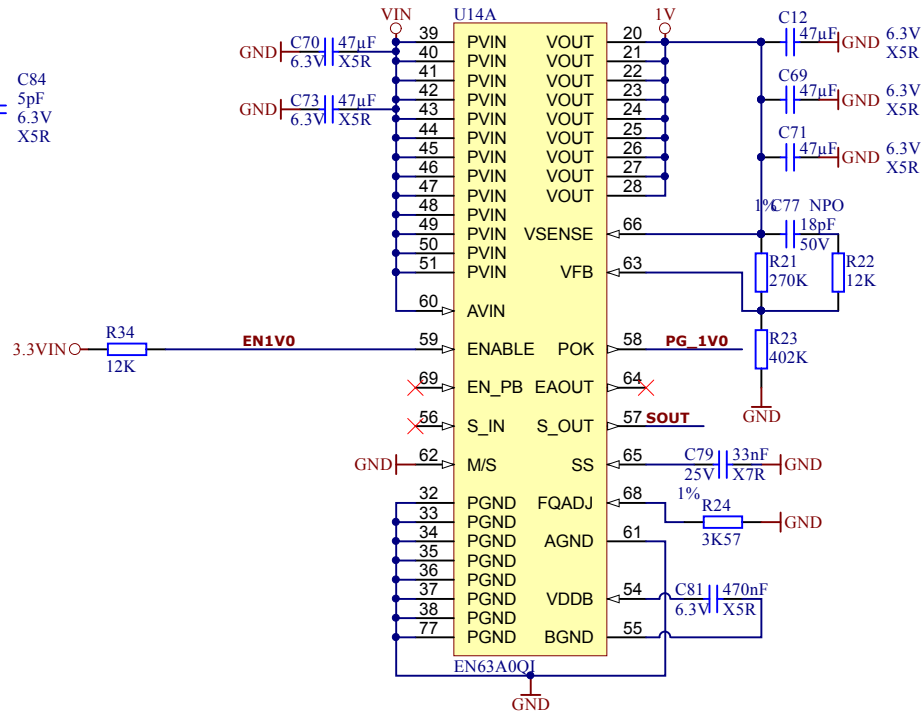
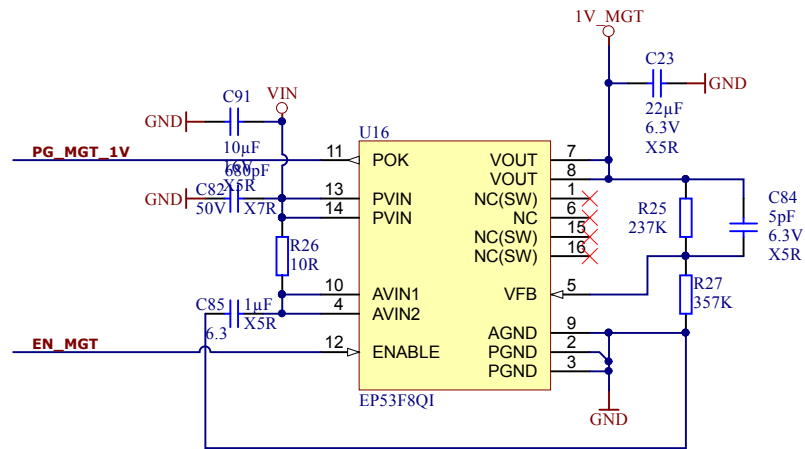
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1

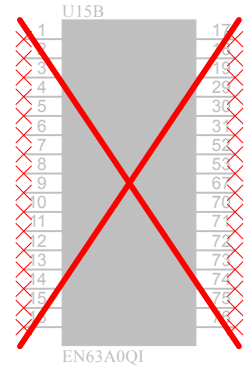
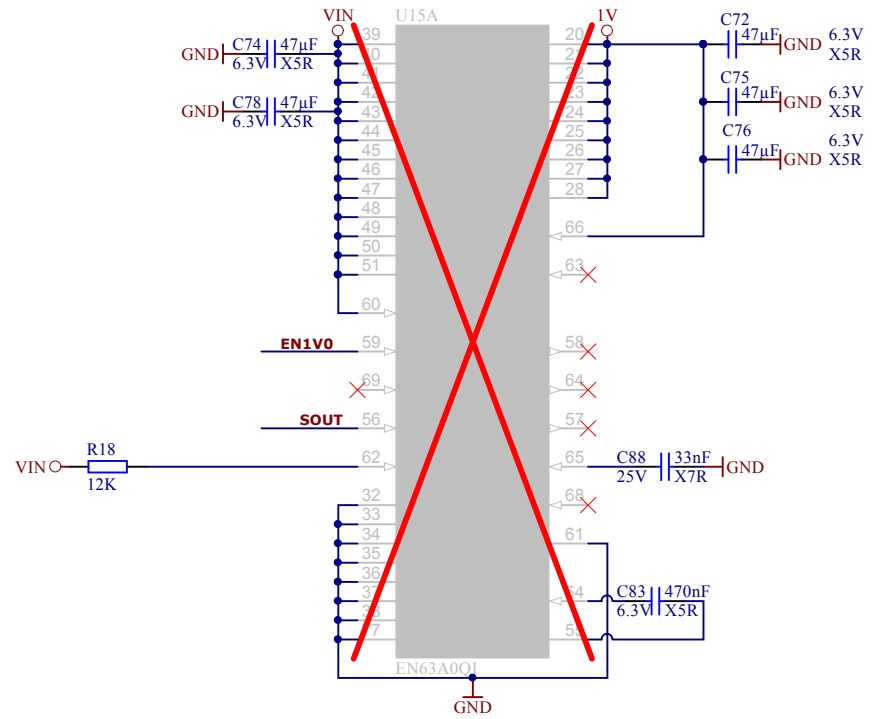
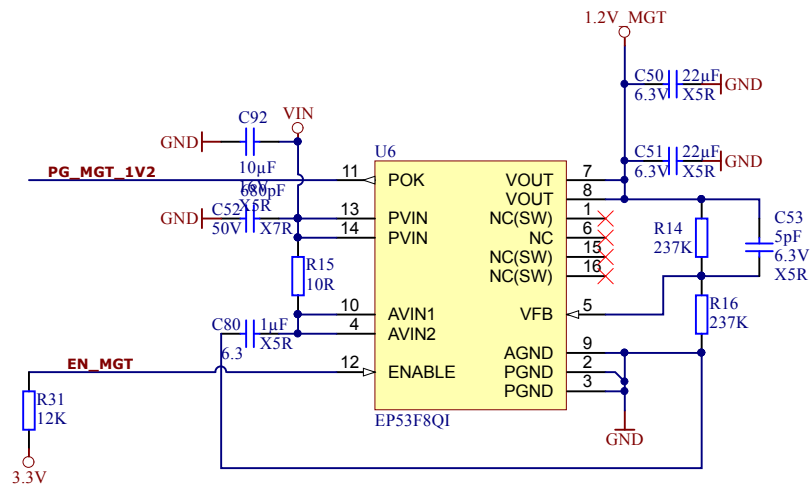
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3

4



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