

U\_FPGA\_IO  
FPGA\_IO.SchDoc

U\_B2B\_Connector  
B2B\_Connector.SchDoc

U\_FPGA\_MGT  
FPGA\_MGT.SchDoc

U\_POWER  
POWER.SchDoc

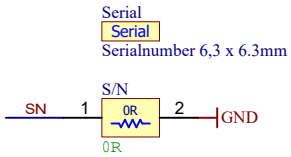
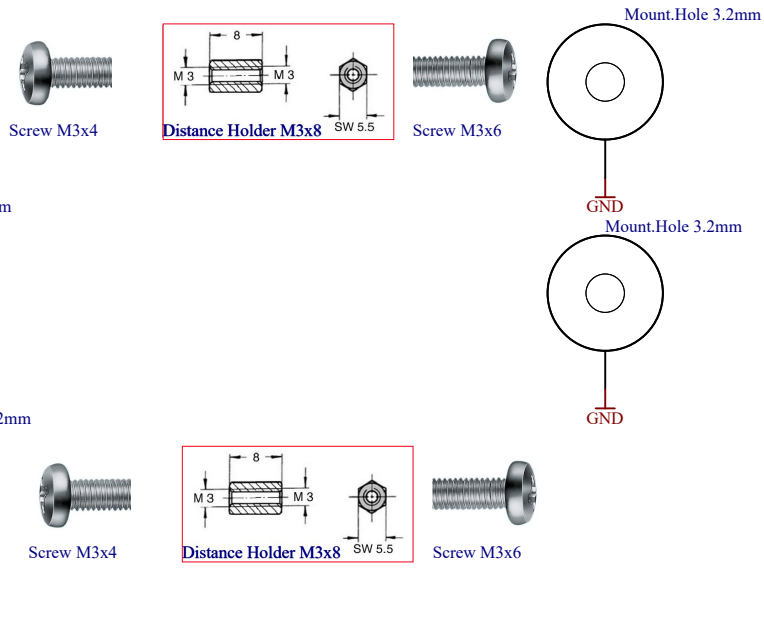
U\_FPGA\_MISC  
FPGA\_MISC.SchDoc

U\_Revision  
Revision\_Changes.SchDoc

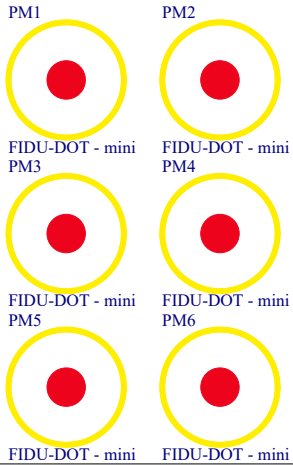
Special notes:

- 
- 

Top of Board



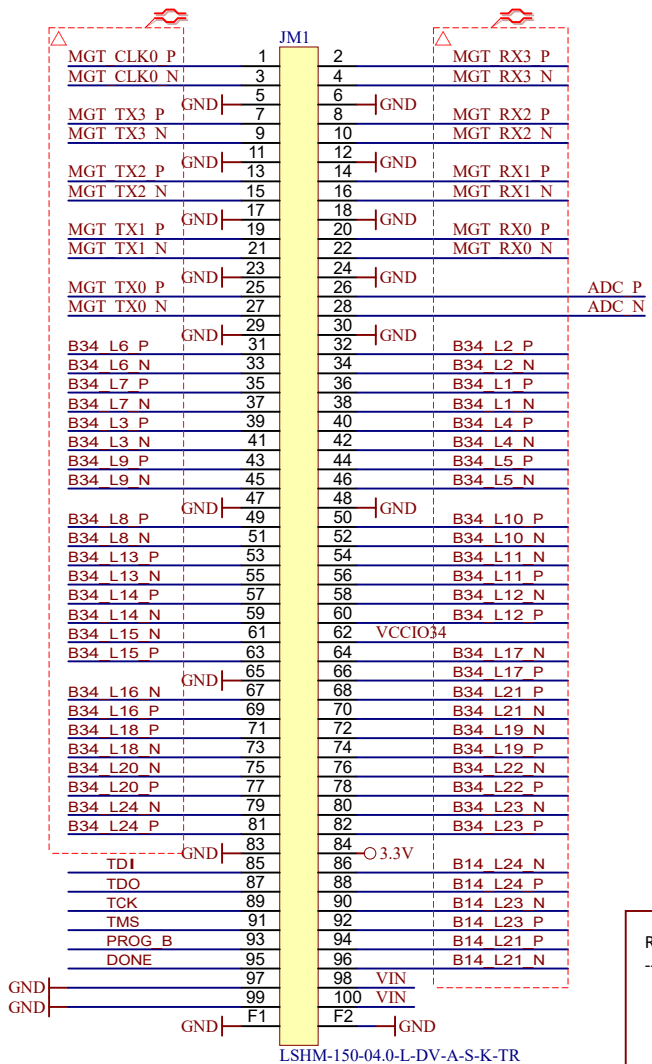
LOGO1  
TE Logo PRINT Layer  
LOGO PRINT



Assembly variant	50-2I
Created by	
Modified by	
Modified at	
SVN Revision	8634



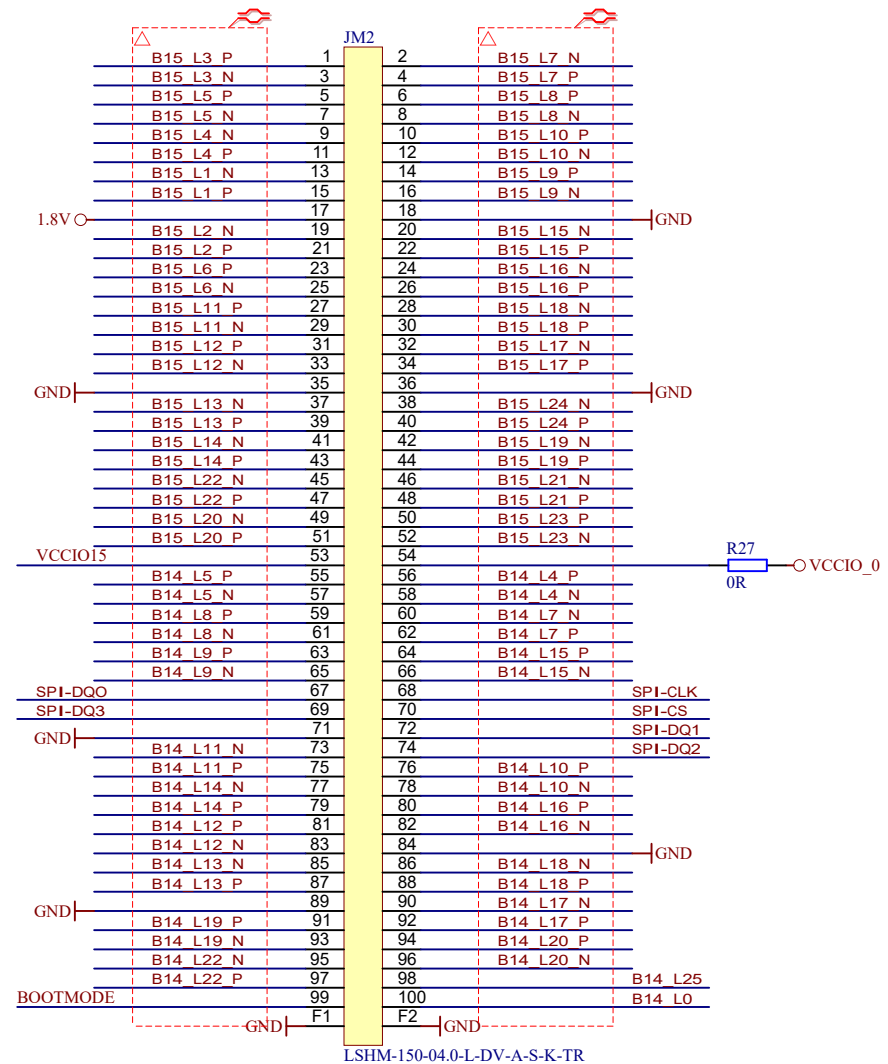
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R21 | R22 | R24 | R25 | R27 | \*JM2 pin 54 function

+	+	+	+	+	3.3V Power OUTPUT
-	-	-	-	-	1.8V Power OUTPUT
-	-	+	-	+	2.5V/3.3V Power Input
-	-	-	+	+	1.8V Power Input
?	?	?	?	-	Not connected

Bank 0  
Bank 14

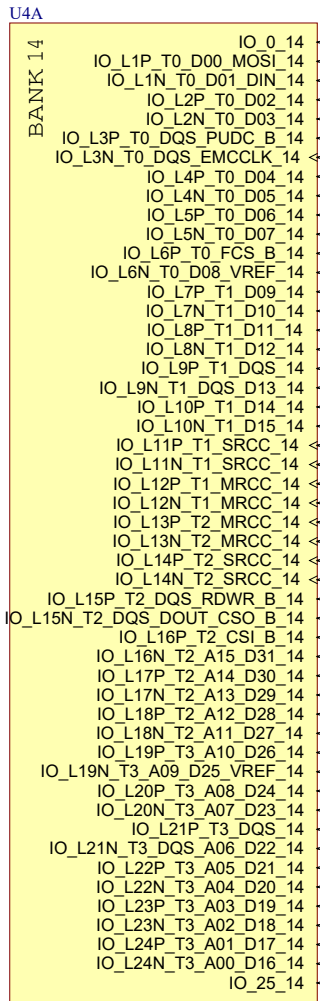


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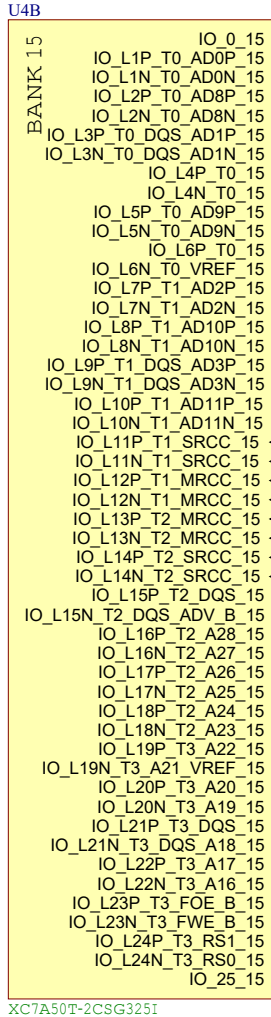
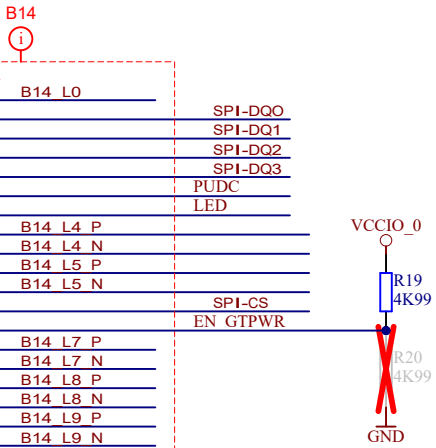
A4 Number: TE0714 50-21 Rev. 03

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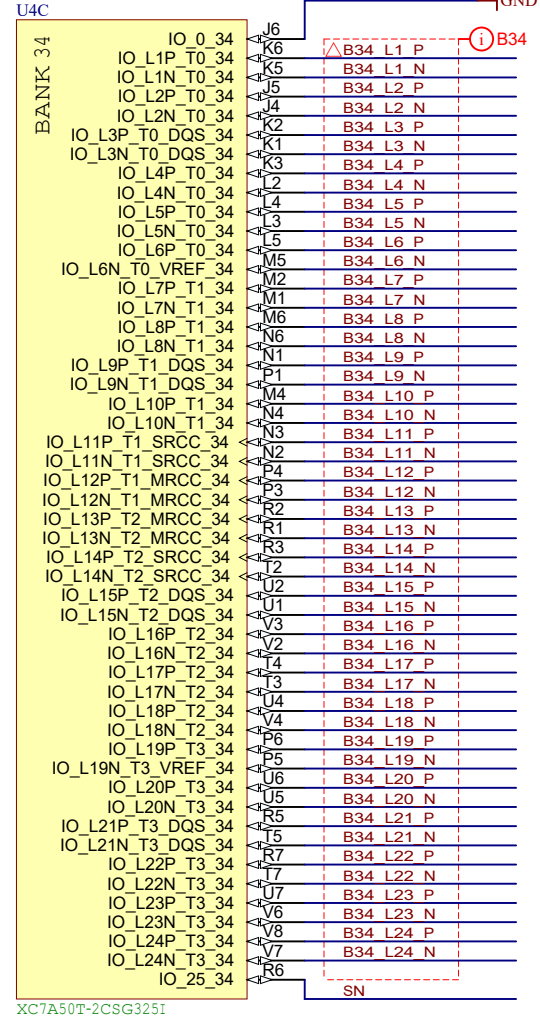
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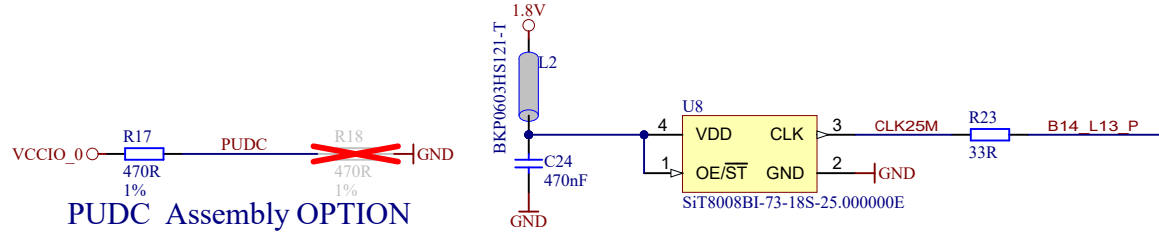
XC7A50T-2CSG325I



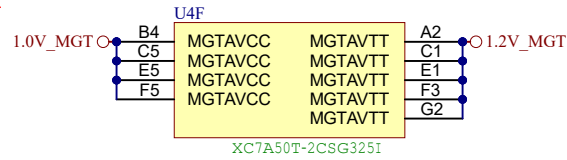
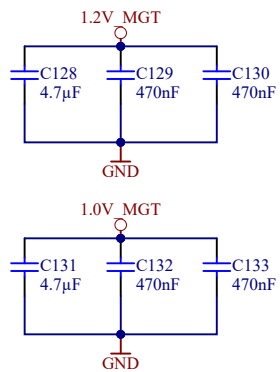
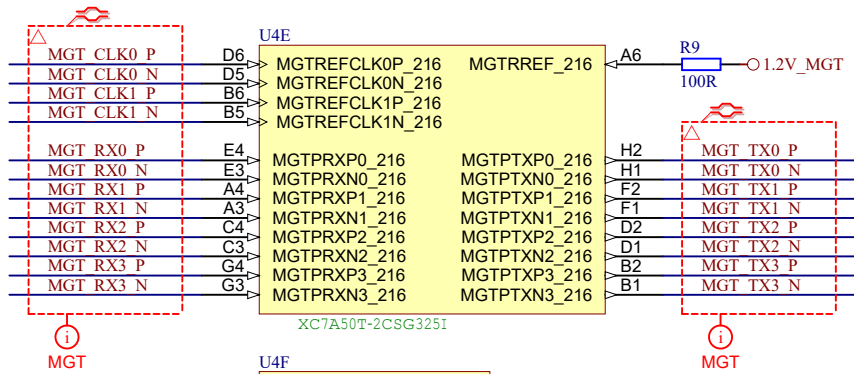
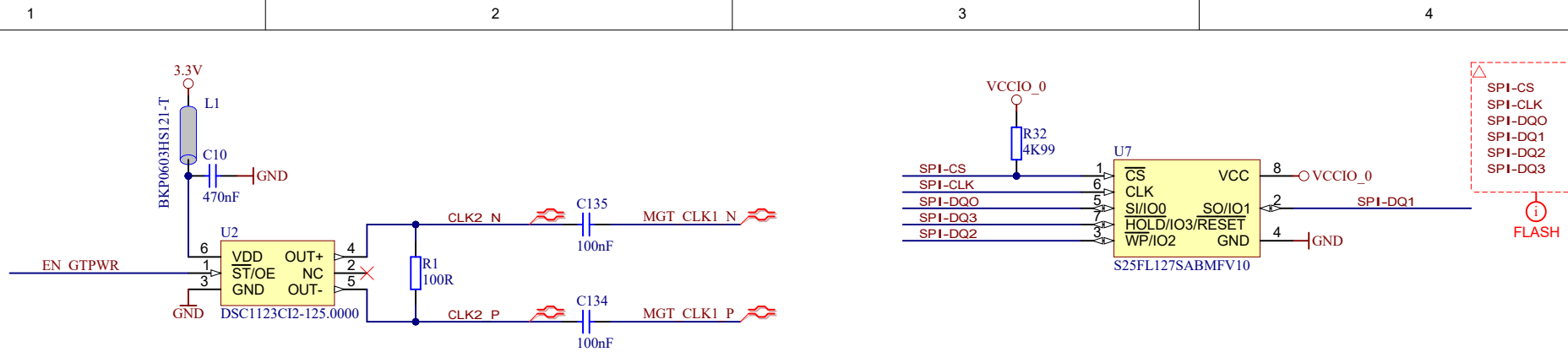
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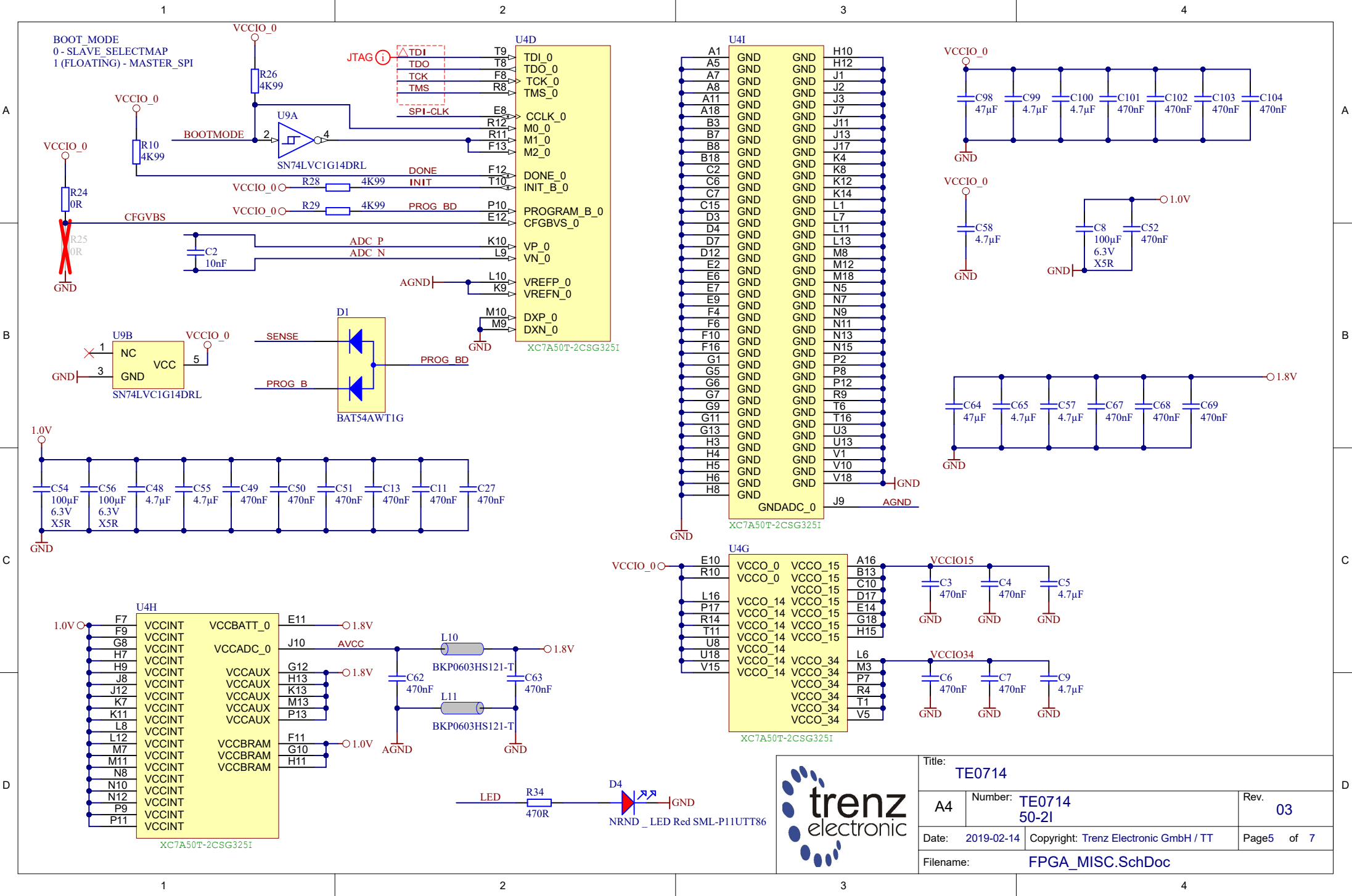
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Changes REV 02:


- 1. Added 0 ohm strap option to supply VCCIO0 on B2B connector
- 2. Added PCB Revision sense support. PCB Revision readout possible from HDL Design
- 3. Updated FPGA pin PROG\_B connection. TPS3805H33 push-pull output RESET\_N not affected on baseboard circuit, connected to PROG\_B.
- 4. C8, C54, C56 updated to 100uF for variant 50-2I
- 5. Added testpoints

Changes REV 02A (12.2018):

- 1. New FLASH memory U7 S25FL127SABMFV10

Changes REV 03:

- 1) Changed obsolete component U3 (LXDC2HL18A-052 -> EP5357HUI)
- 2) DXP/DXN connected to GND (recommendation UG475, p31)
- 3) Added serial number to silk
- 4) Changed obsolete component Q1 (TPS27082LDDCR ->TPS27081ADDCR )
- 5) Full update LIB
- 6) Optimized testpoints placement

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