## Features

- **Low Current Consumption: $I_{DD}$ < 100 µA**
- **RC Oscillator**
- **Internal Reset During Power-up and Supply Voltage Drops (POR)**
- **“Short” Trigger Window for Active Mode, “Long” Trigger Window for Sleep Mode**
- **Cyclical Wake-up of the Microcontroller in Sleep Mode**
- **Trigger Input**
- **Single Wake-up Input**
- **Reset Output**
- **Enable Output**

Pb Lead Free

# Digital Window Watchdog Timer

# U5021M

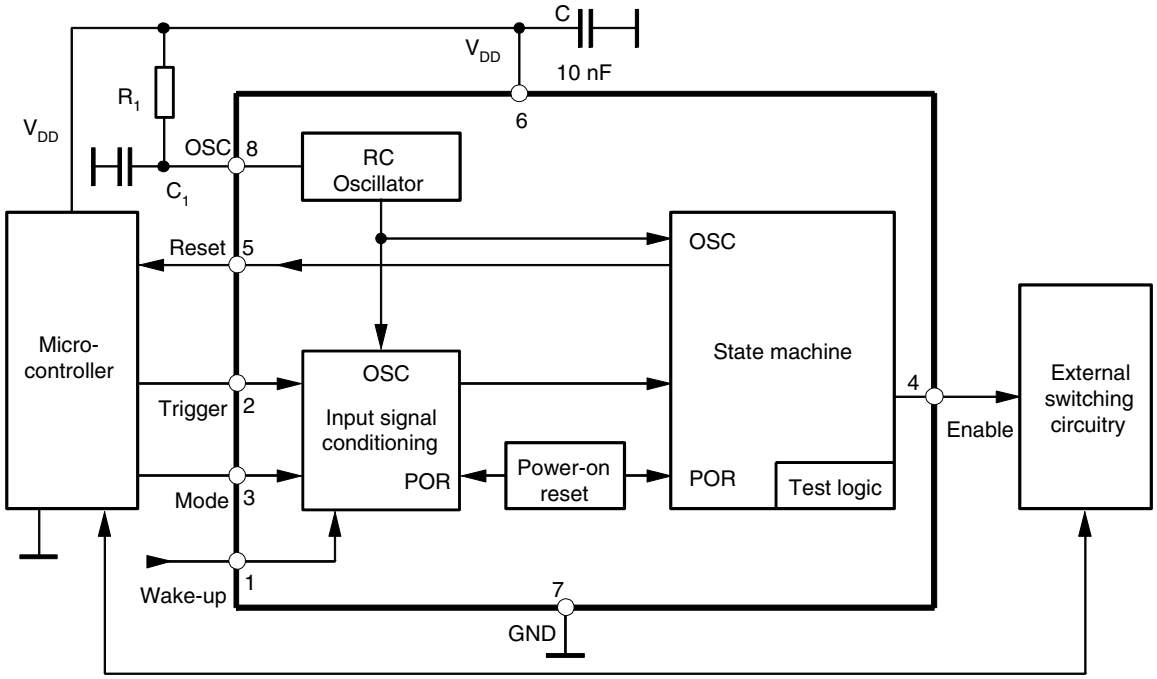
## 1. Description

The digital window watchdog timer, U5021M, is a CMOS integrated circuit. In applications where safety is critical, it is especially important to monitor the microcontroller. Normal microcontroller operation is indicated by a cyclically transmitted trigger signal, which is received by a window watchdog timer within a defined time window.

A missing or a wrong trigger signal causes the watchdog timer to reset the microcontroller. The IC is tailored for microcontrollers which can work in both full-power and sleep mode. With an additional voltage monitoring (power-on reset and supply voltage drop reset), the U5021M offers a complete monitoring solution for microsystems in automotive and industrial applications.

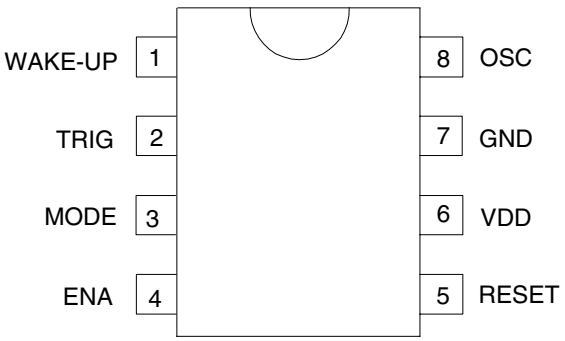
Rev. 4756D–AUTO–11/05

**Figure 1-1.** Block Diagram with External Ciruit




## 2. Pin Configuration

**Figure 2-1.** Pinning SO8



# 3. Pin Description

| Pin | Symbol | Function |
|---|---|---|
| 1 | WAKE-UP | Wake-up input (pull-down resistor)<br>There is one digitally debounced wake-up input. During the long watchdog window, each signal slope at the input initiates a reset pulse at pin 5. |
| 2 | TRIG | Trigger input (pull-up resistor)<br>It is connected to the microprocessor's trigger signal. |
| 3 | MODE | Mode input (pull-up resistor)<br>The processor's mode signal initiates the switchover between the long and the short watchdog time. |
| 4 | ENA | Enable output (push-pull)<br>It is used for the control of peripheral components. It is activated after the processor triggers three times correctly. |
| 5 | RESET | Reset output (open drain)<br>Resets the processor in the case of a trigger error or if a wake-up pulse occurs during the long watchdog period. |
| 6 | VDD | Supply voltage |
| 7 | GND | Ground, reference voltage |
| 8 | OSC | RC oscillator |

# 4. Functional Description

## 4.1 Supply Voltage, Pin 6

The U5021M requires a stabilized supply voltage $V_{DD}$ = 5 V ±5% to comply with its electrical characteristics.

An external buffer capacitor of C = 10 nF may be connected between pin 6 and GND.

## 4.2 RC Oscillator, Pin 8

The clock frequency, f, can be adjusted by the components $R_1$ and $C_1$ according to the formula:

$$f = \frac{1}{t}$$

where $t = 1.35 + 1.57\ R_1\ (C_1 + 0.01)$

$R_1$ in kΩ, $C_1$ in nF and t in µs

The clock frequency determines all time periods of the logic part as shown in the table "Electrical Characteristics" under the subheading "Timing" on page 9. With an appropriate component selection, the clock frequency, f, is nearly independent of the supply voltage as shown in Figure 4-1 on page 4.

Frequency tolerance $\Delta f_{max}$ = 10% with $R_1$ ±1%, $C_1$ = ±5%

**Figure 4-1.** Period t versus $R_1$, at $C_1$ = 500 pF

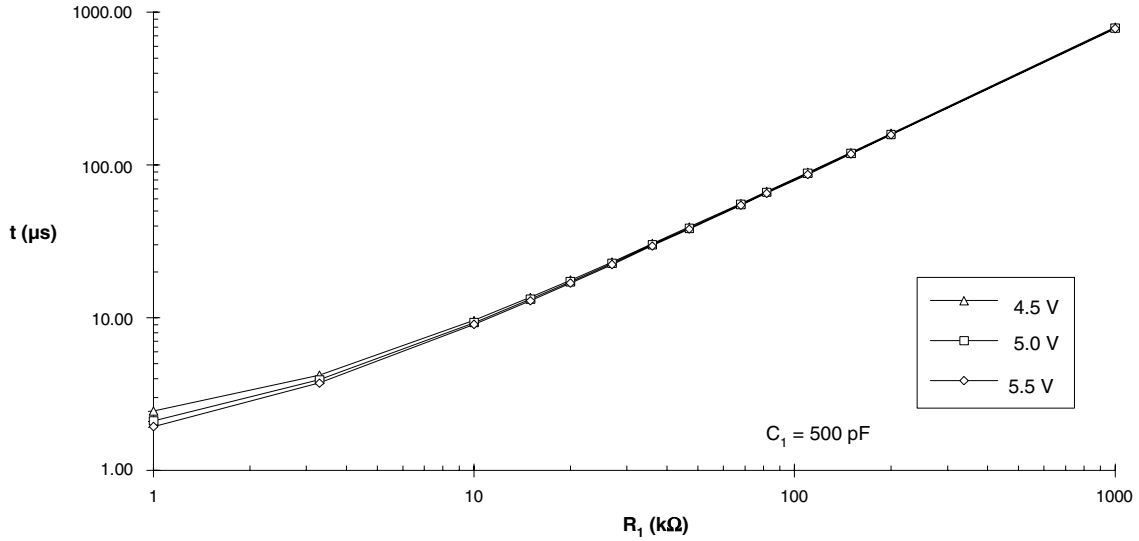



**Figure 4-2.** Power-on Reset and Switch-over Mode


## 4.3 Supply Voltage Monitoring, Pin 5

During ramp-up of the supply voltage and in the case of supply-voltage drops the integrated power-on reset (POR) circuitry sets the internal logic to a defined basic status and generates a reset pulse at the reset output, pin 5. A hysteresis in the POR threshold prevents the circuit from oscillating. During ramp-up of the supply voltage, the reset output stays active for a specified period of time ($t_0$) in order to bring the microcontroller into its defined reset status (see Figure 4-2). Pin 5 has an open-drain output.

## 4.4 Switch-over Mode Time, Pin 3

The switch-over mode time enables the synchronous operation of microcontroller and watchdog. When the power-on reset time has elapsed, the watchdog has to be switched to monitoring mode by the microcontroller by a “low” signal transmitted to the mode pin (pin 3) within the time-out period, $t_1$. If the low signal does not occur within $t_1$ (see Figure 4-2), the watchdog generates a reset pulse, $t_6$, and $t_1$ starts again. Microcontroller and watchdog are synchronized with the switch-over mode time, $t_1$, each time a reset pulse is generated.

## 4.5 Microcontroller in Active Mode

### 4.5.1 Monitoring with the “Short” Trigger Window

After the switch-over mode the watchdog operates in short watchdog mode and expects a trigger pulse from the microcontroller within the defined time window, $t_3$, (enable time). The watchdog generates a reset pulse which resets the microcontroller if

- the trigger pulse duration is too long
- the trigger pulse is within the disable time, $t_2$
- there is no trigger pulse

Figure 4-3 shows the pulse diagram with a missing trigger pulse.

**Figure 4-3.** Pulse Diagram with no Trigger Pulse During the Short Watchdog Time

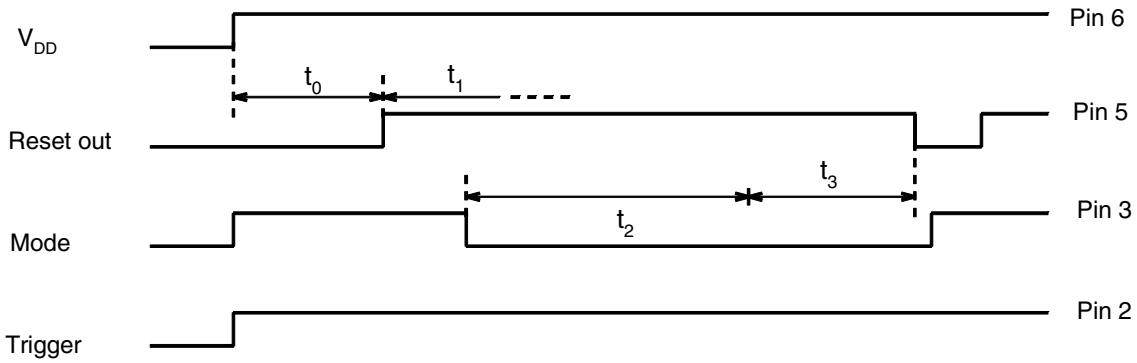



Figure 4-4 on page 6 shows a correct trigger sequence. The positive edge of the trigger signal starts a new monitoring cycle with the disable time, $t_2$. To ensure correct operation of the microcontroller, the watchdog needs to be triggered three times correctly before it sets its enable output. This feature is used to activate or deactivate safety-critical components which have to be switched to a certain condition (emergency status) in the case of a microcontroller malfunction. As soon as there is an incorrect trigger sequence, the enable signal is reset and it takes a sequence of three correct triggers before enable is active.

## 4.6 Microcontroller in Sleep Mode

### 4.6.1 Monitoring with the “Long” Trigger Window

The long watchdog mode allows cyclical wake-up of the microcontroller during sleep mode. As in short watchdog mode, there is a disable time, $t_4$, and an enable time, $t_5$, in which a trigger signal is accepted. The watchdog can be switched from the short trigger window to the long trigger window with a “high” potential at the mode pin (pin 3). In contrast to the short watchdog mode, the time periods are now much longer and the enable output remains inactive so that other components can be switched off to effect a further decrease in current consumption. As soon as a wake-up signal at the wake-up input (pins 1) is detected, the long watchdog mode ends, a reset pulse wakes-up the sleeping microcontroller and the normal monitoring cycle starts with the mode switch-over time.

**Figure 4-4.** Pulse Diagram of a Correct Trigger Sequence During the Short Watchdog Time

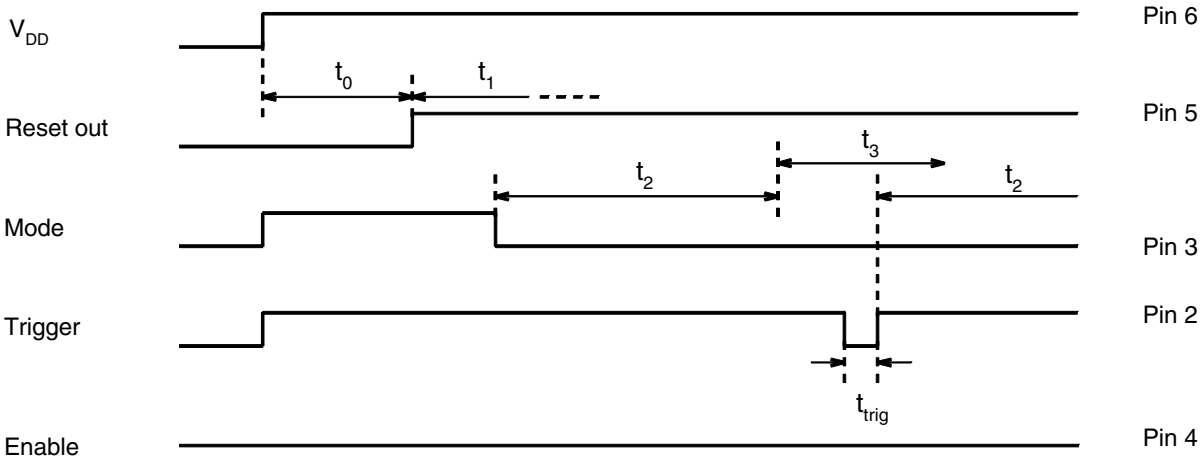
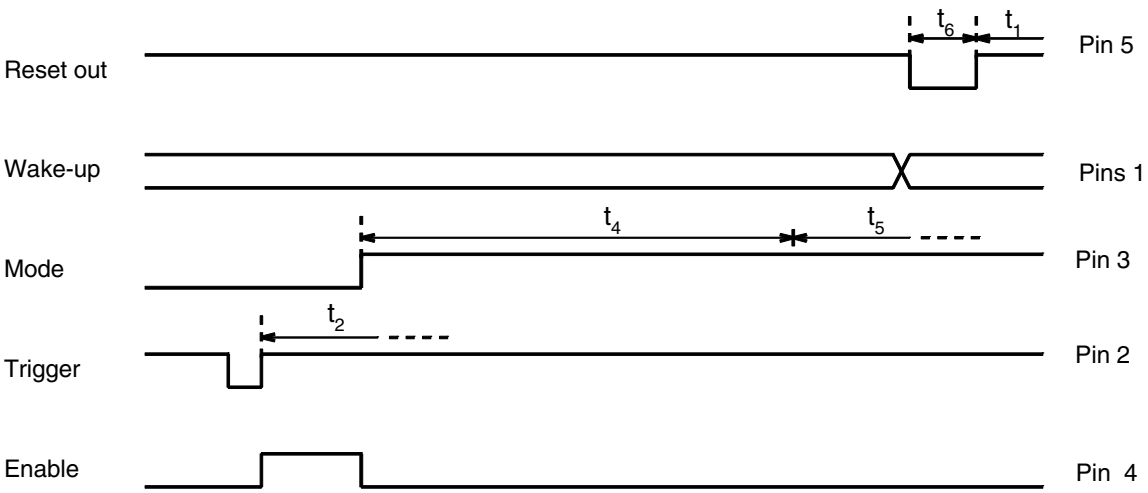



Figure 4-5 shows the switch-over from the short to the long watchdog mode. The wake-up signal during the enable time, $t_5$, activates a reset pulse, $t_6$.

The watchdog can be switched back from the long to the short watchdog mode with a low potential at the mode pin (pin 3).

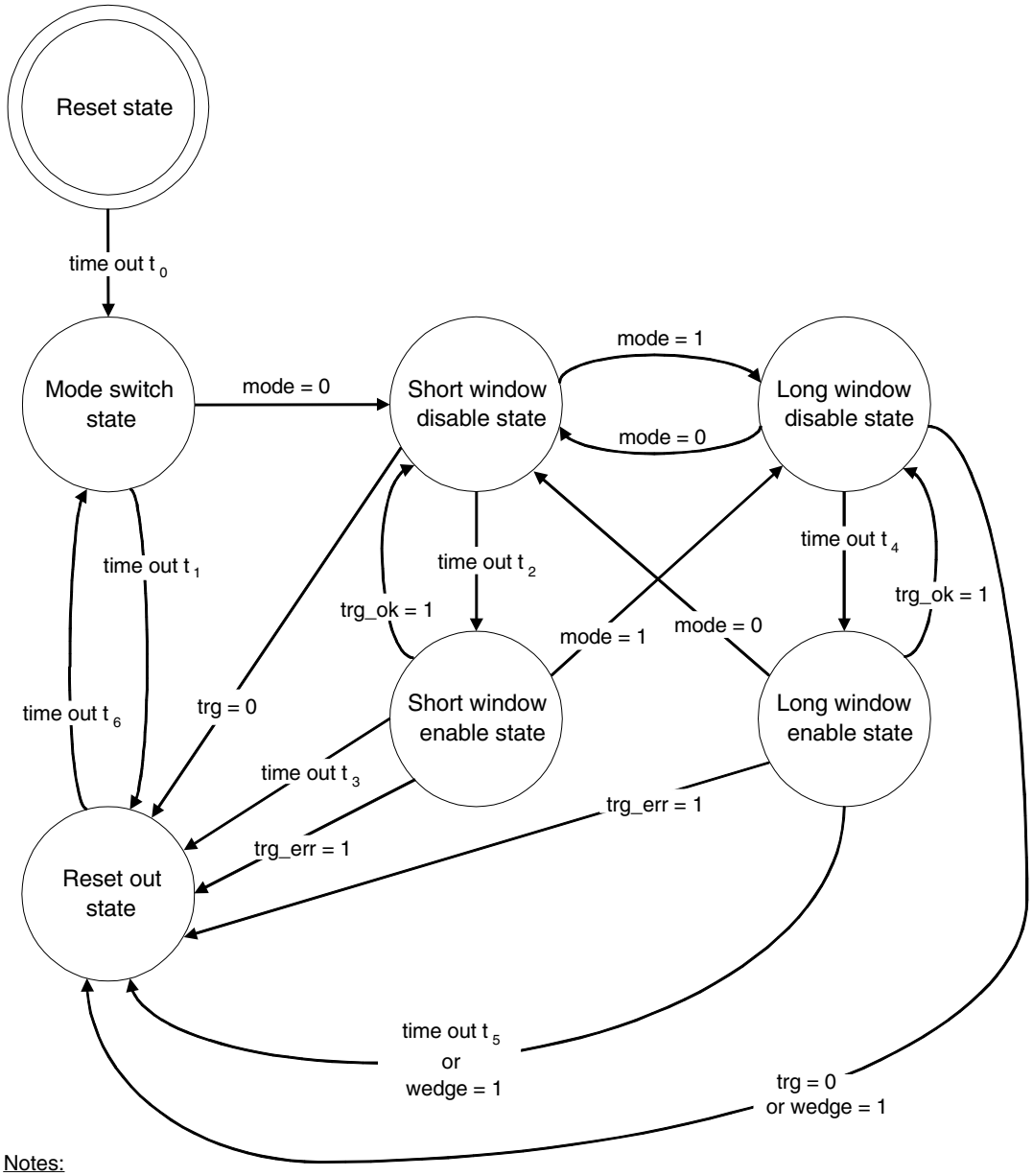
**Figure 4-5.** Pulse Diagram of the Long Watchdog Time




## 5. State Diagram

The kernel of the watchdog is a finite state machine. Figure 5-1 shows the state diagram with all possible states and transmissions. Many transmissions are controlled by an internal timer. The numbers for the time-outs are the same as on the pulse diagrams.

**Figure 5-1.** State Diagram




Notes:

- "mode" and "trg" are the debounced input signals from the pins MODE and TRG
- trg_ok = 1 after the rising edge of the trg signal
- trg_err = 1 when the trg signal low period is too long
- wedge = 1 after detecting the debounced changing of a signal level from the WUP pin
- Every state change restarts the internal timer

- If a state change is generated from an external debounced pin signal exactly one clock cycle before the internal timer initiates a state change itself, the state machine changes its state twice. The first state change is created by the signal change, and the second by the timeout of the internal timer. This occurs due to the timer getting its reset one clock cycle after a state change.

## 6. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | 6.5 | V |
| Output current | $I_{OUT}$ | ±2 | mA |
| Input voltage | $V_{IN}$ | -0.4 V to $V_{DD}$ +0.4 V | V |
| Ambient temperature range | $T_{amb}$ | -40 to +125 | °C |
| Storage temperature range | $T_{stg}$ | -55 to +150 | °C |

## 7. Thermal Resistance

| Parameters | Symbol | Value | Unit |
|---|---|---|---|
| Junction ambient | $R_{thJA}$ | 180 | K/W |

## 8. Electrical Characteristics

$V_{DD}$ = 5 V; $T_{amb}$ = -40°C to +85°C; reference point is pin 7, unless otherwise specified

| Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage | | 6 | $V_{DD}$ | 4.5 | | 5.5 | V |
| Current consumption | $R_1$ = 66 kΩ | 6 | $I_{DD}$ | | | 60 | µA |
| Power-on reset | Release reset state with rising voltage | 6 | $V_{POR1}$ | 3.9 | | 4.5 | V |
| | Get reset state with falling voltage | 6 | $V_{POR2}$ | 3.8 | | 4.4 | V |
| Power-on reset hysteresis | | | $V_{POR\_hys}$ | 40 | | 200 | mV |
| Reset level for low $V_{DD}$ | $V_{DD}$ = 1 V to $V_{POR1}$<br>$I_{RST}$ = -300 µA | | $V_{RST}$ | | | 0.1 | $V_{DD}$ |
| **Inputs** | | 1, 2, 3 | | | | | |
| Logical “high” | | | $V_{IH}$ | 3.4 | | | V |
| Logical “low” | | | $V_{IL}$ | | | 1.6 | V |
| Hysteresis | | | $V_{IN\_hys}$ | 0.6 | | 1.4 | V |
| Input voltage range | | | $V_{IN}$ | -0.3 | | $V_{DD}$ + 0.3 | V |
| Input current | | 2, 3 | $I_{IN1}$ | 5 | | 20 | µA |
| Input current | | 1 | $I_{IN2}$ | -20 | | -5 | µA |
| **Outputs** | | | | | | | |
| Maximum output current | | 4, 5 | $I_{OUT}$ | -2 | | 2 | mA |
| Logical output “low” | $I_{OUT}$ = -1 mA | 4, 5 | $V_{OL}$ | | | 0.2 | V |
| Logical output “high” | $I_{OUT}$ = -1 mA | 4 | $V_{OH}$ | $V_{DD}$ - 0.2 | | | V |
| Leakage current | $V_{OUT}$ = 5 V | 5 | $I_{leak}$ | | | 2 | µA |

## 8. Electrical Characteristics (Continued)

$V_{DD}$ = 5 V; $T_{amb}$ = -40°C to +85°C; reference point is pin 7, unless otherwise specified

| Parameters | Test Conditions | Pin | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Timing** | | | | | | | |
| Frequency deviation(1) | $R_1$ = 66 kΩ, $C_1$ = 470 pF, $V_{DD}$ = 4.5 V to 5.5 V | | Δf | | | 5 | % |
| Debounce time | | 2, 3 | | 3 | | 4 | Cycle |
| Debounce time | | 1 | | 96 | | 128 | Cycle |
| Maximum trigger pulse length | | | $t_{trgmax}$ | | 45 | | Cycle |
| Power-up reset time | | | $t_o$ | | 201 | | Cycle |
| Switch over mode time | | | $t_1$ | | 1,112 | | Cycle |
| Disable time | Short watchdog window | | $t_2$ | | 130 | | Cycle |
| Enable time | Short watchdog window | | $t_3$ | | 124 | | Cycle |
| Disable time | Long watchdog window | | $t_4$ | | 71,970 | | Cycle |
| Enable time | Long watchdog window | | $t_5$ | | 30,002 | | Cycle |
| Reset-out time | | | $t_6$ | | 40 | | Cycle |

Note: 1. Frequency deviation also depends on the tolerances of the external components

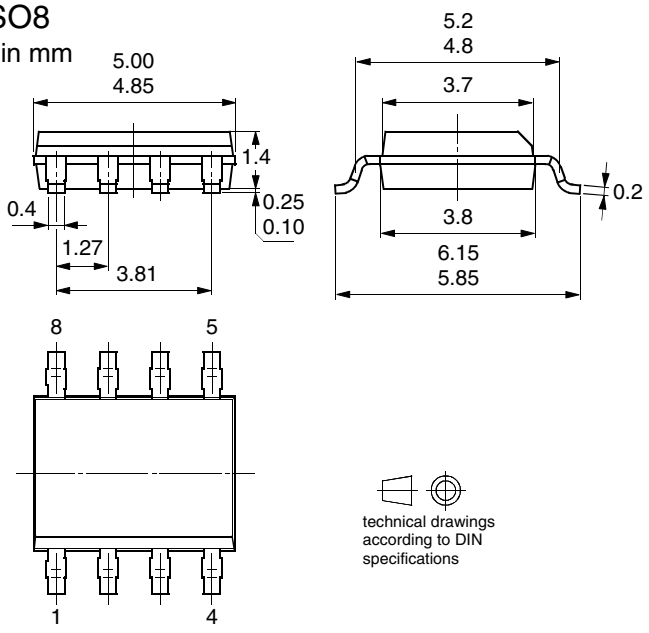
## 9. Ordering Information

| Extended Type Number | Package | Remarks |
|---|---|---|
| U5021M-NFPY | SO8 | Tubed, Pb-free |
| U5021M-NFPG3Y | SO8 | Taped and reeled, Pb-free |

## 10. Package Information

Package SO8

Dimensions in mm



# 11. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

| Revision No. | History |
|---|---|
| 4756D-AUTO-11/05 | • Put datasheet in a new template<br>• First page: Pb-free logo added<br>• Page 7: figure 5-1 changed<br>• Page 9: Ordering Information changed |
| 4756C-AUTO-09/04 | • Electrical Characteristics Table, page 8, row “Reset capability” changed in “Reset level for low VDD“ |
| 4756B-AUTO-07/04 | • Electrical Characteristics Table, page 8, row “Reset capability” added |

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