300MHz to 6GHz Dual Programmable Gain Downconverting Mixer

FEATURES

- **12dB Power Conversion Gain**
- **35dBm Output IP3**
- **15.5dB Range IF DVGA in 0.5dB Steps**
- **Programmable RF Input Tuning**
- **Reduced Power Mode**
- 3.3V Single Supply
- Simple SPI for Fast Development
- –40°C to 105°C Operation (T_C)
- Very Small Solution Size
- 32-Lead (5mm × 5mm) QFN Package

APPLICATIONS

- 4G and 5G MIMO Receivers
- Diversity Receivers
- Distributed Antenna Systems (DAS)
- Network Test/Monitoring Equipment
- Software-Defined Radios

DESCRIPTION

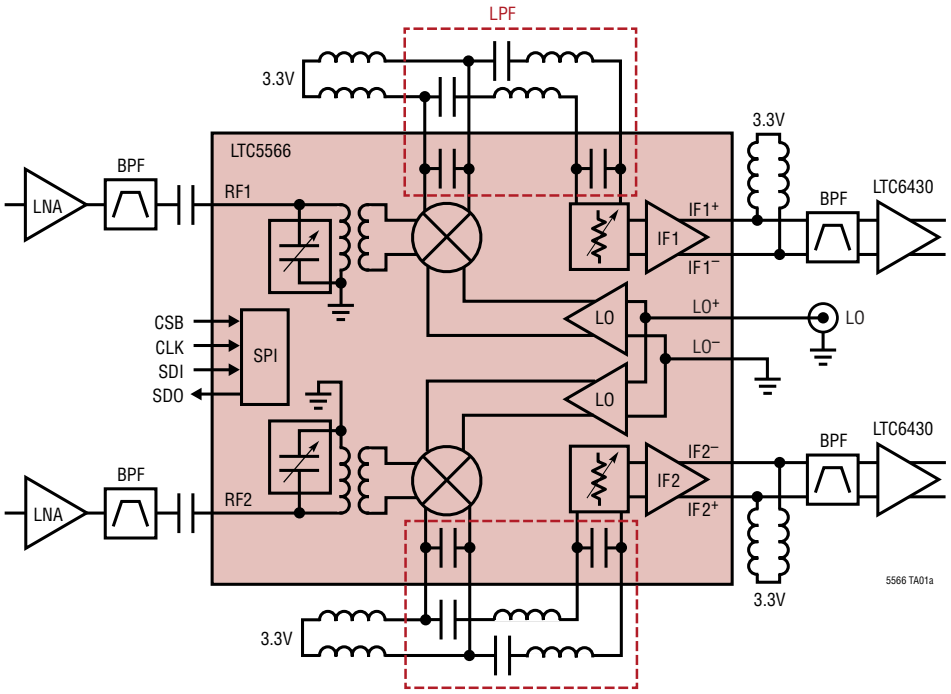
The LTC®5566 dual programmable gain downconverting mixer is ideal for diversity and MIMO receivers that require precise gain setting. Each channel incorporates an active mixer and a digital IF VGA with 15.5dB gain control range. The IF gain of each channel is programmed in 0.5dB steps through the SPI.

Programmable RF input tuning via the SPI or parallel control lines makes the device attractive for wideband radio applications. Furthermore, a reduced power mode is available, programmed through the SPI.

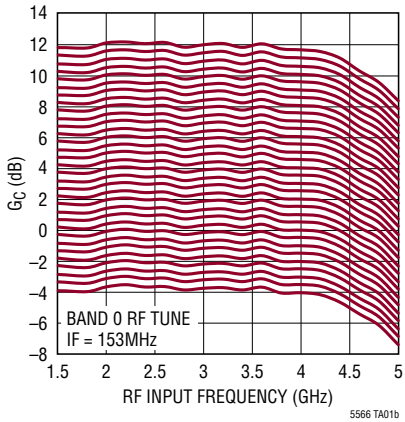
Integrated RF transformers provide single-ended 50Ω inputs. The differential LO input is designed for single-ended or differential drive. The differential IF output simplifies the interface to differential IF filters and amplifiers. The mixers are optimized for use up to 5GHz but may be used up to 6GHz with degraded performance.

TYPICAL APPLICATION

Dual Channel MIMO Receiver with Programmable 0.5dB Gain Steps



LTC5566 Conversion Gain vs RF Frequency and IF Attenuation (0.5dB Gain Steps)

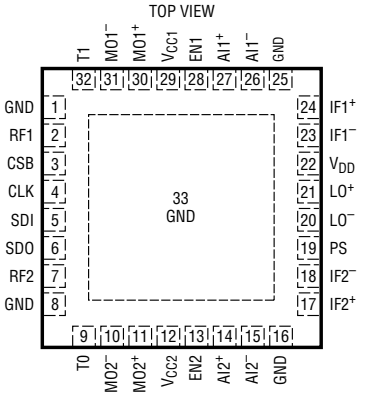


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}, V_{CC1}, V_{CC2}, $IF1^+$, $IF1^-$, $IF2^+$, $IF2^-$) 4V
EN1, EN2, T0, T1 Input Voltages .....–0.3V to V_{CC} + 0.3V
LO^+, LO^- Input Power (150MHz to 6GHz) ..... +10dBm
RF1, RF2 Input Power (300MHz to 6GHz) .....+20dBm
LO^+, LO^- DC Voltage ..... ±0.5V
IF DVGA Peak Differential Input Voltage..... ±4V
SDI, CLK, CSB, PS Input Voltages... –0.3V to V_{DD} + 0.3V
SDO Output Current ..... ±10mA
Operating Temperature Range (T_C) ..... –40°C to 105°C
Junction Temperature (T_J) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JC} = 7.7°C/W
EXPOSED PAD (PIN 33) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

(http://www.linear.com/product/LTC5566#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	CASE TEMPERATURE RANGE
LTC5566IUH#PBF	LTC5566IUH#TRPBF	5566	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V. Test circuit shown in Figure 1. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})		●	3.0	3.3	3.6	V
SPI Supply Voltage (V_{DD})		●	1.6		3.6	V
Supply Current (I_{CC})	One Channel, Full Power Mode			192	225	mA
	Both Channels, Full Power Mode			384	450	mA
	One Channel, Reduced Power Mode			147		mA
	Both Channels, Reduced Power Mode			294		mA
	Shutdown	●		1.2	1.9	mA
SPI Supply Current (I_{DD})	Operating: CSB = Low, f_{CLK} =10MHz			0.2	1	mA
	Idle: CSB = High			10		µA
Enable and RF Tuning Logic Inputs (EN1, EN2, T0, T1) Internal Pull-Down Resistors on Each Pin						
Input High Voltage (On)		●	1.4			V
Input Low Voltage (Off)		●			0.5	V
Input Current	V_{IN} = V_{CC} = 3.6V				100	µA
Enable Turn-On Time				0.3		µs
Enable Turn-Off Time				0.1		µs
RF Input Tuning Parallel Select Logic Input (PS) Internal Pull-Down Resistor						
Input High Voltage (Parallel Enabled)		●	0.7 • V_{DD}			V
Input Low Voltage (Serial Enabled)		●			0.3 • V_{DD}	V
Input Current	V_{IN} = V_{DD} = 3.6V				50	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V. Test circuit shown in Figure 1. (Notes 3, 6)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SPI Port Logic Inputs (CSB, CLK, SDI)						
Input High Voltage		●	0.7 • V_{DD}			V
Input Low Voltage		●			0.3 • V_{DD}	V
Input Current	V_{IN} = V_{DD} = 3.6V				25	µA
Input Hysteresis				200		mV
SPI Port Logic Output (SDO)						
Output High Voltage	I_{SOURCE} = 3mA	●	V_{DD} – 0.4V			V
Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
Output Leakage Current	V_{CSB} = V_{DD} = 3.6V				±20	µA
SPI Port Timing						
SDI Setup Time			5			ns
SDI Hold Time			10			ns
CLK Falling to SDO Valid Time	C_{SDO} = 20pF				15	ns
SDO Rise/Fall Time	C_{SDO} = 20pF			5		ns
SDO Enable Time					10	ns
SDO Disable Time					10	ns
CSB Setup Time			15			ns
CSB Hold Time			5			ns
CLK Frequency	C_{SDO} = 20pF				20	MHz

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN1, EN2 = High, P_{LO} = 0dBm. Test circuit shown in Figure 1. (Notes 3, 4, 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Input Frequency Range	External Matching Required	●		300 to 6000		MHz
LO Input Frequency Range		●		150 to 6000		MHz
IF Output Frequency Range	External Matching Required	●		1 to 500		MHz
1dB IF Gain Rolloff	Relative to 100MHz Gain			400		MHz
IF Gain Error at 150MHz	Differential; Between Any Two 0.5dB Atten Steps Integral; Over Entire 15.5dB IF Atten Range			±0.06 0.3		dB dB
IF Phase Error	IF = 150MHz, Full 15.5dB Atten Range IF = 350MHz, Full 15.5dB Atten Range			2.4 5.5		Deg Deg
LO Input Return Loss	Single-Ended, Z_O = 50Ω, 150MHz to 6000MHz			>10		dB
LO Input Power	Single-Ended or Differential	●	–6	0	6	dBm
Mixer IF Output Impedance	Differential, 10MHz to 400MHz			300Ω || 1pF		R || C
IF DVGA Input Impedance	Differential, 10MHz to 400MHz			300Ω || 1pF		R || C
IF DVGA Output Impedance	Differential, 10MHz to 400MHz			206Ω || 1pF		R || C
RF to LO Isolation	RF = 300MHz to 1000MHz RF = 1000MHz to 3800MHz RF = 3800MHz to 6000MHz			>68 >50 >40		dB dB dB
RF to Unbalanced IF Port Isolation	RF = 300MHz to 900MHz RF = 900MHz to 6000MHz			>32 >54		dB dB
LO to Unbalanced IF Port Leakage	LO = 300MHz to 800MHz LO = 800MHz to 6000MHz			<–33 <–43		dBm dBm

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN1, EN2 = High, P_{RF} = –8dBm/Tone, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 3, 4, 5)

Band 0 (See Figure 1): RF = 4.5GHz, IF = 153MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 3.1GHz to 5.1GHz			>10		>10	dB
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			10.6 4.5 –1.6		10.3 4.2 –1.9	dB dB dB
Conversion Gain Flatness	RF = 4.5GHz ±100MHz, LO = 4.35GHz			±0.4		±0.4	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.014		–0.014	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			22.0 23.6 24.1		17.8 18.7 18.9	dBm dBm dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 154MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			50		46	dBm
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			16.3 17.8 21.1		15.2 17.1 20.9	dB dB dB
LO to RF Leakage	LO = 3.1GHz to 5.2GHz			<–42		<–42	dBm
Input 1dB Compression	0dB IF ATTEN 3dB IF ATTEN 6dB IF ATTEN 9dB IF ATTEN and Higher			7.0 9.6 11.2 11.5		6.4 8.9 10.3 10.6	dBm dBm dBm dBm
Channel-to-Channel Isolation	RF = 4.5GHz			40		40	dB

RF = 3.6GHz, IF = 153MHz, Low Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			11.8 5.7 –0.4		11.5 5.4 –0.7	dB dB dB
Conversion Gain Flatness	RF = 3.6GHz ±100MHz, LO = 3.45GHz			±0.45		±0.45	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.012		–0.012	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			22.0 24.5 25.5		18.4 19.9 20.3	dBm dBm dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 154MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			60		55	dBm
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			13.8 15.4 18.8		12.7 14.8 18.6	dB dB dB
LO to RF Leakage	LO = 3.1GHz to 5.2GHz			<–42		<–42	dBm
Input 1dB Compression	0dB IF ATTEN 3dB IF ATTEN 6dB IF ATTEN 9dB IF ATTEN and Higher			6.0 8.8 10.7 11.5		5.4 8.2 10.1 10.6	dBm dBm dBm dBm
Channel-to-Channel Isolation	RF = 3.6GHz			51		51	dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN1, EN2 = High, P_{RF} = –8dBm/Tone, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 3, 4, 5)

Band 1 (See Figure 1): RF = 2.6GHz, IF = 153MHz, High Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 1.8GHz to 4.4GHz			>12		>12	dB
Power Conversion Gain	0dB IF ATTEN			11.8		11.5	dB
	3dB IF ATTEN		6.8	8.8		8.4	dB
	6dB IF ATTEN			5.8		5.4	dB
	9dB IF ATTEN			2.7		2.4	dB
	12dB IF ATTEN			–0.3		–0.7	dB
	15dB IF ATTEN			–3.4		–3.7	dB
Conversion Gain Flatness	RF = 2.6GHz ±100MHz, LO = 2.75GHz			±0.5		±0.5	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.013		–0.013	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN			23.2		19.5	dBm
	3dB IF ATTEN			24.6		20.6	dBm
	6dB IF ATTEN			26.0		21.2	dBm
	9dB IF ATTEN			26.8		21.4	dBm
	12dB IF ATTEN			27.6		21.4	dBm
	15dB IF ATTEN			28.0		21.4	dBm
Two-Tone Output 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN			35.0		31.0	dBm
	3dB IF ATTEN			33.4		29.0	dBm
	6dB IF ATTEN			31.8		26.6	dBm
	9dB IF ATTEN			29.5		23.8	dBm
	12dB IF ATTEN			27.3		20.7	dBm
	15dB IF ATTEN			24.6		17.7	dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 154MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			59		54	dBm
SSB Noise Figure	0dB IF ATTEN			13.3		13.0	dB
	3dB IF ATTEN			14.1		14.0	dB
	6dB IF ATTEN			15.3		15.3	dB
	9dB IF ATTEN			17.0		17.2	dB
	12dB IF ATTEN			19.3		19.5	dB
	15dB IF ATTEN			21.7		22.1	dB
SSB Noise Figure Under Blocking (2.5GHz Blocker)	+2dBm BLOCKER, 3dB IF ATTEN			18.7		18.3	dB
	+5dBm BLOCKER, 3dB IF ATTEN			21.1		20.9	dB
LO to RF Leakage	LO = 1.6GHz to 4GHz			<–45		<–45	dBm
1/2 IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 153MHz)	f_{RF} = 2676.5MHz, P_{RF} = –6dBm 0dB to 15.5dB IF ATTEN			–71		–69	dBc
1/3 IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 153MHz)	f_{RF} = 2702MHz, P_{RF} = –6dBm 0dB to 15.5dB IF ATTEN			–65		–60	dBc
Input 1dB Compression	0dB IF ATTEN			6.2		5.6	dBm
	3dB IF ATTEN			9.2		8.6	dBm
	6dB IF ATTEN			11.5		10.9	dBm
	9dB IF ATTEN and Higher			12.6		11.6	dBm
Output 1dB Compression	0dB IF ATTEN			17.0		16.1	dBm
	3dB IF ATTEN			17.0		16.0	dBm
	6dB IF ATTEN			16.3		15.3	dBm
	9dB IF ATTEN			14.3		13.0	dBm
Channel-to-Channel Isolation	RF = 2.6GHz			49		49	dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN1, EN2 = 3.3V, P_{RF} = –8dBm/Tone, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 3, 4, 5)

Band 2 (See Figure 1): RF = 1.9GHz, IF = 153MHz, High Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 1.3GHz to 3.9GHz			>10		>10	dB
Power Conversion Gain	0dB IF ATTEN			11.9		11.6	dB
	3dB IF ATTEN			8.8		8.5	dB
	6dB IF ATTEN			5.8		5.5	dB
	9dB IF ATTEN			2.8		2.5	dB
	12dB IF ATTEN			–0.3		–0.5	dB
	15dB IF ATTEN			–3.3		–3.6	dB
Conversion Gain Flatness	RF = 1.9GHz ±100MHz, LO = 2.05GHz			±0.5		±0.5	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.013		–0.013	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN			22.6		19.8	dBm
	3dB IF ATTEN			23.9		21.2	dBm
	6dB IF ATTEN			25.4		22.0	dBm
	9dB IF ATTEN			26.1		22.3	dBm
	12dB IF ATTEN			26.3		22.4	dBm
	15dB IF ATTEN			26.5		22.5	dBm
Two-Tone Output 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN			34.5		31.4	dBm
	3dB IF ATTEN			32.7		29.7	dBm
	6dB IF ATTEN			31.2		27.5	dBm
	9dB IF ATTEN			28.9		24.8	dBm
	12dB IF ATTEN			26.0		21.9	dBm
	15dB IF ATTEN			23.2		18.9	dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 154MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			57		53	dBm
SSB Noise Figure	0dB IF ATTEN			13.0		12.1	dB
	3dB IF ATTEN			13.9		13.2	dB
	6dB IF ATTEN			15.2		14.7	dB
	9dB IF ATTEN			17.0		16.7	dB
	12dB IF ATTEN			19.3		19.2	dB
	15dB IF ATTEN			21.8		21.8	dB
SSB Noise Figure Under Blocking (1.8GHz Blocker)	+2dBm BLOCKER, 3dB IF ATTEN			17.6		17.4	dB
	+5dBm BLOCKER, 3dB IF ATTEN			20.4		20.0	dB
LO to RF Leakage	LO = 1.1GHz to 3.5GHz			<–47		<–47	dBm
1/2 IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 153MHz)	f_{RF} = 1976.5MHz, P_{RF} = –6dBm 0dB to 15.5dB IF ATTEN			–67		–65	dBc
1/3 IF Output Spurious Product (f_{RF} Offset to Produce Spur at f_{IF} = 153MHz)	f_{RF} = 2002MHz, P_{RF} = –6dBm 0dB to 15.5dB IF ATTEN			–71		–65	dBc
Input 1dB Compression	0dB IF ATTEN			6.1		5.4	dBm
	3dB IF ATTEN			9.2		8.5	dBm
	6dB IF ATTEN			11.7		10.9	dBm
	9dB IF ATTEN and Higher			13.3		12.0	dBm
Output 1dB Compression	0dB IF ATTEN			17.0		16.0	dBm
	3dB IF ATTEN			17.0		16.0	dBm
	6dB IF ATTEN			16.5		15.4	dBm
	9dB IF ATTEN			15.1		13.5	dBm
Channel-to-Channel Isolation	RF = 1.9GHz			50		50	dB

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = V_{DD} = 3.3V, EN1, EN2 = High, P_{RF} = –8dBm/Tone, P_{LO} = 0dBm, unless otherwise noted. Test circuit shown in Figure 1. (Notes 3, 4, 5)

Band 3 (See Figure 1): RF = 850MHz, IF = 153MHz, High Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 700MHz to 1.3GHz			>10		>10	dB
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			12.2 6.1 0		11.8 5.7 –0.4	dB dB dB
Conversion Gain Flatness	RF = 850MHz ±75MHz, LO = 1050MHz			±0.3		±0.3	dB
Conversion Gain vs Temperature	T_C = –40°C to 105°C	●		–0.014		–0.014	dB/°C
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			22.0 24.7 26.2		19.5 22.3 23.3	dBm dBm dBm
Two-Tone Input 2nd Order Intercept (Δf_{RF} = 154MHz = f_{IM2})	0dB to 15.5dB IF ATTEN			60.0		56.5	dBm
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			12.6 14.9 19.1		12.1 14.7 19.2	dB dB dB
LO to RF Leakage	LO = 300MHz to 1.5GHz			<–60		<–60	dBm
Input 1dB Compression	0dB IF ATTEN 3dB IF ATTEN 6dB IF ATTEN 9dB IF ATTEN and Higher			5.8 8.8 11.5 13.3		5.1 8.2 10.6 11.9	dBm dBm dBm dBm
Channel-to-Channel Isolation	RF = 850MHz			50		50	dB

Band 4 (See Figure 1): RF = 450MHz, IF = 153MHz, High Side LO

PARAMETER	CONDITIONS		FULL PWR MIN	FULL PWR TYP	FULL PWR MAX	REDUCED PWR TYP	UNITS
RF Input Return Loss	Z_O = 50Ω, 390MHz to 530MHz			>10		>10	dB
Power Conversion Gain	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			11.7 5.6 –0.5		11.1 5.0 –1.1	dB dB dB
SSB Noise Figure	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			13.8 15.9 19.9		13.6 15.9 20.1	dB dB dB
Two-Tone Input 3rd Order Intercept (Δf_{RF} = 2MHz)	0dB IF ATTEN 6dB IF ATTEN 12dB IF ATTEN			21.8 24.1 25.0		19.4 21.7 22.6	dBm dBm dBm
Channel-to-Channel Isolation	RF = 450MHz			57		57	dB

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The mixer output pins on this device are sensitive to ESD greater than 750V (HBM). Proper ESD handling precautions must be observed. All other pins withstand 2kV.

Note 3: The LTC5566 is guaranteed functional over the –40°C to 105°C case temperature range.

Note 4: SSB Noise Figure measured with a small-signal noise source, bandpass filter and 2dB matching pad on RF input, and bandpass filter on the LO input.

Note 5: Channel-to-channel isolation is defined as the relative IF output power of channel 2 to channel 1, with the RF input signal applied to RF1 while the RF2 input is 50Ω terminated. Both channels are enabled and programmed for 3dB IF attenuation.

Note 6: SPI timing guaranteed by design, not subject to test.

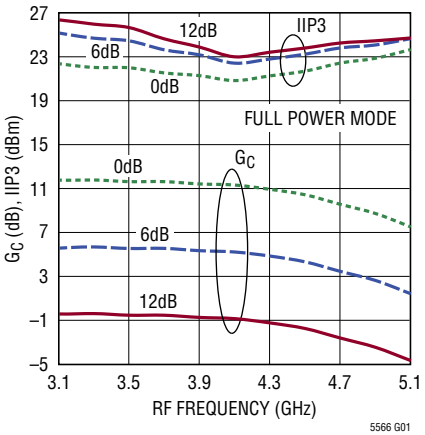
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

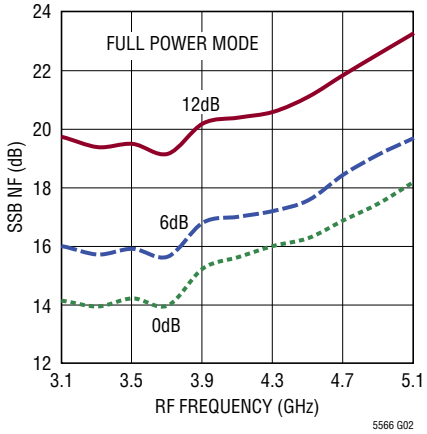
P_{RF} = –8dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, unless otherwise noted.

Band 0: RF = 3.6GHz and 4.5GHz, IF = 153MHz, Low Side LO

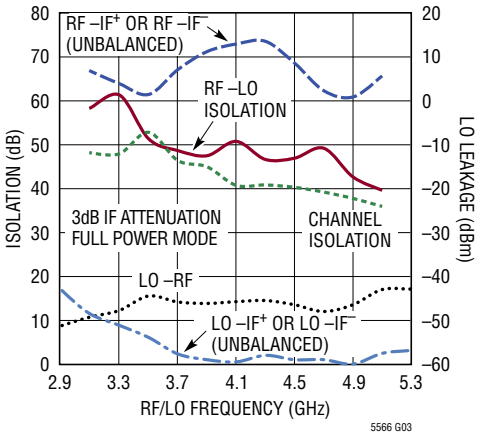
Conv Gain and IIP3 vs RF Frequency 0dB, 6dB and 12dB IF Attenuation



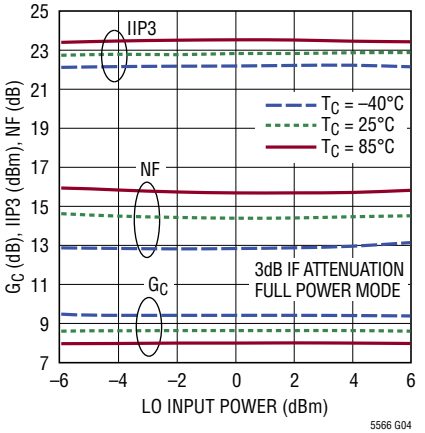
SSB NF vs RF Frequency 0dB, 6dB and 12dB IF Attenuation



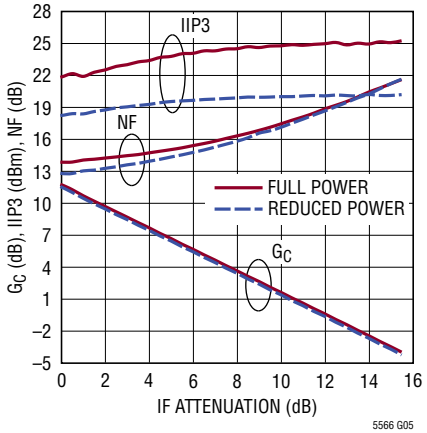
RF Isolation and LO Leakage vs Frequency



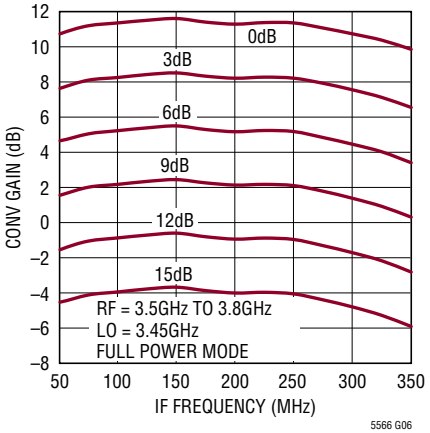
3.6GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



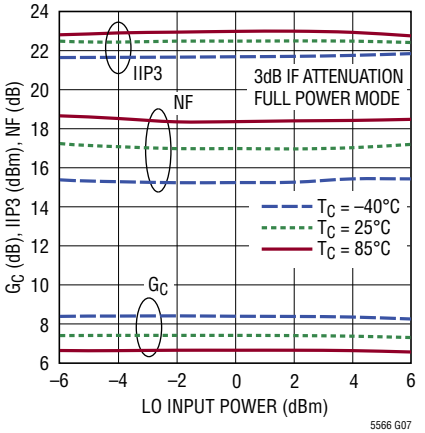
3.6GHz Conv Gain, IIP3 and SSB NF vs IF Attenuation (0.5dB Steps)



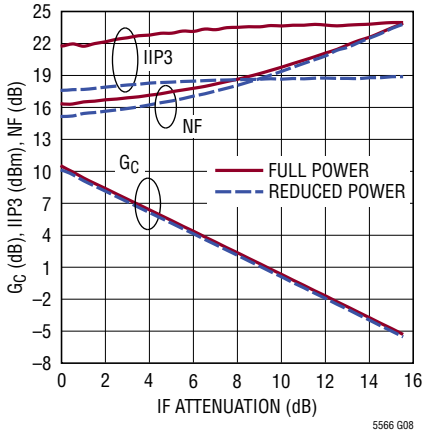
3.6GHz Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



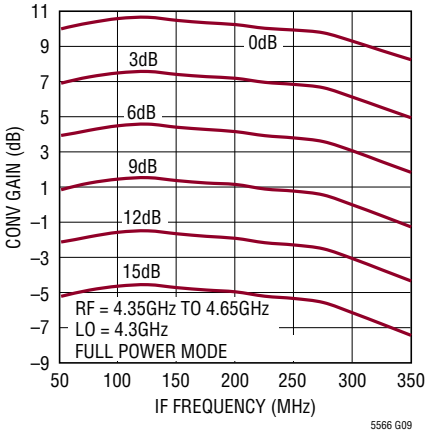
4.5GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



4.5GHz Conv Gain, IIP3 and SSB NF vs IF Attenuation (0.5dB Steps)



4.5GHz Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



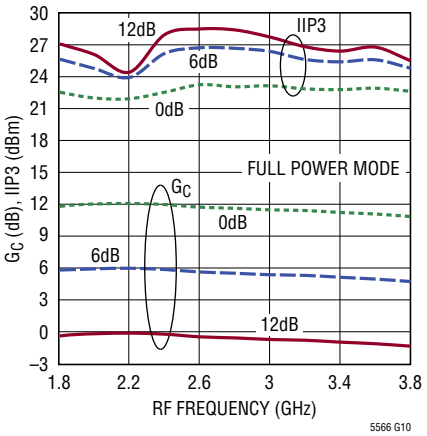
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

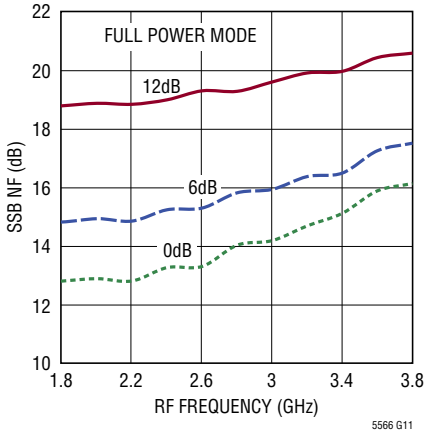
P_{RF} = –8dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, unless otherwise noted.

Band 1: RF = 2.6GHz, IF = 153MHz, High Side LO

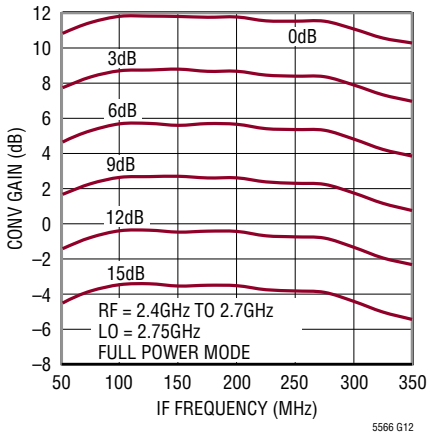
Conv Gain and IIP3 vs RF Frequency 0dB, 6dB and 12dB IF Attenuation



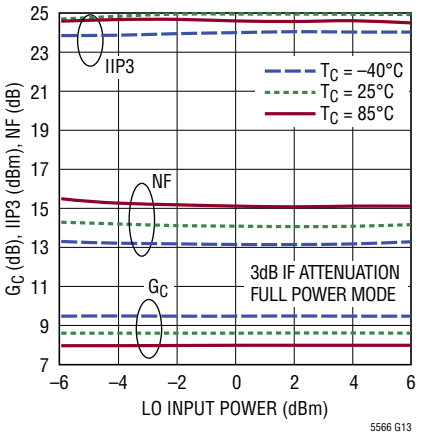
SSB NF vs RF Frequency 0dB, 6dB and 12dB IF Attenuation



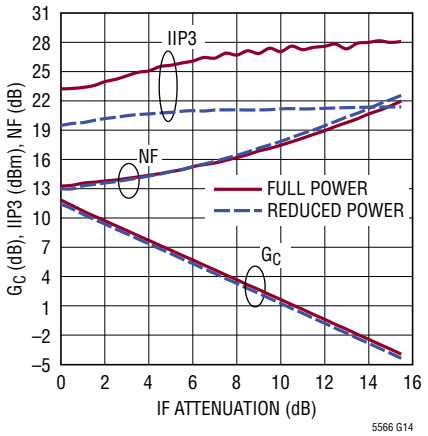
Conv Gain vs IF Frequency and IF Attenuation, Swept RF/Fixed LO



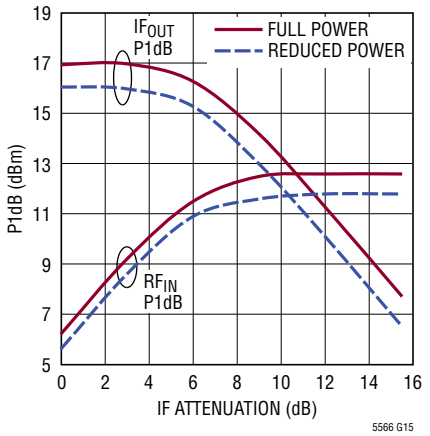
2.6GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



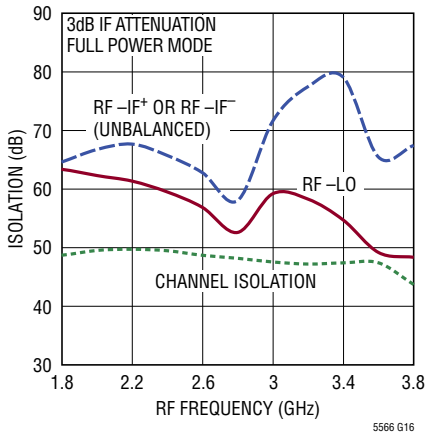
2.6GHz Conv Gain, IIP3 and SSB NF vs IF Attenuation (0.5dB Steps)



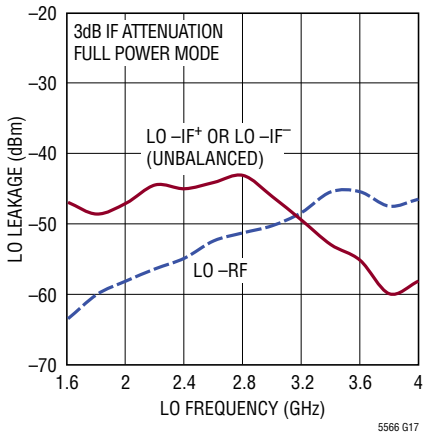
2.6GHz RF Input and IF Output P1dB vs IF Attenuation



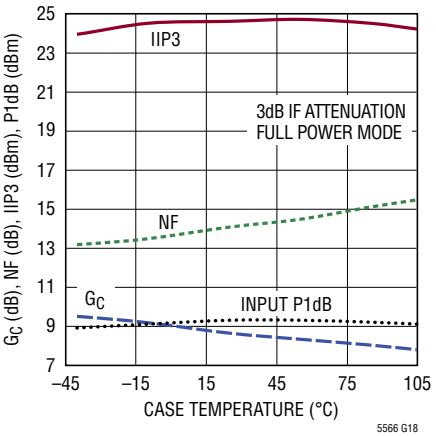
Isolation vs RF Frequency



LO Leakage vs LO Frequency



2.6GHz Conv Gain, IIP3, NF and RF Input P1dB vs Temperature



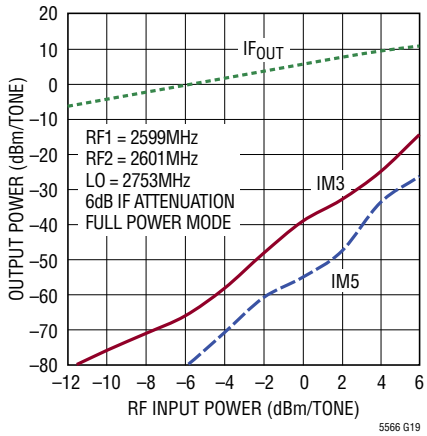
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

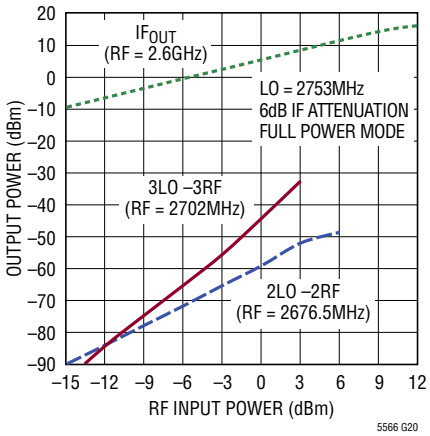
P_{RF} = –8dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, unless otherwise noted.

Band 1: RF = 2.6GHz, IF = 153MHz, High Side LO

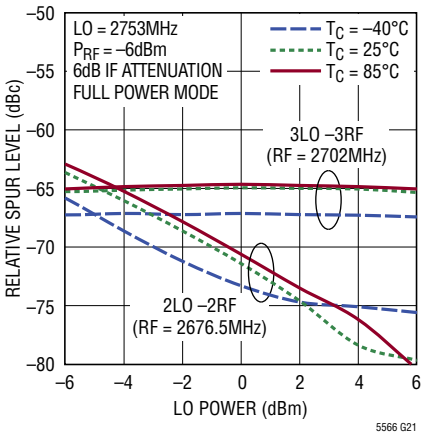
2-Tone IF Output Power, IM3 and IM5 vs RF Input Power



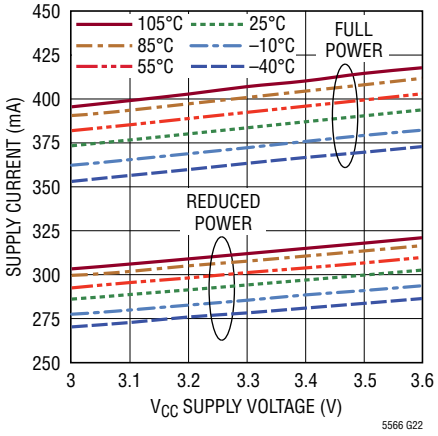
Single-Tone IF Output Power, 2 × 2 and 3 × 3 Spurs vs RF Input Power



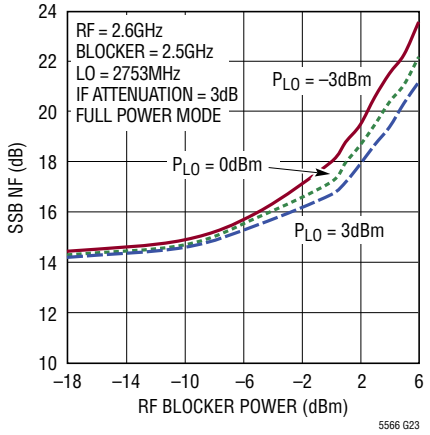
2 × 2 and 3 × 3 Spur Suppression vs LO Power



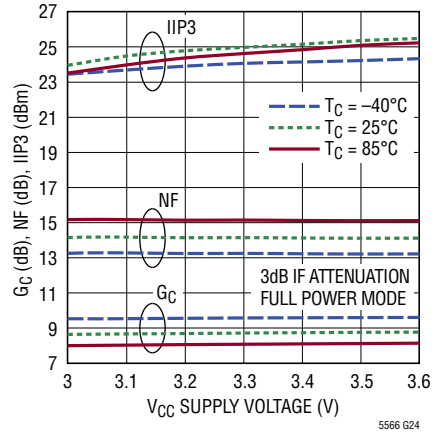
V_{CC} Supply Current vs Supply Voltage (Both Channels Enabled)



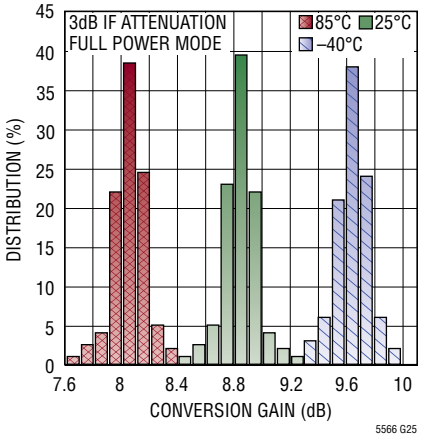
SSB NF vs RF Blocker Power



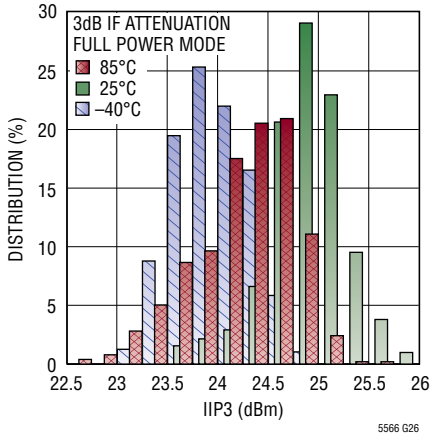
2.6GHz Conv Gain IIP3 and SSB NF vs Supply Voltage and Case Temperature



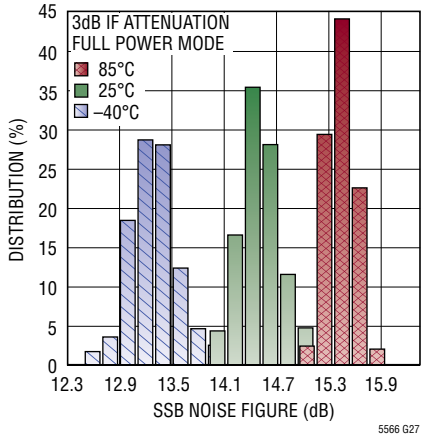
2.6GHz Conversion Gain Distribution



2.6GHz IIP3 Distribution



2.6GHz SSB NF Distribution



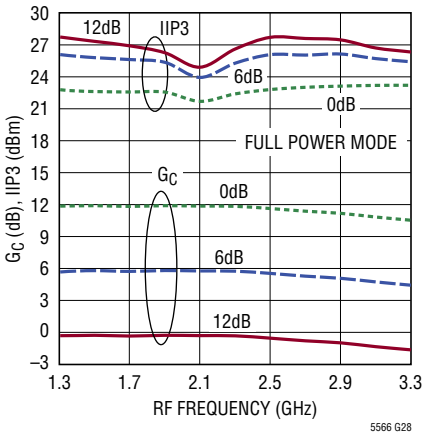
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

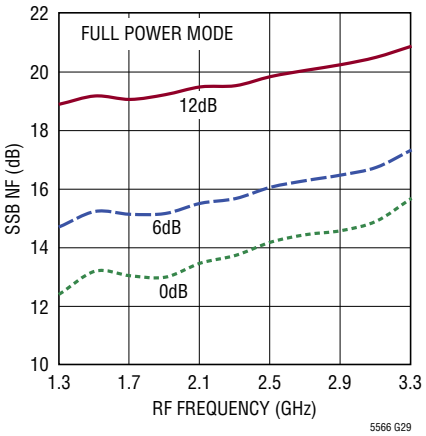
P_{RF} = –8dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, unless otherwise noted.

Band 2: RF = 1.9GHz, IF = 153MHz, High Side LO

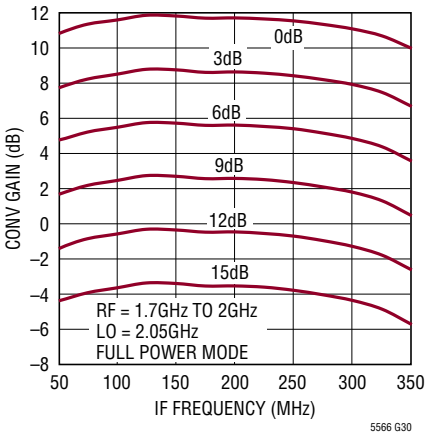
Conv Gain and IIP3 vs RF Frequency 0dB, 6dB and 12dB IF Attenuation



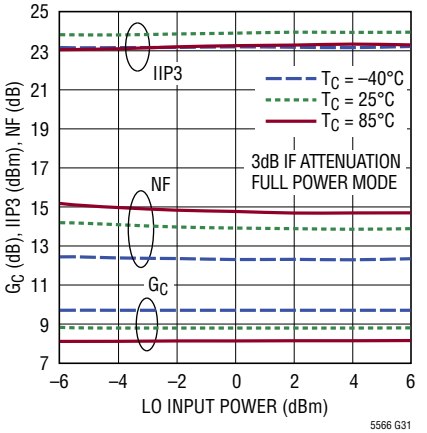
SSB NF vs RF Frequency 0dB, 6dB and 12dB IF Attenuation



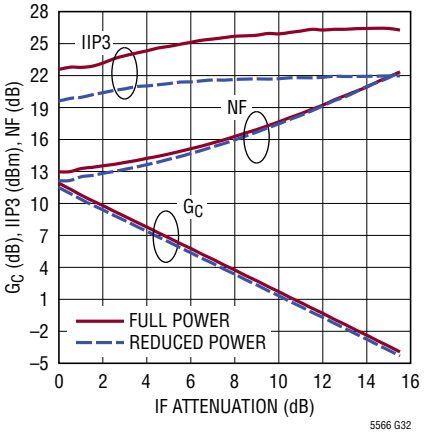
Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



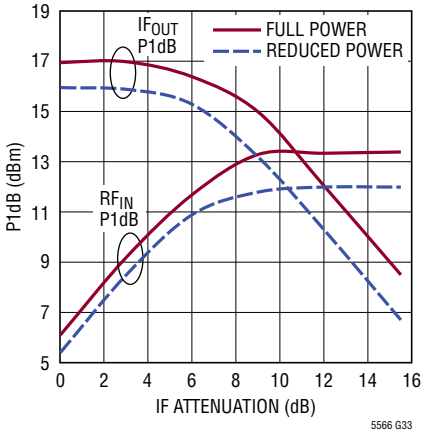
1.9GHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



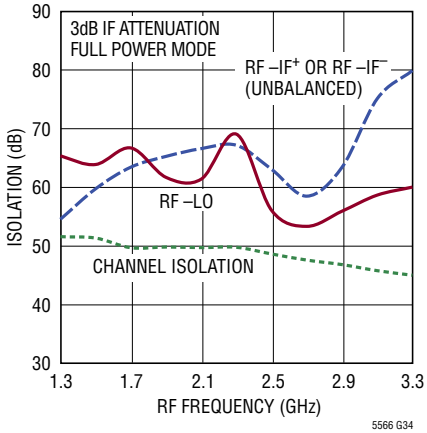
1.9GHz Conv Gain, IIP3 and SSB NF vs IF Attenuation (0.5dB Steps)



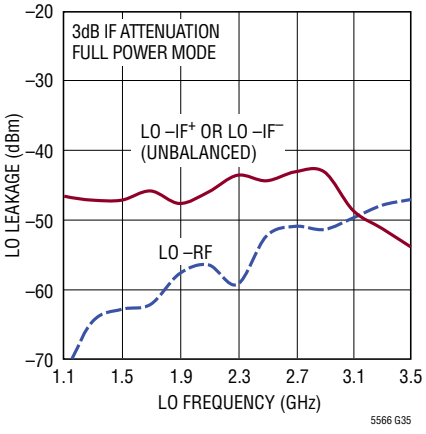
1.9GHz RF Input and IF Output P1dB vs IF Attenuation



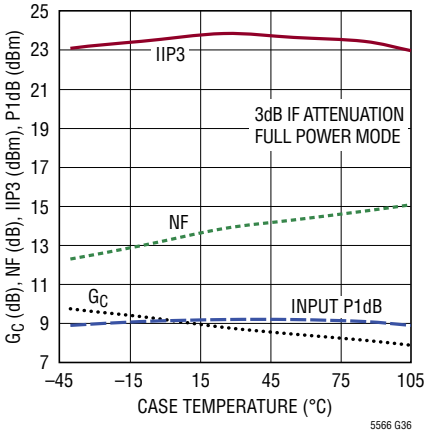
Isolation vs RF Frequency



LO Leakage vs LO Frequency



1.9GHz Conv Gain, IIP3, NF and RF Input P1dB vs Temperature



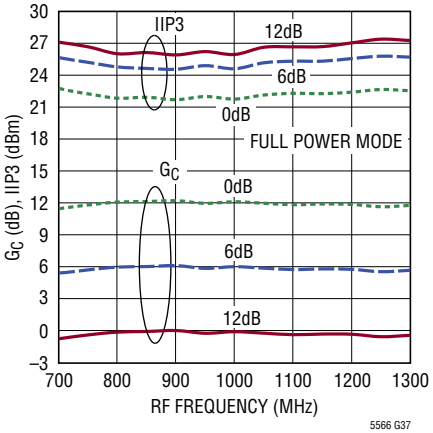
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

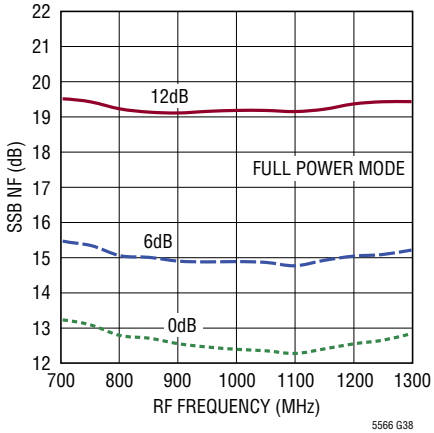
P_{RF} = –8dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, unless otherwise noted.

Band 3: RF = 850MHz, IF = 153MHz, High Side LO

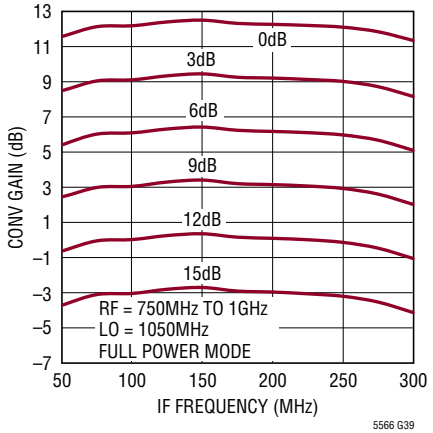
Conv Gain and IIP3 vs RF Frequency 0dB, 6dB and 12dB IF Attenuation



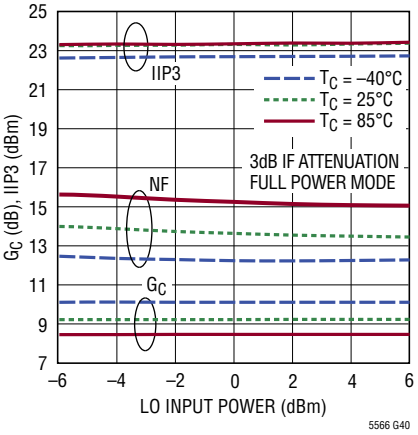
SSB NF vs RF Frequency 0dB, 6dB and 12dB IF Attenuation



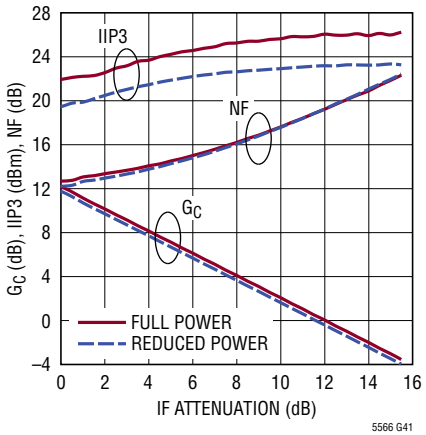
Conv Gain vs IF Frequency and Attenuation, Swept RF/Fixed LO



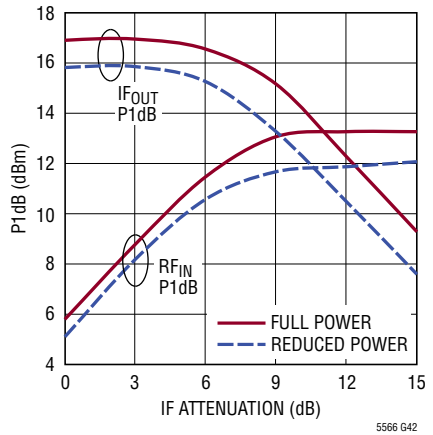
850MHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



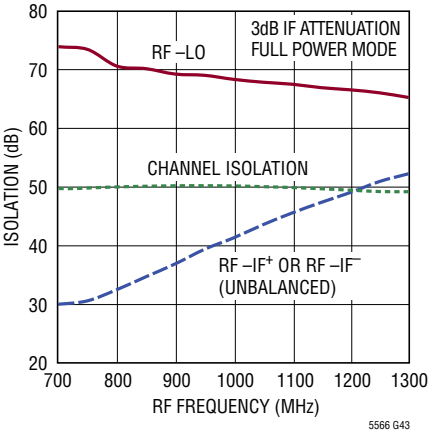
850MHz Conv Gain, IIP3 and SSB NF vs IF Attenuation



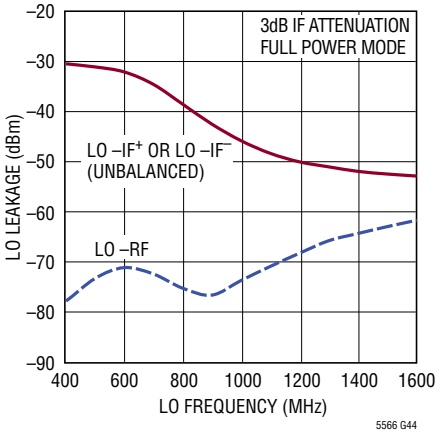
850MHz RF Input and IF Output P1dB vs IF Attenuation



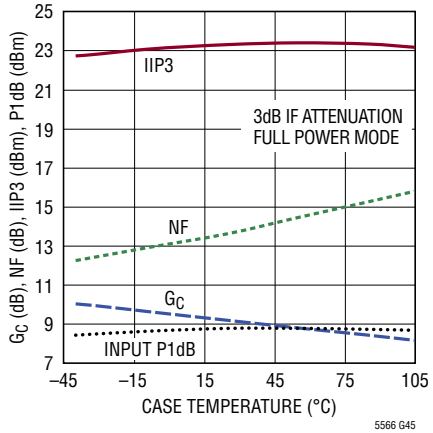
RF Isolation vs RF Frequency



LO Leakage vs LO Frequency



850MHz Conv Gain, IIP3, NF and RF Input P1dB vs Temperature



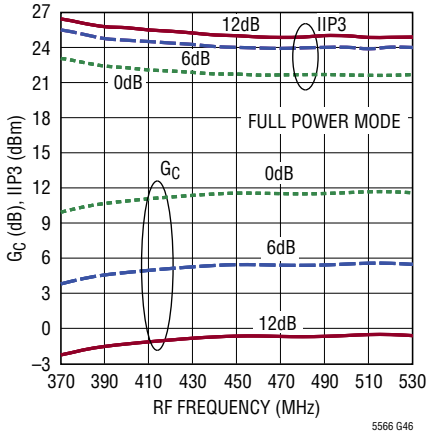
TYPICAL PERFORMANCE CHARACTERISTICS

Test circuit shown in Figure 1.

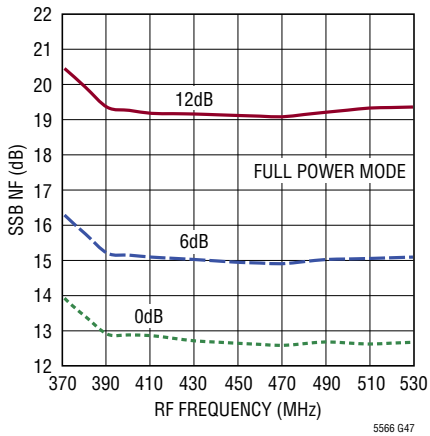
P_{RF} = –8dBm/Tone, Δf = 2MHz, P_{LO} = 0dBm, V_{CC} = 3.3V, V_{DD} = 3.3V, T_C = 25°C, unless otherwise noted.

Band 4: RF = 450MHz, IF = 153MHz, High Side LO

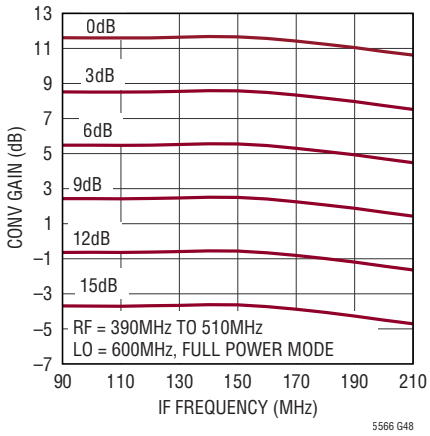
Conv Gain and IIP3 vs RF Frequency 0dB, 6dB and 12dB IF Attenuation



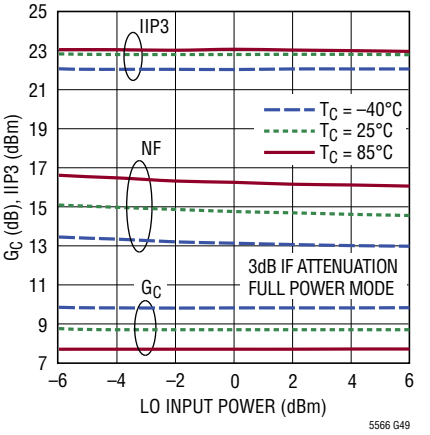
SSB NF vs RF Frequency 0dB, 6dB and 12dB IF Attenuation



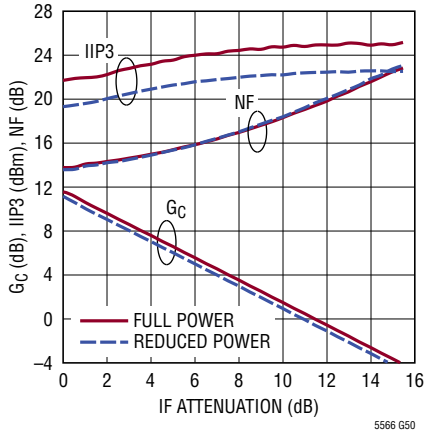
Conv Gain vs IF Frequency and IF Attenuation, Swept RF/Fixed LO



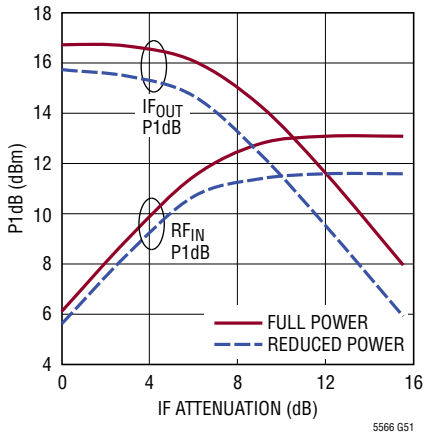
450MHz Conv Gain, IIP3 and SSB NF vs LO Power and Case Temperature



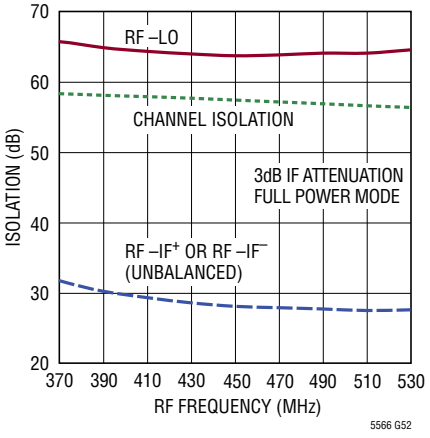
450MHz Conv Gain, IIP3 and SSB NF vs IF Attenuation



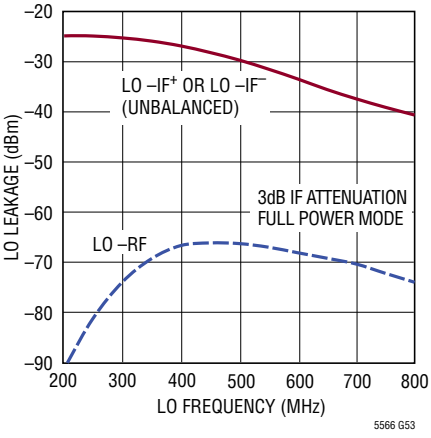
450MHz RF Input and IF Output P1dB vs IF Attenuation



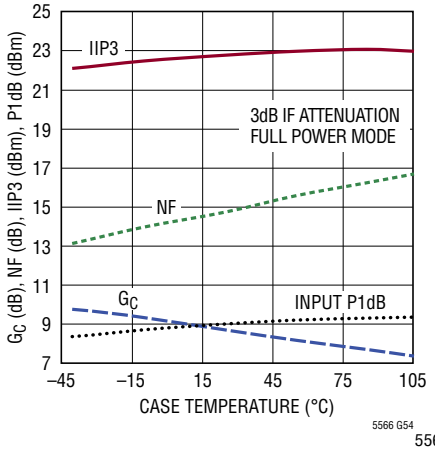
RF Isolation vs RF Frequency



LO Leakage vs LO Frequency



450MHz Conv Gain, IIP3, NF and RF Input P1dB vs Temperature



PIN FUNCTIONS

GND (Pins 1, 8, 16, 25, Exposed Pad Pin 33): Ground. These pins must be soldered to the RF ground plane on the circuit board. The exposed pad provides both electrical ground contact and thermal contact to the printed circuit board.

RF1, RF2 (Pins 2, 7): Single-Ended RF Inputs for Channels 1 and 2, Respectively. These pins are internally biased to $V_{CC}/2$ when V_{CC} is applied. Therefore, a series DC-blocking capacitor must be used. The internal matching capacitance may be adjusted in four discrete steps using the T0 and T1 control pins, or via the SPI interface.

CSB (Pin 3): Serial Port Chip Select. This CMOS input activates the SPI inputs when driven low. When driven high, the inputs are deactivated. See the Applications section for more details.

CLK (Pin 4): Serial Port Clock. This CMOS input clocks serial port input data on its rising edge. See the Applications section for more details.

SDI (Pin 5): Serial Port Data Input. This CMOS input is used to load serial data into the 16-bit register. See the Applications section for more details.

SDO (Pin 6): Serial Port Data Output. This CMOS three-state output presents data from the serial port during a communication burst. Optionally, attach a resistor of >200k to GND to prevent a floating output. See the Applications section for more details.

T0, T1 (Pins 9, 32): 2-Bit RF Input Tuning Control Pins. A CMOS logic high will enable the respective bit for both channels when the PS pin is high. These pins have internal 167k pull-down resistors. The RF input tuning may also be controlled through the serial port when PS is low. For serial control only, these pins should be grounded.

$MO2^-$, $MO2^+$, $MO1^+$, $MO1^-$ (Pins 10, 11, 30, 31): Open-Collector Differential IF Outputs for Mixer 2 and Mixer 1, Respectively. These pins must be connected to V_{CC} through pull-up inductors. Typical DC current is 27mA into each pin.

V_{CC2}, V_{CC1} (Pins 12, 29): Power Supply Pins for Channels 2 and 1, Respectively. These pins must be connected to a regulated 3.3V supply, with a bypass capacitor located close to the pins. Typical DC current consumption is 41mA into each pin.

EN2, EN1 (Pins 13, 28): Enable Control Pins for Channels 2 and 1, Respectively. A CMOS logic high will enable each channel. These pins have internal 330k pull-down resistors, so if unconnected, both channels are shutdown.

$AI2^+$, $AI2^-$, $AI1^-$, $AI1^+$ (Pins 14, 15, 26, 27): Differential IF Attenuator Inputs for Channel 2 and Channel 1, Respectively. These pins are internally biased to $V_{CC}/2$ when V_{CC} is applied. Therefore, a series DC-blocking capacitor must be used.

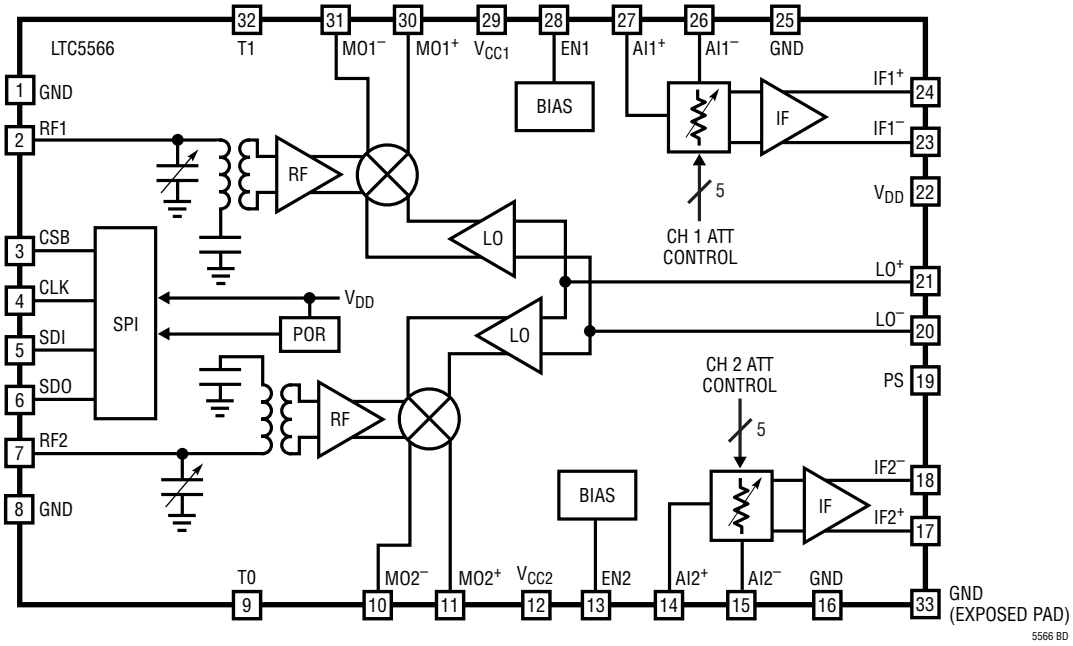
$IF2^+$, $IF2^-$, $IF1^-$, $IF1^+$ (Pins 17, 18, 23, 24): Open-Collector Differential IF Buffer Outputs for Channel 2 and Channel 1, Respectively. These pins must be connected to V_{CC} through pull-up inductors. Typical DC current is 48mA into each pin.

PS (Pin 19): Parallel Select Pin for RF Input Tuning. A CMOS logic high will enable parallel control using the T1 and T0 pins. A CMOS logic low allows the SPI port to set the tuning for each channel independently, while ignoring the voltage on the T1 and T0 pins. This pin has an internal 330k pull-down resistor.

LO^-, LO^+ (Pins 20, 21): Differential Local Oscillator Input. These pins are internally connected to ESD diodes to ground. Therefore, series DC-blocking capacitors must be used if the LO source has a DC voltage present. Single-ended or differential drive may be used. Each pin is internally matched to 50Ω, even when the mixers are disabled.

V_{DD} (Pin 22): Power Supply Pin for Serial Interface Logic. This pin must be connected to a regulated 1.8V to 3.3V supply. Typical DC current consumption is less than 1mA with CSB low and the clock running at 10MHz. When idle, typical current consumption is less than 500µA. The supply voltage on this pin defines the logic levels for the SPI inputs (CSB, CLK and SDI), the SDO output, and the PS pin.

BLOCK DIAGRAM



TEST CIRCUIT

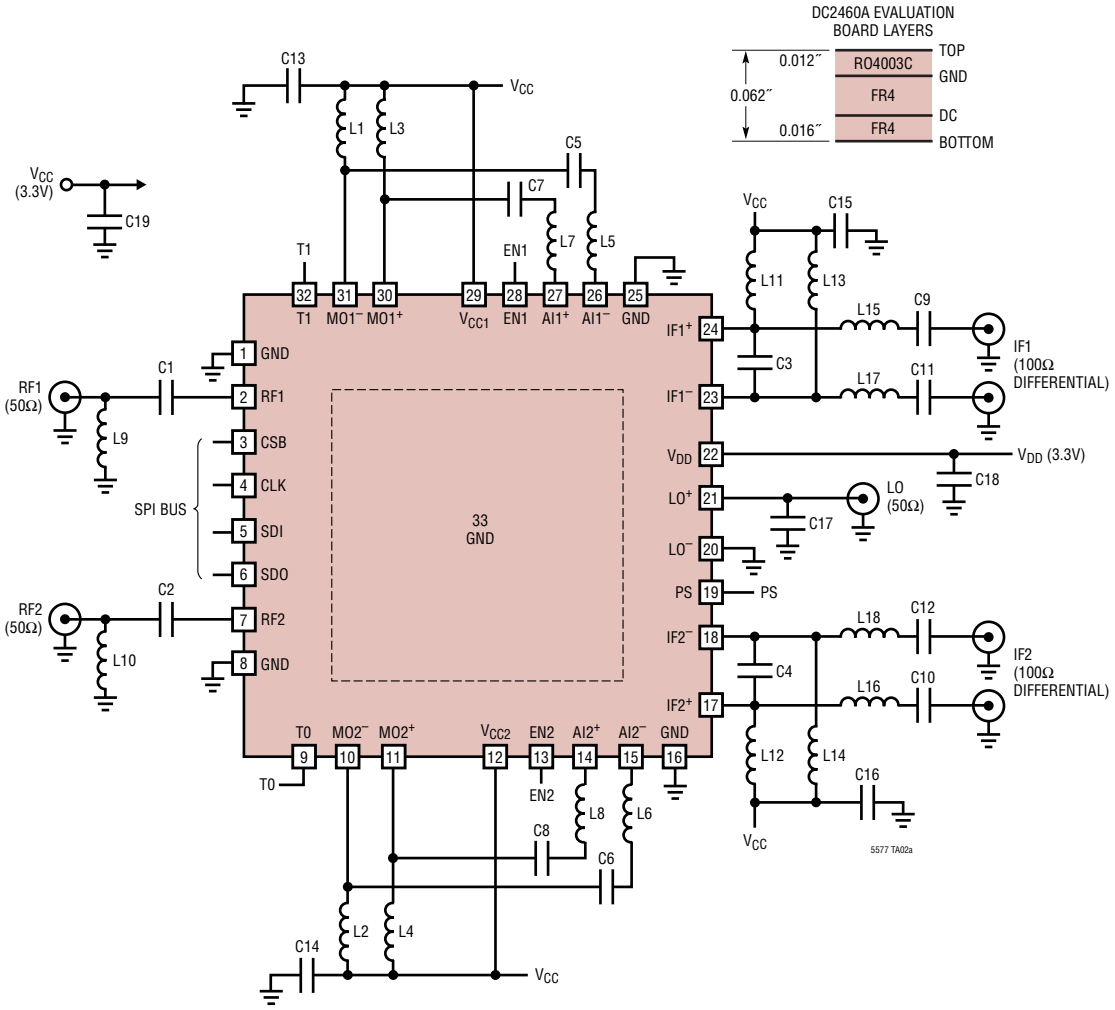


Figure 1. Test Circuit Schematic with 100Ω Matched Differential IF Outputs

RF INPUT TUNING AND EXTERNAL MATCHING						
		PARALLEL TUNE (PS = HIGH)		SERIAL TUNE (VIA SPI) (PS = LOW)		
RF BAND	RF FREQUENCY RANGE (Hz)	T1	T0	RT1[1:0], RT2[1:0]	C1, C2	L9, L10
B0	3.1G TO 5.1G	0	0	0	4.3pF	—
B1	1.8G TO 4.4G	0	1	1		
B2	1.3G TO 3.9G	1	0	2		
B3	0.7G TO 1.3G	1	1	3		8.2nH
B4	0.39G TO 0.53G	1	1	3	12pF	10nH

REF DES	VALUE	SIZE	VENDOR	REF DES	VALUE	SIZE	VENDOR
C18, C19	1µF	0603	Murata 50V X5R	C17	0.3pF	0201	Murata 25V NPO
C1, C2	See Table	0402	Murata 50V NPO	L1 TO L4, L11 TO L14	680nH	0603	Coilcraft 0603AF
C3, C4	2.2pF	0402	Murata 50V NPO	L5 TO L8	47nH	0402	Coilcraft 0402HP
C5 TO C8	1nF	0201	Murata 50V NPO	L9, L10	See Table	0402	Coilcraft 0402HP
C9 TO C16	10nF	0402	Murata 50V X7R	L15 TO L18	33nH	0402	Coilcraft 0402HP

APPLICATIONS INFORMATION

Introduction

The LTC5566 incorporates two identical RF-to-IF down-conversion mixers driven by a common LO input. The symmetry of the IC assures that both mixers are driven with an amplitude- and phase-coherent LO. Each channel includes an IF DVGA (digital variable gain amplifier) consisting of a programmable 15.5dB range digital IF attenuator with 0.5dB steps, and a fixed-gain IF buffer amplifier. The cascaded RF-to-IF conversion gain ranges from 12dB at maximum IF gain, to –3.5dB at minimum IF gain. The IF frequency response is flat within 1dB from 40MHz to 300MHz, and may be modified by adjusting the values of the external pull-up inductors.

The RF inputs have programmable impedance tuning which may be controlled via the SPI or dedicated control lines. Each channel can be programmed to a reduced power mode via the SPI, resulting in a 22% power savings, with reduced linearity performance. The test circuit schematic in Figure 1 shows the external components used to characterize the IC. The evaluation board is shown in Figure 2.

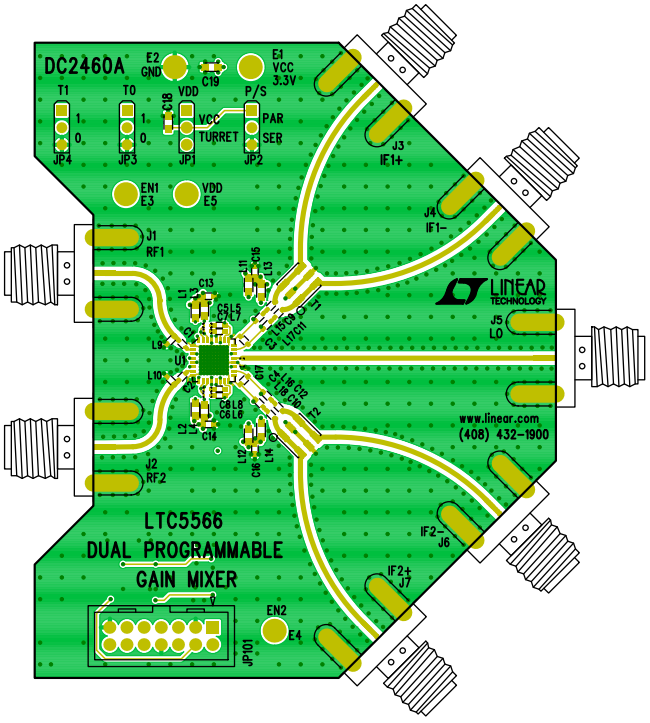


Figure 2. Evaluation Board

RF Inputs

A block diagram of the channel 1 RF input is shown in Figure 3 (channel 2 is identical and not shown). Each RF input includes programmable 2-bit RF frequency tuning, followed by an integrated transformer and a differential RF buffer amplifier. The transformer's primary winding is biased at 1.65V_{DC}, and therefore requires an external DC-blocking capacitor.

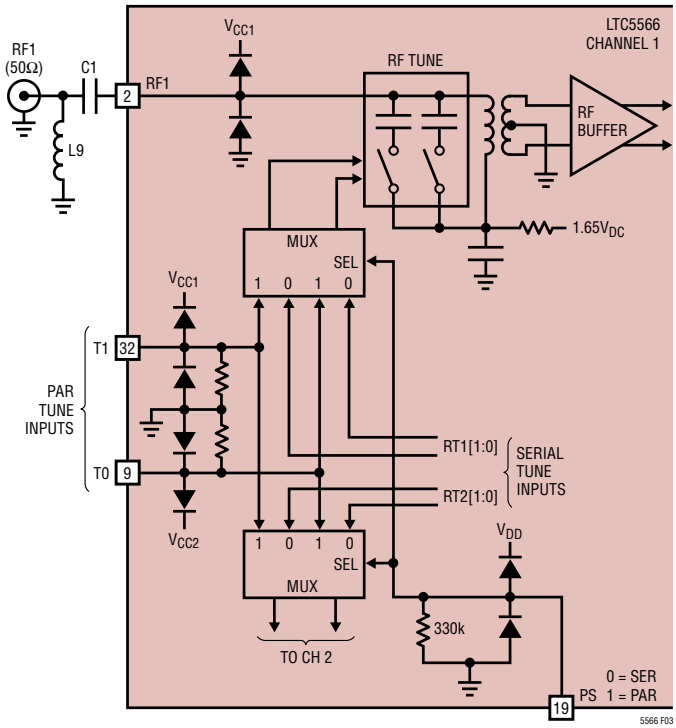


Figure 3. RF Input Block Diagram

The RF input impedance match for each channel is tuned to one of three overlapping frequency bands ranging from 1.3GHz to 5GHz, by programming the RT1[1:0] and RT2[1:0] bits (two bits for each channel). Series matching capacitor, C1, is fixed at 4.3pF for these three bands. For RF frequencies below 1.3GHz, the fourth (lowest frequency) tuning band is used in conjunction with shunt inductor L9.

APPLICATIONS INFORMATION

Figure 1 summarizes the RF tuning and external matching for all frequency bands. The RF input return loss for each band is shown in Figure 4.

As shown in Figure 3, the RF input tuning may also be controlled by the parallel control lines T0 and T1 when the PS (parallel select) control line is high. The tuning bits for this method are also summarized in Figure 1, where T0 is the LSB. When using parallel tuning control, both channels are tuned to the same band simultaneously and the SPI tuning bits are ignored. The T0 and T1 control lines have internal 167k pull-down resistors and the PS pin has an internal 330k pull-down resistor. All three pins will be pulled low if left floating, allowing the SPI to control the RF tuning, although it is recommended to ground these pins if SPI control is used.

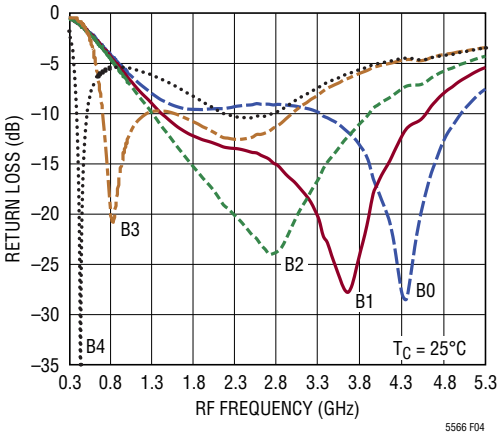


Figure 4. RF Input Return Loss for Each Band

LO Input

A simplified schematic of the LO input is shown in Figure 5. As shown, each mixer has its own LO amplifier. A differential input is provided although the IC is characterized and production-tested with single-ended drive. Differential LO drive improves performance slightly, and is recommended if available. Each LO input is internally matched to 50Ω from 150MHz to 3.8GHz, requiring no external components. Adding shunt capacitor C17(0.3pF), extends the LO input match up to 6GHz. ESD protection diodes on each input limit the peak voltage swing to approximately ±700mV (+7dBm), although higher LO drive, up to 10dBm will not damage the input. An external DC-blocking capacitor is only needed if the LO source has DC voltage present. The measured LO input return loss is shown in Figure 6, with and without C17.

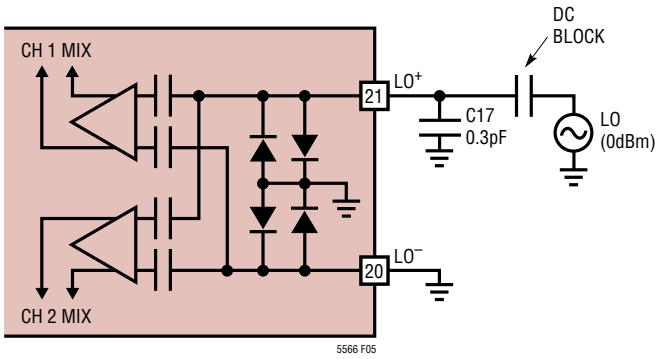


Figure 5. LO Input Schematic

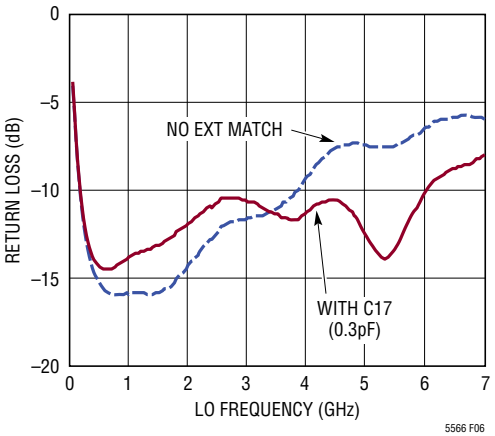


Figure 6. LO Input Return Loss

APPLICATIONS INFORMATION

IF Outputs

A simplified IF output schematic for channel 1, with external matching components is shown in Figure 7 (channel 2 is identical, and not shown). The final output stage is differential, open-collector with integrated matching resistors, capacitors and ESD protection diodes. Each output pin must be biased at the supply voltage (V_{CC}) using external chokes (L11 and L13). Each pin draws approximately 48mA of DC supply current (96mA total). Therefore, inductors with low DC resistance (<1Ω), are required for the highest output IP3 and P1dB.

The integrated output resistors set the differential output resistance at 206Ω. C3, L15 and L17 form a 2:1 impedance transformer which transforms the output to 100Ω differential. If a 200Ω output is desired, C3 is not used and the values of L15 and L17 are reduced to the values shown in Table 1. C9 and C11 are DC-blocking capacitors, which may be omitted if the following stage is already DC-blocked.

The standard evaluation board is built with 100Ω differential IF outputs, but also has pads which allow the use of IF transformers to provide 50Ω single-ended outputs. To implement this, it is recommended to use the 200Ω matching shown in Table 1 and 4:1 IF transformers. Figure 16 shows the circuit schematic and measured performance using this approach.

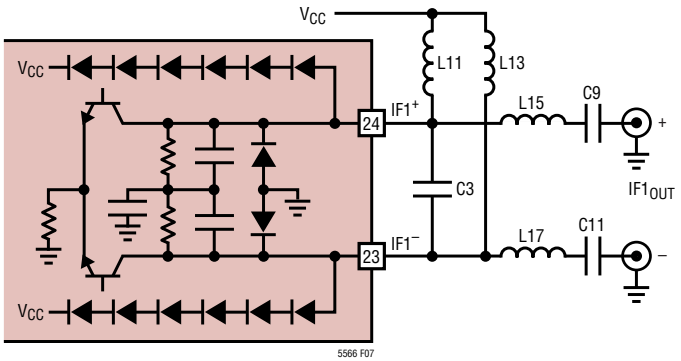


Figure 7. IF Output Schematic

Table 1. IF Output Matching Element Values

DIFFERENTIAL Z_{OUT}	C3	L15, L17	9dB RETURN LOSS BANDWIDTH
200Ω*	—	15nH	30MHz to 440MHz
100Ω	3.9pF	47nH	70MHz to 242MHz
	2.2pF	33nH	87MHz to 352MHz
	1.5pF	24nH	105MHz to 450MHz

*200Ω differential output return loss measured with 4:1 transformer on evaluation board.

The differential IF output impedance vs frequency is listed in Table 2. The impedances are at the package pins with no external components. Measured IF output return losses vs frequency for 100Ω differential matching is shown in Figure 8.

Table 2. Differential IF Output Impedance vs Frequency

IF FREQUENCY (MHz)	DIFFERENTIAL IMPEDANCE (R_{IF} || C_{IF})
10	210 || 1.10pF
50	209 || 1.09pF
100	209 || 1.04pF
150	208 || 0.97pF
200	207 || 0.94pF
300	206 || 0.92pF
400	203 || 0.93pF
500	200 || 0.91pF
600	196 || 0.91pF
700	192 || 0.91pF
800	186 || 0.91pF
900	179 || 0.90pF
1000	172 || 0.89pF

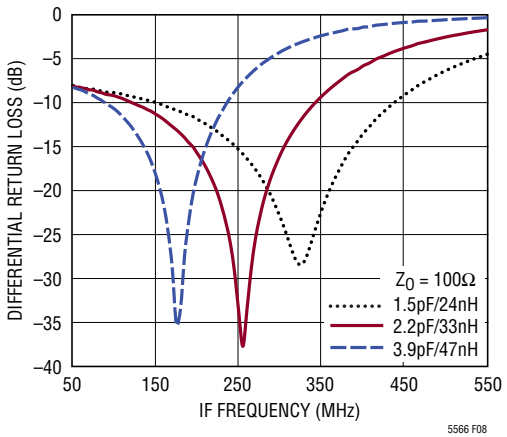


Figure 8. IF Output Return Loss (100Ω Differential Matching)

APPLICATIONS INFORMATION

Mixer Output to IF DVGA Interface

The mixer's 300Ω differential output impedance matches the IF DVGA's 300Ω differential input impedance, even over normal process variation due to the monolithic implementation. This assures minimal and repeatable DNL and INL over the full IF attenuation range. Furthermore, the mixer output and DVGA input include integrated matched capacitors, which simplify the realization of a lowpass filter between the mixer and DVGA. This filter attenuates undesired high frequency mixing products and LO leakage before entering the DVGA.

A simplified schematic of the interface for channel 1 is shown in Figure 9 (channel 2 is identical and not shown). L5 and L7 connect the mixer output to the DVGA input, while forming a 650MHz 3rd-order, 0.2dB ripple Chebyshev lowpass filter. L1 and L3 supply DC current to the mixer and C5 and C7 are DC-blocking capacitors.

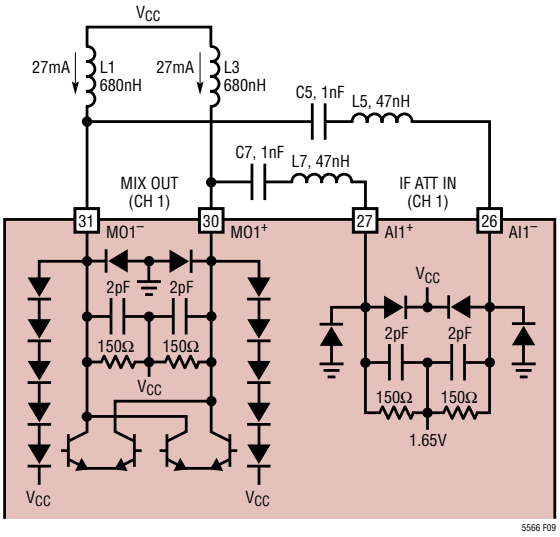


Figure 9. Mixer to IF DVGA Interface

An equivalent AC schematic of the lowpass filter is shown in Figure 10, where the mixer output and DVGA input are modeled as 300Ω in parallel with 1pF. The mixer supply chokes and series DC blocking capacitors are ignored in this schematic.

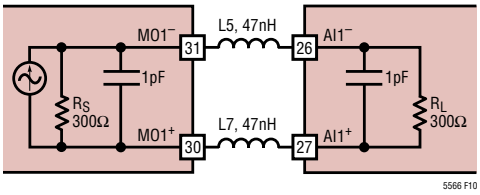


Figure 10. Equivalent Lowpass Filter Schematic

It's also possible to implement a bandpass filter between the mixer and DVGA. An example is shown in Figure 11, where a 3rd-order bandpass filter is realized by changing the values of the reactive components and adding C21, C23 and L19. Figure 19 shows measured conversion gain vs IF output frequency using this bandpass topology.

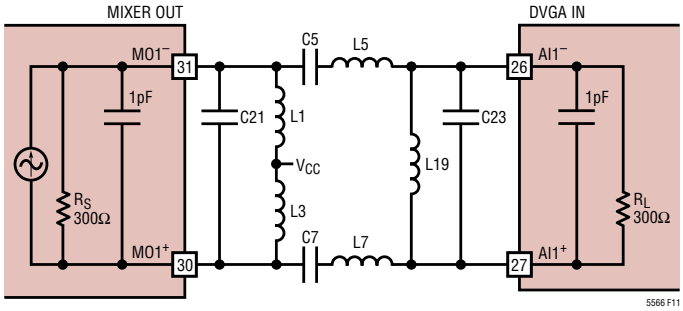


Figure 11. 3rd-Order Bandpass Filter Realization

IF DVGA Phase vs IF Attenuation

Ideally, the phase of the IF output would be constant over the full IF attenuation range. Practically, there is some phase shift due to circuit parasitics in the attenuator. The LTC5566's IF DVGA is optimized for the lowest possible phase variation (or phase error) over the full IF attenuation range. Phase error vs IF attenuation for the complete IF section is listed in Table 3.

Table 3. IF Phase Error vs IF Attenuation

ATT (dB)	150MHz	250MHz	350MHz
0	REF	REF	REF
3	–1.1°	–1.4°	–3.0°
6	–1.6°	–2.1°	–4.2°
9	–2.0°	–2.8°	–5.1°
12	–2.2°	–3.2°	–5.3°
15	–2.4°	–3.0°	–5.5°

APPLICATIONS INFORMATION

Downconverter Performance vs IF Attenuation

RF-IF conversion gain, IIP3, OIP3 and noise figure over the full 15.5dB attenuation range is shown in Figure 12. The same data is listed in Table 4 with the INL and DNL at each attenuator setting.

Table 4. Conversion Gain, IIP3, OIP3 and SSB NF vs IF Attenuation (RF = 2.6GHz, IF = 153MHz, High Side LO)

A (dB)	IF1[4:0] IF2[4:0]	G_C (dB)	IIP3 (dBm)	OIP3 (dBm)	NF (dB)	DNL (dB)	INL (dB)
0	0	11.84	23.2	35.0	13.3	—	—
0.5	1	11.32	23.3	34.6	13.4	0.03	0.03
1.0	2	10.75	23.4	34.2	13.6	0.07	0.09
1.5	3	10.24	23.6	33.8	13.7	0.01	0.10
2.0	4	9.75	24.0	33.8	13.8	–0.01	0.09
2.5	5	9.24	24.2	33.5	13.9	0.01	0.10
3.0	6	8.75	24.6	33.4	14.1	–0.01	0.09
3.5	7	8.24	24.9	33.2	14.2	0.01	0.11
4.0	8	7.75	25.1	32.8	14.4	–0.01	0.10
4.5	9	7.24	25.5	32.8	14.6	0.01	0.11
5.0	10	6.75	25.7	32.4	14.8	–0.01	0.10
5.5	11	6.23	25.9	32.1	15.0	0.01	0.11
6.0	12	5.75	26.1	31.8	15.3	–0.01	0.10
6.5	13	5.23	26.5	31.7	15.5	0.01	0.11
7.0	14	4.74	26.4	31.1	15.7	–0.01	0.10
7.5	15	4.22	26.9	31.1	15.9	0.03	0.13
8.0	16	3.73	26.7	30.4	16.2	–0.02	0.11
8.5	17	3.21	27.1	30.4	16.5	0.02	0.14
9.0	18	2.73	26.9	29.6	16.9	–0.02	0.12
9.5	19	2.20	27.4	29.6	17.2	0.03	0.14
10.0	20	1.72	27.1	28.8	17.5	–0.02	0.13
10.5	21	1.20	27.6	28.8	17.8	0.02	0.15
11.0	22	0.71	27.3	28.0	18.2	–0.01	0.14
11.5	23	0.18	27.5	27.7	18.6	0.02	0.16
12.0	24	–0.31	27.6	27.3	19.0	–0.01	0.15
12.5	25	–0.84	27.8	27.0	19.4	0.03	0.18
13.0	26	–1.33	27.3	26.0	19.8	–0.02	0.17
13.5	27	–1.85	27.9	26.1	20.2	0.03	0.19
14.0	28	–2.35	28.0	25.7	20.7	0.00	0.19
14.5	29	–2.87	28.2	25.3	21.1	0.02	0.21
15.0	30	–3.36	28.0	24.6	21.5	0.00	0.20
15.5	31	–3.89	28.1	24.2	22.0	0.03	0.23

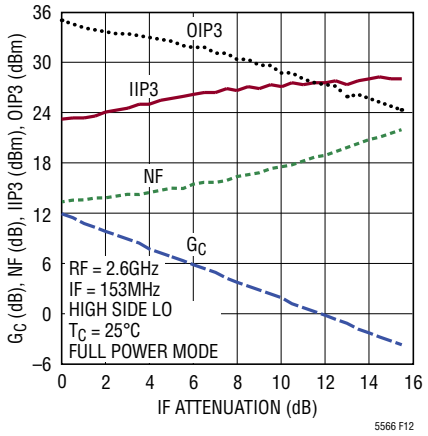


Figure 12. Downconverter RF-IF Conversion Gain, IIP3, OIP3 and Noise Figure vs IF Attenuation.

Individual Stage Performance

The LTC5566 is characterized, specified and production-tested as a complete downconverter, from the RF inputs to the final IF outputs. For some applications, it may be preferred to insert a higher selectivity IF filter between the mixer and IF DVGA. To help with system performance calculations, the nominal performance of the mixer is shown in Table 5 and the IF DVGA performance is listed in Table 6. This information is provided for reference only as these blocks are not production-tested independently.

Table 5. Mixer Power Conversion Gain, IIP3 and SSB NF (RF = 2.6GHz, IF = 153MHz, High Side LO, Band 1 RF Tune)

FULL PWR MODE			REDUCED PWR MODE		
G_P (dB)	IIP3 (dBm)	NF (dB)	G_P (dB)	IIP3 (dBm)	NF (dB)
–0.5	28.0	12.2	–0.7	23.0	11.8

Table 6. IF DVGA Power Gain, OIP3 and SSB NF (153MHz)

IF ATT (dB)	FULL PWR MODE			REDUCED PWR MODE		
	GAIN (dB)	OIP3 (dBm)	NF (dB)	GAIN (dB)	OIP3 (dBm)	NF (dB)
0	12.0	36.4	5.7	11.8	33.2	5.6
3	9.0	35.7	9.3	8.8	33.0	9.3
6	6.0	35.7	12.3	5.8	33.1	12.3
9	3.0	35.7	15.4	2.8	32.9	15.3
12	0.0	35.4	18.4	–0.2	32.9	18.4
15	–3.0	35.0	21.4	–3.2	32.7	21.4

APPLICATIONS INFORMATION

Enable Inputs

Figure 13 shows a schematic of the Channel 1 enable interface. Channel 2 is identical and not shown. As shown, the positive ESD diodes for EN1 are connected to V_{CC1}. The positive ESD diodes for channel 2 are connected to V_{CC2} (not shown). To enable a channel, the applied voltage must be greater than 1.4V. An applied voltage less than 0.5V will disable the channel. If the enable function is not needed, the enable pin can be connected directly to the adjacent V_{CC} pin. If left floating, the internal 330kΩ pull-down resistor will disable the channel.

The voltage on the enable pins should never exceed V_{CC} by more than 0.3V, otherwise supply current may be sourced through the upper ESD diodes. Under no circumstances should voltage be applied to the enable pins before supply voltage is applied to the V_{CC} pins. If this occurs, damage to the IC may result.

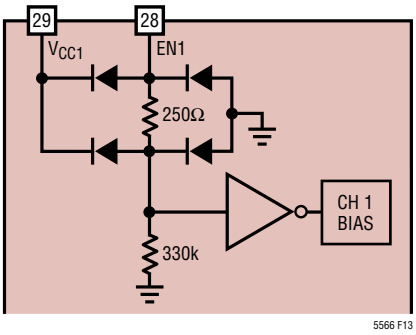


Figure 13. Channel 1 Enable Pin Interface

Supply Voltage Ramping

Fast ramping of the supply can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage transient that exceeds the maximum rating. A supply voltage ramp time greater than 1ms is recommended.

SPI DESCRIPTION

IF DVGA attenuator control, RF input tuning and reduced power mode for each downconverter channel is programmed through the 3-wire SPI consisting of CSB, CLK and SDI. A fourth pin, SDO, is a serial output available to read out the contents of the registers. The SDO pin may also be used to daisy-chain multiple SPI interfaces on a single bus. For example, in an 8-channel MIMO receiver application, all four LTC5566 dual downconverters can be programmed with a single, 64-bit load, while sharing a common CSB line.

A block diagram of the SPI is shown in Figure 14. As shown, it is a 16-bit double-buffered FIFO slave architecture, with 8-bits for each channel. Logic levels for the digital inputs and SDO output are 1.8V to 3.3V CMOS compatible, determined by the supply voltage on the V_{DD} pin. An internal POR (power-on-reset) connected to the V_{DD} pin, resets all 16 bits to logic 0 at power-up, or when V_{DD} drops below 0.9V and then rises back above 1.2V. The POR requires approximately 100µs to reset the registers.

SPI PROGRAMMING

Data transfers to the part are accomplished by first taking CSB low to enable the port. Then, serial input data on SDI is captured on the rising edge of CLK and shifted into a 16-bit shift register, MSB first. Serial data from the registers is driven out to SDO on the clock's falling edge. The communication burst is terminated by taking CSB high. The rising edge on CSB will then latch the shift-register's contents into a 16-bit buffer D-latch. The buffer latch prevents the downconverter's gain, RF input tuning and power mode from changing while data is loaded. See Figure 15 for timing details.

When CSB is high, the clock and data inputs are internally gated off, minimizing current consumption when not selected, and the SDO output is high impedance. However, it is recommended that the serial interface signals should remain idle between data transfers to avoid digital noise coupling into the RF signal paths.

APPLICATIONS INFORMATION

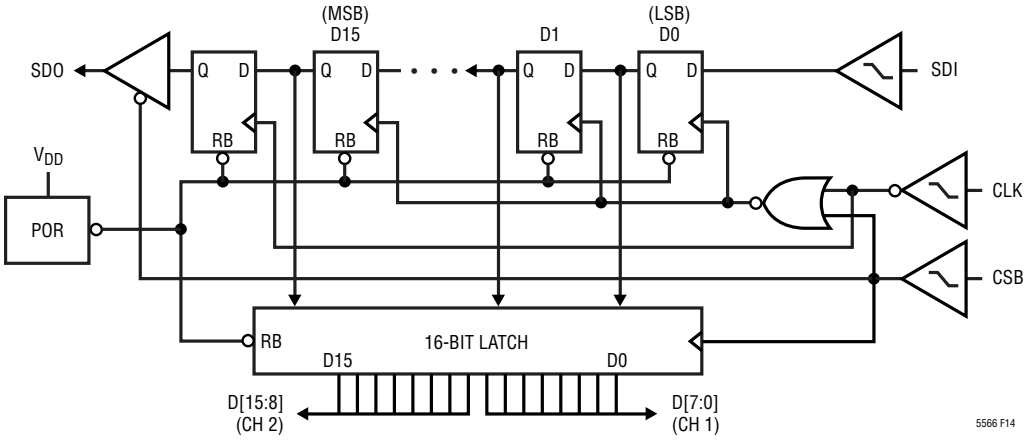


Figure 14. SPI Block Diagram

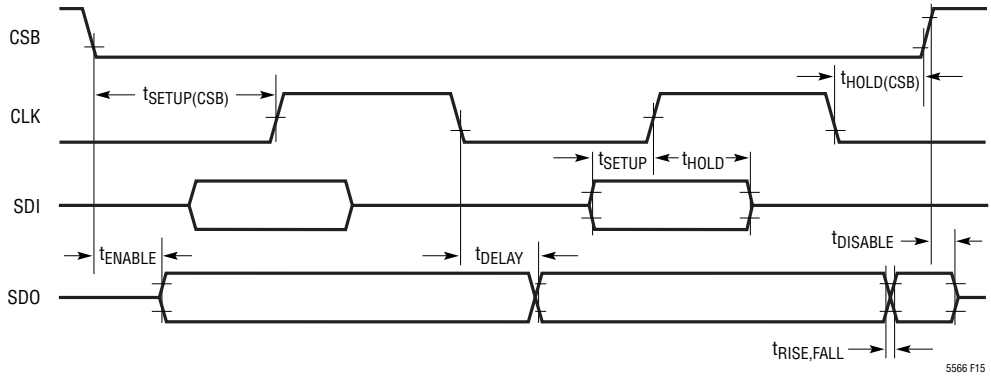


Figure 15. SPI Timing Diagram

APPLICATIONS INFORMATION

A memory map of the register contents is shown in Table 7, with detailed bit descriptions in Table 8. Each register's default power-up value is also shown in Table 8, which is:

- 0dB IF attenuation (maximum gain)
- Full power mode
- RF inputs tuned to band 0 (highest frequency)

Table 7. Serial Port Register Contents

CHANNEL 2 (8 bits)							
MSB D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
RP2	RT2[1]	RT2[0]	IF2[4]	IF2[3]	IF2[2]	IF2[1]	IF2[0]

CHANNEL 1 (8 bits)							
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**LSB D0**
RP1	RT1[1]	RT1[0]	IF1[4]	IF1[3]	IF1[2]	IF1[1]	IF1[0]

Table 8. Serial Port Register Bit Field Summary

BITS	DESCRIPTION	DEFAULT
IF1[4:0]	Ch. 1 IF Attenuator Control	00000 (Max Gain)
RT1[1:0]	Ch. 1 RF Tuning	00 (Band 0)
RP1	Ch. 1 Reduced Power	0 (Full Power)
IF2[4:0]	Ch. 2 IF Attenuator Control	00000 (Max Gain)
RT2[1:0]	Ch. 2 RF Tuning	00 (Band 0)
RP2	Ch. 2 Reduced Power	0 (Full Power)

Spurious Output Levels

Spurious output levels vs harmonics of the RF and LO are tabulated in Table 9. The spur levels were measured using the test circuit shown in Figure 1, with an RF input power of –6dBm and 6dB of IF attenuation. Table 9a shows the relative spur levels in full power mode and Tables 9b shows the relative spur levels in reduced power mode. The mixer spur levels are insensitive to the IF attenuation setting.

The spur frequencies can be calculated using the following equation:

$$f_{SPUR} = (M \bullet f_{RF}) - (N \bullet f_{LO})$$

Table 9. IF Output Spur Levels (dBc).
($RF = 2.6GHz$, $P_{RF} = -6dBm$, $IF = 153MHz$, High Side LO, $P_{LO} = 0dBm$, 6dB IF Attenuation, $T_C = 25°C$)
Table 9a. Full Power Mode

		N							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
M	**0**		–52	*	*	–80	–79	–79	*
	1	*	0	*	*	*	*	–80	–80
	2	*	*	–68	*	*	*	*	–80
	3	*	*	*	–77	*	*	*	*
	4	*	*	*	*	*	*	*	*
	5	*	*	*	*	*	*	*	*
	6	–80	*	*	*	*	*	*	*
	7	*	–80	*	*	*	*	*	*

*Less than –80dBc

Table 9b. Reduced Power Mode

		N							
		0	**1**	**2**	**3**	**4**	**5**	**6**	**7**
M	**0**		–52	*	*	–80	–79	–78	*
	1	*	0	*	*	*	*	–80	–80
	2	*	*	–68	*	*	*	*	–79
	3	*	*	*	–72	*	*	*	*
	4	*	*	*	*	*	*	*	*
	5	*	*	*	*	*	*	*	*
	6	–79	*	*	*	*	*	*	*
	7	*	–80	*	*	*	*	*	*

*Less than –80dBc

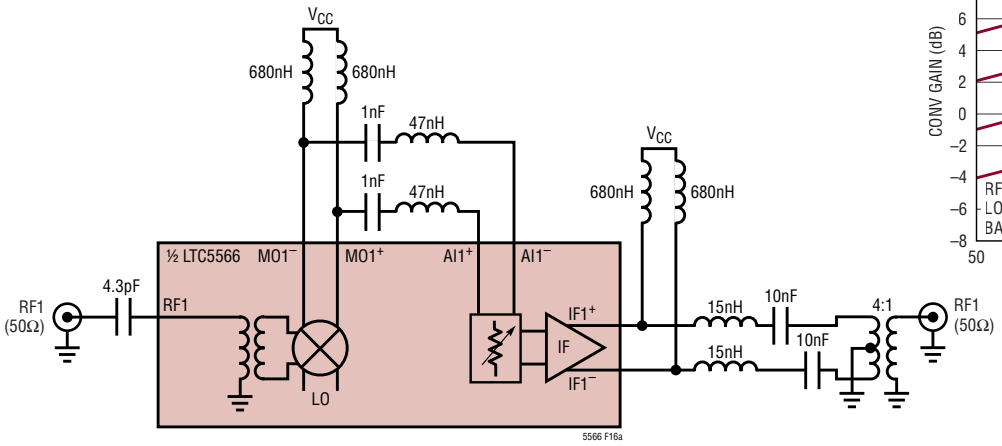
RF and LO Port S-Parameters

S11 vs frequency for the RF and LO port are listed in Table 10. Data is shown for all four RF tuning states. The data is referenced to the IC pin with no external matching.

APPLICATIONS INFORMATION

Table 10. RF and LO Port S11

	RF INPUT								LO INPUT (SINGLE-ENDED)	
	RT = 00		RT = 01		RT = 10		RT = 11			
FREQ (MHz)	MAG	ANGLE (°)	MAG	ANGLE (°)	MAG	ANGLE (°)	MAG	ANGLE (°)	MAG	ANGLE (°)
200	0.77	–160.1	0.77	–160.1	0.77	–160.1	0.77	–160.1	0.29	–61.1
300	0.72	179	0.71	178	0.72	178	0.71	178	0.21	–63.5
400	0.68	167	0.65	167	0.67	167	0.66	167	0.18	–65.2
500	0.64	160	0.61	160	0.63	160	0.62	160	0.17	–66.2
600	0.61	154	0.57	155	0.60	154	0.59	155	0.16	–68.7
700	0.60	149	0.55	150	0.58	149	0.56	150	0.16	–71.8
800	0.58	146	0.52	147	0.56	146	0.54	146	0.16	–75.0
900	0.57	142	0.49	144	0.54	142	0.52	143	0.16	–77.9
1000	0.56	139	0.47	142	0.53	139	0.50	140	0.16	–81.3
1500	0.51	124	0.36	136	0.46	126	0.40	130	0.16	–102.8
2000	0.46	110	0.26	143	0.37	113	0.29	124	0.19	–128.6
2500	0.39	91.5	0.24	165	0.26	100	0.19	133	0.24	–142.9
3000	0.32	68.7	0.31	172	0.14	89	0.17	160	0.26	–154.6
3500	0.24	40.0	0.38	167	0.04	119	0.23	172	0.28	–175.1
4000	0.11	–3.0	0.47	158	0.15	–174	0.34	168	0.35	165.4
4500	0.11	–139	0.54	148	0.30	174	0.45	157	0.42	156.9
5000	0.29	173	0.58	139	0.43	158	0.52	147	0.42	147.3
5500	0.40	153	0.61	135	0.50	147	0.57	141	0.43	127.5
5800	0.46	137	0.65	129	0.55	137	0.61	133	0.45	115.0
6000	0.48	128	0.66	125	0.56	130	0.62	129	0.47	108.8



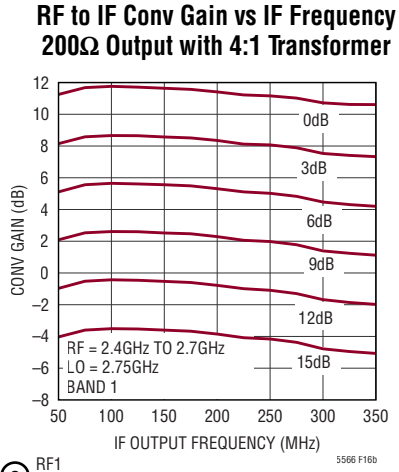


Figure 16. Test Circuit and Measured Conversion Gain Using 200Ω Output Matching with a 4:1 IF Transformer to Realize a 50Ω Single-Ended IF Output

TYPICAL APPLICATIONS

5.8GHz RF Application

The LTC5566's RF inputs are optimized for operation up to 5GHz, but may be used up to 6GHz with degraded performance. Figure 17 shows an example where the RF input is matched for 5.8GHz operation. The RF tuning bits are set to RT1[1:0] = 00 for the lowest internal capacitance (i.e. highest frequency operation). The measured performance is summarized in Figure 18.

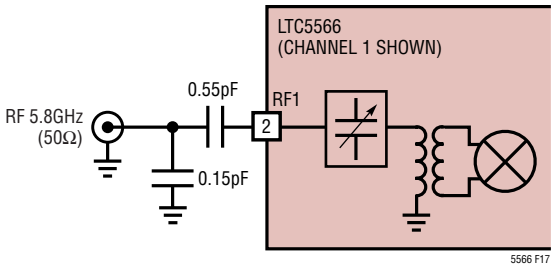
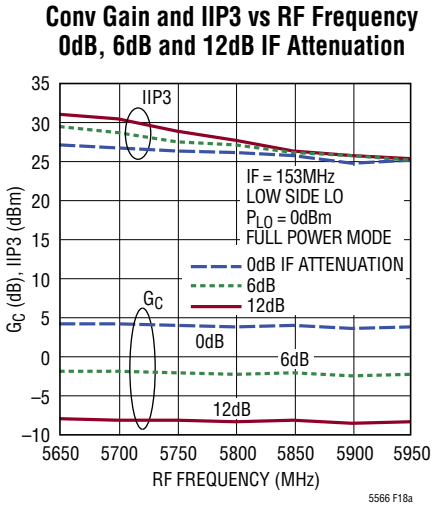
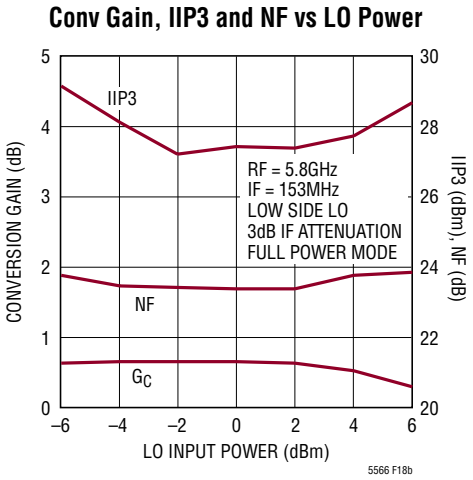


Figure 17. 5.8GHz Input Matching





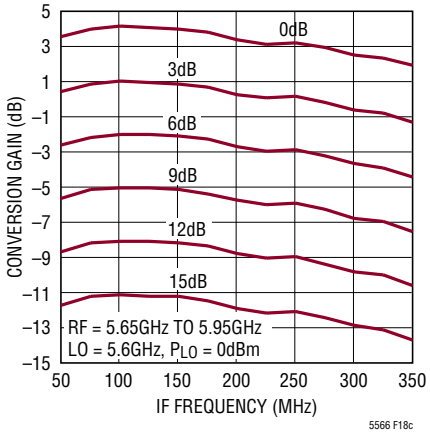
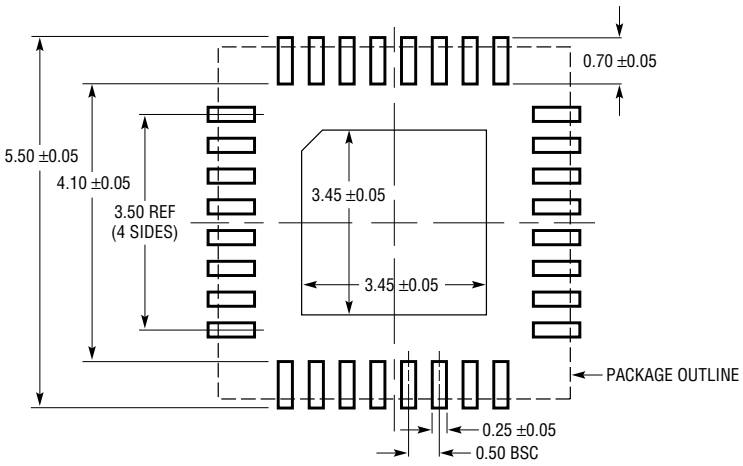


Figure 18. Measured Performance Using 5.8GHz RF Input Matching

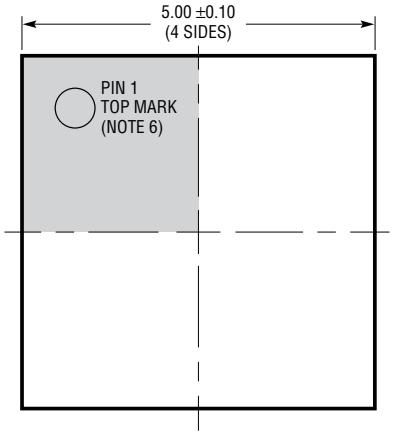
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC5566#packaging for the most recent package drawings.

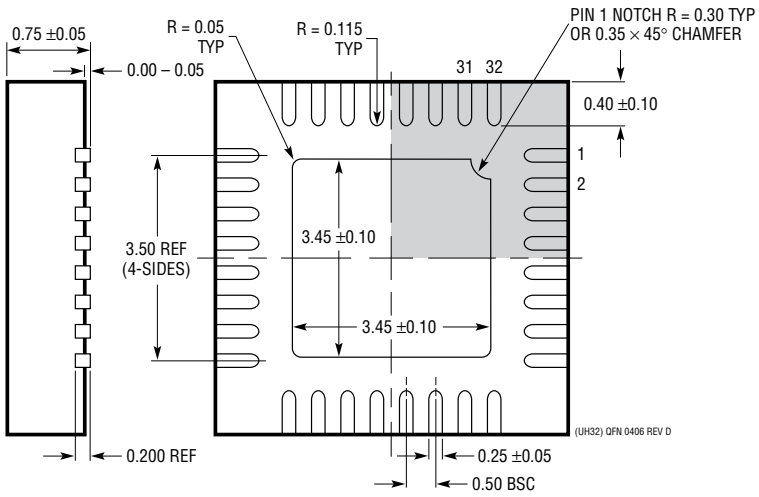
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

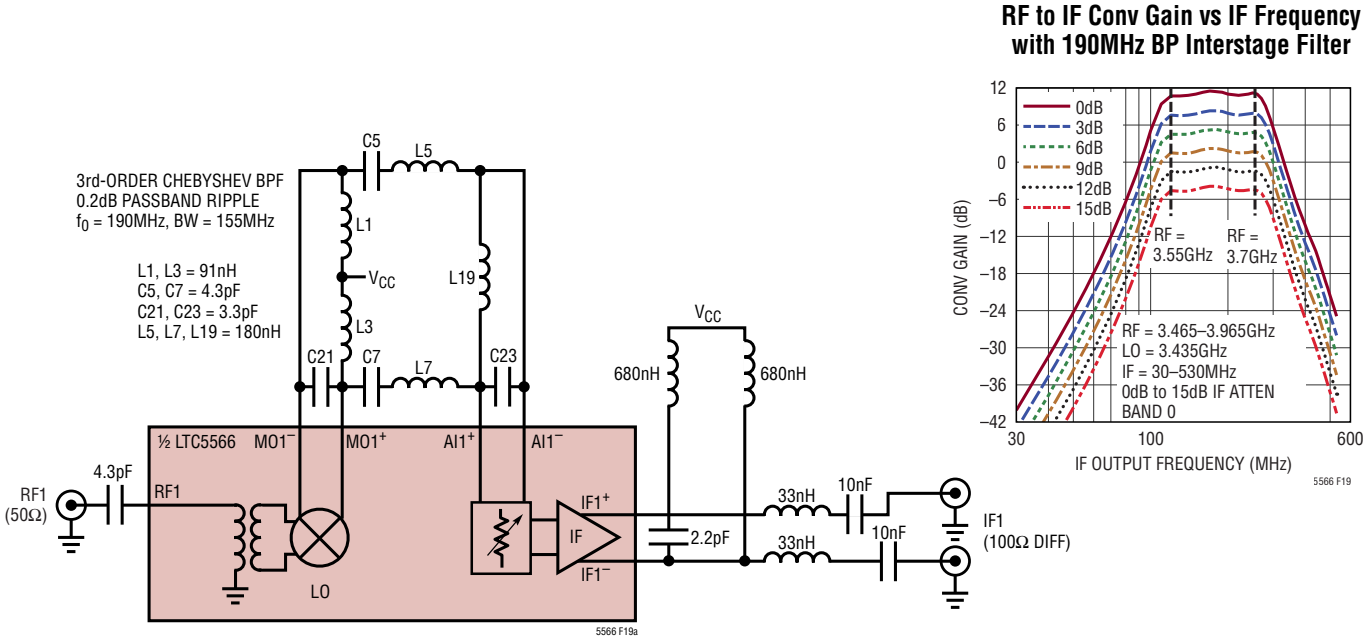


Figure 19. Test Circuit and Measured Conversion Gain with 3rd-Order Bandpass Interstage Filter

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
Infrastructure		
LTC5569	300MHz to 4GHz Dual Active Downconverting Mixer	2dB Gain, 26.7dBm IIP3 and 11.7dB NF at 1950MHz, 3.3V/180mA Supply
LTC6430	High Linearity Differential RF/IF Amplifier	51dBm OIP3 at 240MHz, 100Ω Differential
LTC6409	10GHz GBW Differential Amplifier	DC-Coupled, 48dBm OIP3 at 140MHz, 1.1nV/√Hz Input Noise Density
LTC6412	31dB Linear Analog VGA	35dBm OIP3 at 240MHz, Continuous Gain Range –14dB to 17dB
LTC5544	4GHz to 6GHz Downconverting Mixer Family	7.4dB Gain, >25dBm IIP3, 11.3dB NF, 3.3V/200mA Supply
LT5554	Ultralow Distortion IF Digital VGA	48dBm OIP3 at 200MHz, 2dB to 18dB Gain Range, 0.125dB Gain Steps
LTC5576	3GHz to 8GHz Active Upconverting Mixer	25dBm OIP3, –0.6dB Gain, –154dBm/Hz Output Noise Floor, –36dBm LO Leakage
LTC5548	2GHz to 14GHz Wideband Microwave Mixer	Up- or Down-Conversion, 21.4dBm IIP3 at 9GHz, 0dBm LO Drive, IF Bandwidth DC to 6GHz
LTC5549	2GHz to 14GHz Wideband Microwave Mixer	Up- or Down-Conversion, 22.8dBm IIP3 at 12GHz, 0dBm LO Drive, Integrated Balun with IF BW = 500MHz to 6GHz
LTC5593	Dual 2.3GHz to 4.5GHz Downconverting Mixer	8.5dB Gain, 27.7dBm IIP3, 9.5dB Noise Figure
RF PLL/Synthesizer with VCO		
LTC6946	Low Noise, Low Spurious Integer-N PLL with Integrated VCO	373MHz to 5.79GHz, –157dBc/Hz WB Phase Noise Floor, –100dBc/Hz Closed-Loop Phase Noise
LTC6948	Low Noise, Low Spurious Frac-N PLL with Integrated VCO	373MHz to 6.39GHz, –157dBc/Hz WB Phase Noise Floor, –274dBc/Hz Normalized In-Band 1/f Noise
ADCs		
LTC2145-14	14-Bit, 125Msps 1.8V Dual ADC	73.1dB SNR, 90dB SFDR, 95mW/Ch Power Consumption
LTC2185	16-Bit, 125Msps 1.8V Dual ADC	76.8dB SNR, 90dB SFDR, 185mW/Channel Power Consumption
LTC2158-14	14-Bit, 310Msps 1.8V Dual ADC, 1.25GHz Full-Power Bandwidth	68.8dB SNR, 88dB SFDR, 362mW/Ch Power Consumption, 1.32V_{P-P} Input Range

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC5566
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