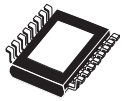
ALED8102S

Datasheet

8 channel LED driver with direct switch control



HTSSOP16
(Exposed pad)

Features

- 8 constant current output channels controlled by four switch inputs
- Output enable input for global dimming
- Output current: from 5 mA to 100 mA
- Current programmable through external resistor
- Supply voltage: 3 V to 5.5 V
- Thermal shutdown
- 20 V current generator rated voltage
- Available in high thermal efficiency HTSSOP exposed pad package
- ESD protection 2.0 kV HBM, 100 V MM

Applications

- Automotive LED interior and exterior lighting
  - Clusters
  - LCD back-light
  - Ambient light
  - Dome light
  - Rear combination light

Maturity status link
ALED8102S

Device summary	
Order code	ALED8102SXTTR
Package	HTSSOP16
Packing	2500 parts per reel

Description

The ALED8102S is a monolithic, low voltage, 8 low-side channels. The ALED8102S guarantees up to 20 V output driving capability allowing users to connect several LEDs in series. In the output stage, 8 regulated current sources provide from 5 mA to 100 mA constant current to drive the LEDs. Current is programmed though a single external resistor.

The ALED8102S is equipped with a thermal management that protects the device forcing it in shutdown (typically: power-off at 170 °C with 15 °C hysteresis to restart). The thermal protection switches OFF the output channels only.
The operative supply voltage range is between 3 V and 5.5 V. The output control is provided by four switch inputs, proving an on/off toggle action suitable also for local dimming. Moreover, on all active output LEDs brightness can be adjusted with a global PWM signal applied to the output enable pin ($\overline{OE}$). Outputs can be connected in parallel, or left unconnected if not used, as required by the application.

1 Pin description

Figure 1. Pinout for HTSSOP16

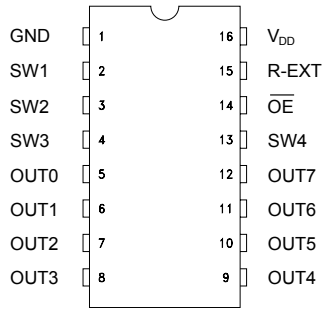
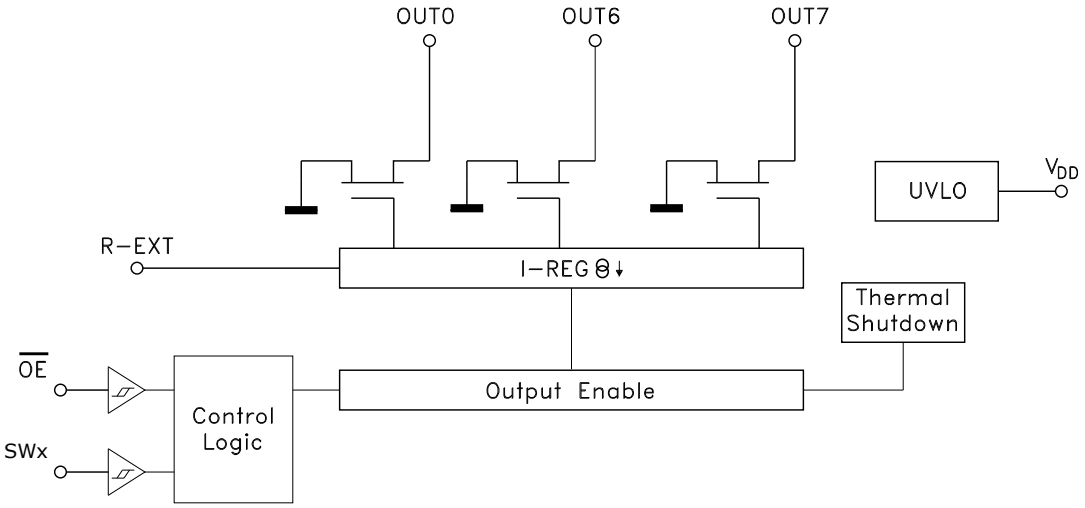


Table 1. Pin description

HTSSOP16	Symbol	Name and function
1	GND	Ground terminal
2	SW1	Providing local dimming capability
3	SW2	Providing local dimming capability
4	SW3	Providing local dimming capability
5-12	OUT0-OUT7	Output terminals
13	SW4	Providing local dimming capability
14	$\overline{OE}$	Global PWM brightness control input terminal (it must be connected to GND if not used)
15	R-EXT	Terminal for external resistor for constant current programming
16	V_{DD}	Supply voltage terminal

2 Simplified internal block diagram

Figure 2. **ALED8102S simplified block diagram**



3 Absolute maximum ratings

Stressing the device above the ratings listed in the table below may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	- 0.5 to 20	V
I_O	Output current	100	mA
V_I	Input voltage	-0.4 to V_{DD}	V
I_{GND}	GND terminal current	800	mA
ESD	Electrostatic discharge protection HBM human body model	±2	KV
	Electrostatic discharge protection MM machine model	100	V

3.1 Thermal characteristics

Table 3. Thermal characteristics

Symbol	Parameter	Value	Unit
T_J	Operative junction temperature range	-40 to +150	°C
T_{STG}	Storage ambient temperature range	-55 to +150	
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (HTSSOP16) (1)	37.5	°C/W

1. *The exposed pad should be soldered directly to the PCB to realize the thermal benefits.*

4 Electrical characteristics

V_{DD} = 5 V, T_j = -40 to 125 °C, R_{EXT} = 386 Ω, V_O = 0.85 V unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0	-	5.5	V
V_{UVLO}	UVLO threshold (rising)			2.7	2.9	
	UVLO threshold (falling)		2.1	2.3		
Hy_{UVLO}	UVLO hysteresis			0.4		
V_O	Output voltage (1)(2)	OUT0 – OUT7	0.85	-	19	
V_{IH}	SWx / $\overline{OE}$ input voltage		0.8V_{DD}	-	V_{DD}	
V_{IL}			GND	-	0.2V_{DD}	
R_{UP}	Pull-up resistor for $\overline{OE}$ pin		-	300	-	KΩ
R_{DW}	Pull-down resistor for SWx pins		-	310	-	
R_{EXT}	External current set-up resistance		-	-	3.9	
$I_{DD(OFF1)}$	Supply current (OFF)	OUT0 to 7 = OFF	-	7	8	mA
$I_{DD(OFF2)}$		R_{EXT} = 190 Ω OUT0 to 7 = OFF	-	14	16	
$I_{DD(ON)}$	Supply current (ON)	R_{EXT} = 190 Ω V_O = 1.4 V OUT0 to 7 = ON	-	14	16	
%/dV_O	Output current vs. outputvoltage regulation (1) (3)	V_O from 1 V to 3 V;	-	0.1	-	|%/V|
%/dV_{DD}	Output current vs. supply voltage regulation (1)(4)	V_{DD} from 3 V to 5.5 V	-	1	-	
ΔI_{OL}	Output current precision: chip to chip (1)		-	-	±6	%
ΔI_{OL1}	Output current precision: channel to channel (1) (5)		-	±1.5	±4	%
ΔI_{OL2}		V_O = 1.4 V; R_{EXT} = 190 Ω	-	±1.2	±4	
I_{Oleak}	Single output leakage current	V_O = 19 V OUTn = OFF	-	0.5	2	µA
T_{sd}	Thermal shutdown (6)			170		°C
T_{sd_hys}	Thermal shutdown hysteresis (6)			15		°C

1. *Test with just one output ON.*
2. *Minimum regulation voltage @ I_O = 50 mA.*
3. $\Delta\left(\%/V\right) = \frac{(Ion@Von3.0V) - (Ion@Von1.0V)}{(Ion@Von = 1.0V)} \times \frac{100}{3-1}$
4. $\Delta\left(\%/V\right) = \frac{(Ion@V_{DD} = 5.5V) - (Ion@V_{DD} = 3.0V)}{(Ion@V_{DD} = 3.0V)} \times \frac{100}{5.5-1}$
5. *((IOn – IOavg0-7)/ IOavg0-7) x 100.*
6. *Not tested in production.*

5 Switching characteristics

V_{DD} = 5 V, T_j = 25 °C, I_O = 50 mA, R_L = 60 Ω, C_L = 10 pF, V_L = 5 V, unless otherwise specified.

Table 5. Switching characteristics

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
t_{PLH1}	SWx – OUTn ($\overline{OE}$ just "0")	Propagation delay time ("L" to "H")	V_{DD} = 3.3 V	-	220	-	ns
			V_{DD} = 5 V	-	200	-	
t_{PLH2}	$\overline{OE}$ - OUTn (SWx just "1")	Propagation delay time ("L" to "H")	V_{DD} = 3.3 V	-	220	-	
			V_{DD} = 5 V	-	200	-	
t_{PHL1}	SWx – OUTn ($\overline{OE}$ just "0")	Propagation delay time ("H" to "L")	V_{DD} = 3.3 V	-	100	-	
			V_{DD} = 5 V	-	100	-	
t_{PHL2}	$\overline{OE}$ - OUTn (SWx just "1")	Propagation delay time ("H" to "L")	V_{DD} = 3.3 V	-	90	-	
			V_{DD} = 5 V	-	100	-	
t_{ON}	OUTn Current rise time. Evaluated as OUTn falling time		V_{DD} = 3.3 V	-	430	-	
			V_{DD} = 5 V	-	400	-	
t_{OFF}	OUTn current fall time. Evaluated as OUTn rising time		V_{DD} = 3.3 V	-	430	-	
			V_{DD} = 5 V	-	400	-	
$t_{W(OE)}$	Output enable minimum pulse width			1	-	-	µs

Figure 3. t_{ON} - t_{OFF} time evaluation

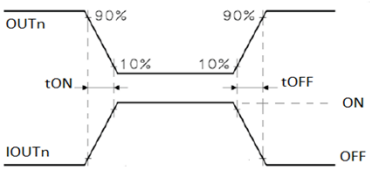
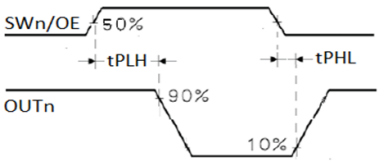


Figure 4. t_{PLH} - t_{PHL} time evaluation



6 Simplified internal block diagram

Inputs $\overline{OE}$ and SWx terminals have pull-up and pull-down connection respectively:

Figure 5. $\overline{OE}$ Terminal

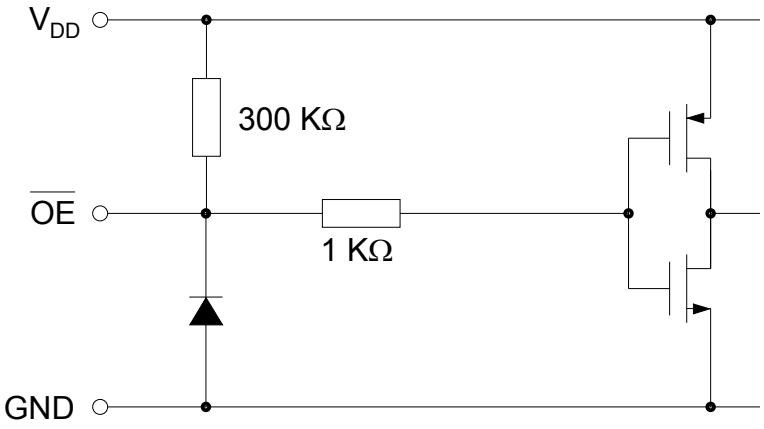
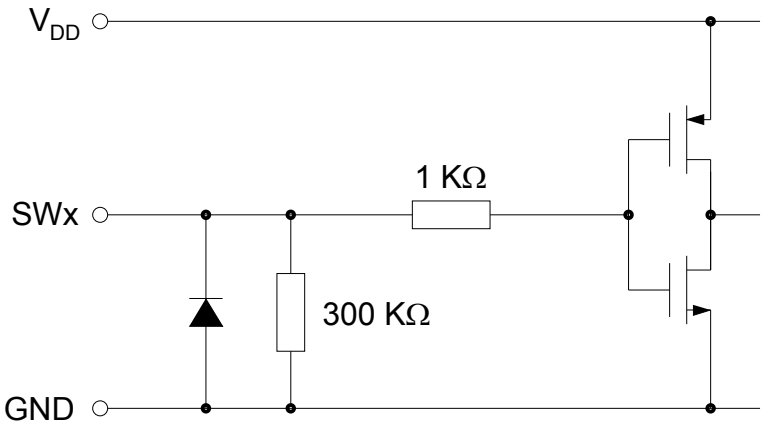


Figure 6. SWx Terminals



7 The switch output control

All switch inputs (SWx) are pulled down by a 300 kΩ. If the generic SWx pin is left floating or connected to GND or polarized at low logic level, the corresponding outputs are in OFF condition. If SWx pin is connected to V_{DD} or polarized at high logic level, the corresponding outputs are in ON condition. See below the complete truth table:

Table 6. Switch output control

Switch inputs	Outputs controlled (ON/OFF)
SW1	OUT0 and OUT1 simultaneously
SW2	OUT2 and OUT3 simultaneously
SW3	OUT4 and OUT5 simultaneously
SW4	OUT6 and OUT7 simultaneously

Table 7. Switches vs. output truth table

SW4	SW3	SW2	SW1	OE	Out0	Out1	Out2	Out3	Out4	Out5	Out6	Out7
0	0	0	0	x	off	off	off	off	off	off	off	off
0	0	0	1	0	on	on	off	off	off	off	off	off
0	0	1	0	0	off	off	on	on	off	off	off	off
0	0	1	1	0	on	on	on	on	off	off	off	off
0	1	0	0	0	off	off	off	off	on	on	off	off
0	1	0	1	0	on	on	off	off	on	on	off	off
0	1	1	0	0	off	off	on	on	on	on	off	off
0	1	1	1	0	on	on	on	on	on	on	off	off
1	0	0	0	0	off	off	off	off	off	off	on	on
1	0	0	1	0	on	on	off	off	off	off	on	on
1	0	1	0	0	off	off	on	on	off	off	on	on
1	0	1	1	0	on	on	on	on	off	off	on	on
1	1	0	0	0	off	off	off	off	on	on	on	on
1	1	0	1	0	on	on	off	off	on	on	on	on
1	1	1	0	0	off	off	on	on	on	on	on	on
1	1	1	1	0	on	on	on	on	on	on	on	on
x	x	x	x	1	off	off	off	off	off	off	off	off

8 Typical characteristics

Figure 7. I_{SET} vs. dropout voltage (V_{DROP} @ 25 °C)

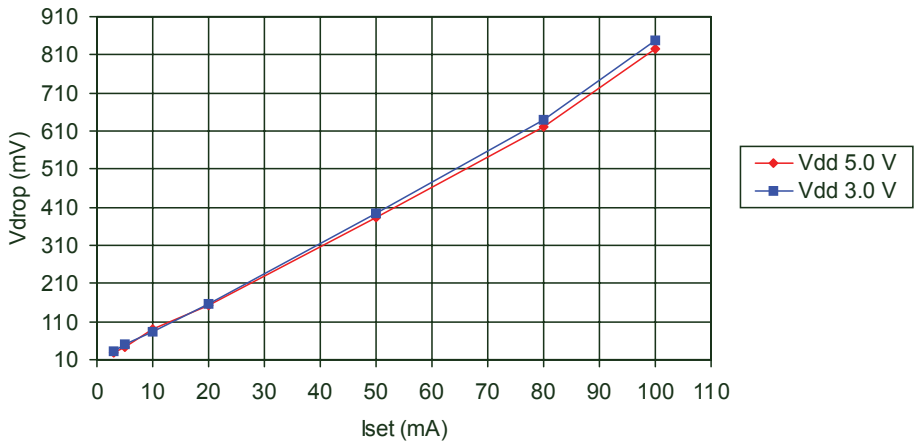
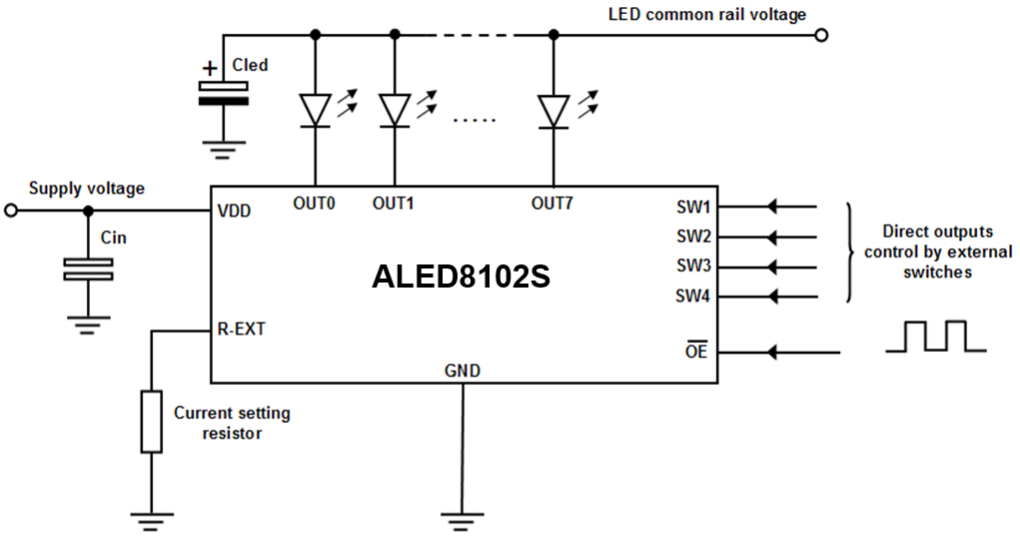


Table 8. Table settings

Vdd	Iset (mA)	Rext (Ω)	V_{DROP} min. (mV)	V_{DROP} max. (mV)	V_{DROP} AVG (mV)
3	5	3930	46.5	52.9	48.63
	10	1910	80.9	100	82.26
	20	963	150	161	157
	50	386	392	396	394.3
	80	241	636	646	640.3
	100	192	846	850	848
5	5	3930	40.8	41.7	41.16
	10	1910	80.1	105	89.2
	20	963	153	154	154
	50	386	379	386	382
	80	241	618	626	621
	100	192	825	830	827

9 Typical application

Figure 8. **Typical application circuit**



Typical application circuit

The figure above shows a typical application schematic for the ALED8102S, Cled value depends on common rail voltage connection length and driver total output current, typically it is around 47 µF; Cin is about 1 µF; current setting resistor depends on output current set (ex. with R_{EXT} = 386 Ω → I_O ≈ 50 mA). The external programming resistor between R-EXT and GND should be connected as close as possible to the device.

To have the proper device functionality, it is strongly suggested to follow a correct power-up sequence: V_{DD} and V_{LED} power supplies must be provided simultaneously or at least, V_{DD} must be connected before V_{LED} so to activate all internal digital control blocks earlier than LEDs power supply. If V_{LED} anticipates driver V_{DD}, this could result in a visible flash on connected LEDs (output stage undesired activation).

Device thermal management

The aim of this section is to provide some recommendation that can be useful to design the application PCB for a better power dissipation:

- To decrease the device working temperature, the package exposed pad needs soldering to the board.
- To improve thermal performance at least a 4-layer (e.g. 2S2P) PCB should be used.
- The copper area below the package thermal pad should be as wide as possible also outside the package perimeter (using the package sides without pins)
- A reasonable number of vias must connect the copper area below the package to all available PCB layers especially just below the device package (e.g. 3x3 or 4x3 vias array) but also outside the package perimeter. The smaller and closely spaced vias are, the better solution is. The best implementation is represented by copper filled vias.
- On each inner layer a copper area must be provided for dissipation (wider it is better, if possible at least 4 times or more the package dimensions). A good condition is to have at least a power layer as an entire copper area (e.g. GND layer)
- Traces for pin connection must be as wide as layout constrains allow
- Several devices in power dissipation on the same board must be properly spaced.

Figure 9 shows, once the maximum power dissipation is fixed, which ambient temperature range can be covered according to the maximum junction temperature and package thermal resistance: 37.5 °C/W for HTSSOP16 on

Jedec PCB (2S2P) and conditions. With the same thermal resistance, figure 10 shows the junction temperature as a function of ambient temperature considering 1 W of power dissipation.

Figure 9. Power dissipation rating vs. ambient temperature (R_{th} = 37.5 °C/W; T_j = 125 °C)

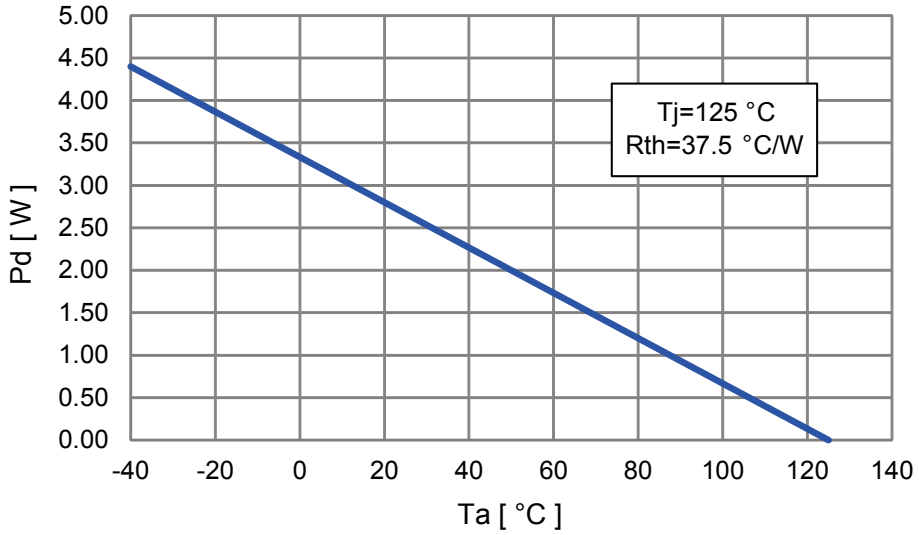
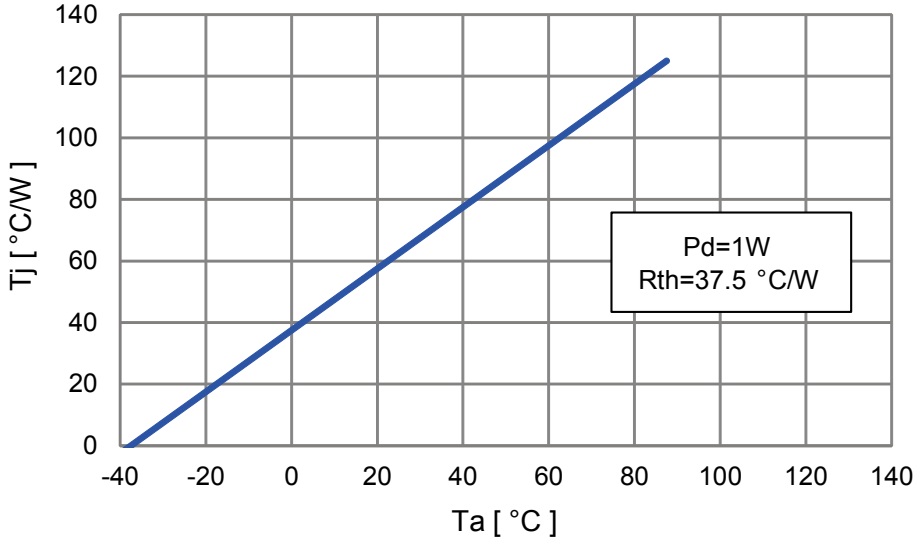


Figure 10. Junction temperature vs. ambient temperature (R_{th} = 37.5°C/W; Pd = 1 W)



10 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

10.1 HTSSOP16 package information

Figure 11. **HTSSOP16 exposed pad package outline**

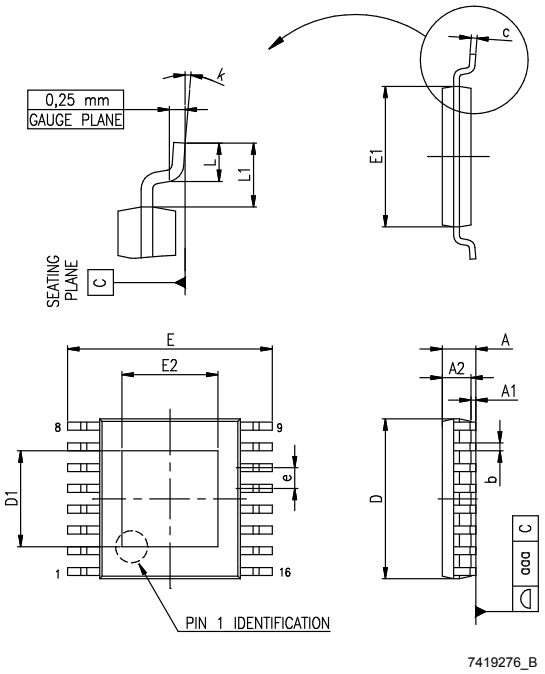


Table 9. **HTSSOP16 exposed pad mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.80	3.00	3.20
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.80	3.00	3.20
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
k	0.00		8.00
aaa			0.10

10.2 HTSSOP16 packing information

Figure 12. **HTSSOP16 tape and reel outline**

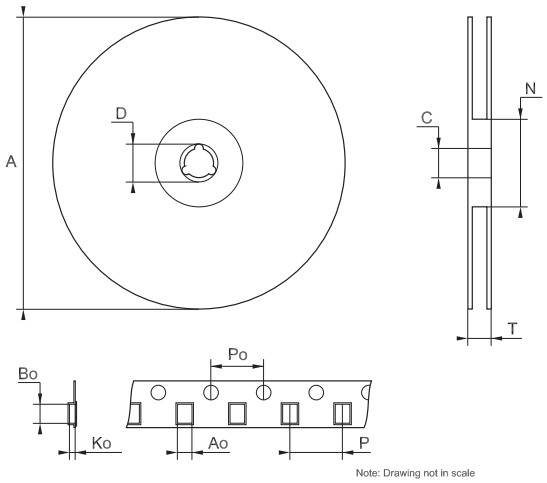


Table 10. **HTSSOP16 tape and reel mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.7		6.9
Bo	5.3		5.5
Ko	1.6		1.8
Po	3.9		4.1
P	7.9		8.1

Revision history

Table 11. **Document revision history**

Date	Version	Changes
29-Jan-2018	1	Initial release.

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