19-5078; Rev 1; 4/10

MAX17119 Evaluation Kit

Evaluates: MAX17119

General Description

The MAX17119 evaluation kit (EV kit) is a fully assembled and tested surface-mount PCB that evaluates the MAX17119 (IC) 10-channel, high-voltage, level-shifting scan driver for active-matrix, thin-film transistor (TFT), liquid-crystal display (LCD) applications.

The EV kit requires a +12V to +38V power supply (GON1, GON2) and a -12V to -2V negative power supply (GOFF) for the IC's level-shifting scan-driver circuitry.

Features

- **+12V to +38V GON_ Input-Voltage Range**
- **-12V to -2V GOFF Input-Voltage Range**
- **Resistor-Adjustable LDO Regulator for Logic Inputs**
- **Demonstrates 10 High-Voltage, Level-Shifting Scan Drivers**
- **Fully Assembled and Tested**

Ordering Information

PART	TYPE
MAX17119EVKIT+	EV Kit

+Denotes lead(Pb)-free and RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
A1–A9, FLK1, FLK2, FLK3, LDO_OUT, TP1–TP10, VST, Y1–Y9, YDCHG	34	Miniature red test points
C1	1	0.1µF ±10%, 25V X5R ceramic capacitor (0603) Murata GRM188R61E104K
C2	1	10µF ±20%, 6.3V X5R ceramic capacitor (0603) Murata GRM188R60J106M
C5, C6, C7	3	1µF ±10%, 50V X7R ceramic capacitors (0805) Murata GRM21BR71H105K
C8–C13, C82	7	1000pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H102J
C14–C25, C83, C84	14	1800pF ±10%, 50V X7R ceramic capacitors (0402) Murata GRM155R71H182K
C26–C31, C85	7	680pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H681J
C32–C37, C86	7	220pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H221J
C38–C43, C62, C64, C65, C66, C68, C70, C72, C73, C74, C76, C87	17	100pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H101J
C44–C49, C67, C75, C88	9	10pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H100J
C50–C55, C89	7	51pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H510J
C56–C61, C90	7	4pF ±0.25pF, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H4R0C
C63, C69, C71, C77	4	12pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H120J
C78, C81	2	1.5pF ±0.25pF, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H1R5C
C79, C80	2	3pF ±0.25pF, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H3R0C
C91, C92, C93	0	Not installed, ceramic capacitors (1206)
GND	1	Miniature black test point

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Component List (continued)

DESIGNATION	QTY	DESCRIPTION
J1	1	2 x 10 right-angle receptacle
JU1–JU10	10	2-pin headers, 0.1in centers
JU11–JU24	14	3-pin headers, 0.1in centers
P1	0	Not installed, 100-position, right-angle header
R1	1	68.1kΩ ±1% resistor (0402)
R2	1	100kΩ ±1% resistor (0402)
R3, R8, R13, R18, R23, R28, R42	7	64.9Ω ±1%, 1/2W resistors (2010)
R4, R9, R14, R19, R24, R29, R43	7	64.9Ω ±%1, 1/4W resistors (1206)
R5, R10, R15, R20, R25, R30, R44	7	64.9Ω ±1 resistors (0603)
R6, R11, R16, R21, R26, R31, R45	7	124Ω ±1% resistors (0603)
R7, R12, R17, R22, R27, R32, R46	7	249Ω ±1% resistors (0603)
R33–R38	6	178Ω ±1% resistors (0603)
R39, R40, R41	3	10Ω± 5% resistors (0603)
R47–R58	12	100kΩ ±5% resistors (0603)
R59	1	100kΩ ±1% resistor (0603)
R60	1	100kΩ potentiometer (single turn)
R61	1	30.1kΩ ±1% resistor (0603)
R62	1	3.4kΩ ±1% resistor (0603)
SW1	1	9-position DIP switch
SW2	1	3-position DIP switch
U1	1	10-channel scan driver with GPM (28 TQFN-EP*) Maxim MAX17119ETI+
U2	1	Adjustable LDO regulator (8 TDFN-EP*) Maxim MAX6771TALD2+ (Top Mark: BEG)
—	21	Shunts
—	1	PCB: MAX17119 EVALUATION KIT+

**EP = Exposed pad.*

Component Supplier

SUPPLIER	PHONE	WEBSITE
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com

Note: *Indicate that you are using the MAX17119 when contacting this component supplier.*

Quick Start

Required Equipment

- +12V to +38V, 1A DC power supply
- -12V to -2V, 1A DC power supply
- Two voltmeters

Procedure

The MAX17119 EV kit is fully assembled and tested. Follow the steps below to verify board operation. **Caution: Do not turn on the power supply until all connections are completed. When ready, turn on V_{GOFF} before turning on V_{GON1} and V_{GON2}.**

1) Verify that shunts are installed across jumpers JU1–JU10 (RC loads connected at scan-driver outputs).
2) Verify that a shunt is installed across pins 1-2 of jumper JU11 (GON2 = GON1).
3) Verify that shunts are installed across pins 2-3 of jumpers JU12–JU20 (DC voltage applied at A_ inputs).
4) Verify that shunts are installed across pins 1-2 of jumper JU21 (VSENSE derived from LDO_OUT).
5) Verify that shunts are installed across pins 2-3 of jumpers JU22, JU23, and JU24 (DC voltage applied at FLK_ inputs).
6) Verify that all positions of DIP switches SW1 and SW2 are in the on position (logic-high DC voltage at inputs).
7) Connect a voltmeter to the LDO_OUT and GND test points.
8) Connect the +12V to +38V power-supply positive terminal to the GON1 PCB pad. Connect the power-supply ground terminal to the PGND pad.
9) Connect the negative terminal of the negative power supply to the GOFF PCB pad. Connect the ground terminal of the negative power supply to the PGND pad.
10) Enable the negative power supply and set it to -12V.
11) Enable the GON1 positive power supply and set it to +20V.
12) Adjust potentiometer R60 until the voltmeter at LDO_OUT reads +3.3V.
13) Verify that test points TP1–TP9 outputs are +20V.
14) Verify that test point TP10 output is -12V.

Table 1. Default Jumper Positions

JUMPER	SHUNT POSITION
JU1–JU10	Installed
JU11	1-2
JU12–JU20, JU22, JU23, JU24	2-3
JU21	1-2

Detailed Description of Hardware

The MAX17119 EV kit is a fully assembled and tested surface-mount PCB that evaluates the MAX17119 10-channel, high-voltage, level-shifting scan drivers for thin-film transistor (TFT) liquid-crystal display (LCD) applications. The EV kit requires two positive power supplies and one negative power supply. GON1 and GON2 require +12V to +38V power supplies that provide up to 1A of current. GOFF requires a -12V to -2V power supply that provides up to 1A of current.

The IC's logic level to high-voltage, level-shifting scan drivers can buffer nine logic inputs (A1–A9) and shift them to a desired level (Y1–Y9) for driving TFT-LCD row logic. GON1 supplies the high-voltage levels at the IC buffers Y1–Y7 and YDCHG when its respective input is a logic-high. GON2 supplies the high-voltage levels at the IC buffers Y8 and Y9 when its respective input is a logic-high. GOFF supplies the low-voltage level at all of the scan-driver outputs when their input is a logic-low. DIP switch SW1 is used to set a DC logic-high level at A1–A9 inputs for testing purposes, by using a high-voltage input LDO regulator, U2 (MAX6771), and potentiometer R56.

Jumper JU11 is provided for evaluation of the EV kit when utilizing one power source for the IC's GON1 and GON2 power inputs. See the *Power-Supply Configurations* section for proper configuration of jumper JU11. Jumpers JU1–JU10 are provided to connect RC loads at the IC's Y1–Y9 and YDCHG outputs.

Power-Supply Configurations

The EV kit requires two positive power supplies and one negative power supply for proper evaluation of the kit. GON1 and GON2 require a +12V to +38V power supply that provides up to 1A of current. GOFF requires a -12V to -2V power supply that provides up to 1A of current.

Jumper JU11 configures the input power source for GON2. Install a shunt across pins 1-2 of jumper JU11 to select GON1 as the input power source for GON2. Install a shunt across pins 2-3 of jumper JU11 to apply an external power source across the GON2 and PGND PCB pads. Buffers Y8 and Y9 output the voltage applied at the GON2 PCB pad. See Table 2 for proper jumper JU11 configuration.

Additional surface-mount 1206 PCB pads are provided for adding additional bulk capacitance at C91, C92, and C93 when interfacing long wires to the EV kit's GON1, GON2, and GOFF power-supply inputs.

Output Load Connection

The EV kit provides resistor/capacitor loads for each output channel to mimic TFT-LCD panel load models for easy evaluation of the EV kit. Install shunts across jumpers JU1–JU11 to connect the RC loads to the IC's scan-driver outputs. **Place scope probes across the shunts installed at jumpers JU1–JU10 for proper evaluation of the MAX17119 buffers (Y1–Y10), when applying input signals through the SIGNAL_IN PCB pad, P1 header, or J1 header.** Test points TP1–TP10 can be used to monitor the loaded buffer outputs when applying static DC voltages at the A1–A9 inputs.

Inputs (A_) Logic-Level Selection (JU12–JU20)

Jumpers JU12–JU21 configure the EV kit's A1–A9 inputs to accept either a DC voltage or square-wave input signal. Install a shunt across pins 1-2 of the individual channels to use a square-wave signal applied at the SIGNAL_IN PCB pad and J1 or P1 headers. The square-wave signal should have a +2V to +5.5V logic-high level. **Place scope probes across the shunts installed at jumpers JU2–JU11 for proper evaluation of the MAX17119 scan-driver outputs (Y1–Y9 and YDCHG).**

Install a shunt across pins 2-3 of the individual channels to configure the inputs to static logic-low or logic-high DC levels. DIP switch SW1 sets the buffer inputs to a logic-high level using the output of LDO regulator (U2) and potentiometer R60. Set SW1 to the on position to place a logic-high voltage at the inputs. Set SW1 to the off position to place a logic-low voltage at the inputs through pulldown resistors R47–R55.

Table 2. GON2 Power Source Selection (JU11)

SHUNT POSITION	GON2 IC PIN	GON2 INPUT RANGE (V)
1-2	Connected to GON1	—
2-3	Connected to external power source at GON2 and PGND PCB pads	+12 to +38

Table 3. Output Load Connection (JU1–JU10)

SHUNT POSITION	MAX17119 Y1–Y9 AND YDCHG OUTPUTS	EV KIT FUNCTION
Installed	Connected to RC loads	Outputs monitored at shunts
Not installed	Disconnected from RC load	No-load condition for scan drivers

Inputs (FLK_) Logic-Level Selection (JU22, JU23, JU24)

Jumpers JU22, JU23, and JU24 configure the MAX17119 EV kit's FLK1, FLK2, and FLK3 inputs to accept either a DC voltage or square-wave input signal. Install a shunt across pins 1-2 of the individual channels to use a square-wave signal applied at the FLK1, FLK2, and FLK3 test points or at the J1 or P1 headers. The square-wave signal should have a +2V to +5.5V logic-high level.

Install a shunt across pins 2-3 of the individual channels to configure the inputs to static logic-low or logic-high DC levels. DIP switch SW2 sets the buffer inputs to a logic-high level using the output of the LDO regulator (U2) and potentiometer R60. Set SW2 to the on position to place a logic-high voltage at the inputs. Set SW2 to the off position to place a logic-low voltage at the inputs through pulldown resistors R56–R58.

LDO Regulator

The LDO regulator output voltage can be adjusted from +2.2V to +5.3V using R60 and monitored by probing test point LDO_OUT. Rotate potentiometer R60 clockwise to decrease the LDO output voltage and vice versa.

Table 4. Logic-Input Configuration (JU12–JU20)

SHUNT POSITION	SW1 POSITION	A_ INPUT LOGIC LEVEL
1-2	—	Square-wave signal applied through header P1 or J1 (A1–A6)
		Square-wave signal applied at SIGNAL_IN PCB pad (A7, A8, A9)
2-3	Off	Low
	On	High

Table 5. Logic-Input Configuration (JU22, JU23, JU24)

SHUNT POSITION	SW2 POSITION	FLK_ INPUT LOGIC LEVEL
1-2	—	Square-wave signal applied through header P1 or J1
2-3	Off	Low
	On	High

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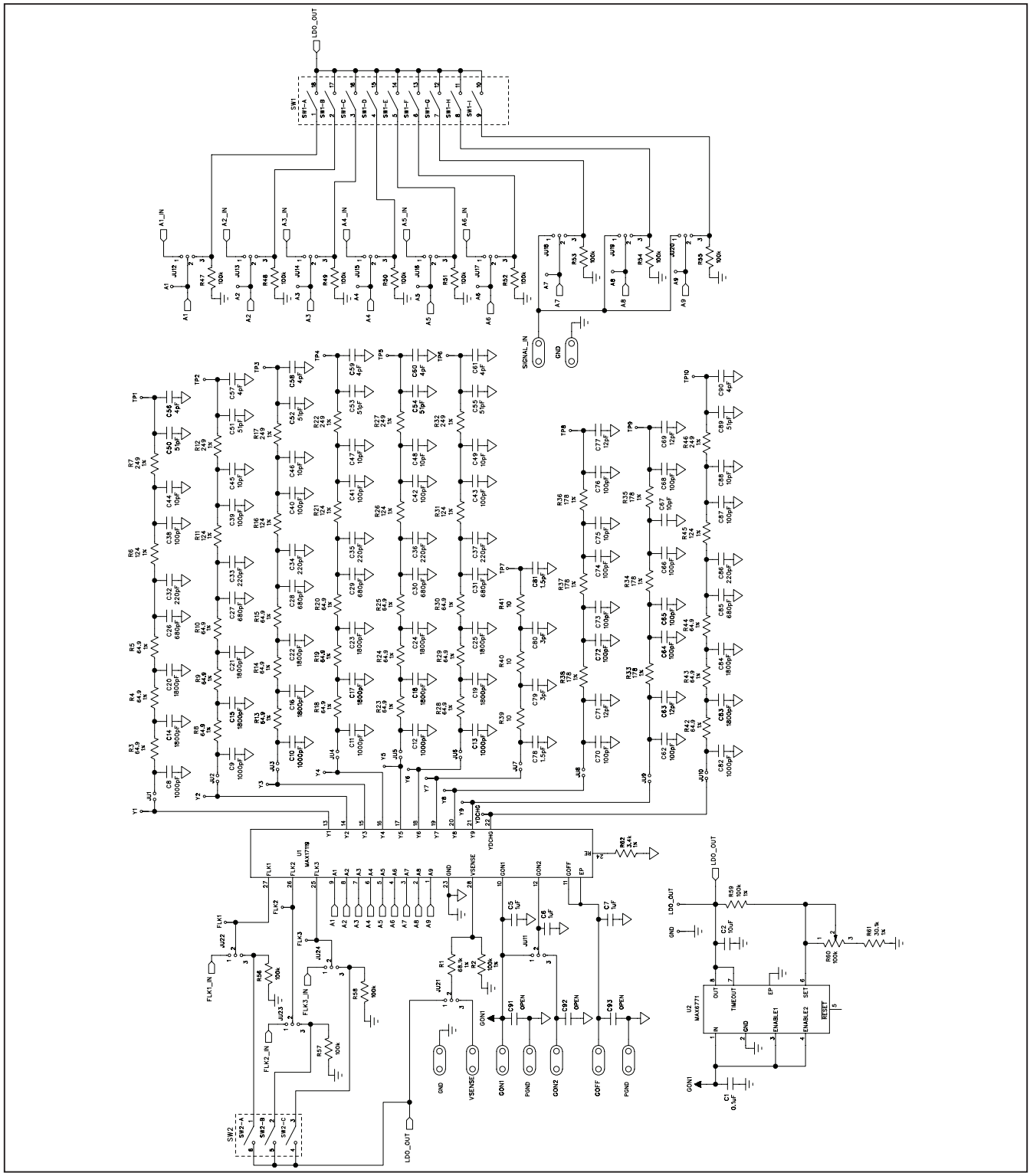

Figure 1a. MAX17119 EV Kit Schematic (Sheet 1 of 2)

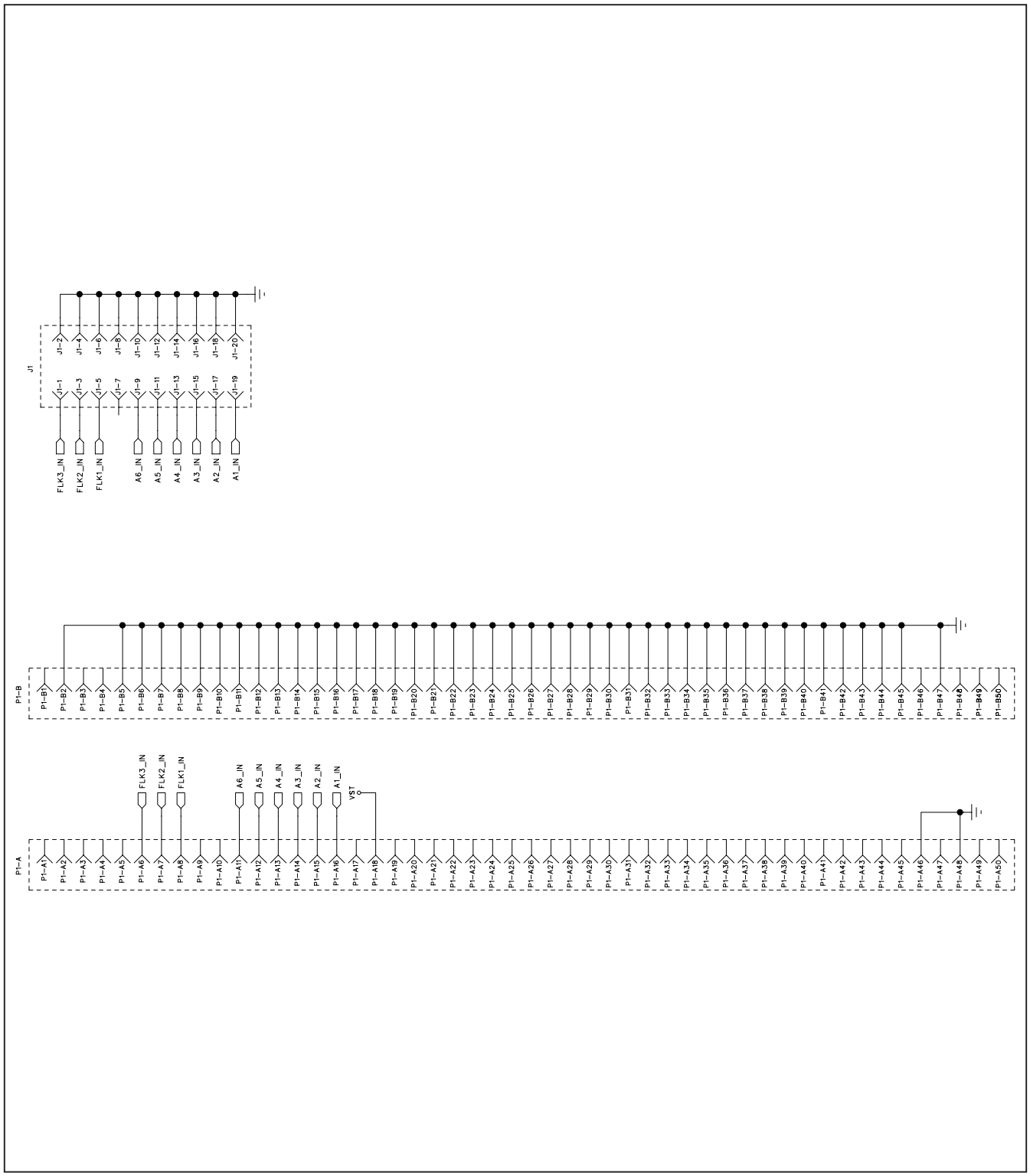

Figure 1a. MAX17119 EV Kit Schematic (Sheet 2 of 2)

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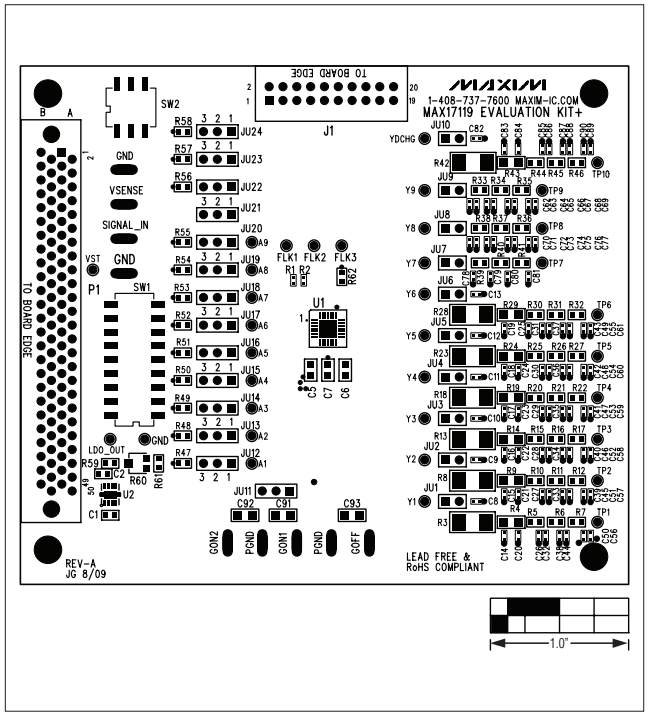

Figure 2. MAX17119 EV Kit Component Placement Guide—Component Side

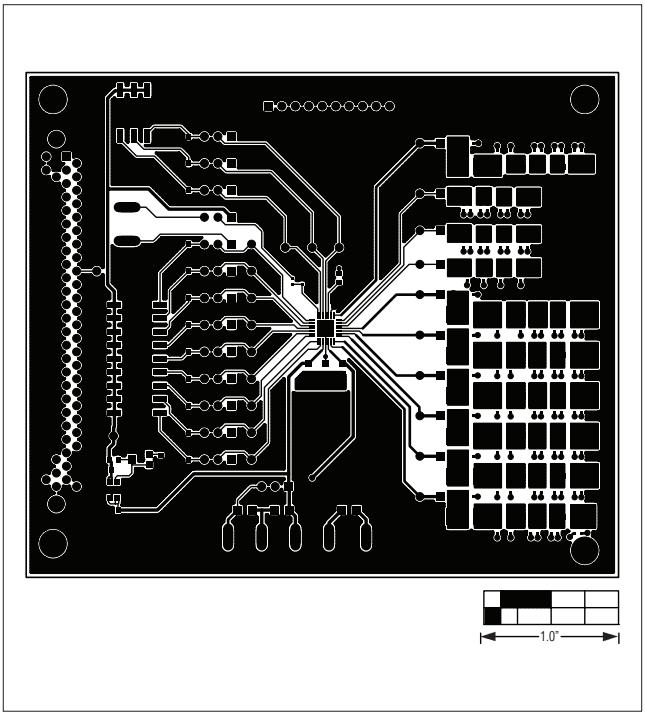

Figure 3. MAX17119 EV Kit PCB Layout—Component Side

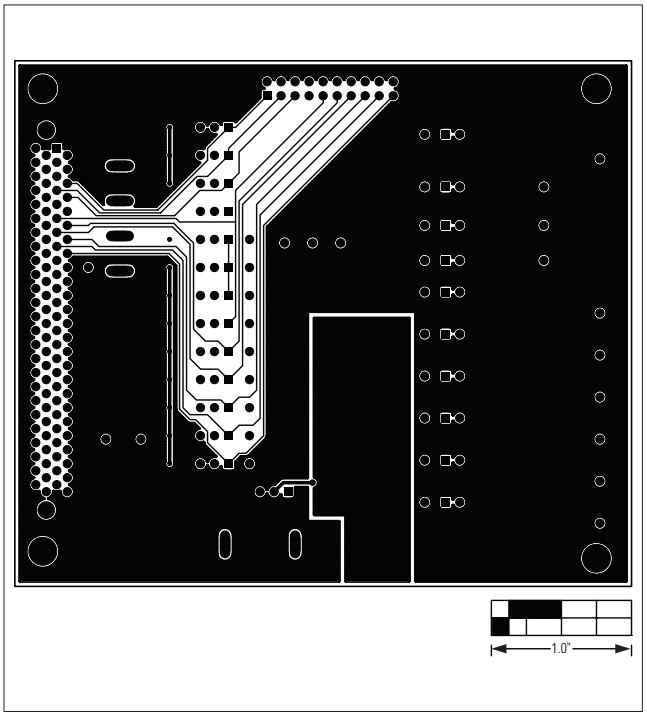

Figure 4. MAX17119 EV Kit PCB Layout—Solder Side

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/09	Initial release	—
1	4/10	Corrected step 13 and added step 14 in the *Quick Start Procedures* section	3