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CY91FV360GA/F362GB/F364G
CY91F365GB/366GA/F366GB
CY91F367GB/F368GB/F369GA/F376G

32-bit Microcontroller
FR50 CY91360G Series

The CY91360G series is a standard microcontroller containing a wide range of I/O peripherals and bus control functions. The CY91360G series features a 32-bit RISC CPU (FR50) core and is suitable for embedded control applications requiring high-performance and high-speed CPU processing. Also, Internal memories to improve the execution speed of the CPU.

Features

■ **Execution time**: **down to 15.6 ns** (**64 MHz**)

■ **FR50 CPU**: **RISC architecture**

The CPU has a general-purpose register architecture with improved numeric implementation whereby a wide range of delayed branch instructions reduces losses in execution time due to pipeline breaks.
Bit manipulation instructions and memory access instructions have been enhanced resulting in improved code efficiency and execution speed for control implementation.

- A five-stage pipeline structure provides high-speed processing (one instruction per cycle)
- 32-bit linear address space: 4 Gbytes
- Fixed 16-bit instruction size (basic instructions)
- High-speed multiplication/step division
- High-speed interrupt processing (6 cycles)
- General-purpose registers: 16 × 32 bits

■ **External bus interface unit with a wide range of functions**

Divides the external memory space into a maximum of eight areas. Chip select signal setting, data bus width selection (8, 16, 32-bit), and area size can be specified for each area.

- Address bus up to 32 bit wide
- Programmable auto-wait function

■ **DMAC**

Direct memory access (DMA) can be used to perform various types of data transfer without going via the CPU. This improves system performance.

- Eight channels (including up to 3 external channels)
- Four transfer modes supported: single/block, burst, continuous transfer, and fly-by

■ **Power consumption control mechanisms**

The CY91360G series contains a number of functions for controlling the operating clock to reduce power consumption.

- Software control: Sleep and stop/real time clock functions
- Hardware control: Hardware standby function
- Gear (divider) function: The CPU and peripheral clock frequencies can be set independently.

■ **Contains a range of peripheral functions**

- UART, U-timer
- Real Time Clock (with optional subclock operation and subclock calibration module)
- Stepper Motor Control
- Sound Generator
- Serial I/O (SIO), SIO-Prescaler
- Power Down Reset
- Alarm Comparator
- I/O-Timer
- I^2C Interface
- 10-bit D/A Converter
- CAN Interface
- 10-bit A/D converter
- 16-bit reload timer
- 16-bit PWM timer
- Watchdog timer
- Bit search module
- Interrupt controller
- External interrupt inputs
- I/O port function

■ **Interrupt levels**

"16 maskable interrupt levels"

■ **Other**

- Power supply voltage
- 5 V power supply used, the internal regulator creates internal supply of 3.3 V
- Package: CY91F362GB is delivered in a QFP208 package, and CY91F369GA in QFP160 package.
  CY91F364G, CY91F365GB, CY91F366GB, CY91F367GB, CY91F368GB, CY91366GA and CY91F376G will be delivered in an LQFP120 package.
  (See also section Package Dimensions.)

Contents

1. Product Lineup

Table 1-1. CY91FV360GA, CY91F362GB, CY91F364G, CY91F369GA

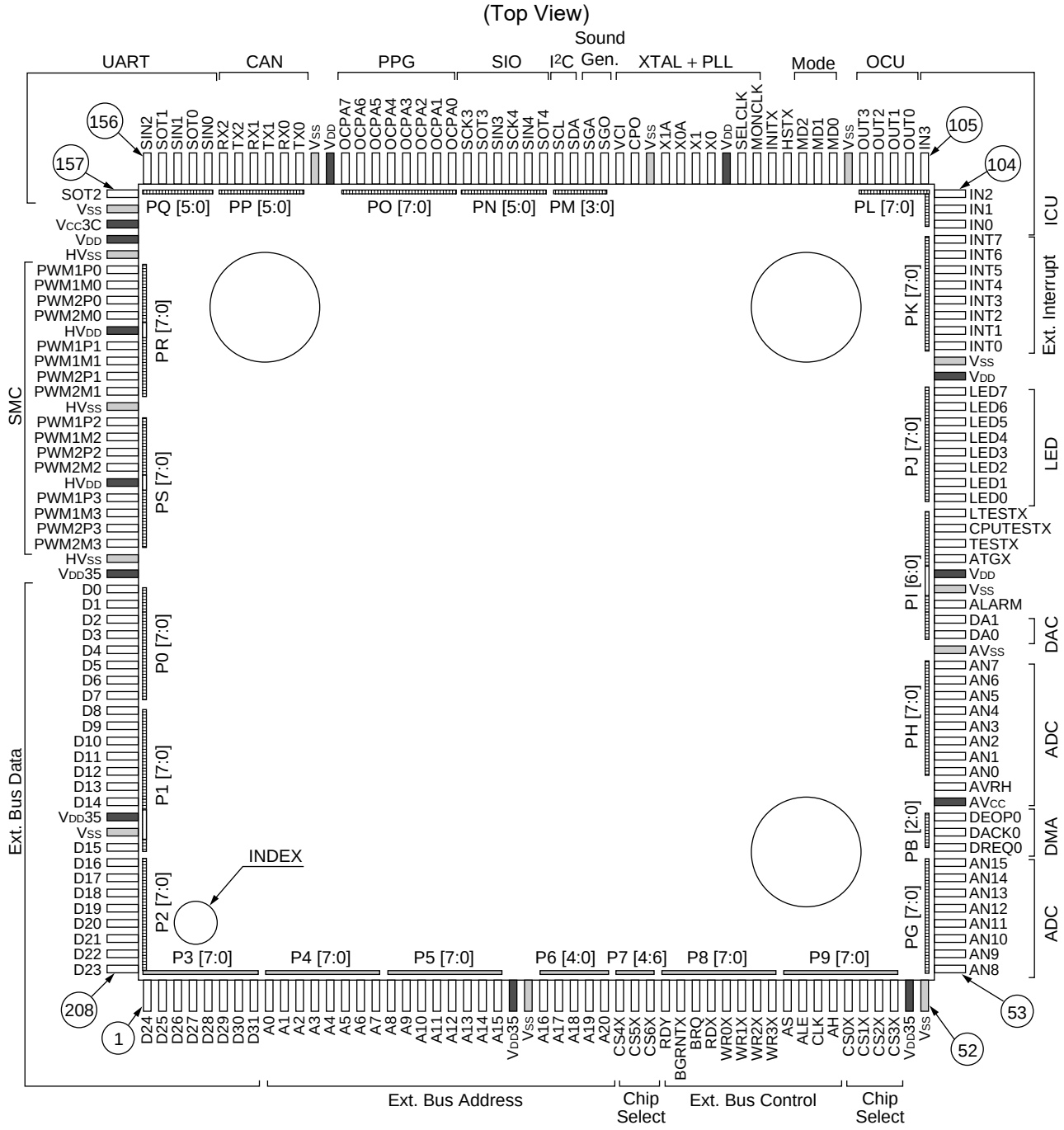
Resource Channels Memory Size	CY91FV360GA	CY91F362GB	CY91F364G	CY91F369GA
Cache/Instruction RAM	4 KB / 4 KB	- / 4 KB	- / -	- / 4 KB
D-bus RAM	16 KB	12 KB	12 KB	16 KB
F-bus RAM	16 KB	4 KB	4 KB	16 KB
Flash/ROM (F-bus)	512 KB Fast Flash	512 KB Normal Flash	256 KB Fast Flash	512 KB Fast Flash
Boot ROM	2 KB	2 KB	2 KB	2 KB
EDSU	–	–	1	–
CAN	4 ch	3 ch	1 ch	2 ch
Stepper Motor Control	4 ch	4 ch	–	–
Sound Generator	1 ch	1 ch	–	1 ch
PPG	8 ch	8 ch	4 ch	4 ch
Input Capture	4 ch	4 ch	4 ch	–
Output Compare	4 ch	4 ch	4 ch	–
Free Running Timer	2 ch	2 ch	2 ch	–
D/A Converter	2 ch	2 ch	2 ch	–
A/D Converter	16 ch	16 ch	12 ch	10 ch
400 kHz I^2C interface	1 ch	1 ch	1 ch	1 ch
Alarm Comparator	1 ch	1 ch	–	1 ch
SIO/SIO Prescaler	2 ch	2 ch	1 ch	2 ch
UART/U-Timer	3 ch	3 ch	1 ch	1 ch
USART with LIN Function	–	–	2 ch	–
16-bit Reload Timer	6 ch	6 ch	3 ch	6 ch
Ext. Interrupt	8 ch	8 ch	8 ch	8 ch
Non Maskable Interrupt	1	–	1	–
Real Time Clock	1	1	1	1
32 kHz Subclock Option for RTC	yes	no	yes	no
Subclock Calibration	yes	no	yes	no
LED Port	8 bit	8 bit	8 bit	–
Power Down Reset	1	1	–	1
Bit Search Module	1	1	1	1
Watchdog Timer	1	1	1	1
Ext. Address Bus	32 bit	21 bit	–	up to 24 bit
Ext. Data Bus	32 bit	32 bit	–	32 bit
Ext. DMA	3 ch	1 ch	–	1 ch
Max Operating Frequency	64 MHz	64 MHz	64 MHz	64 MHz

Table 1-2. CY91F365GB, CY91F366GB, CY91366GA, CY91F367GB, CY91F368GB

Resource Channels Memory Size	CY91F365GB	CY91F366GB CY91366GA	CY91F367GB	CY91F368GB	CY91F376G
Cache/Instruction RAM	- / 4 KB	- / 4 KB	- / 4 KB	- / 4 KB	- / 4 KB
D-bus RAM	16 KB	16 KB	16 KB	16 KB	16 KB
F-bus RAM	16 KB	16 KB	16 KB	16 KB	16 KB
Flash/ROM (F-bus)	512 KB Fast Flash	512 KB Normal Flash	512 KB Fast Flash	512 KB Fast Flash	768 KB Fast Flash
Boot ROM	2 KB	2 KB	2 KB	2 KB	2 KB
EDSU	–	–	–	–	–
CAN	2 ch	2 ch	2 ch	2 ch	2 ch
Stepper Motor Control	4 ch	4 ch	–	–	4 ch
Sound Generator	1 ch	1 ch	–	–	1 ch
PPG	8 ch	8 ch	4 ch	4 ch	8 ch
Input Capture	4 ch	4 ch	4 ch	4 ch	4 ch
Output Compare	2 ch	2 ch	2 ch	2 ch	2 ch
Free Running Timer	2 ch	2 ch	2 ch	2 ch	2 ch
D/A Converter	2 ch	–	–	–	–
A/D Converter	8 ch	8 ch	8 ch	8 ch	8 ch
I^2C 400kHz	1 ch	1 ch	1 ch	1 ch	1 ch
Alarm Comparator	1 ch	1 ch	1 ch	1 ch	1 ch
SIO/SIO Prescaler	2 ch	2 ch	2 ch	2 ch	2 ch
UART/U-Timer	2 ch	2 ch	1 ch	1 ch	2 ch
USART with LIN function	–	–	–	–	–
16-bit Reload Timer	6 ch	6 ch	3 ch	3 ch	6 ch
Ext. Interrupt	8 ch	8 ch	8 ch	8 ch	8 ch
Non Maskable Interrupt	–	–	–	–	–
Real Time Clock	1	1	1	1	1
32 kHz Subclock Option for RTC	no	yes	no	yes	yes
Subclock Calibration	no	yes	no	yes	yes
LED Port	–	–	–	–	–
Power Down Reset	1	1	1	1	1
Bit Search Module	1	1	1	1	1
Watchdog Timer	1	1	1	1	1
Ext. Address Bus	–	–	–	–	–
Ext. Data Bus	–	–	–	–	–
Ext. DMA	–	–	–	–	–
Max Operating Frequency	64 MHz	64 MHz	64 MHz	64 MHz	64 MHz

2. Pin Assignments

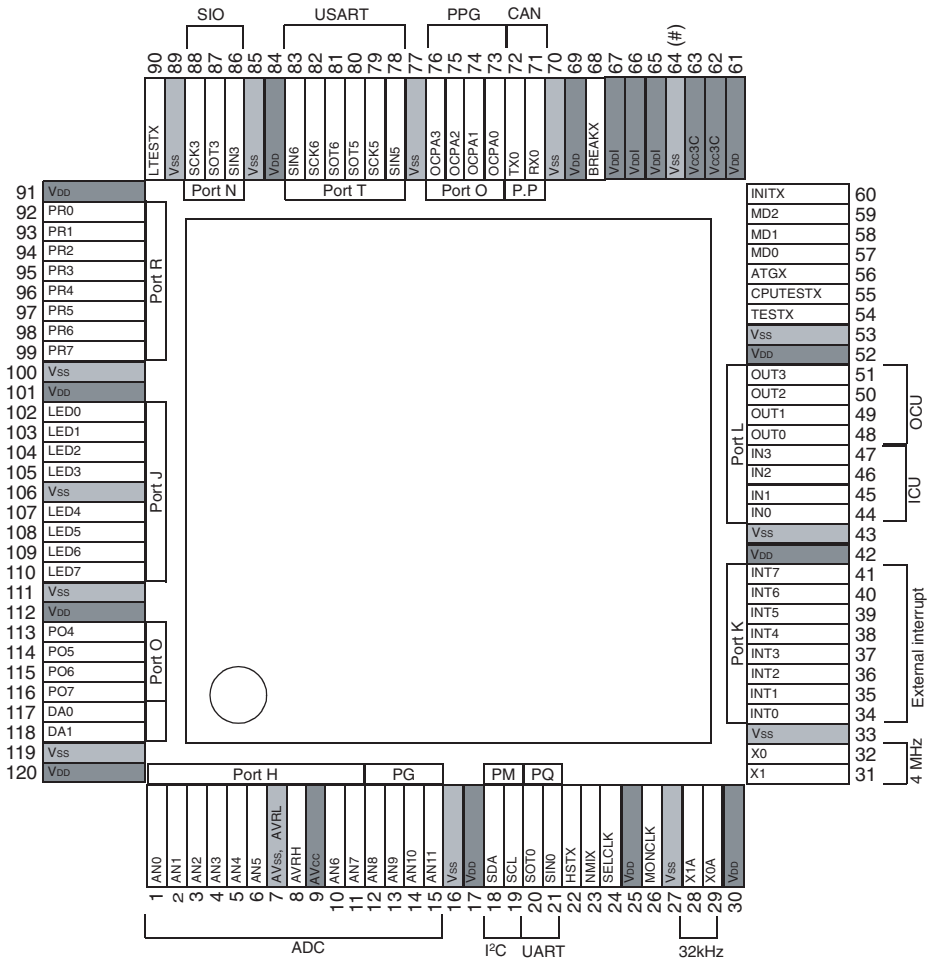
Figure 2-1. CY91F362GB



(HQB208)

Figure 2-2. CY91F364G

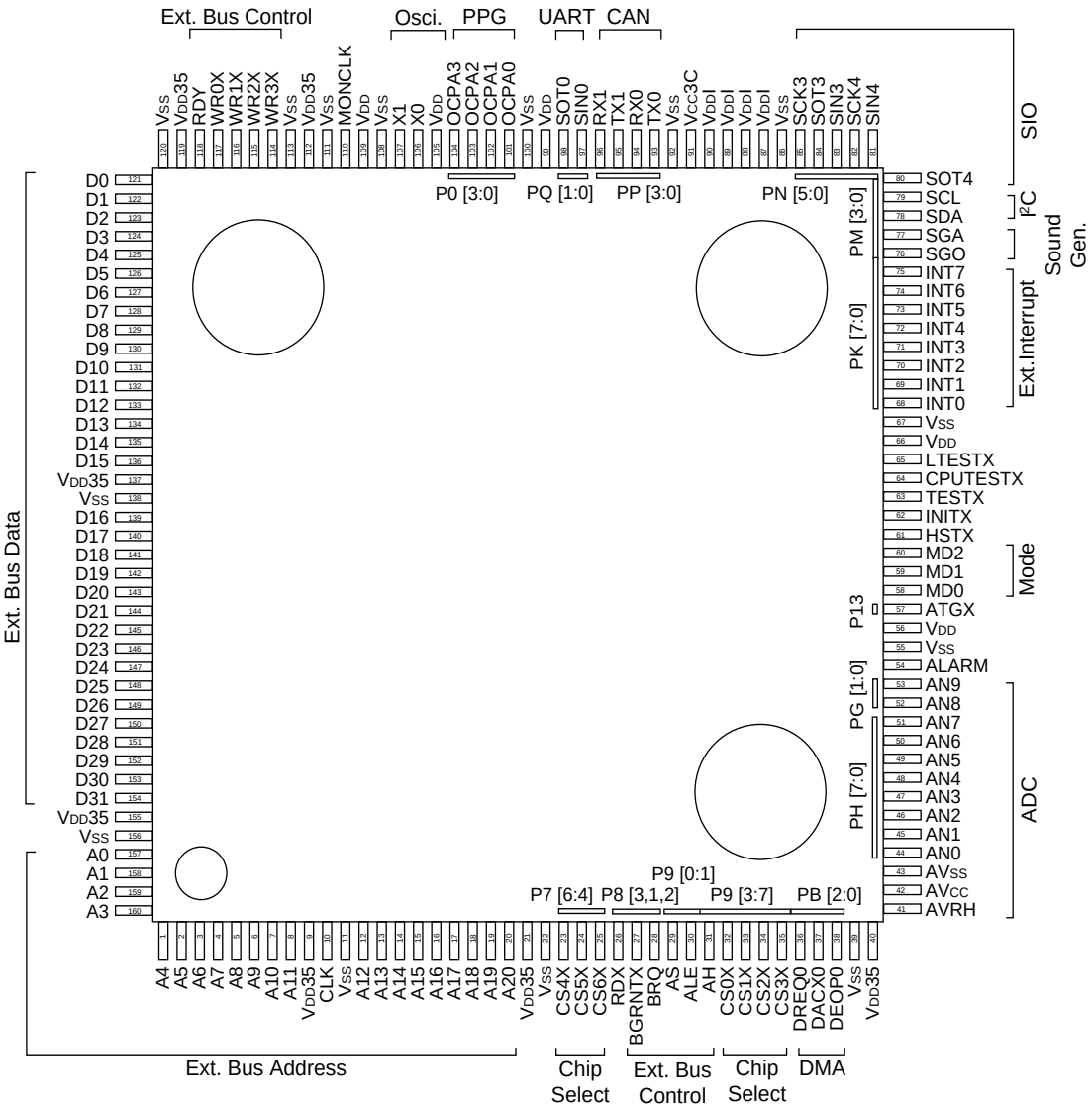
(Top View)



(LQM120)

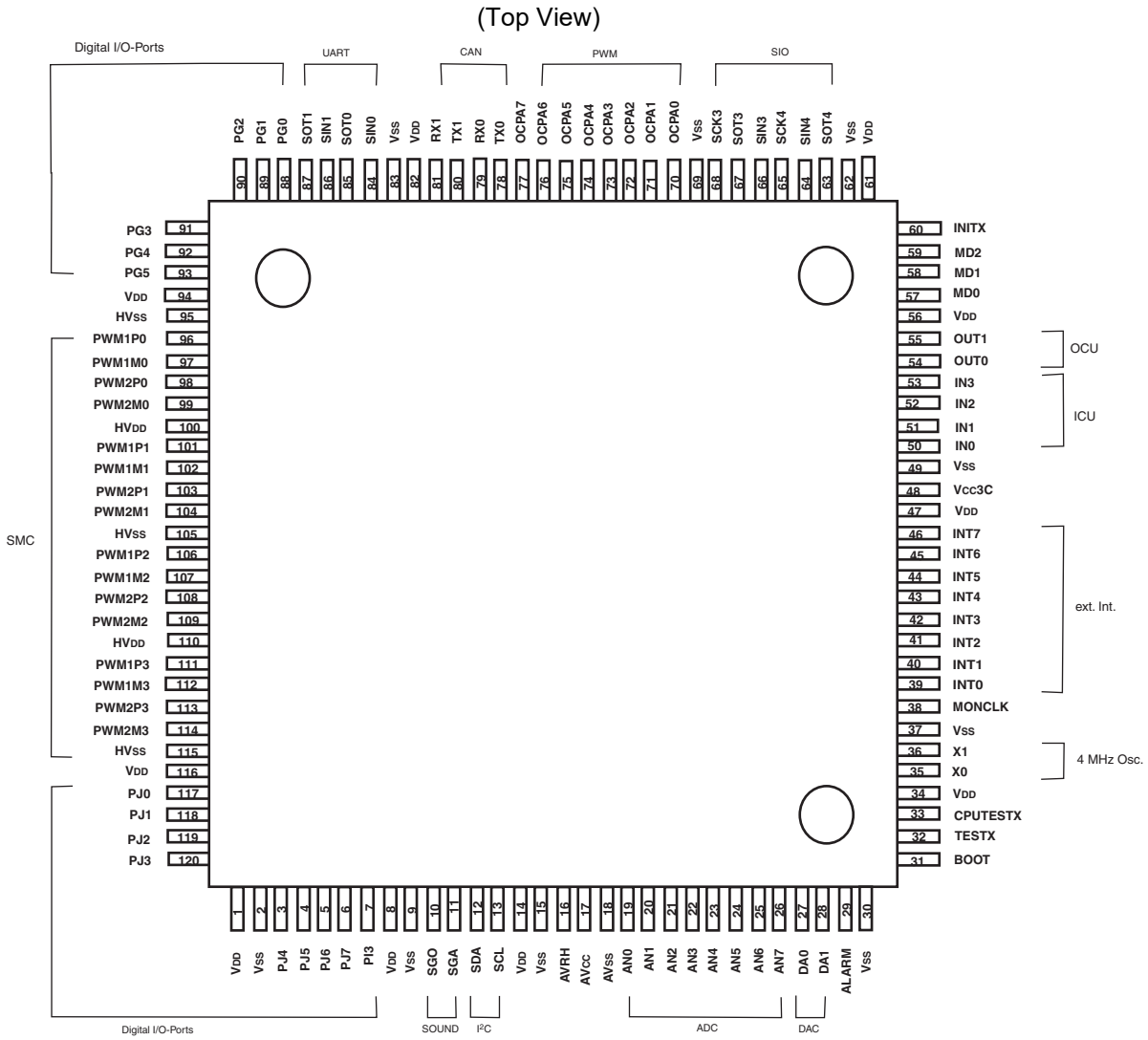
Figure 2-3. CY91F369GA

(Top View)



(HQA160)

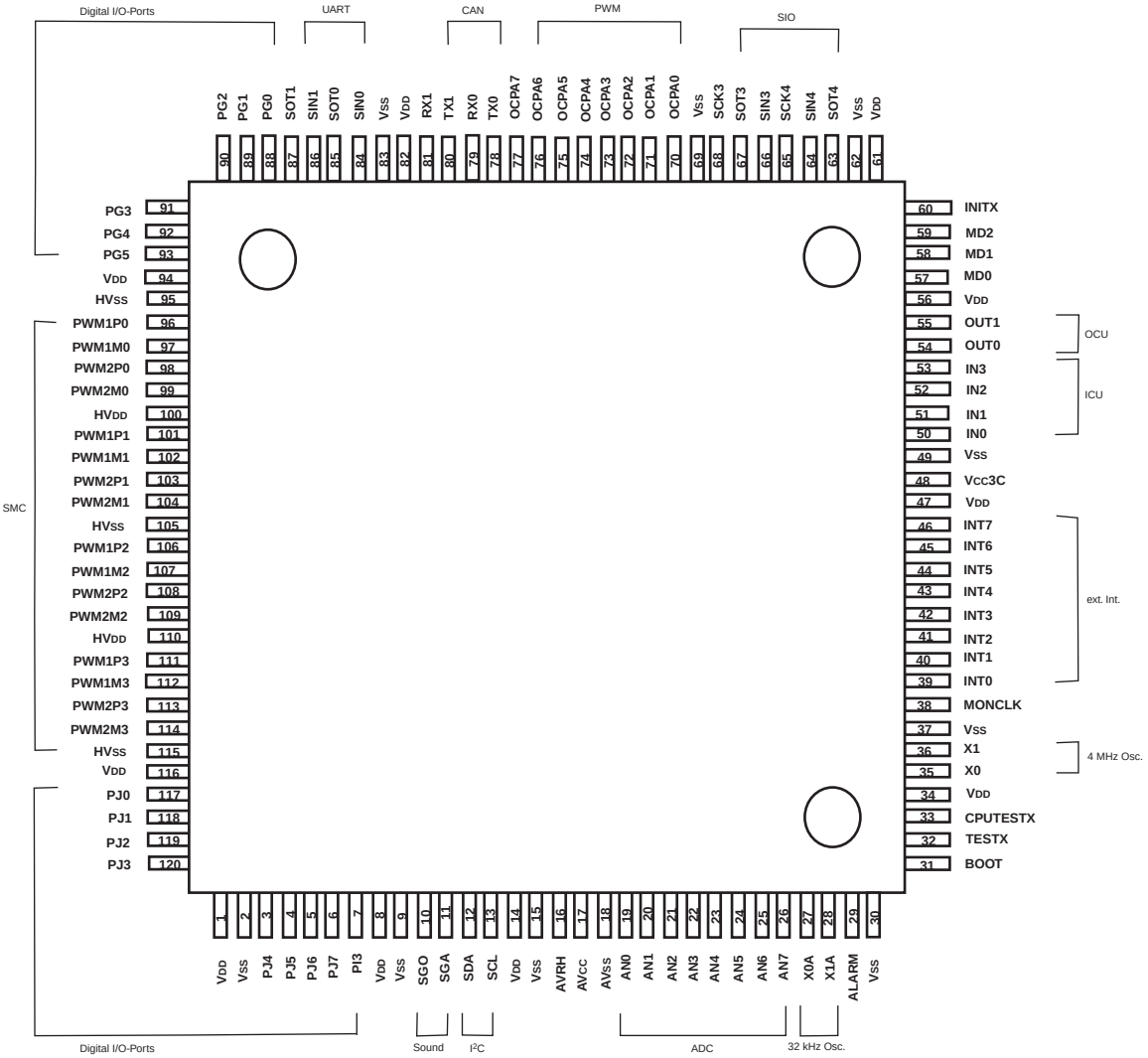
Figure 2-4. CY91F365GB



(LQM120)

Figure 2-5. CY91F366GB/CY91F376G

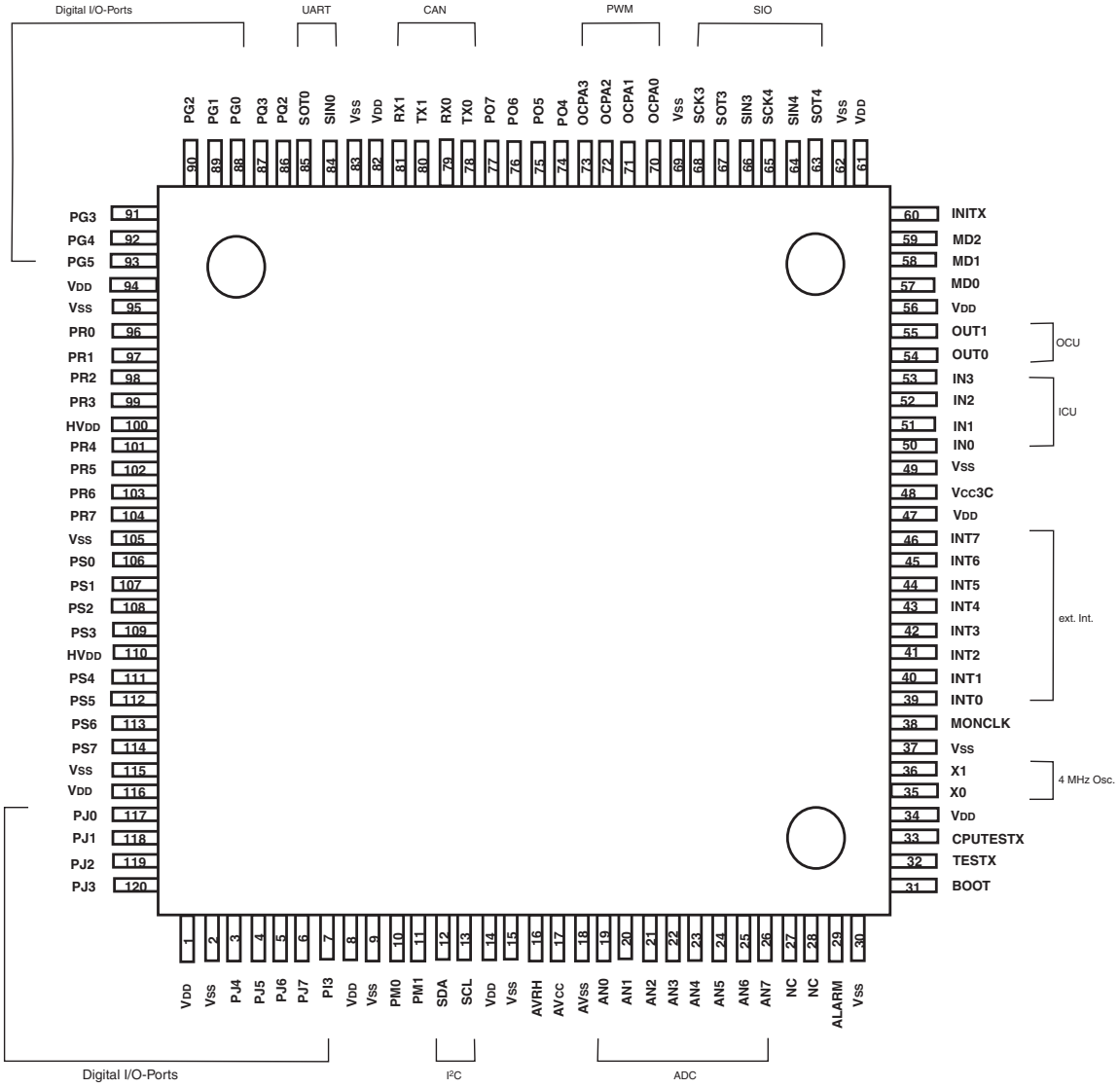
(Top View)



(LQM120)

Figure 2-6. CY91F367GB

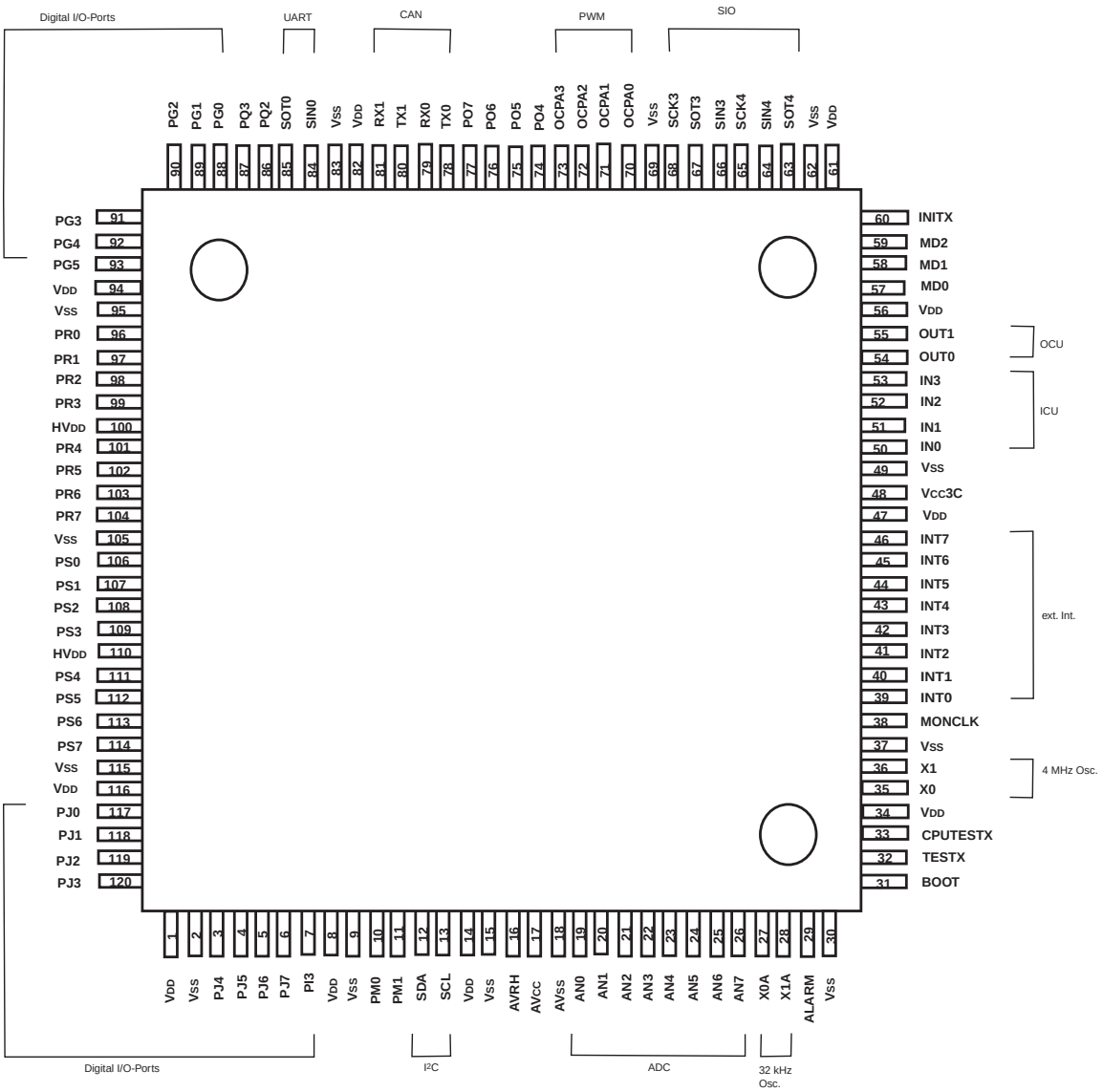
(Top View)



(LQM120)

Figure 2-7. CY91F368GB

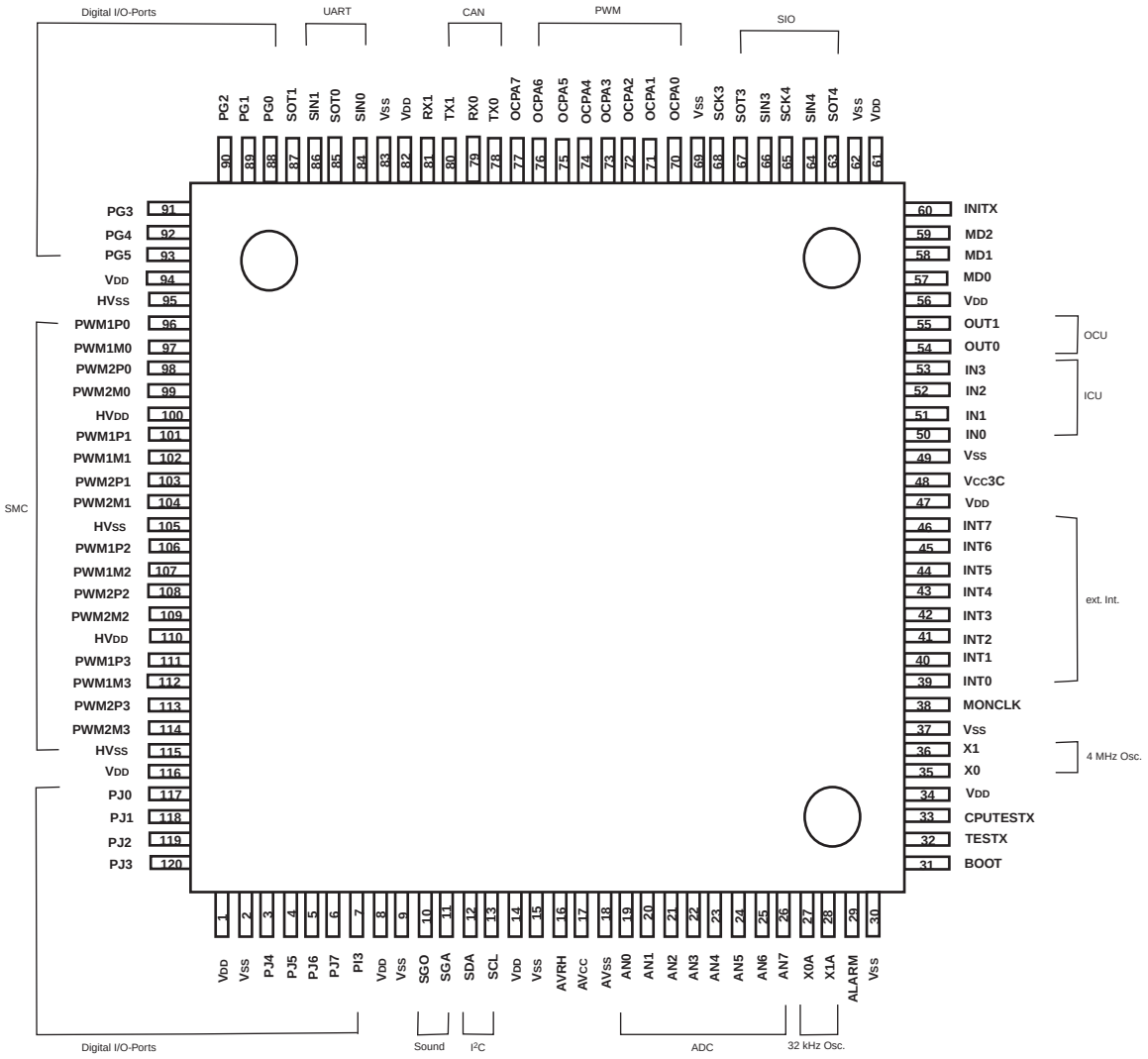
(Top View)



(LQM120)

Figure 2-8. CY91366GA

(Top View)



(LQM120)

3. Pin Descriptions

Table 3-1. CY91FV360GA I/O Pins and their Functions

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	D18	I/O	–	Q	Ext. Bus Data Bit 18
2	D11	I/O	–	Q	Ext. Bus Data Bit 11
3	D2	I/O	–	Q	Ext. Bus Data Bit 2
4	Not Connected				
5	HV_{SS}	–	–	–	–
6	$HV_{DD}5B$	–	–	–	–
7	PWM2M1	I/O	PR7	M	SMC 1
8	PWM1M1	I/O	PR5	K	SMC 1
9	PWM1P0	I/O	PR0	K	SMC 0
10	$V_{DD}5R$	–	–	–	–
11	$V_{DD}5P$	–	–	–	–
12	SCK4	I/O	PN2	A	SIO Clock
13	$V_{DD}5J$	–	–	–	–
14	EXRAM	I	–	P	Trace Control
15	TWRX	O	–	X	Trace Control
16	TAD9	O	–	X	Trace Address
17	TAD5	O	–	X	Trace Address
18	TAD3	O	–	X	Trace Address
19	TDT68	I/O	–	W	Trace Data
20	TDT63	I/O	–	W	Trace Data
21	TDT57	I/O	–	W	Trace Data
22	TDT49	I/O	–	W	Trace Data
23	TDT23	I/O	–	W	Trace Data
24	TDT16	I/O	–	W	Trace Data
25	TDT7	I/O	–	W	Trace Data
26	TDT2	I/O	–	W	Trace Data
27	ICD0	I/O	–	N	ICE Data
28	ICLK	I/O	–	L	ICE Clock
29	X0	I	–	H	4 MHz Oscillator Pin
30	INTX	I	–	U	Initial Pin
31	MD1	I	–	T	Mode Pin 1
32	IN3	I/O	PL3	A	ICU Input 3
33	INT3	I/O	PK3	A	Ext. Interrupt 3
34	AN3	I/O	PH3	B	ADC Input 3
35	DACK2	I/O	PB6	A	DMA Acknowledge 2
36	AN13	I/O	PG5	B	ADC Input 13
37	AN8	I/O	PG0	B	ADC Input 8
38	ALE	I/O	P91	A	Ext. Bus Control

Table 3-1. CY91FV360GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
39	WR1X	I/O	P85	S	Ext. Bus Control
40	RDX	I/O	P83	S	Ext. Bus Control
41	CS7X	I/O	–	A	Chip Select 7 (CAN)
42	A26	I/O	–	Q	Ext. Bus Address Bit 26
43	A20	I/O	–	Q	Ext. Bus Address Bit 20
44	A12	I/O	–	Q	Ext. Bus Address Bit 12
45	D21	I/O	–	Q	Ext. Bus Data Bit 21
46	D16	I/O	–	Q	Ext. Bus Data Bit 16
47	D13	I/O	–	Q	Ext. Bus Data Bit 13
48	D7	I/O	–	Q	Ext. Bus Data Bit 7
49	D3	I/O	–	Q	Ext. Bus Data Bit 3
50	V_{SS}	–	–	–	–
51	PWM2P2	I/O	PS2	K	SMC 2
52	PWM2P1	I/O	PR6	K	SMC 1
53	PWM1P1	I/O	PR4	K	SMC 1
54	Not Connected				
55	SIN1	I/O	PQ2	A	UART 1 Input
56	TX3	I/O	PP6	Q	CAN 3 TX
57	SOT3	I/O	PN4	A	SIO Output
58	SOT4	I/O	PN0	A	SIO Output
59	Not Connected				
60	Not Connected				
61	SGO	I/O	PM0	A	Sound Generator SGO
62	TOEX	O	–	X	Trace Control
63	TAD8	O	–	X	Trace Address
64	TAD2	O	–	X	Trace Address
65	TDT67	I/O	–	W	Trace Data
66	TDT60	I/O	–	W	Trace Data
67	TDT54	I/O	–	W	Trace Data
68	TDT48	I/O	–	W	Trace Data
69	TDT26	I/O	–	W	Trace Data
70	TDT21	I/O	–	W	Trace Data
71	TDT18	I/O	–	W	Trace Data
72	TDT12	I/O	–	W	Trace Data
73	TDT8	I/O	–	W	Trace Data
74	TDT3	I/O	–	W	Trace Data
75	ICS2	O	–	G	ICE Status
76	$V_{DD}5F$	–	–	–	–
77	RSTX	I	–	E	Reset Pin

Table 3-1. CY91FV360GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
78	OUT2	I/O	PL6	A	OCU Output 2
79	IN0	I/O	PL0	A	ICU Input 0
80	INT2	I/O	PK2	A	Ext. Interrupt 2
81	AN6	I/O	PH6	B	ADC Input 6
82	AN1	I/O	PH1	B	ADC Input 1
83	AV_{CC}	–	–	–	Analog V_{CC}
84	DEOP0	I/O	PB2	A	DMA EOP 0
85	AN14	I/O	PG6	B	ADC Input 14
86	AN9	I/O	PG1	B	ADC Input 9
87	AS	I/O	P90	A	Ext. Bus Control
88	BRQ	I/O	P82	A	Ext. Bus Control
89	CS6X	I/O	P76	A	Chip Select 6
90	A23	I/O	–	Q	Ext. Bus Address Bit 23
91	A17	I/O	–	Q	Ext. Bus Address Bit 17
92	A11	I/O	–	Q	Ext. Bus Address Bit 11
93	D27	I/O	–	Q	Ext. Bus Data Bit 27
94	D22	I/O	–	Q	Ext. Bus Data Bit 22
95	D17	I/O	–	Q	Ext. Bus Data Bit 17
96	D6	I/O	–	Q	Ext. Bus Data Bit 16
97	$V_{DD}5S$	–	–	–	–
98	PWM1M3	I/O	PS5	K	SMC 3
99	PWM2M3	I/O	PS7	M	SMC 3
100	$HV_{DD}5A$		–	–	–
101	PWM2P0	I/O	PR2	K	SMC0
102	$V_{CC}3C$	–	–	C	Bypass Capacitor Pin
103	SOT1	I/O	PQ3	A	UART 1 Output
104	SIN0	I/O	PQ0	A	UART 0 Input
105	TX1	I/O	PP2	Q	CAN 1 TX
106	OCPA2	I/O	PO2	A	PPG Output
107	SCK3	I/O	PN5	A	SIO Clock
108	SIN4	I/O	PN1	A	SIO Input
109	SCL	I/O	PM3	Y	I^2C SCL
110	TCLK	I/O	–	W	Trace Control
111	TAD12	O	–	X	Trace Address
112	TAD15	O	–	X	Trace Address
113	TAD1	O	–	X	Trace Address
114	TDT65	I/O	–	W	Trace Data
115	TDT59	I/O	–	W	Trace Data
116	TDT55	I/O	–	W	Trace Data

Table 3-1. CY91FV360GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
117	TDT51	I/O	–	W	Trace Data
118	TDT42	I/O	–	W	Trace Data
119	TDT32	I/O	–	W	Trace Data
120	TDT27	I/O	–	W	Trace Data
121	TDT22	I/O	–	W	Trace Data
122	TDT11	I/O	–	W	Trace Data
123	TDT4	I/O	–	W	Trace Data
124	ICD3	I/O	–	N	ICE Data
125	TDT1	I/O	–	W	Trace Data
126	SELCLK	I	–	F	Clock Selection
127	NMIX	I	–	E	Non maskable Interrupt
128	OUT1	I/O	PL5	A	OCU Output 1
129	IN1	I/O	PL1	A	ICU Input 1
130	INT5	I/O	PK5	A	Ext. Interrupt 5
131	LED4	I/O	PJ4	J	LED Port 4
132	ALARM	I	–	D	Alarm Comparator Input
133	AN7	I/O	PH7	B	ADC Input 7
134	AN2	I/O	PH2	B	ADC Input 2
135	DACK0	I/O	PB1	A	DMA acknowledge 0
136	AN10	I/O	PG2	B	ADC Input 10
137	CS0X	I/O	P94	A	Chip select 0
138	CS3X	I/O	P97	A	Chip select 3
139	BGRNTX	I/O	P81	A	Ext. Bus Control
140	CS4X	I/O	P74	A	Chip select 4
141	A22	I/O	–	Q	Ext. Bus Address Bit 22
142	A18	I/O	–	Q	Ext. Bus Address Bit 18
143	A14	I/O	–	Q	Ext. Bus Address Bit 14
144	A5	I/O	–	Q	Ext. Bus Address Bit 5
145	INDEX	–	–	–	Index Pin
146	D30	I/O	–	Q	Ext. Bus Data Bit 30
147	D26	I/O	–	Q	Ext. Bus Data Bit 26
148	D19	I/O	–	Q	Ext. Bus Data Bit 19
149	D10	I/O	–	Q	Ext. Bus Data Bit 10
150	D9	I/O	–	Q	Ext. Bus Data Bit 9
151	D5	I/O	–	Q	Ext. Bus Data Bit 5
152	PWM2M2	I/O	PS3	M	SMC 2
153	PWM1P3	I/O	PS4	K	SMC 3
154	PWM2M0	I/O	PR3	M	SMC 0
155	V_{SS}	–	–	–	–

Table 3-1. CY91FV360GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
156	SOT2	I/O	PQ5	A	UART 2 Output
157	SOT0	I/O	PQ1	A	UART 0 Output
158	$V_{DD}5O$	–	–	–	–
159	OCPA7	I/O	PO7	A	PPG Output
160	OCPA5	I/O	PO5	A	PPG Output
161	OCPA1	I/O	PO1	A	PPG Output
162	$V_{DD}5K$	–	–	–	–
163	X1A	O	–	I	32 kHz Oscillator Pin
164	X0A	I	–	I	32 kHz Oscillator Pin
165	SDA	I/O	PM2	Y	I^2C SDA
166	TAD10	O	–	X	Trace Address
167	TAD11	O	–	X	Trace Address
168	TDT66	I/O	–	W	Trace Data
169	TDT61	I/O	–	W	Trace Data
170	TDT58	I/O	–	W	Trace Data
171	TDT52	I/O	–	W	Trace Data
172	TDT45	I/O	–	W	Trace Data
173	TDT39	I/O	–	W	Trace Data
174	TDT35	I/O	–	W	Trace Data
175	TDT31	I/O	–	W	Trace Data
176	TDT24	I/O	–	W	Trace Data
177	TDT15	I/O	–	W	Trace Data
178	TDT14	I/O	–	W	Trace Data
179	TDT10	I/O	–	W	Trace Data
180	ICD1	I/O	–	N	ICE Data
181	ICD2	I/O	–	N	ICE Data
182	HSTX	I	–	E	Hardware Standby
183	OUT3	I/O	PL7	A	OCU Output 3
184	OUT0	I/O	PL4	A	OCU Output 0
185	INT6	I/O	PK6	A	Ext. Interrupt 6
186	LED7	I/O	PJ7	J	LED Port 7
187	LED1	I/O	PJ1	J	LED Port 1
188	CPUTESTX	I	–	E	Test Input
189	DA1	O	–	C	DAC Output
190	AN4	I/O	PH4	B	ADC Input 4
191	DEOP1	I/O	PB5	A	DMA EOP 1
192	DACK1	I/O	PB4	A	DMA Acknowledge 1
193	DREQ0	I/O	PB0	A	DMA Request 0
194	CLK	I/O	P92	A	Ext. Bus Clock

Table 3-1. CY91FV360GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
195	AH/BOOT	I/O	P93	A	Ext. Bus Control/Boot Signal
196	CS5X	I/O	P75	A	Chip Select 5
197	A24	I/O	–	Q	Ext. Bus Address Bit 24
198	A21	I/O	–	Q	Ext. Bus Address Bit 21
199	A15	I/O	–	Q	Ext. Bus Address Bit 15
200	A8	I/O	–	Q	Ext. Bus Address Bit 8
201	A2	I/O	–	Q	Ext. Bus Address Bit 2
202	A0	I/O	–	Q	Ext. Bus Address Bit 0
203	D29	I/O	–	Q	Ext. Bus Address Bit 29
204	D25	I/O	–	Q	Ext. Bus Address Bit 25
205	D20	I/O	–	Q	Ext. Bus Address Bit 20
206	D15	I/O	–	Q	Ext. Bus Address Bit 15
207	D4	I/O	–	Q	Ext. Bus Address Bit 4
208	$HV_{DD}5C$	–	–	–	–
209	PWM1M2	I/O	PS1	K	SMC2
210	PWM1P2	I/O	PS0	K	SMC2
211	PWM1M0	I/O	PR1	K	SMC0
212	SIN2	I/O	PQ4	A	UART 2 Input
213	RX3	I/O	PP7	Q	CAN 3 RX
214	V_{SS}	–	–	–	–
215	RX0	I/O	PP1	Q	CAN 0 RX
216	$V_{DD}5N$	–	–	–	–
217	OCPA4	I/O	PO4	A	PPG Output
218	OCPA0	I/O	PO0	A	PPG Output
219	SIN3	I/O	PN3	A	SIO Input
220	V_{SS}	–	–	–	–
221	SGA	I/O	PM1	A	Sound Generator SGA
222	TAD13	O	–	X	Trace Address
223	TAD7	O	–	X	Trace Address
224	TAD6	O	–	X	Trace Address
225	TDT64	I/O	–	W	Trace Data
226	TDT56	I/O	–	W	Trace Data
227	TDT50	I/O	–	W	Trace Data
228	TDT44	I/O	–	W	Trace Data
229	TDT41	I/O	–	W	Trace Data
230	TDT37	I/O	–	W	Trace Data
231	TDT34	I/O	–	W	Trace Data
232	TDT30	I/O	–	W	Trace Data
233	TDT25	I/O	–	W	Trace Data

Table 3-1. CY91FV360GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
234	TDT20	I/O	–	W	Trace Data
235	TDT9	I/O	–	W	Trace Data
236	BREAK	I	–	O	ICE Break
237	ICS1	O	–	G	ICE Status
238	ICS0	O	–	G	ICE Status
239	MD2	I	–	T	Mode Pin 2
240	IN2	I/O	PL2	A	ICU Input 2
241	INT4	I/O	PK4	A	Ext. Interrupt 4
242	LED6	I/O	PJ6	J	LED Port 6
243	LED3	I/O	PJ3	J	LED Port 3
244	Not Connected				
245	TESTX	I	–	E	Test Input
246	DA0	O	–	C	DAC Output
247	AN5	I/O	PH5	B	ADC Input 5
248	AN0	I/O	PH0	B	ADC Input 0
249	AN15	I/O	PG7	B	ADC Input 15
250	CS1X	I/O	P95	A	Chip select 1
251	WR3X	I/O	P87	S	Ext. Bus Control
252	WR2X	I/O	P86	S	Ext. Bus Control
253	DREQ2	I/O	P73	A	DMA Request 2
254	A19	I/O	–	Q	Ext. Bus Address Bit 19
255	A13	I/O	–	Q	Ext. Bus Address Bit 13
256	A7	I/O	–	Q	Ext. Bus Address Bit 7
257	A4	I/O	–	Q	Ext. Bus Address Bit 4
258	D31	I/O	–	Q	Ext. Bus Data Bit 31
259	D28	I/O	–	Q	Ext. Bus Data Bit 28
260	D23	I/O	–	Q	Ext. Bus Data Bit 23
261	D14	I/O	–	Q	Ext. Bus Data Bit 14
262	D8	I/O	–	Q	Ext. Bus Data Bit 8
263	D1	I/O	–	Q	Ext. Bus Data Bit 1
264	D0	I/O	–	Q	Ext. Bus Data Bit 0
265	Not Connected				
266	HV_{SS}	–	–	–	–
267	Not Connected				
268	V_{SS}	–	–	–	–
269	RX2	I/O	PP5	Q	CAN 2 RX
270	RX1	I/O	PP3	Q	CAN 1 RX
271	V_{SS}	–	–	–	–
272	OCPA3	I/O	PO3	A	PPG Output

Table 3-1. CY91FV360GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
273	V_{SS}	–	–	–	–
274	Not Connected				
275	$V_{DD}5I$	–	–	–	–
276	TADSCX	O	–	X	Trace Control
277	TCE1X	O	–	X	Trace Control
278	TAD4	O	–	X	Trace Address
279	TAD0	O	–	X	Trace Address
280	TDT62	I/O	–	W	Trace Data
281	TDT53	I/O	–	W	Trace Data
282	TDT47	I/O	–	W	Trace Data
283	TDT43	I/O	–	W	Trace Data
284	TDT36	I/O	–	W	Trace Data
285	TDT33	I/O	–	W	Trace Data
286	TDT28	I/O	–	W	Trace Data
287	TDT19	I/O	–	W	Trace Data
288	TDT13	I/O	–	W	Trace Data
289	TDT6	I/O	–	W	Trace Data
290	TDT5	I/O	–	W	Trace Data
291	X1	O	–	H	4 MHz Oscillator Pin
292	MONCLK	O	–	G	Clock Output for test purposes
293	MD0	I	–	T	Mode Pin 0
294	INT7	I/O	PK7	A	Ext. Interrupt 7
295	INT1	I/O	PK1	A	Ext. Interrupt 1
296	LED5	I/O	PJ5	J	LED Port 5
297	LTESTX	I	–	E	Test Input
298	ATGX	I/O	PI3	A	Analog Reference Low
299	AVRL	–	–	R	Analog Reference High
300	AVRH	–	–	R	DMA Request 1
301	DREQ1	I/O	PB3	A	ADC Input 12
302	AN12	I/O	PG4	B	ADC Input 11
303	AN11	I/O	PG3	B	Ext. Bus Control
304	WR0X	I/O	P84	S	Ext. Bus Control
305	RDY	I/O	–	S	Ext. Bus Control
306	A25	I/O	–	Q	Ext. Bus Address Bit 25
307	A16	I/O	–	Q	Ext. Bus Address Bit 16
308	A10	I/O	–	Q	Ext. Bus Address Bit 10
309	A6	I/O	–	Q	Ext. Bus Address Bit 6
310	A1	I/O	–	Q	Ext. Bus Address Bit 1
311	Not Connected				

Table 3-1. CY91FV360GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
312	D24	I/O	–	Q	Ext. Bus Data Bit 24
313	D12	I/O	–	Q	Ext. Bus Data Bit 12
314	Not Connected				
315	PWM2P3	I/O	PS6	K	SMC 3
316	HV_{SS}	–	–	–	–
317	HV_{SS}	–	–	–	–
318	Not Connected				
319	$V_{DD}5Q$	–	–	–	–
320	TX2	I/O	PP4	Q	CAN 2 TX
321	TX0	I/O	PP0	Q	CAN 0 TX
322	OCPA6	I/O	PO6	A	PPG Output
323	$V_{DD}5M$	–	–	–	–
324	$V_{DD}5L$	–	–	–	–
325	Not Connected				
326	$V_{DD}5H$	–	–	–	–
327	TAD14	O	–	X	Trace Address
328	$V_{SS}3$	–	–	–	–
329	$V_{SS}3$	–	–	–	–
330	Not Connected				
331	$V_{DD}3C$	–	–	–	–
332	TDT46	I/O	–	W	Trace Data
333	TDT40	I/O	–	W	Trace Data
334	TDT38	I/O	–	W	Trace Data
335	$V_{DD}3B$	–	–	–	–
336	TDT29	I/O	–	W	Trace Data
337	TDT17	I/O	–	W	Trace Data
338	$V_{DD}3A$	–	–	–	–
339	TDT0	I/O	–	W	Trace Data
340	V_{SS}	–	–	–	–
341	V_{SS}	–	–	–	–
342	Not Connected				
343	$V_{DD}5E$	–	–	–	–
344	INT0	I/O	PK0	A	Ext. Interrupt 0
345	LED2	I/O	PJ2	J	LED Port 2
346	LED0	I/O	PJ0	J	LED Port 0
347	$V_{DD}5D$	–	–	–	–
348	AV_{SS}	–	–	–	Analog V_{SS}
349	DEOP2	I/O	PB7	A	DMA EOP 2
350	$V_{DD}5C$	–	–	–	–

Table 3-1. CY91FV360GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
351	CS2X	I/O	P96	A	Chip Select 2
352	V_{SS}	–	–	–	–
353	V_{SS}	–	–	–	–
354	$V_{DD}5B$	–	–	–	–
355	Not Connected				
356	A9	I/O	–	Q	Ext. Bus Address Bit 9
357	A3	I/O	–	Q	Ext. Bus Address Bit 3
358	V_{SS}	–	–	–	–
359	V_{SS}	–	–	–	–
360	$V_{DD}5T$	–	–	–	–
361	V_{SS}	–	–	–	–
362	V_{SS}	–	–	–	–
363	V_{SS}	–	–	–	–
364	Not Connected				
365	HV_{SS}	–	–	–	–
366	V_{SS}	–	–	–	–
367	V_{SS}	–	–	–	–
368	Not Connected				
369	V_{SS}	–	–	–	–
370	V_{SS}	–	–	–	–
371	Not Connected				
372	V_{SS}	–	–	–	–
373	V_{SS}	–	–	–	–
374	V_{SS}	–	–	–	–
375	$V_{DD}3D$	–	–	–	–
376	$V_{SS}3$	–	–	–	–
377	$V_{SS}3$	–	–	–	–
378	$V_{SS}3$	–	–	–	–
379	Not Connected				
380	$V_{SS}3$	–	–	–	–
381	$V_{SS}3$	–	–	–	–
382	Not Connected				
383	$V_{SS}3$	–	–	–	–
384	$V_{SS}3$	–	–	–	–
385	$V_{SS}3$	–	–	–	–
386	$V_{DD}5G$	–	–	–	–
387	V_{SS}	–	–	–	–
388	V_{SS}	–	–	–	–
389	V_{SS}	–	–	–	–

Table 3-1. CY91FV360GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
390	Not Connected				
391	V_{SS}	–	–	–	–
392	V_{SS}	–	–	–	–
393	Not Connected				
394	V_{SS}	–	–	–	–
395	V_{SS}	–	–	–	–
396	V_{SS}	–	–	–	–
397	Not Connected				
398	V_{SS}	–	–	–	–
399	V_{SS}	–	–	–	–
400	V_{SS}	–	–	–	–
401	$V_{DD}5A$	–	–	–	–

Table 3-2. CY91FV362GB I/O Pins and their Functions

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	D24	I/O	–	Q	Ext. Bus Data Bit 24
2	D25	I/O	–	Q	Ext. Bus Data Bit 25
3	D26	I/O	–	Q	Ext. Bus Data Bit 26
4	D27	I/O	–	Q	Ext. Bus Data Bit 27
5	D28	I/O	–	Q	Ext. Bus Data Bit 28
6	D29	I/O	–	Q	Ext. Bus Data Bit 29
7	D30	I/O	–	Q	Ext. Bus Data Bit 30
8	D31	I/O	–	Q	Ext. Bus Data Bit 31
9	A0	I/O	–	Q	Ext. Bus Address Bit 0
10	A1	I/O	–	Q	Ext. Bus Address Bit 1
11	A2	I/O	–	Q	Ext. Bus Address Bit 2
12	A3	I/O	–	Q	Ext. Bus Address Bit 3
13	A4	I/O	–	Q	Ext. Bus Address Bit 4
14	A5	I/O	–	Q	Ext. Bus Address Bit 5
15	A6	I/O	–	Q	Ext. Bus Address Bit 6
16	A7	I/O	–	Q	Ext. Bus Address Bit 7
17	A8	I/O	–	Q	Ext. Bus Address Bit 8
18	A9	I/O	–	Q	Ext. Bus Address Bit 9
19	A10	I/O	–	Q	Ext. Bus Address Bit 10
20	A11	I/O	–	Q	Ext. Bus Address Bit 11
21	A12	I/O	–	Q	Ext. Bus Address Bit 12
22	A13	I/O	–	Q	Ext. Bus Address Bit 13
23	A14	I/O	–	Q	Ext. Bus Address Bit 14

Table 3-2. CY91FV362GB I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
24	A15	I/O	–	Q	Ext. Bus Address Bit 15
25	$V_{DD}35$	–	–	–	Separated Ext. Bus VDD, 3.3 V or 5.0 V
26	V_{SS}	–	–	–	–
27	A16	I/O	–	Q	Ext. Bus Address Bit 16
28	A17	I/O	–	Q	Ext. Bus Address Bit 17
29	A18	I/O	–	Q	Ext. Bus Address Bit 18
30	A19	I/O	–	Q	Ext. Bus Address Bit 19
31	A20	I/O	–	Q	Ext. Bus Address Bit 20
32	CS4X	I/O	P74	A	Chip Select 4
33	CS5X	I/O	P75	A	Chip Select 5
34	CS6X	I/O	P76	A	Chip Select 6
35	RDY	I/O	–	S	Ext. Bus Control
36	BGRNT	I/O	P81	A	Ext. Bus Control
37	BRQ	I/O	P82	A	Ext. Bus Control
38	RDX	I/O	–	S	Ext. Bus Control
39	WR0X	I/O	–	S	Ext. Bus Control
40	WR1X	I/O	–	S	Ext. Bus Control
41	WR2X	I/O	–	S	Ext. Bus Control
42	WR3X	I/O	–	S	Ext. Bus Control
43	AS	I/O	P90	A	Ext. Bus Control
44	ALE	I/O	P91	A	Ext. Bus Control
45	CLK	I/O	–	A	Ext. Bus Clock
46	AH	I/O	P93	A	Ext. Bus Control Signal
47	CS0X	I/O	P94	A	Chip select 0
48	CS1X	I/O	P95	A	Chip select 1
49	CS2X	I/O	P96	A	Chip select 2
50	CS3X	I/O	P97	A	Chip select 3
51	$V_{DD}35$	–	–	–	Separated Ext. Bus V_{DD}, 3.3 or 5.0 V
52	V_{SS}	–	–	–	–
53	AN8	I/O	PG0	B	ADC Input 8
54	AN9	I/O	PG1	B	ADC Input 9
55	AN10	I/O	PG2	B	ADC Input 10
56	AN11	I/O	PG3	B	ADC Input 11
57	AN12	I/O	PG4	B	ADC Input 12
58	AN13	I/O	PG5	B	ADC Input 13
59	AN14	I/O	PG6	B	ADC Input 14
60	AN15	I/O	PG7	B	ADC Input 15
61	DREQ0	I/O	PB0	A	DMR Request 0
62	DACK0	I/O	PB1	A	DMA Acknowledge 0

Table 3-2. CY91FV362GB I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
63	DEOP0	I/O	PB2	A	DMA EOP 0
64	A	–	–	–	Analog V_{CC}
65	AVRH	–	–	R	Analog Reference High
66	AN0	I/O	PH0	B	ADC Input 0
67	AN1	I/O	PH1	B	ADC Input 1
68	AN2	I/O	PH2	B	ADC Input 2
69	AN3	I/O	PH3	B	ADC Input 3
70	AN4	I/O	PH4	B	ADC Input 4
71	AN5	I/O	PH5	B	ADC Input 5
72	AN6	I/O	PH6	B	ADC Input 6
73	AN7	I/O	PH7	B	ADC Input 7
74	AV_{SS}	–	–	–	Analog V_{SS}, Analog Reference Low
75	DA0	O	–	C	DAC Output
76	DA1	O	–	C	DAC Output
77	ALARM	I	–	D	Alarm Comparator Input
78	V_{SS}	–	–	–	–
79	V_{DD}	–	–	–	–
80	ATGX	I/O	PI3	A	ADC Trigger Input
81	TESTX	I	–	E	Test Input (should be connected to V_{DD})
82	CPUTESTX	I	–	E	Test Input (should be connected to V_{DD})
83	LTESTX	I	–	E	Test Input (should be connected to V_{DD})
84	LED0	I/O	PJ0	J	LED Port 0
85	LED1	I/O	PJ1	J	LED Port 1
86	LED2	I/O	PJ2	J	LED Port 2
87	LED3	I/O	PJ3	J	LED Port 3
88	LED4	I/O	PJ4	J	LED Port 4
89	LED5	I/O	PJ5	J	LED Port 5
90	LED6	I/O	PJ6	J	LED Port 6
91	LED7	I/O	PJ7	J	LED Port 7
92	V_{DD}	–	–	–	–
93	V_{SS}	–	–	–	–
94	INT0	I/O	PK0	A	Ext. Interrupt 0
95	INT1	I/O	PK1	A	Ext. Interrupt 1
96	INT2	I/O	PK2	A	Ext. Interrupt 2
97	INT3	I/O	PK3	A	Ext. Interrupt 3
98	INT4	I/O	PK4	A	Ext. Interrupt 4
99	INT5	I/O	PK5	A	Ext. Interrupt 5

Table 3-2. CY91FV362GB I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
100	INT6	I/O	PK6	A	Ext. Interrupt 6
101	INT7	I/O	PK7	A	Ext. Interrupt 7
102	IN0	I/O	PL0	A	ICU Input 0
103	IN1	I/O	PL1	A	ICU Input 1
104	IN2	I/O	PL2	A	ICU Input 2
105	IN3	I/O	PL3	A	ICU Input 3
106	OUT0	I/O	PL4	A	OCU Output 0
107	OUT1	I/O	PL5	A	OCU Output 1
108	OUT2	I/O	PL6	A	OCU Output 2
109	OUT3	I/O	PL7	A	OCU Output 3
110	V_{SS}	–	–	–	–
111	MD0	I	–	T	Mode Pin 0
112	MD1	I	–	T	Mode Pin 1
113	MD2	I	–	T	Mode Pin 2
114	HSTX	I	–	E	Hardware Standby
115	INITX	I	–	U	Initial Pin
116	MONCLK	O	–	G	System Clock Output for Evaluation Purposes
117	SELCLK	I	–	F	Clock Selection, must be connected to V_{DD}
118	V_{DD}	–	–	–	–
119	X0	I	–	H	4 MHz Oscillator Pin
120	X1	O	–	H	4 MHz Oscillator Pin
121	X0A	I	–	I	Reserved-must be connected to V_{SS}
122	X1A	O	–	I	Reserved-should be left open
123	V_{SS}	–	–	–	–
124	CPO	–	–	C	Reserved-should be left open
125	VCI	–	–	D	Reserved-must be connected to V_{SS}
126	SGO	I/O	PM0	A	Sound Generator SGO
127	SGA	I/O	PM1	A	Sound Generator SGA
128	SDA	I/O	PM2	Y	I^2C SDA
129	SCL	I/O	PM3	Y	I^2C SCL
130	SOT4	I/O	PN0	A	SIO Output
131	SIN4	I/O	PN1	A	SIO Input
132	SCK4	I/O	PN2	A	SIO Clock
133	SIN3	I/O	PN3	A	SIO Input
134	SOT3	I/O	PN4	A	SIO Output
135	SCK3	I/O	PN5	A	SIO Clock
136	OCPA 0	I/O	PO0	A	PPG Output
137	OCPA 1	I/O	PO1	A	PPG Output

Table 3-2. CY91FV362GB I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
138	OCPA 2	I/O	PO2	A	PPG Output
139	OCPA 3	I/O	PO3	A	PPG Output
140	OCPA 4	I/O	PO4	A	PPG Output
141	OCPA 5	I/O	PO5	A	PPG Output
142	OCPA 6	I/O	PO6	A	PPG Output
143	OCPA 7	I/O	PO7	A	PPG Output
144	V_{DD}	–	–	–	–
145	V_{SS}	–	–	–	–
146	TX0	I/O	PP0	Q	CAN 0 TX
147	RX0	I/O	PP1	Q	CAN 0 RX
148	TX1	I/O	PP2	Q	CAN 1 TX
149	RX1	I/O	PP3	Q	CAN 1 RX
150	TX2	I/O	PP4	Q	CAN 2 TX
151	RX2	I/O	PP5	Q	CAN 2 RX
152	SIN0	I/O	PQ0	A	UART 0 Input
153	SOT0	I/O	PQ1	A	UART 0 Output
154	SIN1	I/O	PQ2	A	UART 1 Input
155	SOT1	I/O	PQ3	A	UART 1 Output
156	SIN2	I/O	PQ4	A	UART 2 Input
157	SOT2	I/O	PQ5	A	UART 2 Output
158	V_{SS}	–	–	–	–
159	$V_{CC}3C$	–	–	C	Bypass Capacitor Pin
160	V_{DD}	–	–	–	–
161	HV_{SS}	–	–	–	–
162	PWM1P0	I/O	PR0	K	SMC 0
163	PWM1M0	I/O	PR1	K	SMC 0
164	PWM2P0	I/O	PR2	K	SMC 0
165	PWM2M0	I/O	PR3	M	SMC 0
166	HV_{DD}	–	–	–	–
167	PWM1P1	I/O	PR4	K	SMC 1
168	PWM1M1	I/O	PR5	K	SMC 1
169	PWM2P1	I/O	PR6	K	SMC 1
170	PWM2M1	I/O	PR7	M	SMC 1
171	HV_{SS}	–	–	–	–
172	PWM1P2	I/O	PS0	K	SMC 2
173	PWM1M2	I/O	PS1	K	SMC 2
174	PWM2P2	I/O	PS2	K	SMC 2
175	PWM2M2	I/O	PS3	M	SMC 2
176	HV_{DD}	–	–	–	–

Table 3-2. CY91FV362GB I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
177	PWM1P3	I/O	PS4	K	SMC 3
178	PWM1M3	I/O	PS5	K	SMC 3
179	PWM2P3	I/O	PS6	K	SMC 3
180	PWM2M3	I/O	PS7	M	SMC 3
181	HV_{SS}	–	–	–	–
182	$V_{DD}35$	–	–	–	Separated Ext. Bus V_{DD}, 3.3 or 5.0 V
183	D0	I/O	–	Q	Ext. Bus Data Bit 0
184	D1	I/O	–	Q	Ext. Bus Data Bit 1
185	D2	I/O	–	Q	Ext. Bus Data Bit 2
186	D3	I/O	–	Q	Ext. Bus Data Bit 3
187	D4	I/O	–	Q	Ext. Bus Data Bit 4
188	D5	I/O	–	Q	Ext. Bus Data Bit 5
189	D6	I/O	–	Q	Ext. Bus Data Bit 6
190	D7	I/O	–	Q	Ext. Bus Data Bit 7
191	D8	I/O	–	Q	Ext. Bus Data Bit 8
192	D9	I/O	–	Q	Ext. Bus Data Bit 9
193	D10	I/O	–	Q	Ext. Bus Data Bit 10
194	D11	I/O	–	Q	Ext. Bus Data Bit 11
195	D12	I/O	–	Q	Ext. Bus Data Bit 12
196	D13	I/O	–	Q	Ext. Bus Data Bit 13
197	D14	I/O	–	Q	Ext. Bus Data Bit 14
198	$V_{DD}35$	–	–	–	Separated Ext. Bus V_{DD}, 3.3 or 5.0 V
199	V_{SS}	–	–	–	–
200	D15	I/O	–	Q	Ext. Bus Data Bit 15
201	D16	I/O	–	Q	Ext. Bus Data Bit 16
202	D17	I/O	–	Q	Ext. Bus Data Bit 17
203	D18	I/O	–	Q	Ext. Bus Data Bit 18
204	D19	I/O	–	Q	Ext. Bus Data Bit 19
205	D20	I/O	–	Q	Ext. Bus Data Bit 20
206	D21	I/O	–	Q	Ext. Bus Data Bit 21
207	D22	I/O	–	Q	Ext. Bus Data Bit 22
208	D23	I/O	–	Q	Ext. Bus Data Bit 23

Note: If pins $V_{DD}35$ (25, 51, 182, 198) are connected to 3.3 V then the external bus interface (pins 1-52, 182-208) can be operated at 3.3 V levels.

Table 3-3. CY91F364G I/O Pins and their Functions

Pin No	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	AN0	I/O	PH0	B	ADC Input 0
2	AN1	I/O	PH1	B	ADC Input 1
3	AN2	I/O	PH2	B	ADC Input 2
4	AN3	I/O	PH3	B	ADC Input 3
5	AN4	I/O	PH4	B	ADC Input 4
6	AN5	I/O	PH5	B	ADC Input 5
7	AV_{SS}, AVRL	–	–	–	AV_{SS}, Analog Reference Low
8	AVRH	–	–	R	Analog Reference High
9	AV_{CC}	–	–	–	AV_{CC}
10	AN6	I/O	PH6	B	ADC Input 6
11	AN7	I/O	PH7	B	ADC Input 7
12	AN8	I/O	PG0	B	ADC Input 8
13	AN9	I/O	PG1	B	ADC Input 9
14	AN10	I/O	PG2	B	ADC Input 10
15	AN11	I/O	PG3	B	ADC Input 11
16	V_{SS}	–	–	–	–
17	V_{DD}	–	–	–	–
18	SDA	I/O	PM2	YA	I^2C SDA
19	SCL	I/O	PM3	YA	I^2C SCL
20	SOT0	I/O	PQ1	A	UART 0 SOT
21	SIN0	I/O	PQ0	A	UART 0 SIN
22	HSTX	I	–	F	Hardware Standby
23	NMIX	I	–	E	Non Maskable Interrupt
24	SELCLK	I	–	F	Select RTC Clock
25	V_{DD}	–	–	–	–
26	MONCLK	O	–	Q1	Modulated Clock Output
27	V_{SS}	–	–	–	–
28	X1A	O	–	I	32 kHz Oscillator Pin
29	X0A	I	–	I	32 kHz Oscillator Pin
30	V_{DD}	–	–	–	–
31	X1	O	–	H	4 MHz Oscillator Pin
32	X0	I	–	H	4 MHz Oscillator Pin
33	V_{SS}	–	–	–	–
34	INT0	I/O	PK0	B	External Interrupt 0
35	INT1	I/O	PK1	B	External Interrupt 1
36	INT2	I/O	PK2	B	External Interrupt 2
37	INT3	I/O	PK3	B	External Interrupt 3

Table 3-3. CY91F364G I/O Pins and their Functions *(continued)*

Pin No	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
38	INT4	I/O	PK4	B	External Interrupt 4
39	INT5	I/O	PK5	B	External Interrupt 5
40	INT6	I/O	PK6	B	External Interrupt 6
41	INT7	I/O	PK7	B	External Interrupt 7
42	V_{DD}	–	–	–	–
43	V_{SS}	–	–	–	–
44	IN0	I/O	PL0	B	ICU Input 0 [a]
45	IN1	I/O	PL1	B	ICU Input 1 [a]
46	IN2	I/O	PL2	B	ICU Input 2 [a]
47	IN3	I/O	PL3	B	ICU Input 3 [a]
48	OUT0	I/O	PL4	B	OCU Output 0
49	OUT1	I/O	PL5	B	OCU Output 1
50	OUT2	I/O	PL6	B	OCU Output 2
51	OUT3	I/O	PL7	B	OCU Output 3
52	V_{DD}	–	–	–	–
53	V_{SS}	–	–	–	–
54	TESTX	I	–	E	Test Input
55	CPUTESTX	I	–	E	Test Input
56	ATGX	I/O	PI3	A	ADC Trigger
57	MD0	I	–	T	Mode Pin 0
58	MD1	I	–	T	Mode Pin 1
59	MD2	I	–	T	Mode Pin 2
60	INITX	I	–	U	Initial Pin
61	V_{DD}	–	–	–	–
62	V_{CC}3C	–	–	–	Pins for power supply capacitor or for external power supply of core voltage
63	V_{CC}3C	–	–	–	
64	V_{SS} (#)	–	–	–	Don't connect to V_{SS} in first ES series. Leave open. [b]
65	V_{DD}I	–	–	–	Separate Core Power Supply
66	V_{DD}I	–	–	–	
67	V_{DD}I	–	–	–	
68	BREAKX	I	BREAKX	E	EDSU Break Pin
69	V_{DD}	–	–	–	–
70	V_{SS}	–	–	–	–
71	RX0	I/O	PP1	Q	CAN RX
72	TX0	I/O	PP0	Q	CAN TX
73	OCPA0	I/O	PO0	A	PPG Output 0
74	OCPA1	I/O	PO1	A	PPG Output 1
75	OCPA2	I/O	PO2	A	PPG Output 2

Table 3-3. CY91F364G I/O Pins and their Functions *(continued)*

Pin No	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
76	OCPA3	I/O	PO3	A	PPG Output 3
77	V_{SS}	–	–	–	–
78	SIN5	I/O	PT0	A	USART 5 SIN
79	SCK5	I/O	PT1	A	USART 5 SCK
80	SOT5	I/O	PT2	A	USART 5 SOT
81	SOT6	I/O	PT3	A	USART 6 SOT
82	SCK6	I/O	PT4	A	USART 6 SCK
83	SIN6	I/O	PT5	A	USART 6 SIN
84	V_{DD}	–	–	–	–
85	V_{SS}	–	–	–	–
86	SIN3	I/O	PN3	A	SIO SIN
87	SOT3	I/O	PN4	A	SIO SOT
88	SCK3	I/O	PN5	A	SIO SCK
89	V_{SS}	–	–	–	–
90	LTESTX	I	LTESTX	E	Test Pin
91	V_{DD}	–	–	–	–
92	PR0	I/O	PR0	A	Port R 0
93	PR1	I/O	PR1	A	Port R 1
94	PR2	I/O	PR2	A	Port R 2
95	PR3	I/O	PR3	A	Port R 3
96	PR4	I/O	PR4	A	Port R 4
97	PR5	I/O	PR5	A	Port R 5
98	PR6	I/O	PR6	A	Port R 6
99	PR7	I/O	PR7	A	Port R 7
100	V_{SS}	–	–	–	–
101	V_{DD}	–	–	–	–
102	LED0	I/O	PJ0	J	LED Port 0
103	LED1	I/O	PJ1	J	LED Port 1
104	LED2	I/O	PJ2	J	LED Port 2
105	LED3	I/O	PJ3	J	LED Port 3
106	V_{SS}	–	–	–	–
107	LED4	I/O	PJ4	J	LED Port 4
108	LED5	I/O	PJ5	J	LED Port 5
109	LED6	I/O	PJ6	J	LED Port 6
110	LED7	I/O	PJ7	J	LED Port 7
111	V_{SS}	–	–	–	–
112	V_{DD}	–	–	–	–
113	PO4	I/O	PO4	A	Port O 4

Table 3-3. CY91F364G I/O Pins and their Functions *(continued)*

Pin No	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
114	PO5	I/O	PO5	A	Port O 5
115	PO6	I/O	PO6	A	Port O 6
116	PO7	I/O	PO7	A	Port O 7
117	DA0	O	–	C	[c]
118	DA1	O	–	C	[c]
119	V_{SS}	–	–	–	–
120	V_{DD}	–	–	–	–

a. If the port L function register bits are cleared, the ICU input lines are connected with the LSYNC outputs of the LIN-USARTs.
b. Pin 064 (V_{SS}) will be available after redesign.
c. he pins DA1 and DA0 are also used for digital test functions. To ensure proper system function, always write “0” to port P R-bus port data direction register DDRP [3:2] and port P R-bus port function register PFRP [3:2].

Table 3-4. CY91F369GA I/O Pins and their Functions

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	A4	I/O	–	Q	Ext. Bus Address Bit 4
2	A5	I/O	–	Q	Ext. Bus Address Bit 5
3	A6	I/O	–	Q	Ext. Bus Address Bit 6
4	A7	I/O	–	Q	Ext. Bus Address Bit 7
5	A8	I/O	–	Q	Ext. Bus Address Bit 8
6	A9	I/O	–	Q	Ext. Bus Address Bit 9
7	A10	I/O	–	Q	Ext. Bus Address Bit 10
8	A11	I/O	–	Q	Ext. Bus Address Bit 11
9	V_{DD}35	–	–	–	Separated Ext. Bus V_{DD}, 3.3 or 5.0 V
10	CLK	I/O	–	A	Ext. Bus Clock
11	V_{SS}	–	–	–	–
12	A12	I/O	–	Q	Ext. Bus Address Bit 12
13	A13	I/O	–	Q	Ext. Bus Address Bit 13
14	A14	I/O	–	Q	Ext. Bus Address Bit 14
15	A15	I/O	–	Q	Ext. Bus Address Bit 15
16	A16	I/O	–	Q	Ext. Bus Address Bit 16
17	A17	I/O	–	Q	Ext. Bus Address Bit 17
18	A18	I/O	–	Q	Ext. Bus Address Bit 18
19	A19	I/O	–	Q	Ext. Bus Address Bit 19
20	A20	I/O	–	Q	Ext. Bus Address Bit 20
21	V_{DD}35	–	–	–	Separated Ext. Bus V_{DD}, 3.3 or 5.0 V
22	V_{SS}	–	–	–	–
23	CS4X	I/O	P74	A	Chip Select 4
24	CS5X	I/O	P75	A	Chip Select 5
25	CS6X	I/O	P76	A	Chip Select 6

Table 3-4. CY91F369GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
26	RDX	I/O	–	S	Ext. Bus Control
27	BGRNTX	I/O	P81	A	Ext. Bus Control
28	BRQ	I/O	P82	A	Ext. Bus Control
29	AS	I/O	P90	A	Ext. Bus Control
30	ALE	I/O	P91	A	Ext. Bus Control
31	AH	I/O	P93	A	Ext. Bus Control Signal
32	CS0X	I/O	P94	A	Chip select 0
33	CS1X	I/O	P95	A	Chip select 1
34	CS2X	I/O	P96	A	Chip select 2
35	CS3X	I/O	P97	A	Chip select 3
36	DREQ0	I/O	PB0	A	DMA Request 0
37	DACK0	I/O	PB1	A	DMA Acknowledge 0
38	DEOP0	I/O	PB2	A	DMA EOP 0
39	V_{SS}	–	–	–	–
40	$V_{DD}35$	–	–	–	Separated Ext. Bus V_{DD}, 3.3 or 5.0 V
41	AVRH	–	–	R	Analog Reference High
42	AV_{CC}	–	–	–	Analog V_{CC}
43	AV_{SS}	–	–	–	Analog V_{SS}, Analog Reference Low
44	AN0	I/O	PH0	B	ADC Input 0
45	AN1	I/O	PH1	B	ADC Input 1
46	AN2	I/O	PH2	B	ADC Input 2
47	AN3	I/O	PH3	B	ADC Input 3
48	AN4	I/O	PH4	B	ADC Input 4
49	AN5	I/O	PH5	B	ADC Input 5
50	AN6	I/O	PH6	B	ADC Input 6
51	AN7	I/O	PH7	B	ADC Input 7
52	AN8	I/O	PG0	B	ADC Input 8
53	AN9	I/O	PG1	B	ADC Input 9
54	ALARM	I	–	D	Alarm Comparator Input
55	V_{SS}	–	–	–	–
56	V_{DD}	–	–	–	–
57	ATGX	I/O	P13	A	ADC Trigger Input
58	MD0	I	–	T	Mode Pin 0
59	MD1	I	–	T	Mode Pin 1
60	MD2	I	–	T	Mode Pin 2
61	HSTX	I	–	E	Hardware Standby
62	INITX	I	–	U	Initual Pin
63	TESTX	I	–	E	Test Input (should be connected to V_{DD})

Table 3-4. CY91F369GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
64	CPUTESTX	I	–	E	Test Input (should be connected to V_{DD})
65	LTESTX	I	–	E	Test Input (should be connected to V_{DD})
66	V_{DD}	–	–	–	–
67	V_{SS}	–	–	–	–
68	INT0	I/O	PK0	A	Ext. Interrupt 0
69	INT1	I/O	PK1	A	Ext. Interrupt 1
70	INT2	I/O	PK2	A	Ext. Interrupt 2
71	INT3	I/O	PK3	A	Ext. Interrupt 3
72	INT4	I/O	PK4	A	Ext. Interrupt 4
73	INT5	I/O	PK5	A	Ext. Interrupt 5
74	INT6	I/O	PK6	A	Ext. Interrupt 6
75	INT7	I/O	PK7	A	Ext. Interrupt 7
76	SGO	I/O	PM0	A	Sound Generator SGO
77	SGA	I/O	PM1	A	Sound Generator SGA
78	SDA	I/O	PM2	Y	I^2C SDA
79	SCL	I/O	PM3	Y	I^2C SCL
80	SOT4	I/O	PN0	A	SIO Output
81	SIN4	I/O	PN1	A	SIO Input
82	SCK4	I/O	PN2	A	SIO Clock
83	SIN3	I/O	PN3	A	SIO Input
84	SOT3	I/O	PN4	A	SIO Output
85	SCK3	I/O	PN5	A	SIO Clock
86	V_{SS}	–	–	–	–
87	$V_{DD}I$	–	–	–	Supply Voltage for Internal Regulator
88	$V_{DD}I$	–	–	–	Supply Voltage for Internal Regulator
89	$V_{DD}I$	–	–	–	Supply Voltage for Internal Regulator
90	$V_{DD}I$	–	–	–	Supply Voltage for Internal Regulator
91	$V_{CC}3C$	–	–	–	Capacitor Pin for Internal Regulator
92	V_{SS}	–	–	–	–
93	TX0	I/O	PP0	Q	CAN 0 TX
94	RX0	I/O	PP1	Q	CAN 0 RX
95	TX1	I/O	PP2	Q	CAN 1 TX
96	RX1	I/O	PP3	Q	CAN 1 RX
97	SIN0	I/O	PQ0	A	UART 0 Input
98	SOT0	I/O	PQ1	A	UART 0 Output
99	V_{DD}	–	–	–	–
100	V_{SS}	–	–	–	–
101	OCPA0	I/O	PO0	A	PPG Output

Table 3-4. CY91F369GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
102	OCPA1	I/O	PO1	A	PPG Output
103	OCPA2	I/O	PO2	A	PPG Output
104	OCPA3	I/O	PO3	A	PPG Output
105	V_{DD}	–	–	–	–
106	X0	I	–	H	4 MHz Oscillator Pin
107	X1	O	–	H	4 MHz Oscillator Pin
108	V_{SS}	–	–	–	–
109	V_{DD}	–	–	–	–
110	MONCLK	O	–	Q1	System Clock Output
111	V_{SS}	–	–	–	–
112	$V_{DD}35$	–	–	–	Separated Ext. Bus V_{DD}, 3.3 or 5.0 V
113	V_{SS}	–	–	–	–
114	WR3X	I/O	–	S	Ext. Bus Control
115	WR2X	I/O	–	S	Ext. Bus Control
116	WR1X	I/O	–	S	Ext. Bus Control
117	WR0X	I/O	–	S	Ext. Bus Control
118	RDY	I/O	–	S	Ext. Bus Control
119	$V_{DD}35$	–	–	–	Separated Ext. Bus V_{DD}, 3.3 or 5.0 V
120	V_{SS}	–	–	–	–
121	D0	I/O	–	Q	Ext. Bus Data Bit 0
122	D1	I/O	–	Q	Ext. Bus Data Bit 1
123	D2	I/O	–	Q	Ext. Bus Data Bit 2
124	D3	I/O	–	Q	Ext. Bus Data Bit 3
125	D4	I/O	–	Q	Ext. Bus Data Bit 4
126	D5	I/O	–	Q	Ext. Bus Data Bit 5
127	D6	I/O	–	Q	Ext. Bus Data Bit 6
128	D7	I/O	–	Q	Ext. Bus Data Bit 7
129	D8	I/O	–	Q	Ext. Bus Data Bit 8
130	D9	I/O	–	Q	Ext. Bus Data Bit 9
131	D10	I/O	–	Q	Ext. Bus Data Bit 10
132	D11	I/O	–	Q	Ext. Bus Data Bit 11
133	D12	I/O	–	Q	Ext. Bus Data Bit 12
134	D13	I/O	–	Q	Ext. Bus Data Bit 13
135	D14	I/O	–	Q	Ext. Bus Data Bit 14
136	D15	I/O	–	Q	Ext. Bus Data Bit 15
137	$V_{DD}35$	–	–	–	Separated Ext. Bus V_{DD}, 3.3 or 5.0 V
138	V_{SS}	–	–	–	–
139	D16	I/O	–	Q	Ext. Bus Data Bit 16
140	D17	I/O	–	Q	Ext. Bus Data Bit 17

Table 3-4. CY91F369GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
141	D18	I/O	–	Q	Ext. Bus Data Bit 18
142	D19	I/O	–	Q	Ext. Bus Data Bit 19
143	D20	I/O	–	Q	Ext. Bus Data Bit 20
144	D21	I/O	–	Q	Ext. Bus Data Bit 21
145	D22	I/O	–	Q	Ext. Bus Data Bit 22
146	D23	I/O	–	Q	Ext. Bus Data Bit 23
147	D24	I/O	–	Q	Ext. Bus Data Bit 24
148	D25	I/O	–	Q	Ext. Bus Data Bit 25
149	D26	I/O	–	Q	Ext. Bus Data Bit 26
150	D27	I/O	–	Q	Ext. Bus Data Bit 27
151	D28	I/O	–	Q	Ext. Bus Data Bit 28
152	D29	I/O	–	Q	Ext. Bus Data Bit 29
153	D30	I/O	–	Q	Ext. Bus Data Bit 30
154	D31	I/O	–	Q	Ext. Bus Data Bit 31
155	$V_{DD}35$	–	–	–	Separated Ext. Bus V_{DD}, 3.3 or 5.0 V
156	V_{SS}	–	–	–	–
157	A0	I/O	–	Q	Ext. Bus Address Bit 0
158	A1	I/O	–	Q	Ext. Bus Address Bit 1
159	A2	I/O	–	Q	Ext. Bus Address Bit 2
160	A3	I/O	–	Q	Ext. Bus Address Bit 3

Note: If pins $V_{DD}35$ (9, 21, 40, 112, 119, 137, 155) are connected to a 3.3 V supply the external bus interface (pins 1-40, 112-160) can be operated at 3.3 V levels.

Table 3-5. CY91F365GB/F366GB/F376G, CY91366GA I/O Pins and their Functions

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type (Flash Device)	Circuit Type (ROM Device)	Function
1	V_{DD}	–	–	–	–	–
2	V_{SS}	–	–	–	–	–
3	PJ4	I/O	PJ4	A	A	Digital I/O-Port
4	PJ5	I/O	PJ5	A	A	Digital I/O-Port
5	PJ6	I/O	PJ6	A	A	Digital I/O-Port
6	PJ7	I/O	PJ7	A	A	Digital I/O-Port
7	PI3	I/O	PI3	A	A	Digital I/O-Port
8	V_{DD}	–	–	–	–	–
9	V_{SS}	–	–	–	–	–
10	SGO	I/O	PM0	A	A	Sound Gen. SGO
11	SGA	I/O	PM1	A	A	Sound Gen. SGA
12	SDA	I/O	PM2	Y	Y	I^2C SDA (no internal pull-up)
13	SCL	I/O	PM3	Y	Y	I^2C SCL (no internal pull-up)

Table 3-5. CY91F365GB/F366GB/F376G, CY91366GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type (Flash Device)	Circuit Type (ROM Device)	Function
14	V_{DD}	–	–	–	–	–
15	V_{SS}	–	–	–	–	–
16	AVRH	–	–	R	R	Analog Ref. High
17	AV_{CC}	–	–	–	–	Analog V_{CC}
18	AV_{SS}	–	–	–	–	Analog Ref. Low/Analog V_{SS}
19	AN0	I/O	PH0	B	B	ADC Input
20	AN1	I/O	PH1	B	B	ADC Input
21	AN2	I/O	PH2	B	B	ADC Input
22	AN3	I/O	PH3	B	B	ADC Input
23	AN4	I/O	PH4	B	B	ADC Input
24	AN5	I/O	PH5	B	B	ADC Input
25	AN6	I/O	PH6	B	B	ADC Input
26	AN7	I/O	PH7	B	B	ADC Input
27	DA0	O	–	C	C	DAC Output (CY91F365GB)
	X0A	I	–	I	I	32 kHz Osc. Pin (CY91F366GB/366GA/ CY91F376G)
28	DA1	O	–	C	C	DAC Output (CY91F365GB)
	X1A	O	–	I	I	32 kHz Osc. Pin (CY91F366GB/366GA/ CY91F376G)
29	ALARM	I	–	D	D	Alarm Comparator Input
30	V_{SS}	–	–	–	–	–
31	BOOT	I/O	P93	A	A	BOOT Pin (see note)
32	TESTX	I	–	E	E	Test Mode Pin
33	CPUTESTX	I	–	E	E	Test Mode Pin
34	V_{DD}	–	–	–	–	–
35	X0	I	–	H	H	4 MHz Oscillator Pin
36	X1	O	–	H	H	4 MHz Oscillator Pin
37	V_{SS}	–	–	–	–	–
38	MONCLK	O	–	G	G	Clock Output
39	INT0	I/O	PK0	A	A	Ext. Interrupt
40	INT1	I/O	PK1	A	A	Ext. Interrupt
41	INT2	I/O	PK2	A	A	Ext. Interrupt
42	INT3	I/O	PK3	A	A	Ext. Interrupt
43	INT4	I/O	PK4	A	A	Ext. Interrupt
44	INT5	I/O	PK5	A	A	Ext. Interrupt
45	INT6	I/O	PK6	A	A	Ext. Interrupt
46	INT7	I/O	PK7	A	A	Ext. Interrupt
47	V_{DD}	–	–	–	–	Internal Power Supply Voltage pin
48	$V_{CC}3C$	–	–	–	–	Capacitor Pin for Internal Power Supply.

Table 3-5. CY91F365GB/F366GB/F376G, CY91366GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type (Flash Device)	Circuit Type (ROM Device)	Function
49	V_{SS}	–	–	–	–	–
50	IN0	I/O	PL0	A	A	ICU Input
51	IN1	I/O	PL1	A	A	ICU Input
52	IN2	I/O	PL2	A	A	ICU Input
53	IN3	I/O	PL3	A	A	ICU Input
54	OUT0	I/O	PL4	A	A	OCU Output
55	OUT1	I/O	PL5	A	A	OCU Output
56	V_{DD}	–	–	–	–	Internal Power Supply Voltage pin
57	MD0	I	–	T	F	Mode Pin
58	MD1	I	–	T	F	Mode Pin
59	MD2	I	–	T	F	Mode Pin
60	INITX	I	–	U	U	Initial Pin
61	V_{DD}	–	–	–	–	Internal Power Supply Voltage pin
62	V_{SS}	–	–	–	–	–
63	SOT4	I/O	PN0	A	A	SIO Output
64	SIN4	I/O	PN1	A	A	SIO Input
65	SCK4	I/O	PN2	A	A	SIO Clock
66	SIN3	I/O	PN3	A	A	SIO Input
67	SOT3	I/O	PN4	A	A	SIO Output
68	SCK3	I/O	PN5	A	A	SIO Clock
69	V_{SS}	–	–	–	–	–
70	OCPA0	I/O	PO0	A	A	PPG Output
71	OCPA1	I/O	PO1	A	A	PPG Output
72	OCPA2	I/O	PO2	A	A	PPG Output
73	OCPA3	I/O	PO3	A	A	PPG Output
74	OCPA4	I/O	PO4	A	A	PPG Output
75	OCPA5	I/O	PO5	A	A	PPG Output
76	OCPA6	I/O	PO6	A	A	PPG Output
77	OCPA7	I/O	PO7	A	A	PPG Output
78	TX0	I/O	PP0	Q	Q	CAN TX Output
79	RX0	I/O	PP1	Q	Q	CAN RX Output
80	TX1	I/O	PP2	Q	Q	CAN TX Output
81	RX1	I/O	PP3	Q	Q	CAN RX Output
82	V_{DD}	–	–	–	–	–
83	V_{SS}	–	–	–	–	–
84	SIN0	I/O	PQ0	A	A	UART Input
85	SOT0	I/O	PQ1	A	A	UART Output
86	SIN1	I/O	PQ2	A	A	UART Input

Table 3-5. CY91F365GB/F366GB/F376G, CY91366GA I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type (Flash Device)	Circuit Type (ROM Device)	Function
87	SOT1	I/O	PQ3	A	A	UART Output
88	PG0	I/O	PG0	A	A	Digital I/O-Port
89	PG1	I/O	PG1	A	A	Digital I/O-Port
90	PG2	I/O	PG2	A	A	Digital I/O-Port
91	PG3	I/O	PG3	A	A	Digital I/O-Port
92	PG4	I/O	PG4	A	A	Digital I/O-Port
93	PG5	I/O	PG5	A	A	Digital I/O-Port
94	V_{DD}	–	–	–	–	–
95	HV_{SS}	–	–	–	–	SMC V_{SS}
96	PWM1P0	I/O	PR0	K	K	SMC 0
97	PWM1M0	I/O	PR1	K	K	SMC 0
98	PWM2P0	I/O	PR2	K	K	SMC 0
99	PWM2M0	I/O	PR3	M	M	SMC 0
100	HVDD	–	–	–	–	SMC V_{DD}
101	PWM1P1	I/O	PR4	K	K	SMC 1
102	PWM1M1	I/O	PR5	K	K	SMC 1
103	PWM2P1	I/O	PR6	K	K	SMC 1
104	PWM2M1	I/O	PR7	M	M	SMC 1
105	HV_{SS}	–	–	–	–	SMC V_{SS}
106	PWM1P2	I/O	PS0	K	K	SMC 2
107	PWM1M2	I/O	PS1	K	K	SMC 2
108	PWM2P2	I/O	PS2	K	K	SMC 2
109	PWM2M2	I/O	PS3	M	M	SMC 2
110	HV_{DD}	–	–	–	–	SMC V_{DD}
111	PWM1P3	I/O	PS4	K	K	SMC 3
112	PWM1M3	I/O	PS5	K	K	SMC 3
113	PWM2P3	I/O	PS6	K	K	SMC 3
114	PWM2M3	I/O	PS7	M	M	SMC 3
115	HV_{SS}	–	–	–	–	–
116	V_{DD}	–	–	–	–	–
117	PJ0	I/O	PJ0	A	A	Digital I/O-Port
118	PJ1	I/O	PJ1	A	A	Digital I/O-Port
119	PJ2	I/O	PJ2	A	A	Digital I/O-Port
120	PJ3	I/O	PJ3	A	A	Digital I/O-Port

Note: Pin 31 (BOOT) should be low by default (pull down resistor). To avoid disturbances in case of reset/boot, it should preferably only be used as output by any application.

Table 3-6. CY91F367GB/F368GB I/O Pins and their Functions

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
1	V_{DD}	–	–	–	–
2	V_{SS}	–	–	–	–
3	PJ4	I/O	PJ4	A	Digital I/O-Port
4	PJ5	I/O	PJ5	A	Digital I/O-Port
5	PJ6	I/O	PJ6	A	Digital I/O-Port
6	PJ7	I/O	PJ7	A	Digital I/O-Port
7	PI3	I/O	PI3	A	Digital I/O-Port
8	V_{DD}	–	–	–	–
9	V_{SS}	–	–	–	–
10	PM0	I/O	PM0	A	Digital I/O-Port
11	PM1	I/O	PM1	A	Digital I/O-Port
12	SDA	I/O	PM2	Y	I^2C SDA (no internal pull-up)
13	SCL	I/O	PM3	Y	I^2C SCL (no internal pull-up)
14	V_{DD}	–	–	–	–
15	V_{SS}	–	–	–	–
16	AVRH	–	–	R	Analog Ref. High
17	AV_{CC}	–	–	–	Analog V_{CC}
18	AV_{SS}	–	–	–	Analog Ref. Low/Analog V_{SS}
19	AN0	I/O	PH0	B	ADC Input
20	AN1	I/O	PH1	B	ADC Input
21	AN2	I/O	PH2	B	ADC Input
22	AN3	I/O	PH3	B	ADC Input
23	AN4	I/O	PH4	B	ADC Input
24	AN5	I/O	PH5	B	ADC Input
25	AN6	I/O	PH6	B	ADC Input
26	AN7	I/O	PH7	B	ADC Input
27	X0A	I	–	I	32 kHz Oscillator Pin (CY91F368GB)
	N.C.	–	–	–	Not Connected (CY91F367GB)
28	X1A	O	–	I	32 kHz Oscillator Pin (CY91F368GB)
	N.C.	–	–	–	Not Connected (CY91F367GB)
29	ALARM	I	–	D	Alarm Comparator Input
30	V_{SS}	–	–	–	–
31	BOOT	I/O	P93	A	BOOT Pin [a]
32	TESTX	I	–	E	Test mode pin
33	CPUTESTX	I	–	E	Test mode pin
34	V_{DD}	–	–	–	–
35	X0	I	–	H	4 MHz Oscillator Pin

Table 3-6. CY91F367GB/F368GB I/O Pins and their Functions *(continued)*

Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
36	X1	O	–	H	4 MHz Oscillator Pin
37	V_{SS}	–	–	–	–
38	MONCLK	O	–	G	Clock output
39	INT0	I/O	PK0	A	Ext. Interrupt
40	INT1	I/O	PK1	A	Ext. Interrupt
41	INT2	I/O	PK2	A	Ext. Interrupt
42	INT3	I/O	PK3	A	Ext. Interrupt
43	INT4	I/O	PK4	A	Ext. Interrupt
44	INT5	I/O	PK5	A	Ext. Interrupt
45	INT6	I/O	PK6	A	Ext. Interrupt
46	INT7	I/O	PK7	A	Ext. Interrupt
47	V_{DD}	–	–	–	Internal Power Supply Voltage pin
48	V_{CC}3C	–	–	–	Capacitor Pin for Internal Power Supply
49	V_{SS}	–	–	–	–
50	IN0	I/O	PL0	A	ICU Input
51	IN1	I/O	PL1	A	ICU Input
52	IN2	I/O	PL2	A	ICU Input
53	IN3	I/O	PL3	A	ICU Input
54	OUT0	I/O	PL4	A	OCU Output
55	OUT1	I/O	PL5	A	OCU Output
56	V_{DD}	–	–	–	Internal Power Supply Voltage pin
57	MD0	I	–	T	Mode Pin
58	MD1	I	–	T	Mode Pin
59	MD2	I	–	T	Mode Pin
60	INITX	I	–	U	Initial Pin
61	V_{DD}	–	–	–	Internal Power Supply Voltage pin
62	V_{SS}	–	–	–	–
63	SOT4	I/O	PN0	A	SIO Output
64	SIN4	I/O	PN1	A	SIO Input
65	SCK4	I/O	PN2	A	SIO Clock
66	SIN3	I/O	PN3	A	SIO Input
67	SOT3	I/O	PN4	A	SIO Output
68	SCK3	I/O	PN5	A	SIO Clock
69	V_{SS}	–	–	–	–
70	OCPA0	I/O	PO0	A	PPG Output
71	OCPA1	I/O	PO1	A	PPG Output
72	OCPA2	I/O	PO2	A	PPG Output
73	OCPA3	I/O	PO3	A	PPG Output

Table 3-6. CY91F367GB/F368GB I/O Pins and their Functions *(continued)*

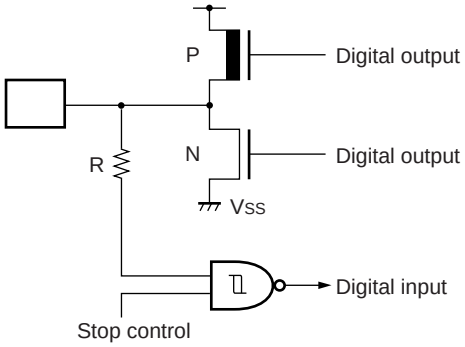
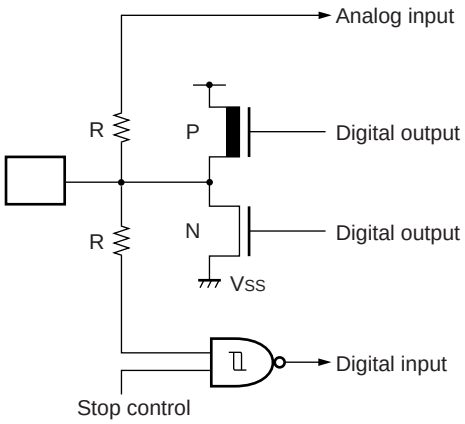
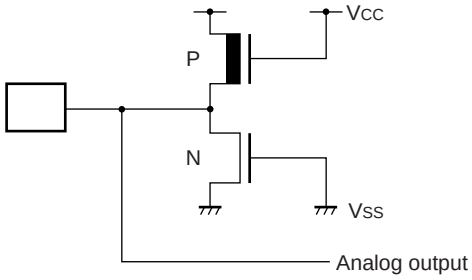
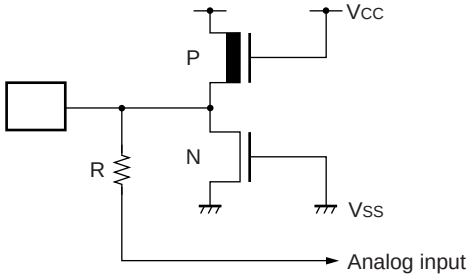
Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
74	PO4	I/O	PO4	A	Digital I/O-Port
75	PO5	I/O	PO5	A	Digital I/O-Port
76	PO6	I/O	PO6	A	Digital I/O-Port
77	PO7	I/O	PO7	A	Digital I/O-Port
78	TX0	I/O	PP0	Q	CAN TX Output
79	RX0	I/O	PP1	Q	CAN RX Output
80	TX1	I/O	PP2	Q	CAN TX Output
81	RX1	I/O	PP3	Q	CAN RX Output
82	V_{DD}	–	–	–	–
83	V_{SS}	–	–	–	–
84	SIN0	I/O	PQ0	A	UART Input
85	SOT0	I/O	PQ1	A	UART Output
86	PQ2	I/O	PQ2	A	Digital I/O-Port
87	PQ3	I/O	PQ3	A	Digital I/O-Port
88	PG0	I/O	PG0	A	Digital I/O-Port
89	PG1	I/O	PG1	A	Digital I/O-Port
90	PG2	I/O	PG2	A	Digital I/O-Port
91	PG3	I/O	PG3	A	Digital I/O-Port
92	PG4	I/O	PG4	A	Digital I/O-Port
93	PG5	I/O	PG5	A	Digital I/O-Port
94	V_{DD}	–	–	–	–
95	V_{SS}	–	–	–	–
96	PR0	I/O	PR0	K	Digital I/O-Port
97	PR1	I/O	PR1	K	Digital I/O-Port
98	PR2	I/O	PR2	K	Digital I/O-Port
99	PR3	I/O	PR3	M	Digital I/O-Port
100	HV_{DD}	–	–	–	V_{DD} for Ports R and S
101	PR4	I/O	PR4	K	Digital I/O-Port
102	PR5	I/O	PR5	K	Digital I/O-Port
103	PR6	I/O	PR6	K	Digital I/O-Port
104	PR7	I/O	PR7	M	Digital I/O-Port
105	V_{SS}	–	–	–	–
106	PS0	I/O	PS0	K	Digital I/O-Port
107	PS1	I/O	PS1	K	Digital I/O-Port
108	PS2	I/O	PS2	K	Digital I/O-Port
109	PS3	I/O	PS3	M	Digital I/O-Port
110	HV_{DD}	–	–	–	V_{DD} for Ports R and S
111	PS4	I/O	PS4	K	Digital I/O-Port

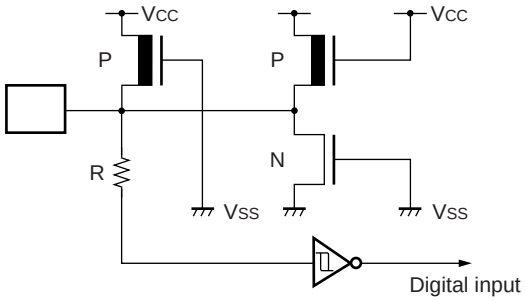
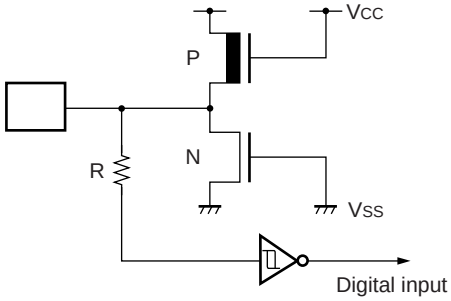
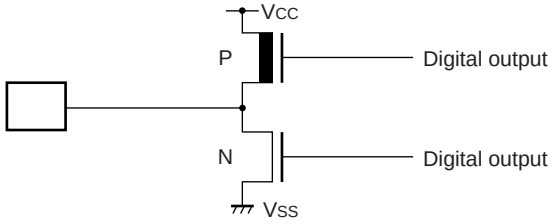
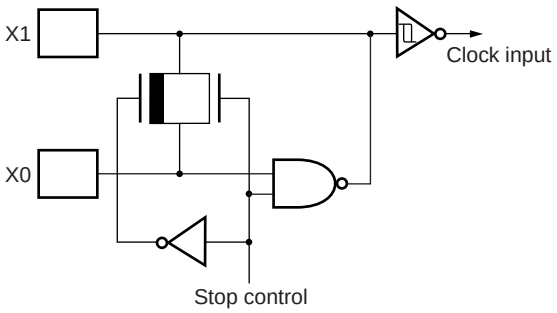
Table 3-6. CY91F367GB/F368GB I/O Pins and their Functions *(continued)*

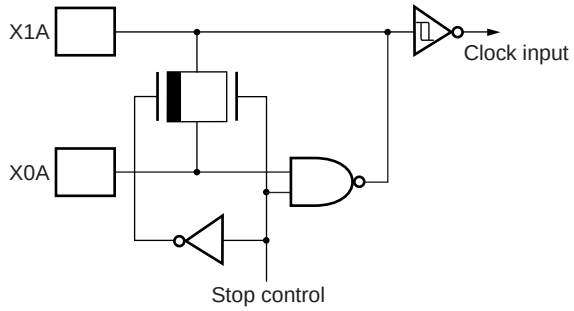
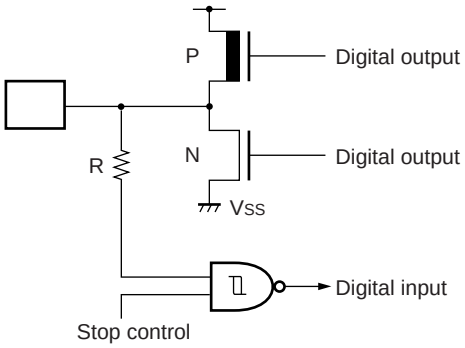
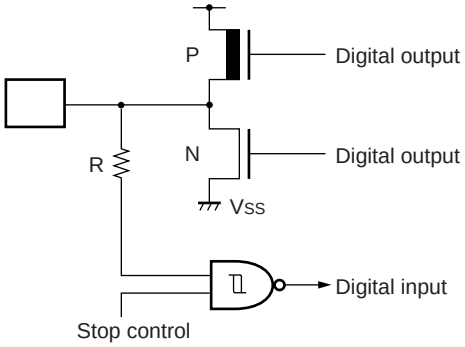
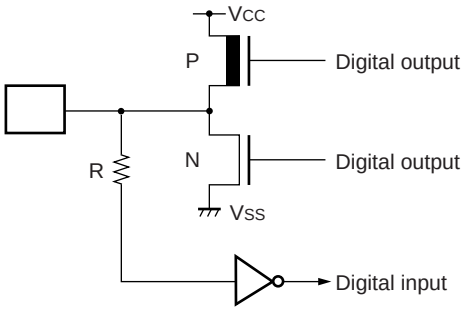
Pin No.	Pin Name	I/O	General Purpose I/O Port	Circuit Type	Function
112	PS5	I/O	PS5	K	Digital I/O-Port
113	PS6	I/O	PS6	K	Digital I/O-Port
114	PS7	I/O	PS7	M	Digital I/O-Port
115	V_{SS}	–	–	–	–
116	V_{DD}	–	–	–	–
117	PJ0	I/O	PJ0	A	Digital I/O-Port
118	PJ1	I/O	PJ1	A	Digital I/O-Port
119	PJ2	I/O	PJ2	A	Digital I/O-Port
120	PJ3	I/O	PJ3	A	Digital I/O-Port

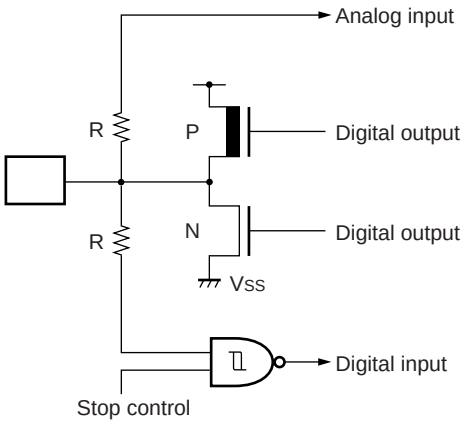
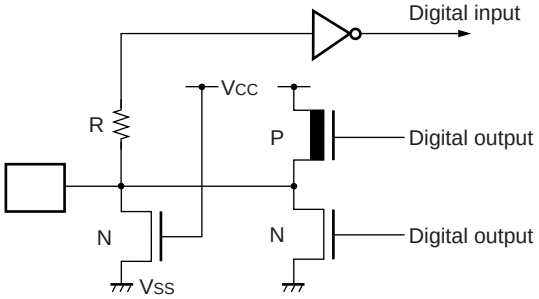
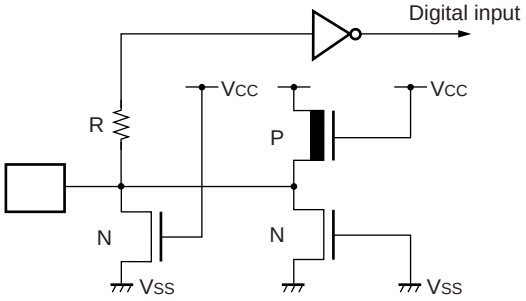
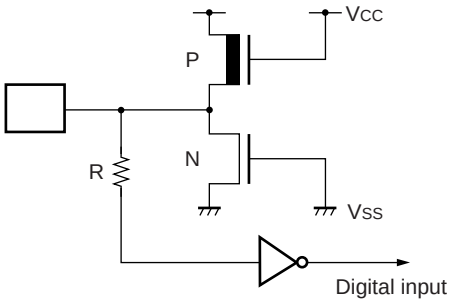
a. Pin 31 (BOOT) should be low by default (pull down resistor). To avoid disturbances in case of reset/boot, it should preferably only be used as output by any application.

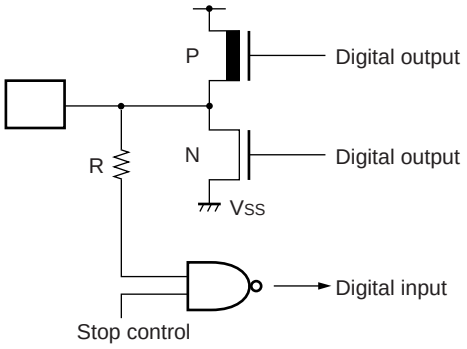
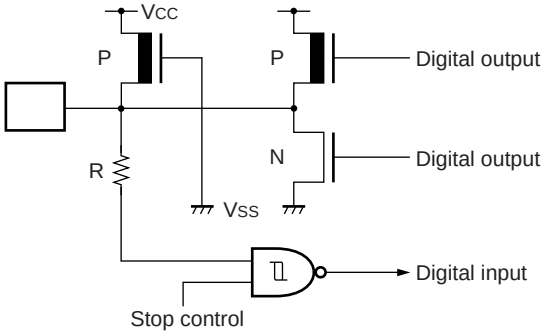
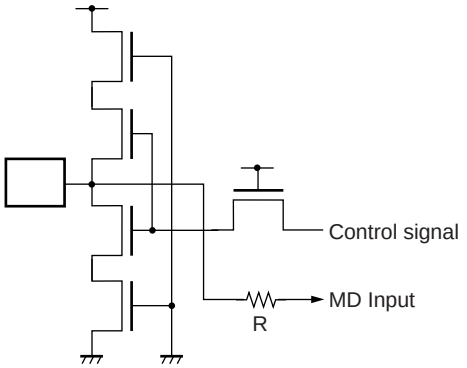
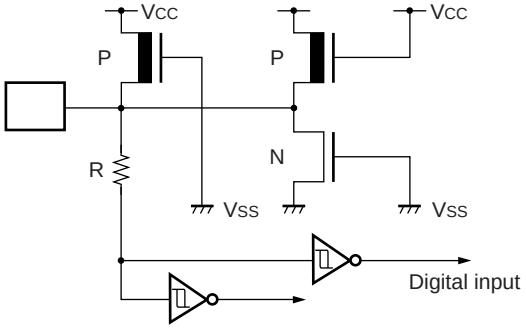
4. I/O Circuit Type

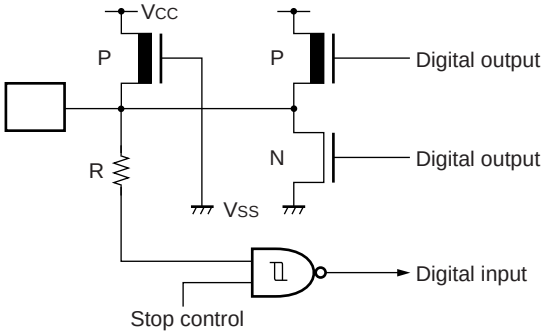
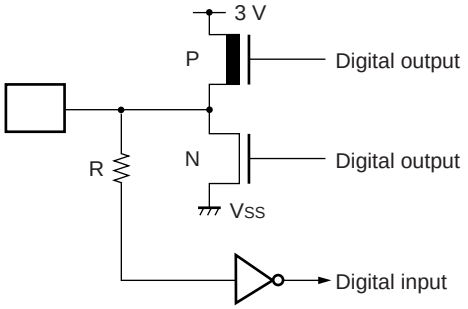
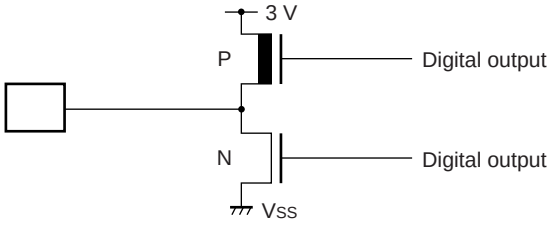
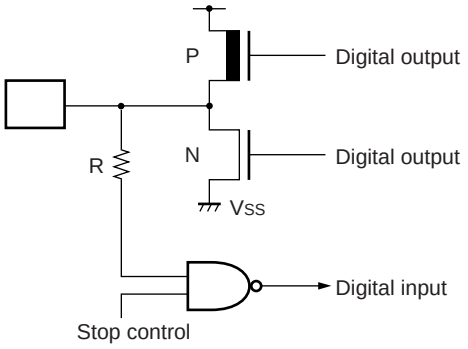
Type	Circuit Type	Remarks
A		■ CMOS Automotive level Schmitt-Trigger Input ■ STOP control ■ I_{OH} = 4 mA, I_{OL} = 4 mA
B		■ CMOS Automotive level Schmitt-Trigger Input ■ Analog Input ■ STOP control ■ I_{OH} = 4 mA, I_{OL} = 4 mA
C		■ Analog output
D		■ Analog Input

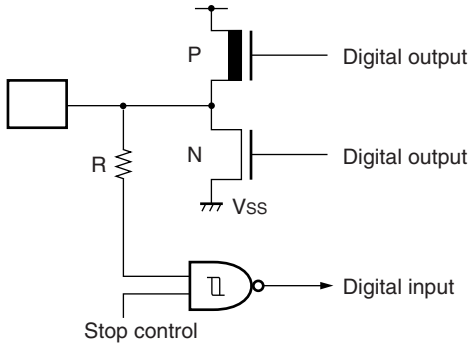
Type	Circuit Type	Remarks
E		■ CMOS Schmitt-Trigger Input ■ Pullup Resistor: 50 kΩ
F		■ CMOS Schmitt-Trigger Input
G		■ Tristate Output ■ I_{OH} = 4 mA, I_{OL} = 4 mA
H		■ 4 MHz Oscillator Pin

Type	Circuit Type	Remarks
I		■ 32 kHz Oscillator Pin
J		■ CMOS Automotive level Schmitt-Trigger Input ■ STOP control (LED) ■ I_{OH} = 14 mA, I_{OL} = 24 mA
K		■ CMOS Automotive level Schmitt-Trigger Input ■ STOP control (SMC) ■ I_{OH} = 30 mA, I_{OL} = 30 mA ■ Typ slew rate of 40 ns
L		■ CMOS Input ■ 5 V or 3 V input ■ I_{OH} = 4 mA, I_{OL} = 4 mA

Type	Circuit Type	Remarks
M		■ CMOS Automotive level Schmitt-Trigger Input ■ Analog Input ■ STOP control (SMC) ■ I_{OH} = 30 mA, I_{OL} = 30 mA ■ Typ slew rate of 40 ns
N		■ CMOS Input ■ Pulldown Resistor: 50 kΩ ■ 5 V or 3 V input ■ I_{OH} = 4 mA, I_{OL} = 4 mA
O		■ CMOS Input ■ Pulldown Resistor: 50 kΩ ■ 5 V or 3 V input
P		■ CMOS Input ■ 3 V input

Type	Circuit Type	Remarks
Q/Q1		■ Q: CMOS Input, STOP control, I_{OH} = 4 mA, I_{OL} = 4 mA ■ Q1: CMOS Input, STOP control, I_{OH} = 8 mA, I_{OL} = 8 mA
S		■ CMOS Schmitt-Trigger Input ■ STOP control ■ Pullup Resistor: 10 kΩ ■ I_{OH} = 4 mA, I_{OL} = 4 mA
T		■ CMOS Input ■ Can withstand high V_{ID} for flash programming
U		■ CMOS Schmitt-Trigger Input ■ Pullup Resistor to the core: 50 kΩ ■ 3 V and 5 V input

Type	Circuit Type	Remarks
V		■ CMOS Schmitt-Trigger Input ■ STOP control ■ Pullup Resistor: 50 kΩ ■ I_{OH} = 4 mA, I_{OL} = 4 mA
W		■ CMOS Input ■ 3 V input
X		■ Tristate Output, 3 V
Y		■ CMOS Input in I²C mode operating as open drain outputs ■ STOP control ■ I_{OH} = 3 mA, I_{OL} = 3 mA

Type	Circuit Type	Remarks
YA		■ I/O in I²C mode operating as open drain outputs ■ CMOS Schmitt-Trigger Input ■ STOP control ■ I_{OH} = 3 mA, I_{OL} = 3 mA

Note: Symbols used in circuit types (Common to all circuit diagrams)
P: P channel transistor
N: N channel transistor
R: Diffusion resistor

Circuit Type	Description
A	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Automotive Schmitt-Trigger Input, STOP control
B	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control
C	Analog Output
D	Analog Input
E	CMOS Schmitt-Trigger Input, Pull-up Resistor: 50 kΩ,
F	CMOS Schmitt-Trigger Input
G	Tristate Output, I_{OH} = 4 mA / I_{OL} = 4 mA
H	4 MHz Oscillator Pin
I	32 kHz Oscillator pin
J	I/O, I_{OH} = 14 mA / I_{OL} = 24 mA, CMOS Automotive Schmitt-Trigger Input, STOP control (LED)
K	I/O, I_{OH} = 30 mA / I_{OL} = 30 mA, CMOS Automotive Schmitt-Trigger Input, STOP control, slew rate improved for EMC (SMC)
L	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Input: 5 V or 3 V input
M	I/O, I_{OH} = 30 mA / I_{OL} = 30 mA, CMOS Automotive Schmitt-Trigger Input, Analog Input, STOP control, slew rate improved for EMC (SMC)
N	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Input: 5 V or 3 V input, Pulldown Resistor: 50 kΩ
O	CMOS Input: 5 V or 3 V input, Pulldown Resistor: 50 kΩ
P	CMOS Input: 3 V input
Q	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Input, STOP control
Q1	I/O, I_{OH} = 8 mA / I_{OL} = 8 mA, CMOS Input, STOP control
R	AVRL / AVRH Input
S	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Input, STOP control, Pull-up Resistor: 10 kΩ,
T	CMOS Input, can withstand V_{ID} for flash programming
U	CMOS Schmitt-Trigger Input, Pull-up Resistor: 50 kΩ, 3.3 V and 5 V inputs to core
W	I/O, I_{OH} = 4 mA / I_{OL} = 4 mA, CMOS Input: 3 V input
X	Tristate Output, I_{OH} = 4 mA / I_{OL} = 4 mA, 3 V
Y	I/O, I_{OH} = 3 mA / I_{OL} = 3 mA (I^2C), CMOS Input, STOP control
YA	I/O, I_{OH} = 3 mA / I_{OL} = 3 mA (I^2C), CMOS Schmitt-Trigger Input, STOP control

5. Handling Devices

5.1 Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage greater than V_{DD} or less than V_{SS} is applied to an input or output pin or if the voltage applied between V_{DD} and V_{SS} exceeds the rating. If latch-up occurs, the power supply current increases rapidly resulting in thermal damage to circuit elements. Therefore, ensure that maximum ratings are not exceeded in circuit operation.

5.2 Connecting Unused Pins

Leaving unused input pins open may result in misbehavior or latch up and possible permanent damage of the device. Therefore they must be tied to V_{DD} or V_{SS} through resistors. In this case those resistors should be more than 2 kΩ.

Unused bidirectional pins should be set to the output state and can be left open, or the input state with the above described connection.

The resistor of more than 2 kΩ is used to limit currents through the protection diodes. In case of voltages at the not used pin of 0.3 V or more below V_{SS} or 0.3 V or more above V_{DD} currents which could cause latch-up will flow through those diodes.

5.3 External Reset Input

When inputting an “L” level to the INITX pin, hold this low level at the INITX pin long enough so that after release of the low level at INITX and the passing of the built in waiting time stable oscillation of the oscillation circuit is achieved. INITX must be pulled low for at least 8 cycles of the 4 MHz oscillation clock.

5.4 Power Supply Pins

All V_{DD} pins should be connected to the same potential (exception can be the external bus interface on F362GB and F369GA). The analogue supply voltage (AV_{CC}) must not be turned on before the digital supply voltage. If the external bus interface is supplied with 3.3 V this voltage also must not be turned on before the 5 V digital voltage has been switched on. If the supply voltage to the external bus interface is switched off (it may not be tristate but should be pulled low) it must be made sure that all related signals do not have a voltage higher than this pulled down supply.

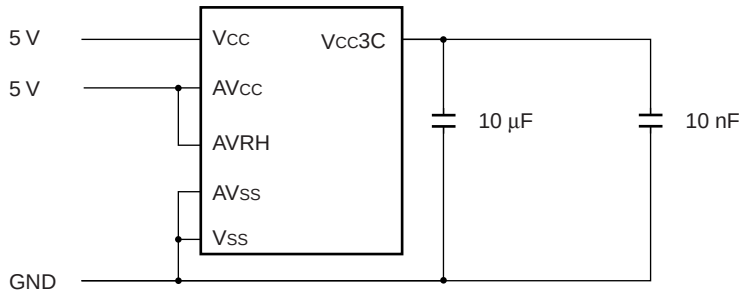
When multiple V_{DD} and V_{SS} pins are provided, be sure to connect all V_{DD} and V_{SS} pins to the power supply or ground externally. Although pins at the same potential are connected together in the internal device design so as to prevent malfunctions such as latch-up, connecting all V_{DD} and V_{SS} pins appropriately minimizes unwanted radiation, prevents malfunction of strobe signals due to increases in the ground level, and keeps the overall output current rating.

Also, take care to connect V_{DD} and V_{SS} to current source in the lowest possible impedance.

Connection of a ceramic bypass capacitor of approximately 0.1 µF between V_{DD} and V_{SS} close to the device is recommended.

The CY91360G series contains a regulator. To use the device with the 5-V power supply, supply 5-V power to the V_{CC} pins and be sure to connect a bypass capacitor of 10 µF parallel to 10 nF to the V_{CC}3C pin for the regulator.

[Use with 5-V power supply]



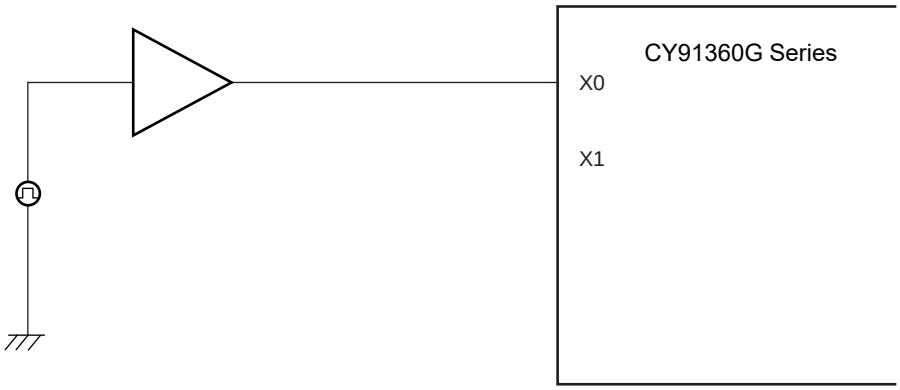
5.5 Crystal Oscillator Circuit

Noise in the vicinity of the X0 and X1 pins can be a cause of device malfunction. Design the circuit board so that X0, X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

A printed circuit board design that surrounds the X0 and X1 pins with ground provides for stable operation and is strongly recommended.

5.6 Using an External Clock

To use an external clock, drive X0 pin only and leave X1 pin open.
Below is a diagram of how to use external clock.



5.7 Mode Pins

Connect the mode pins (MD0 to MD2) directly to V_{DD} or V_{SS}.

To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pins to V_{DD} or V_{SS} and to provide a low-impedance connection.

5.8 Turning the Power Supply on

Immediately after power on always execute INIT at the INITX pin (start with a low level at the INITX pin). Hold this low level at the INITX pin long enough so that after release of the low level at INITX and the passing of the built in waiting time stable oscillation of the oscillation circuit is achieved. INITX must be pulled low for at least 8 cycles of the 4 MHz oscillation clock.

The analogue supply voltage (AV_{CC}) must not be turned on before the digital supply voltage. If the external bus interface is supplied with 3.3 V this voltage also must not be turned on before the 5 V digital voltage has been switched on.

5.9 A State in Turning Power on

As long as the minimum operating voltage has not been reached during power-on the output pin levels are not guaranteed.

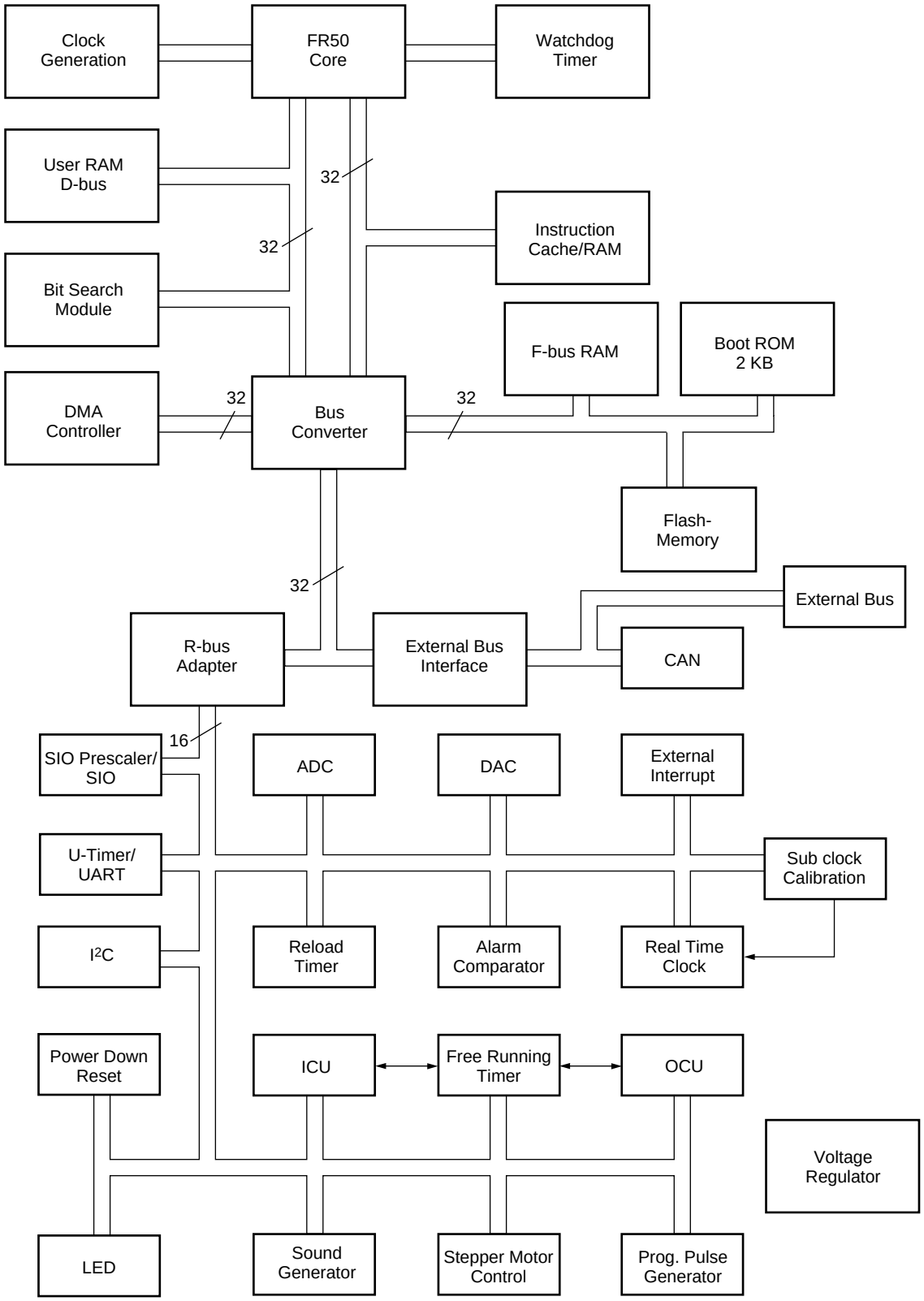
5.10 Note on During Operation of PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempts to be working with the self-frequency of the self-oscillating circuit within the PLL even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

5.11 The Function of the Watchdog Timer

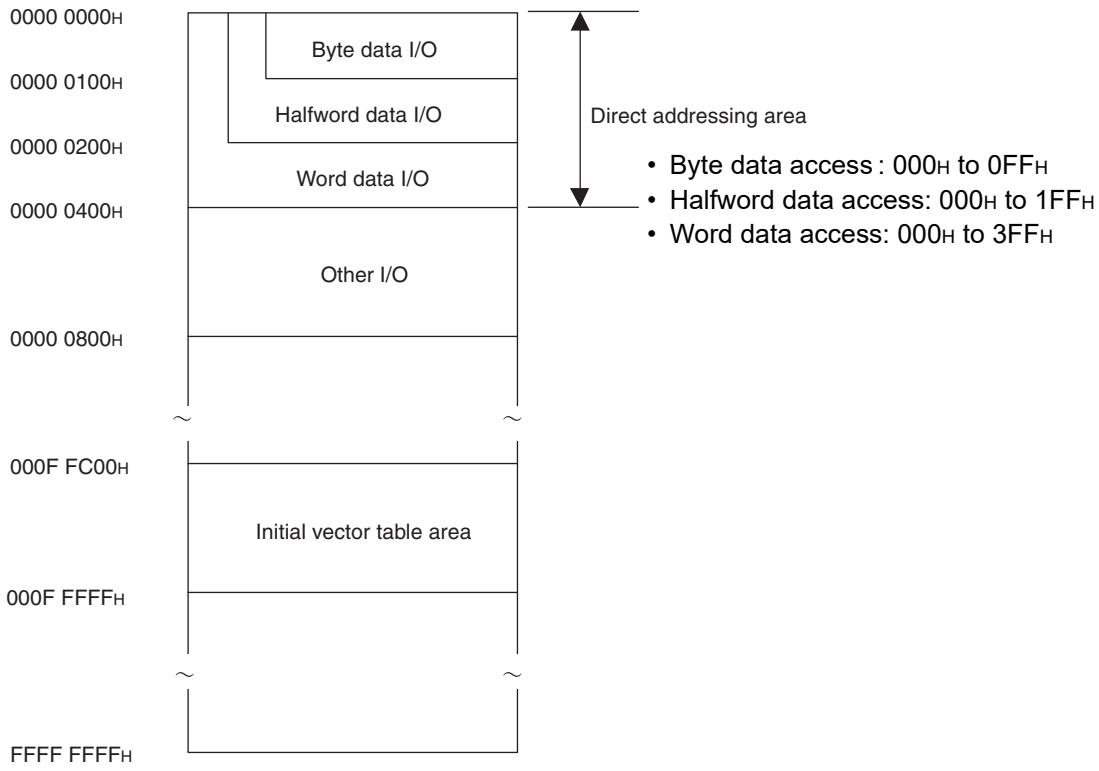
The watchdog timer in this model has the functions watching that the program performs the delay of reset within a fixed period and resetting the CPU when the delay of reset is not performed because of the program malfunction.
Therefore, once the function of the watchdog timer is enabled, the watchdog timer keeps on operating until the reset operation.
As an exceptional processing, the watchdog timer performs the delay of reset automatically under the condition in which the CPU program operation is stopped. Please refer to the explanation item of the function of the watchdog timer about the exceptional condition.
By the way, if above condition will be issued by the system program or hardware malfunction, a watchdog reset may be not performed. In this case please perform the reset operation (INIT) by using the external INITX pin.

6. Block Diagram



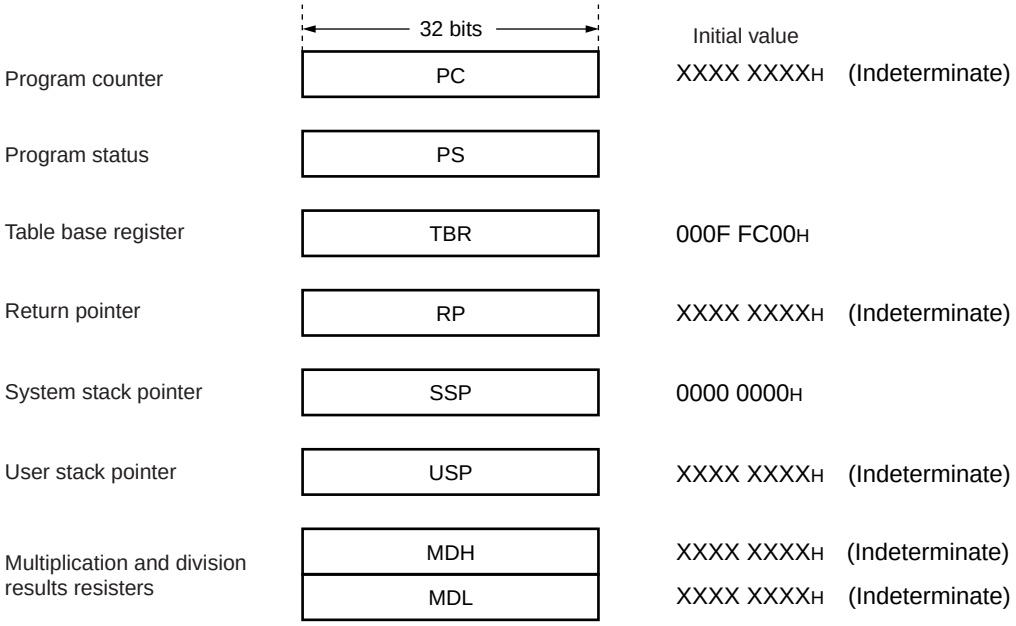
7. CPU Core

7.1 Memory Space

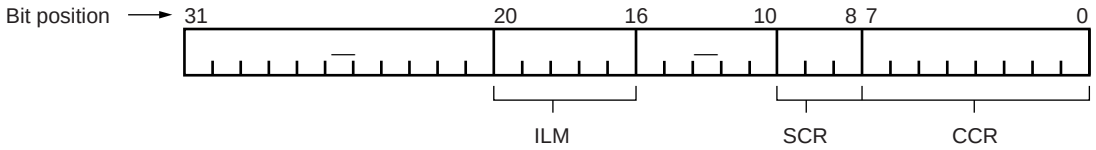


7.2 Dedicated Registers

Each of the dedicated registers is used for a particular purpose. The dedicated registers consist of the program counter (PC), program status (PS), table base register (TBR), return pointer (RP), system stack pointer (SSP), user stack pointer (USP), and multiplication and division result registers (MDH/MDL).

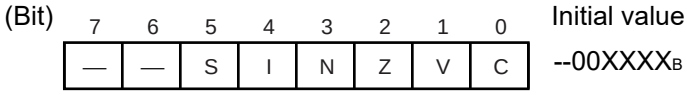


7.2.1 Program Status (PS)



CCR: Condition Code Register
SCR: System Condition Code Register
ILM: Interrupt Level Mask

7.2.2 Condition Code Register (CCR)



7.2.3 System Condition Code Register (SCR)

(Bit)	10	9	8	Initial value
	D1	D0	T	XX0B

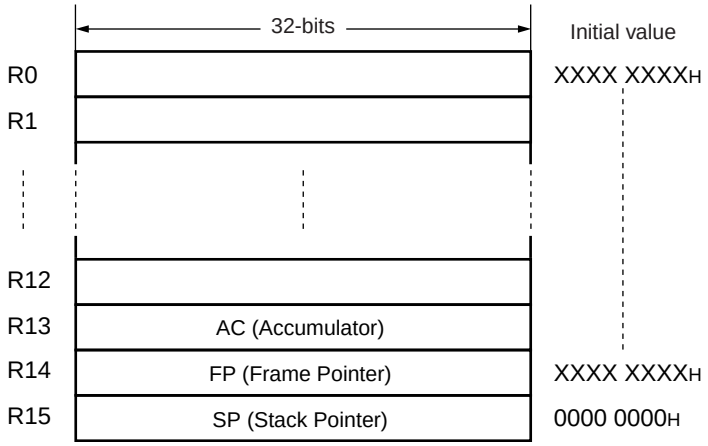
7.2.4 Interrupt Level Mask Register (ILM)

(Bit)	20	19	18	17	16	Initial value
	ILM4	ILM3	ILM2	ILM1	ILM0	01111B

7.3 General-Purpose Registers

The general-purpose registers are CPU registers R0 to R15. The register are used as the accumulator for operations and as pointers (a field indicating an address) for memory access. The user can specify the purpose for which the general-purpose registers are used.

Register Bank Structure



Among 16 general-purpose registers, the following registers assume a special purpose. This enhances some instructions.

R13 : Virtual accumulator (AC)
R14 : Frame pointer (FP)
R15 : Stack pointer (SP)

The initial value of R0 to R14 after a reset is indeterminate. The initial value of R15 is 00000000H (SSP value).

8. Mode Setting

The FR50 of devices uses mode pins (MD2 to MD0) and a mode register (MODR) to set the operation mode.

8.1 Mode Pins

Three mode pins (MD2 to MD0) are used to specify the reset mode vector access area.

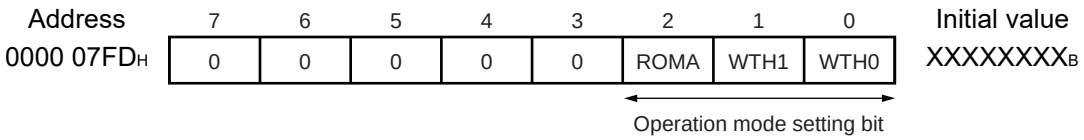
Mode Pins			Mode Name	Reset Vector Access Area	Remarks
MD2	MD1	MD0			
0	0	0	Internal ROM mode vector	Internal	
0	0	1	External ROM mode vector	External	The mode register is used to set the bus width.
remaining settings			–	–	Reserved

8.2 Mode Register (MODR)

The data to be written to 0000 07FD$_H$ using mode vector fetch is called mode data.

MODR is located at 0000 07FD$_H$. After an operation mode has been set in MODR, the device operates in this operation mode. MODR is set only when a reset factor (INIT level) occurs. User programs cannot write data to MODR.

< Mode Register (MODR) >



[Bits 7 to 3]: (Reserved bits)

Always set 00000 at bits 7 to 3. Operation is not guaranteed when other values are set.

[Bit 2]: ROMA (internal ROM enable bit)

The ROMA bit is used to set whether to validate the internal ROM area (F-bus memory area).

ROMA	Function	Remarks
0	External ROM mode	Access to the F-bus area is external.
1	Internal ROM mode	

[Bits 1 and 0]: WTH1 and WTH0 (bus width/single chip mode specifying bits)

The WTH1 and WTH0 bits are used to set the bus width (valid when operation mode is external bus mode) and the single chip mode. When the operation mode is the external bus mode, this value is set at the BW1 and BW0 bits of AMD0 (CS0 area).

WTH1	WTH0	Function	Remarks
0	0	8-bit bus width	External bus mode
0	1	16-bit bus width	External bus mode
1	0	32-bit bus width	External bus mode
1	1	Single chip mode	

8.3 Fixed Vector

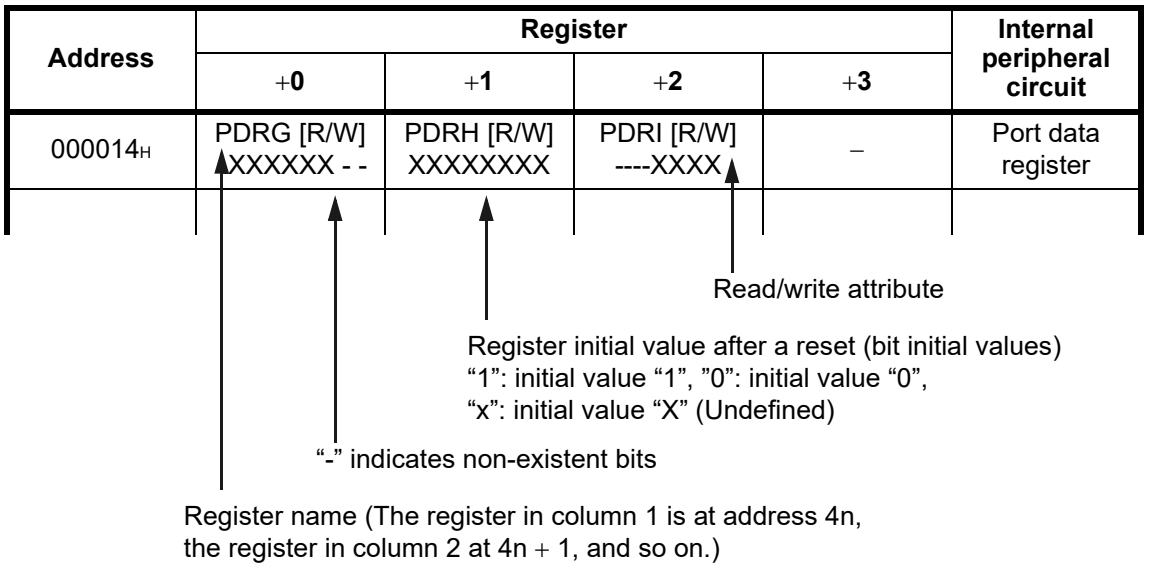
If CY91360 series devices are started in mode MD[2:0] = 000, the internal fixed mode vector (FMV = 0x06) and the fixed reset vector are used. The fixed reset vector points to the start address of the internal Boot ROM.

This enables access to the F-bus area, to the internal CAN modules and the internal flash memory.

See also section Boot ROM.

9. I/O Map

9.1 How to Read the I/O Map



Address of far left of register (+0), +1, +2, and +3 each increment the address by one. When performing word access, the register in column 1 is placed at the MSB end of the data.

Note: Do not use RMW instructions on registers containing write-only (W) bits.
RMW instructions (RMW: read-modify-write):

AND	Rj, @Ri	OR	Rj, @Ri	EOR	Rj, @Ri
ANDH	Rj, @Ri	ORH	Rj, @Ri	EORH	Rj, @Ri
ANDB	Rj, @Ri	ORB	Rj, @Ri	EORB	Rj, @Ri
BANDL	#u4, @Ri	BORL	#u4, @Ri	BEORL	#u4, @Ri
BANDH	#u4, @Ri	BORH	#u4, @Ri	BEORH	#u4, @Ri

The data in reserved areas and areas marked “–” is indeterminate.
Do not use those areas.

Address	Register				Block
	+0	+1	+2	+3	
000000H	Reserved	Reserved	Reserved	Reserved	T-unit Port Data Register
000004H	Reserved	Reserved	Reserved	PDR7 [R/W] 1111XXXX	
000008H	PDR8 [R/W] XXXXXXXX	PDR9 [R/W] XXXXXXX1	–	PDRB [R/W] XXXXXXXX	
00000CH	–				
000010H	PDRG [R/W] XXXXXXXX	PDRH [R/W] XXXXXXXX	PDRI [R/W] X - - - X - - -	PDRJ [R/W] XXXXXXXX	R-bus Port Data Register
000014H	PDRK [R/W] XXXXXXXX	PDRL [R/W] XXXXXXXX	PDRM [R/W] - - - - XXXX	PDRN [R/W] - - XXXXXX	
000018H	PDRO [R/W] XXXXXXXX	PDRP [R/W] XXXXXXXX	PDRQ [R/W] - - XXXXXX	PDRR [R/W] XXXXXXXX	
00001CH	PDRS [R/W] XXXXXXXX	–	–	–	

Address	Register				Block
	+0	+1	+2	+3	
000020H to 00003CH	–				Reserved
000040H	EIRR [R/W] 00000000	ENIR [R/W] 00000000	ELVR [R/W] 00000000 00000000		Ext int/NMI
000044H	DICR [R/W] - - - - - - - 0	HRCL [R/W, R] 0 - - 11111	CLKR2 [R/W] - - - - - 000	reserved	DLYI/I-unit RTC
000048H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
00004CH	–		TMCSR0 [R/W] - - - - 0000 - - - 00000		
000050H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
000054H	–		TMCSR1 [R/W] - - - - 0000 - - - 00000		
000058H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2
00005CH	–		TMCSR2 [R/W] - - - - 0000 - - - 00000		
000060H	SSR0 [R/W] 00001 - 00	SIDR0 [R/W] XXXXXXXX	SCR0 [R/W, W] 00000100	SMR0 [R/W, W] 00 - - 0 - 00	UART0
000064H	ULS0 [R/W] - - - - 0000	–	–	–	
000068H	UTIM0/UTIMR0 [R/W] 00000000 00000000		DRCL0 [W] - - - - - - - -	UTIMC0 [R/W] 0 - - - 0001	U-TIMER 0
00006CH	SSR1 [R/W, R] 00001 - 00	SIDR1 [R/W] XXXXXXXX	SCR1 [R/W, W] 00000100	SMR1 [R/W, W] 00 - - 0 - 00	UART1
000070H	ULS1 [R/W] - - - - 0000	–	–	–	
000074H	UTIM1/UTIMR1 [R/W] 00000000 00000000		DRCL1 [W] - - - - - - - -	UTIMC1 [R/W] 0 - - - 0001	U-TIMER 1
000078H	SSR2 [R/W, R] 00001 - 00	SIDR2 [R/W] XXXXXXXX	SCR2 [R/W, W] 00000100	SMR2 [R/W, W] 00 - - 0 - 00	UART2
00007CH	ULS2 [R/W] - - - - 0000	–	–	–	
000080H	UTIM2/UTIMR2 [R/W] 00000000 00000000		DRCL2 [W] - - - - - - - -	UTIMC2 [R/W] 0 - - - 0001	U-TIMER2
000084H	SMCS0 [R/W, R] 00000010 - - - - 00-0		SES0 [R/W] - - - - - - 00	SDR0 [R/W] 00000000	SIO 0
000088H	SMCS1 [R/W, R] 00000010 - - - - 00 - 0		SES1 [R/W] - - - - - - 00	SDR1 [R/W] 00000000	SIO 1
00008CH	CDCR0 [R/W] 0 - - - 1111	Reserved	CDCR1 [R/W] 0 - - - 1111	Reserved	SIO 0/1 Prescaler
000090H	–				Reserved
000094H	–	–	–	–	Reserved
000098H	–	–	–	–	

Address	Register				Block
	+0	+1	+2	+3	
00009CH	ADMD [R/W, W] - - - X0000	ADCH [R/W] 00000000	–	ADCS [R/W, W] 0000 - - 00	A/D Converter
0000A0H	ADCD [R/W] 000000XX XXXXXXXX		–	ADBL [R/W] - - - - - - - 0	
0000A4H	–	DACR [R/W] - - - - - 000	DADR0 [R/W] - - - - - - XX XXXXXXXX		DAC
0000A8H	DADR1 [R/W] - - - - - - XX XXXXXXXX		–	DDBL [R/W] - - - - - - - 0	
0000ACH	IOTDBL0 [R/W] - - - - - 000	ICS01 [R/W] 00000000	IOTDBL1 [R/W] - - - - - 000	ICS23 [R/W] 00000000	Input Capture 0, 1, 2, 3
0000B0H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
0000B4H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
0000B8H	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		reserved		Output Compare 0, 1, 2.3
0000BCH	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
0000C0H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
0000C4H	–				Reserved
0000C8H	TCDT0 [R/W] XXXXXXXX XXXXXXXX		–	TCCS0 [R/W] - 0000000	Free Running Counter 0 for ICU/OCU
0000CCH	TCDT1 [R/W] XXXXXXXX XXXXXXXX		–	TCCS1 [R/W] - 0000000	Free Running Counter 1 for ICU/OCU
0000D0H	ZPD0 [R/W] 00000010	PWC0 [R/W] - - 000 - - 0	ZPD1 [R/W] 00000010	PWC1 [R/W] 00000 - - 0	SMC 0, 1
0000D4H	ZPD2 [R/W] 00000010	PWC2 [R/W] - - 000 - - 0	ZPD3 [R/W] 00000010	PWC3 [R/W] 00000 - - 0	SMC 2, 3
0000D8H	PWC20 [R/W] XXXXXXXX	PWC10 [R/W] XXXXXXXX	PWS20 [R/W] - 0000000	PWS10 [R/W] - - 000000	SMC 0
0000DCH	PWC21 [R/W] XXXXXXXX	PWC11 [R/W] XXXXXXXX	PWS21 [R/W] - 0000000	PWS11 [R/W] - - 000000	SMC 1
0000E0H	PWC22 [R/W] XXXXXXXX	PWC12 [R/W] XXXXXXXX	PWS22 [R/W] - 0000000	PWS12 [R/W] - - 000000	SMC 2
0000E4H	PWC23 [R/W] XXXXXXXX	PWC13 [R/W] XXXXXXXX	PWS23 [R/W] - 0000000	PWS13 [R/W] - - 000000	SMC 3
0000E8H	SMDBL0 [R/W] - - - - - - - 0	SMDBL1 [R/W] - - - - - - 0	SMDBL2 [R/W] - - - - - - - 0	SMDBL3 [R/W] - - - - - - - 0	SMC 0, 1, 2, 3
0000ECH	–	SGDBL [R/W] - - - - - - - 0	SGCR [R/W, R] 0 - - - - - 00 000 - - 000		Sound generator
0000F0H	SGAR [R/W] 00000000	SGFR [R/W] XXXXXXXX	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	

Address	Register				Block
	+0	+1	+2	+3	
0000F4H	–	WTDBL [R/W] - - - - - - - 0	WTCR [R/W, R] 00000000 000 - 00 - 0		Real Time Clock (WatchTimer)
0000F8H	–	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
0000FCH	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	–	
000100H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3
000104H	–		TMCSR3 [R/W] - - - - XX - - - - - XXXXX		
000108H	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4
00010CH	–		TMCSR4 [R/W] - - - - XX - - - - - XXXXX		
000110H	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5
000114H	–		TMCSR5 [R/W] - - - - XX - - - - - XXXXX		
000118H	GCN10 [R/W] 00110010 00010000		PDBL0 [R/W] - - - 00000	GCN20 [R/W] - - - - 0000	PWM Control 0
00011CH	GCN11 [R/W] 00110010 00010000		PDBL1 [R/W] - - - 00000	GCN21 [R/W] - - - - 0000	PWM Control 1
000120H	PTMR0 [R] 11111111 11111111		PCSR0 [W] XXXXXXXX XXXXXXXX		PWM0
000124H	PDUT0 [W] XXXXXXXX XXXXXXXX		PCNH0 [R/W] 0000000 -	PCNL0 [R/W] 000000 - 0	
000128H	PTMR1 [R] 11111111 11111111		PCSR1 [W] XXXXXXXX XXXXXXXX		PWM1
00012CH	PDUT1 [W] XXXXXXXX XXXXXXXX		PCNH1 [R/W] 0000000 -	PCNL1 [R/W] 000000 - 0	
000130H	PTMR2 [R] 11111111 11111111		PCSR2 [W] XXXXXXXX XXXXXXXX		PWM2
000134H	PDUT2 [W] XXXXXXXX XXXXXXXX		PCNH2 [R/W] 0000000 -	PCNL2 [R/W] 000000 - 0	
000138H	PTMR3 [R] 11111111 11111111		PCSR3 [W] XXXXXXXX XXXXXXXX		PWM3
00013CH	PDUT3 [W] XXXXXXXX XXXXXXXX		PCNH3 [R/W] 0000000 -	PCNL3 [R/W] 000000 - 0	
000140H	PTMR4 [R] 11111111 11111111		PCSR4 [W] XXXXXXXX XXXXXXXX		PWM4
000144H	PDUT4 [W] XXXXXXXX XXXXXXXX		PCNH4 [R/W] 0000000 -	PCNL4 [R/W] 000000 - 0	
000148H	PTMR5 [R] 11111111 11111111		PCSR5 [W] XXXXXXXX XXXXXXXX		PWM5
00014CH	PDUT5 [W] XXXXXXXX XXXXXXXX		PCNH5 [R/W] 0000000 -	PCNL5 [R/W] 000000 - 0	

Address	Register				Block
	+0	+1	+2	+3	
000150H	PTMR6 [R] 11111111 11111111		PCSR6 [W] XXXXXXXX XXXXXXXX		PWM6
000154H	PDUT 6 [W] XXXXXXXX XXXXXXXX		PCNH6 [R/W] 0000000 -	PCNL6 [R/W] 000000 - 0	
000158H	PTMR7 [R] 11111111 11111111		PCSR7 [W] XXXXXXXX XXXXXXXX		PWM7
00015CH	PDUT7 [W] XXXXXXXX XXXXXXXX		PCNH7 [R/W] 0000000 -	PCNL7 [R/W] 000000 - 0	
000160H	–				Reserved
000164H	CMCR [R/W] 11111111 0000000		CMPR [R/W] - - - -1001 1 - - -0001		Clock Modulation
000168H	CMLS0 [R/W] 01110111 1111111		CMLS1 [R/W] 01110111 1111111		
00016CH	CMLS2 [R/W] 01110111 1111111		CMLS3 [R/W] 01110111 1111111		
000170H	CMLT0 [R/W, R] - - - - -100 00000010		CMLT1 [R/W, R] 11110100 00000010		
000174H	CMLT2 [R/W] - - - - -100 00000010		CMLT3 [R/W, R] - - - - -100 00000010		
000178H	CMAC [R/W] 11111111 1111111		CMTS [R] - -000001 01111111		
00017CH	–	PDRCR [R/W] - - - - - 000	–	–	Power down reset
000180H	ACCDBL[R/W] - - - - - - - 0	ACSR [R/W, R] -11XXX00	–	–	Alarm comparator
000184H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH [R/W] - - - - - - 00	ITBAL [R/W] 00000000	I²C (new)
000188H	ITMKH [R/W, R] 00 - - - - 11	ITMKL [R/W] 11111111	ISMK [R/W] 01111111	ISBA [R/W] - 0000000	
00018CH	IDARH [-] 00000000	IDAR2 [R/W] 00000000	ICCR2 [R/W] - 0011111	IDBL2 [R/W] - - - - - - - 0	
000190H	CUCR [R/W, R] - - - - - - - - - - - 0 - -00		CUTD [R/W] 10000000 00000000		Calibration Unit of 32 kHz oscillator
000194H	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
000198H to 0001F8H	–				Reserved
0001FCH	–	–	F362MD [R/W] 00000000	–	F362GB Mode Register
000200H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
000210H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000214H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H to 00023CH	–				
000240H	DMACR [R/W] 00 - - 0000 -				
000244H to 0002FCH	–				Reserved
000300H	IRBS [R/W, R] 00000000 00000001 00100000 - - - - - - - -				Instruction Cache
000304H	–			ISIZE [R/W] - - - - - -11	
000308H to 0003E0H	–				Reserved
0003E4H	–			ICHCR [R/W] 0-000000	Instruction Cache
0003E8H to 0003ECH	–				Reserved
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H	DDRG [R/W] 00000000	DDRH [R/W] 00000000	DDRI [R/W] - - - -0- - -	DDRJ [R/W] 00000000	R-bus Data Direction Register
000404H	DDRK [R/W] 00000000	DDRL [R/W] 00000000	DDRM [R/W] - - - -0000	DDRN [R/W] - -000000	
000408H	DDRO [R/W] 00000000	DDRP [R/W] 00000000	DDRQ [R/W] - -000000	DDRR [R/W] 00000000	
00040CH	DDRS [R/W] 00000000	–	–	–	

Address	Register				Block
	+0	+1	+2	+3	
000410H	PFRG [R/W] 00000000	PFRH [R/W] 00000000	PFRI [R/W] ----0---	PFRJ [R/W] 00000000	R-bus Port Function Register
000414H	PFRK [R/W] 00000000	PFRL [R/W] 00000000	PFRM [R/W] ----0000	PFRN [R/W] --000000	
000418H	PFRO [R/W] 00000000	PFRP [R/W] 00000000	PFRQ [R/W] --000000	PFRR [R/W] 00000000	
00041CH	PFRS [R/W] 00000000	–	–	–	
000420H to 00043CH	–				Reserved
000440H	ICR00 [R/W, R] ---11111	ICR01 [R/W, R] ---11111	ICR02 [R/W, R] ---11111	ICR03 [R/W, R] ---11111	Interrupt Control unit
000444H	ICR04 [R/W, R] ---11111	ICR05 [R/W, R] ---11111	ICR06 [R/W, R] ---11111	ICR07 [R/W, R] ---11111	
000448H	ICR08 [R/W, R] ---11111	ICR09 [R/W, R] ---11111	ICR10 [R/W, R] ---11111	ICR11 [R/W, R] ---11111	
00044CH	ICR12 [R/W, R] ---11111	ICR13 [R/W, R] ---11111	ICR14 [R/W, R] ---11111	ICR15 [R/W, R] ---11111	
000450H	ICR16 [R/W, R] ---11111	ICR17 [R/W, R] ---11111	ICR18 [R/W, R] ---11111	ICR19 [R/W, R] ---11111	
000454H	ICR20 [R/W, R] ---11111	ICR21 [R/W, R] ---11111	ICR22 [R/W, R] ---11111	ICR23 [R/W, R] ---11111	
000458H	ICR24 [R/W, R] ---11111	ICR25 [R/W, R] ---11111	ICR26 [R/W, R] ---11111	ICR27 [R/W, R] ---11111	
00045CH	ICR28 [R/W, R] ---11111	ICR29 [R/W, R] ---11111	ICR30 [R/W, R] ---11111	ICR31 [R/W, R] ---11111	Interrupt Control unit
000460H	ICR32 [R/W, R] ---11111	ICR33 [R/W, R] ---11111	ICR34 [R/W, R] ---11111	ICR35 [R/W, R] ---11111	
000464H	ICR36 [R/W, R] ---11111	ICR37 [R/W, R] ---11111	ICR38 [R/W, R] ---11111	ICR39 [R/W, R] ---11111	
000468H	ICR40 [R/W, R] ---11111	ICR41 [R/W, R] ---11111	ICR42 [R/W, R] ---11111	ICR43 [R/W, R] ---11111	
00046CH	ICR44 [R/W, R] ---11111	ICR45 [R/W, R] ---11111	ICR46 [R/W, R] ---11111	ICR47 [R/W, R] ---11111	
000470H to 00047CH	–				Reserved
000480H	RSRR [R, R/W] 10000-00	STCR [R/W] 00110011	TBCR [R/W] 00XXXX00	CTBR [W] XXXXXXXX	Clock Control unit
000484H	CLKR [R/W] 00000000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488H to 0005FCH	–				Reserved

Address	Register				Block
	+0	+1	+2	+3	
000600H	–	–	–	–	T-unit Port Direction Register
000604H	–	–	–	DDR7 [R/W] 00000000	
000608H	DDR8 [R/W] 00000000	DDR9 [R/W] 00000000	–	DDRB [R/W] 00000000	
00060CH	–				
000610H	–	–	–	–	T-unit Port Function Register
000614H	–	–	–	PFR7 [R/W] 00001111	
000618H	PFR8 [R/W] 111110--	PFR9 [R/W] 11110101	–	PFRB [R/W] 00000000	
00061CH	–				
000620H	–				
000624H	–			PFR27 [R/W] 1111-00-	
000628H to 00063FH	–				Reserved
000640H	ASR0 [W] 00000000 00000000		AMR0 [W] 11111000 11111111		T-unit
000644H	ASR1 [W] 00000000 00000000		AMR1 [W] 00000000 00000000		
000648H	ASR2 [W] 00000000 00000000		AMR2 [W] 00000000 00000000		
00064CH	ASR3 [W] 00000000 00000000		AMR3 [W] 00000000 00000000		
000650H	ASR4 [W] 00000000 00000000		AMR4 [W] 00000000 00000000		
000654H	ASR5 [W] 00000000 00000000		AMR5 [W] 00000000 00000000		
000658H	ASR6 [W] 00000000 00000000		AMR6 [W] 00000000 00000000		
00065CH	ASR7 [W] 00000000 00000000		AMR7 [W] 00000000 00000000		
000660H	AMD0 [R/W] -0000111	AMD1 [R/W] -0000000	AMD2 [R/W] --000000	AMD3 [R/W] --000000	
000664H	AMD4 [R/W] --000000	AMD5 [R/W] --000000	AMD6 [R/W] --000000	AMD7 [R/W] --000000	
000668H	CSE 11000011	–	–	–	
00066CH	–		–		
000670H	CHE 11111111	–	–		
000674H to 0007F8H	–				Reserved

Address	Register				Block
	+0	+1	+2	+3	
0007FC$_H$	–	MODR [W] XXXXXXXX	–	–	Mode Register
000800$_H$ to 000AFC$_H$	–				Reserved
000B00$_H$	ESTS0 X0000000	ESTS1 XXXXXXXX	ESTS2 XXXXXXXX	–	DSU
000B04$_H$	ECTL0 0X000000	ECTL1 00000000	ECTL2 000X0000	ECTL3 00000X11	
000B08$_H$	ECNT0 XXXXXXXX	ECNT1 XXXXXXXX	EUSA XXX0000X	EDTC 0000XXXX	
000B0C$_H$	EWPT XXXXXXXX XXXXXXXX		–		
000B10$_H$	EDTR0 XXXXXXXX XXXXXXXX		EDTR1 XXXXXXXX XXXXXXXX		
000B14$_H$ to 000B1C$_H$	–				
000B20$_H$	EIA0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B24$_H$	EIA1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B28$_H$	EIA2 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B2C$_H$	EIA3 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B30$_H$	EIA4 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B34$_H$	EIA5 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B38$_H$	EIA6 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B3C$_H$	EIA7 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B40$_H$	EDTA XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B44$_H$	EDTM XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B48$_H$	EOA0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B4C$_H$	EOA1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B50$_H$	EPCR XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B54$_H$	EPSR XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
000B58H	EIAM0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DSU
000B5CH	EIAM1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B60H	EOAM0/EODM0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B64H	EOAM1/EODM1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B68H	EOD0 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000B6CH	EOD1 XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001000H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 003FFCH	–				Reserved
004000H to 006FFFH	–				Reserved
007000H	FMCS [R, R/W] 1110X000	–	–	–	Flash Memory Control Register
007004H	FMWT [R/W] -0000011	–	–	–	
007008H to 00FFFCH	–				Reserved
010000H to 010FFCH	Cache memory is only available on CY91FV360GA.				I-Cache 4 KB

Address	Register				Block	
	+0	+1	+2	+3		
011000H to 011FFCH	Not available on CY91F364G. On CY91FV360GA, the cache memory can be used in I-RAM mode.				I-RAM 4 4 KB	
012000H to 01FFFCH	–				Reserved	
020000H to 03BFFCH	–				Reserved	
03C000H to 03FFFCH	CY91F362GB, CY91F364G: Only 12 KB (03D000H to 03FFCH)				User RAM 16 KB (D-bus)	
040000H to 043FFCH	CY91F362GB, CY91F364G: Only 4 KB (040000H to 040FFCH)				Fast RAM 16 KB (F-bus)	
044000H to 0FEFFCH	–				Reserved	
050000H to 0507FCH	–				Boot ROM 2 KB (F-bus)	
050800H to 07FFF4H	–				reserved	
080000H to 09FFFCH	Sector 0 64 KB		Sector 7 64 KB			512 KB Flash on F-bus
0A0000H to 0BFFFCH	Sector 1 64 KB		Sector 8 64 KB			
0C0000H to 0DFFFCH	Sector 2 64 KB		Sector 9 64 KB		256 KB Flash[a] on F-bus	
0E0000H to 0EFFFCH	Sector 3 32 KB		Sector 10 32 KB			
0F0000H to 0F3FFCH	Sector 4 8 KB		Sector 11 8 KB			
0F4000H to 0F7FFCH	Sector 5 8 KB		Sector 12 8 KB			
0F8000H to 0FFFF4H	Sector 6 16 KB		Sector 13 16 KB			
0FFFF8H[b]	FMV [R] 06 00 00 00H				Mode Vector	
0FFFFCH[b]	FRV [R] 00 05 00 00H (CY91F376G: 00 04 40 00H)				Fixed Reset Vector	

CY91F376G: Please refer to the CY91F376G Special I/O Map.

Address	Register				Block
	+0	+1	+2	+3	
100000H	BVALR0 [R/W] 00000000 00000000		TREQR0 [R/W] 00000000 00000000		CAN 0 Remark: Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100004H	TCANR0 [W] 00000000 00000000		TCR0 [R/W] 00000000 00000000		
100008H	RCR0 [R/W] 00000000 00000000		RRTRR0 [R/W] 00000000 00000000		
10000CH	ROVRR0 [R/W] 00000000 00000000		RIER0 [R/W] 00000000 00000000		
100010H	CSR0 [R/W, R] 00000000 00000001		–	LEIR0 [R/W] 000-0000	
100014H	RTEC0 [R] 00000000 00000000		BTR0 [R/W] -1111111 11111111		
100018H	IDER0 [R/W] XXXXXXXX XXXXXXXX		TRTRR0 [R/W] 00000000 00000000		
10001CH	RFWTR0 [R/W] XXXXXXXX XXXXXXXX		TIER0 [R/W] 00000000 00000000		
100020H	AMSR0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100024H	AMR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100028H	AMR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10002CH to 100048H	GENERAL PURPOSE RAM [R/W]				
10004CH	IDR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100050H	IDR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100054H	IDR20 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100058H	IDR30 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10005CH	IDR40 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100060H	IDR50 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100064H	IDR60 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100068H	IDR70 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

↑ CY91F376G: Please refer to the CY91F376G Special I/O Map. ↓

Address	Register				Block
	+0	+1	+2	+3	
10006CH	IDR80 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 0
100070H	IDR90 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100074H	IDR100 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100078H	IDR110 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10007CH	IDR120 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100080H	IDR130 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100084H	IDR140 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100088H	IDR150 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10008CH	DLCR00 [R/W] -------- ----XXXX		DLCR10 [R/W] -------- ----XXXX		
100090H	DLCR20 [R/W] -------- ----XXXX		DLCR30 [R/W] -------- ----XXXX		
100094H	DLCR40 [R/W] -------- ----XXXX		DLCR50 [R/W] -------- ----XXXX		
100098H	DLCR60 [R/W] -------- ----XXXX		DLCR70 [R/W] -------- ----XXXX		
10009CH	DLCR80 [R/W] -------- ----XXXX		DLCR90 [R/W] -------- ----XXXX		
1000A0H	DLCR100 [R/W] -------- ----XXXX		DLCR110 [R/W] -------- ----XXXX		
1000A4H	DLCR120 [R/W] -------- ----XXXX		DLCR130 [R/W] -------- ----XXXX		
1000A8H	DLCR140 [R/W] -------- ----XXXX		DLCR150 [R/W] -------- ----XXXX		
1000ACH	DTR00 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000B4H	DTR10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000BCH	DTR20 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000C4H	DTR30 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000CCH	DTR40 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

CY91F376G: Please refer to the CY91F376G Special I/O Map.

Address	Register				Block
	+0	+1	+2	+3	
1000D4H	DTR50 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 0
1000DCH	DTR60 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000E4H	DTR70 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000ECH	DTR80 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000F4H	DTR90 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1000FCH	DTR100 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100104H	DTR110 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10010CH	DTR120 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100114H	DTR130 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10011CH	DTR140 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100124H	DTR150 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10012CH	CREG0 [R/W] 00000000 00000110		–		

CY91F376G: Please refer to the CY91F376G Special I/O Map.

Address	Register				Block
	+0	+1	+2	+3	
100200H	BVALR1 [R/W] 00000000 00000000	–	TREQR1 [R/W] 00000000 00000000	–	CAN 1 Remark: Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100204H	TCANR1 [W] 00000000 00000000		TCR1 [R/W] 00000000 00000000		
100208H	RCR1 [R/W] 00000000 00000000		RRTRR1 [R/W] 00000000 00000000		
10020CH	ROVRR1 [R/W] 00000000 00000000		RIER1 [R/W] 00000000 00000000		
100210H	CSR1 [R/W, R] 00000000 00000001		–	LEIR1 [R/W] 000-0000	
100214H	RTEC1 [R] 00000000 00000000		BTR1 [R/W] -1111111 11111111		
100218H	IDER1 [R/W] XXXXXXXX XXXXXXXX		TRTRR1 [R/W] 00000000 00000000		
10021CH	RFWTR1 [R/W] XXXXXXXX XXXXXXXX		TIER1 [R/W] 00000000 00000000		
100220H	AMSR1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100224H	AMR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100228H	AMR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10022CH to 100248H	GENERAL PURPOSE RAM [R/W]				
10024CH	IDR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100250H	IDR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100254H	IDR21[R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100258H	IDR31 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10025CH	IDR41 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100260H	IDR51 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100264H	IDR61 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

↑
CY91F376G: Please refer to the CY91F376G Special I/O Map.
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Address	Register				Block
	+0	+1	+2	+3	
100268H	IDR71 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 1
10026CH	IDR81 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100270H	IDR91 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100274H	IDR101 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100278H	IDR111 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10027CH	IDR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX---				
100280H	IDR131 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100284H	IDR141 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100288H	IDR151 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10028CH	DLCR01 [R/W] -------- ----XXXX		DLCR11 [R/W] -------- ----XXXX		
100290H	DLCR21 [R/W] -------- ----XXXX		DLCR31 [R/W] -------- ----XXXX		
100294H	DLCR41 [R/W] -------- ----XXXX		DLCR51 [R/W] -------- ----XXXX		
100298H	DLCR61 [R/W] -------- ----XXXX		DLCR71 [R/W] -------- ----XXXX		
10029CH	DLCR81[R/W] -------- ----XXXX		DLCR91 [R/W] -------- ----XXXX		
1002A0H	DLCR101 [R/W] -------- ----XXXX		DLCR111 [R/W] -------- ----XXXX		
1002A4H	DLCR121 [R/W] -------- ----XXXX		DLCR131 [R/W] -------- ----XXXX		
1002A8H	DLCR141 [R/W] -------- ----XXXX		DLCR151 [R/W] -------- ----XXXX		
1002ACH	DTR01 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002B4H	DTR11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002BCH	DTR21 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002C4H	DTR31 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

CY91F376G: Please refer to the CY91F376G Special I/O Map.

Address	Register				Block
	+0	+1	+2	+3	
1002CC$_H$	DTR41 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 1
1002D4$_H$	DTR51 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002DC$_H$	DTR61 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002E4$_H$	DTR71 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002EC$_H$	DTR81 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002F4$_H$	DTR91 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1002FC$_H$	DTR101 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100304$_H$	DTR111 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10030C$_H$	DTR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100314$_H$	DTR131 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10031C$_H$	DTR141 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100324$_H$	DTR151 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10032C$_H$	CREG1 [R/W] 00000000 00000110		–		

CY91F376G: Please refer to the CY91F376G Special I/O Map.

Address	Register				Block
	+0	+1	+2	+3	
100400H	BVALR2 [R/W] 00000000 00000000		TREQR2 [R/W] 00000000 00000000		CAN 2 Remark: Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100404H	TCANR2 [W] 00000000 00000000		TCR2 [R/W] 00000000 00000000		
100408H	RCR2 [R/W] 00000000 00000000		RRTRR1 [R/W] 00000000 00000000		
10040CH	ROVRR2 [R/W] 00000000 00000000		RIER2 [R/W] 00000000 00000000		
100410H	CSR2 [R/W, R] 00000000 00000001		–	LEIR2 [R/W] 000-0000	
100414H	RTEC2 [R] 00000000 00000000		BTR2 [R/W] -1111111 11111111		
100418H	IDER2 [R/W] XXXXXXXX XXXXXXXX		TRTRR2 [R/W] 00000000 00000000		
10041CH	RFWTR2 [R/W] XXXXXXXX XXXXXXXX		TIER2 [R/W] 00000000 00000000		
100420H	AMSR2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100424H	AMR02 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100428H	AMR12 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10042CH to 100448H	GENERAL PURPOSE RAM [R/W]				
10044CH	IDR02 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100450H	IDR12 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100454H	IDR22[R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100458H	IDR32 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10045CH	IDR42 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
100460H	IDR52 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 2
100464H	IDR62 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100468H	IDR72 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10046CH	IDR82 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100470H	IDR92 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100474H	IDR102 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100478H	IDR112 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10047CH	IDR122 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX---				
100480H	IDR132 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100484H	IDR142 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100488H	IDR152 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10048CH	DLCR02 [R/W] -------- ----XXXX		DLCR12 [R/W] -------- ----XXXX		
100490H	DLCR22 [R/W] -------- ----XXXX		DLCR32 [R/W] -------- ----XXXX		
100494H	DLCR42 [R/W] -------- ----XXXX		DLCR52 [R/W] -------- ----XXXX		
100498H	DLCR62 [R/W] -------- ----XXXX		DLCR72 [R/W] -------- ----XXXX		
10049CH	DLCR82[R/W] -------- ----XXXX		DLCR92 [R/W] -------- ----XXXX		
1004A0H	DLCR102 [R/W] -------- ----XXXX		DLCR112 [R/W] -------- ----XXXX		
1004A4H	DLCR122 [R/W] -------- ----XXXX		DLCR132 [R/W] -------- ----XXXX		
1004A8H	DLCR142 [R/W] -------- ----XXXX		DLCR152 [R/W] -------- ----XXXX		

Address	Register				Block
	+0	+1	+2	+3	
1004AC$_H$	DTR02 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 2
1004B4$_H$	DTR12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004BC$_H$	DTR22 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004C4$_H$	DTR32 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004CC$_H$	DTR42 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004D4$_H$	DTR52 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004DC$_H$	DTR62 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004E4$_H$	DTR72 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004EC$_H$	DTR82 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004F4$_H$	DTR92 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1004FC$_H$	DTR102 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100504$_H$	DTR112 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10050C$_H$	DTR122 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100514$_H$	DTR132 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10051C$_H$	DTR142 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 2
100524$_H$	DTR152 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10052C$_H$	CREG2 [R/W] 00000000 00000110		–		

Address	Register				Block
	+0	+1	+2	+3	
100600H	BVALR3 [R/W] 00000000 00000000		TREQR3 [R/W] 00000000 00000000		CAN 3 Remark: Address range for CAN 0 to CAN 3 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
100604H	TCANR3 [W] 00000000 00000000		TCR3 [R/W] 00000000 00000000		
100608H	RCR3 [R/W] 00000000 00000000		RRTRR31 [R/W] 00000000 00000000		
10060CH	ROVRR3 [R/W] 00000000 00000000		RIER3 [R/W] 00000000 00000000		
100610H	CSR3 [R/W, R] 00000000 00000001		–	LEIR3 [R/W] 000-0000	
100614H	RTEC3 [R] 00000000 00000000		BTR3 [R/W] -1111111 11111111		
100618H	IDER3 [R/W] XXXXXXXX XXXXXXXX		TRTRR3 [R/W] 00000000 00000000		
10061CH	RFWTR3 [R/W] XXXXXXXX XXXXXXXX		TIER3 [R/W] 00000000 00000000		
100620H	AMSR3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100624H	AMR03 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100628H	AMR13 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10062CH to 100648H	GENERAL PURPOSE RAM [R/W]				
10064CH	IDR03 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100650H	IDR13 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100654H	IDR23[R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100658H	IDR33 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
10065CH	IDR43 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 3
100660H	IDR53 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100664H	IDR63 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100668H	IDR73 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10066CH	IDR83 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100670H	IDR93 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100674H	IDR103 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100678H	IDR113 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10067CH	IDR123 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX---				
100680H	IDR133 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100684H	IDR143 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
100688H	IDR153 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
10068CH	DLCR032 [R/W] -------- ----XXXX		DLCR13 [R/W] -------- ----XXXX		
100690H	DLCR232 [R/W] -------- ----XXXX		DLCR33 [R/W] -------- ----XXXX		
100694H	DLCR43 [R/W] -------- ----XXXX		DLCR53 [R/W] -------- ----XXXX		
100698H	DLCR63 [R/W] -------- ----XXXX		DLCR733 [R/W] -------- ----XXXX		
10069CH	DLCR83[R/W] -------- ----XXXX		DLCR93 [R/W] -------- ----XXXX		
1006A0H	DLCR103 [R/W] -------- ----XXXX		DLCR113 [R/W] -------- ----XXXX		
1006A4H	DLCR123 [R/W] -------- ----XXXX		DLCR133 [R/W] -------- ----XXXX		
1006A8H	DLCR143 [R/W] -------- ----XXXX		DLCR153 [R/W] -------- ----XXXX		
1006ACH	DTR03 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006B4H	DTR13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
1006BC$_H$	DTR23 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 3
1006C4$_H$	DTR33 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006CC$_H$	DTR43 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006D4$_H$	DTR53 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006DC$_H$	DTR63 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006E4$_H$	DTR73 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006EC$_H$	DTR83 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006F4$_H$	DTR93 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
1006FC$_H$	DTR103 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100704$_H$	DTR113 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10070C$_H$	DTR123 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100714$_H$	DTR133 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10071C$_H$	DTR143 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
100724$_H$	DTR153 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
10072C$_H$	CREG3 [R/W] 00000000 00000110		–		

a. Note: For the 256 KB Flash macro, used only on the CY91F364G.
b. Write operations to address 0FFFF8$_H$ and 0FFFFC$_H$ are not possible. When reading these addresses, the values shown above will be read.

Note: Data in reserved areas and in the areas marked with "–" is indeterminate. Do not use these areas.

10. CY91F376G Special I/O Map

Address	Register				Block
	+0	+1	+2	+3	
044000H to 0447FCH	————				Boot ROM 2 KB (F-bus)
044800H to 05FFFCH	Sector 0 (parity) 56 KB		Sector 2 (parity) 56 KB		Flash Memory 768 KB (F-bus)
060000H to 07FFFCH	Sector 1 64 KB		Sector 3 64 KB		
080000H to 09FFFCH	Sector 4 64 KB		Sector 11 64 KB		
0A0000H to 0BFFFCH	Sector 5 64 KB		Sector 12 64 KB		
0C0000H to 0DFFFCH	Sector 6 64 KB		Sector 13 64 KB		
0E0000H to 0EFFFCH	Sector 7 32 KB		Sector 14 32 KB		
0F0000H to 0F3FFCH	Sector 8 8 KB		Sector 15 8 KB		
0F4000H to 0F7FFCH	Sector 9 8 KB		Sector 16 8 KB		
0F8000H to 0FFFFCH	Sector 10 16 KB		Sector 17 16 KB		
	Fixed Mode and Reset Vector				
100000H to 11FFFCH	Sector 0 - mirrored 64 KB		Sector 2 - mirrored 64 KB		
120000H to 13FFFCH	Sector 1 - mirrored 64 KB		Sector 3 - mirrored 64 KB		

Address	Register				Block
	+0	+1	+2	+3	
200000H	BVALR0 [R/W] 00000000 00000000		TREQR0 [R/W] 00000000 00000000		CAN 0 Remark: Address range for CAN 0 to CAN 1 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
200004H	TCANR0 [W] 00000000 00000000		TCR0 [R/W] 00000000 00000000		
200008H	RCR0 [R/W] 00000000 00000000		RRTRR0 [R/W] 00000000 00000000		
20000CH	ROVRR0 [R/W] 00000000 00000000		RIER0 [R/W] 00000000 00000000		
200010H	CSR0 [R/W, R] 00000000 00000001		–	LEIR0 [R/W] 000-0000	
200014H	RTEC0 [R] 00000000 00000000		BTR0 [R/W] -1111111 11111111		
200018H	IDER0 [R/W] XXXXXXXX XXXXXXXX		TRTRR0 [R/W] 00000000 00000000		
20001CH	RFWTR0 [R/W] XXXXXXXX XXXXXXXX		TIER0 [R/W] 00000000 00000000		
200020H	AMSR0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200024H	AMR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200028H	AMR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20002CH to 200048H	GENERAL PURPOSE RAM [R/W]				
20004CH	IDR00 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200050H	IDR10 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200054H	IDR20 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200058H	IDR30 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20005CH	IDR40 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200060H	IDR50 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200064H	IDR60 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200068H	IDR70 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
20006CH	IDR80 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 0
200070H	IDR90 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200074H	IDR100 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200078H	IDR110 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20007CH	IDR120 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200080H	IDR130 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200084H	IDR140 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200088H	IDR150 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20008CH	DLCR00 [R/W] -------- ----XXXX		DLCR10 [R/W] -------- ----XXXX		
200090H	DLCR20 [R/W] -------- ----XXXX		DLCR30 [R/W] -------- ----XXXX		
200094H	DLCR40 [R/W] -------- ----XXXX		DLCR50 [R/W] -------- ----XXXX		
200098H	DLCR60 [R/W] -------- ----XXXX		DLCR70 [R/W] -------- ----XXXX		
20009CH	DLCR80 [R/W] -------- ----XXXX		DLCR90 [R/W] -------- ----XXXX		
2000A0H	DLCR100 [R/W] -------- ----XXXX		DLCR110 [R/W] -------- ----XXXX		
2000A4H	DLCR120 [R/W] -------- ----XXXX		DLCR130 [R/W] -------- ----XXXX		
2000A8H	DLCR140 [R/W] -------- ----XXXX		DLCR150 [R/W] -------- ----XXXX		
2000ACH	DTR00 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000B4H	DTR10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000BCH	DTR20 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
2000C4H	DTR30 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 0
2000CCH	DTR40 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000D4H	DTR50 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000DCH	DTR60 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000E4H	DTR70 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000ECH	DTR80 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000F4H	DTR90 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2000FCH	DTR100 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200104H	DTR110 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20010CH	DTR120 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200114H	DTR130 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20011CH	DTR140 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200124H	DTR150 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20012CH	CREG0 [R/W] 00000000 00000110		–		

Address	Register				Block
	+0	+1	+2	+3	
200200H	BVALR1 [R/W] 00000000 00000000		TREQR1 [R/W] 00000000 00000000		CAN 1 Remark: Address range for CAN 0 to CAN 1 depends on chip select range. Mentioned addresses are default values, determined by boot ROM contents.
200204H	TCANR1 [W] 00000000 00000000		TCR1 [R/W] 00000000 00000000		
200208H	RCR1 [R/W] 00000000 00000000		RRTRR1 [R/W] 00000000 00000000		
20020CH	ROVRR1 [R/W] 00000000 00000000		RIER1 [R/W] 00000000 00000000		
200210H	CSR1 [R/W] 00000000 00000001		–	LEIR1 [R/W] 000-0000	
200214H	RTEC1 [R] 00000000 00000000		BTR1 [R/W] -1111111 11111111		
200218H	IDER1 [R/W] XXXXXXXX XXXXXXXX		TRTRR1 [R/W] 00000000 00000000		
20021CH	RFWTR1 [R/W] XXXXXXXX XXXXXXXX		TIER1 [R/W] 00000000 00000000		
200220H	AMSR1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200224H	AMR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200228H	AMR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20022CH to 200248H	GENERAL PURPOSE RAM [R/W]				
20024CH	IDR01 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200250H	IDR11 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200254H	IDR21[R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200258H	IDR31 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX-				
20025CH	IDR41 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200260H	IDR51 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200264H	IDR61 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200268H	IDR71 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
20026CH	IDR81 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				CAN 1
200270H	IDR91 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200274H	IDR101 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200278H	IDR111 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20027CH	IDR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXX---				
200280H	IDR131 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200284H	IDR141 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
200288H	IDR151 [R/W] XXXXXXXX XXXXXXXX XXXXX--- XXXXXXXX				
20028CH	DLCR01 [R/W] -------- ----XXXX		DLCR11 [R/W] -------- ----XXXX		
200290H	DLCR21 [R/W] -------- ----XXXX		DLCR31 [R/W] -------- ----XXXX		
200294H	DLCR41 [R/W] -------- ----XXXX		DLCR51 [R/W] -------- ----XXXX		
200298H	DLCR61 [R/W] -------- ----XXXX		DLCR71 [R/W] -------- ----XXXX		
20029CH	DLCR81[R/W] -------- ----XXXX		DLCR91 [R/W] -------- ----XXXX		
2002A0H	DLCR101 [R/W] -------- ----XXXX		DLCR111 [R/W] -------- ----XXXX		
2002A4H	DLCR121 [R/W] -------- ----XXXX		DLCR131 [R/W] -------- ----XXXX		
2002A8H	DLCR141 [R/W] -------- ----XXXX		DLCR151 [R/W] -------- ----XXXX		
2002ACH	DTR01 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002B4H	DTR11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002BCH	DTR21 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Register				Block
	+0	+1	+2	+3	
2002C4H	DTR31 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				CAN 1
2002CCH	DTR41 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002D4H	DTR51 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002DCH	DTR61 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002E4H	DTR71 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002ECH	DTR81 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002F4H	DTR91 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
2002FCH	DTR101 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200304H	DTR111 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20030CH	DTR121 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200314H	DTR131 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20031CH	DTR141 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
200324H	DTR151 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
20032CH	CREG1 [R/W] 00000000 00000110				

11. Interrupt Causes, Interrupt Vectors, and Interrupt Control Register

Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		RN
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
Reset	0	00	–	–	0x3FCH	0x000FFFFCH	–
Mode vector	1	01	–	–	0x3F8H	0x000FFFF8H	–
System reserved	2	02	–	–	0x3F4H	0x000FFFF4H	–
System reserved	3	03	–	–	0x3F0H	0x000FFFF0H	–
System reserved	4	04	–	–	0x3ECH	0x000FFFECH	–
System reserved	5	05	–	–	0x3E8H	0x000FFFE8H	–
System reserved	6	06	–	–	0x3E4H	0x000FFFE4H	–
Co-processor default trap *4	7	07	–	–	0x3E0H	0x000FFFE0H	–
Co-processor error trap *4	8	08	–	–	0x3DCH	0x000FFFDCH	–
INTE instruction *4	9	09	–	–	0x3D8H	0x000FFFD8H	–
Instruction break exception *4	10	0A	–	–	0x3D4H	0x000FFFD4H	–
Operand break trap *4	11	0B	–	–	0x3D0H	0x000FFFD0H	–
Step trace trap *4	12	0C	–	–	0x3CCH	0x000FFFCCH	–
NMI interrupt (tool) *4	13	0D	–	–	0x3C8H	0x000FFFC8H	–
Undefined instruction exception	14	0E	–	–	0x3C4H	0x000FFFC4H	–
NMI request	15	0F	FH fixed		0x3C0H	0x000FFFC0H	–
External Interrupt 0	16	10	ICR00	0x440H	0x3BCH	0x000FFFBCH	4
External Interrupt 1	17	11	ICR01	0x441H	0x3B8H	0x000FFFB8H	5
External Interrupt 2	18	12	ICR02	0x442H	0x3B4H	0x000FFFB4H	8
External Interrupt 3	19	13	ICR03	0x443H	0x3B0H	0x000FFFB0H	9
External Interrupt 4	20	14	ICR04	0x444H	0x3ACH	0x000FFFACH	–
External Interrupt 5	21	15	ICR05	0x445H	0x3A8H	0x000FFFA8H	–
External Interrupt 6	22	16	ICR06	0x446H	0x3A4H	0x000FFFA4H	–
External Interrupt 7	23	17	ICR07	0x447H	0x3A0H	0x000FFFA0H	–
Reload Timer 0	24	18	ICR08	0x448H	0x39CH	0x000FFF9CH	6
Reload Timer 1	25	19	ICR09	0x449H	0x398H	0x000FFF98H	7
Reload Timer 2	26	1A	ICR10	0x44AH	0x394H	0x000FFF94H	–
CAN 0 RX	27	1B	ICR11	0x44BH	0x390H	0x000FFF90H	–
CAN 0 TX/NS	28	1C	ICR12	0x44CH	0x38CH	0x000FFF8CH	–
CAN 1 RX	29	1D	ICR13	0x44DH	0x388H	0x000FFF88H	–
CAN 1 TX/NS	30	1E	ICR14	0x44EH	0x384H	0x000FFF84H	–
CAN 2 RX	31	1F	ICR15	0x44FH	0x380H	0x000FFF80H	–
CAN 2 TX/NS	32	20	ICR16	0x450H	0x37CH	0x000FFF7CH	–
CAN 3 RX *5	33	21	ICR17	0x451H	0x378H	0x000FFF78H	–
CAN 3 TX/NS *5	34	22	ICR18	0x452H	0x374H	0x000FFF74H	–
PPG 0/1	35	23	ICR19	0x453H	0x370H	0x000FFF70H	–

Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		RN
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
PPG 2/3	36	24	ICR20	0x454H	0x36CH	0x000FFF6CH	–
PPG 4/5	37	25	ICR21	0x455H	0x368H	0x000FFF68H	–
PPG 6/7	38	26	ICR22	0x456H	0x364H	0x000FFF64H	–
Reload Timer 3	39	27	ICR23	0x457H	0x360H	0x000FFF60H	–
Reload Timer 4	40	28	ICR24	0x458H	0x35CH	0x000FFF5CH	–
Reload Timer 5	41	29	ICR25	0x459H	0x358H	0x000FFF58H	–
ICU 0/1	42	2A	ICR26	0x45AH	0x354H	0x000FFF54H	–
OCU 0/1	43	2B	ICR27	0x45BH	0x350H	0x000FFF50H	–
ICU 2/3	44	2C	ICR28	0x45CH	0x34CH	0x000FFF4CH	–
OCU 2/3	45	2D	ICR29	0x45DH	0x348H	0x000FFF48H	–
ADC	46	2E	ICR30	0x45EH	0x344H	0x000FFF44H	14
Timebase Overflow	47	2F	ICR31	0x45FH	0x340H	0x000FFF40H	–
Free Running Counter 0	48	30	ICR32	0x460H	0x33CH	0x000FFF3CH	–
Free Running Counter 1	49	31	ICR33	0x461H	0x338H	0x000FFF38H	–
SIO 0 *6	50	32	ICR34	0x462H	0x334H	0x000FFF34H	12
SIO 1 *6	51	33	ICR35	0x463H	0x330H	0x000FFF30H	15
Sound Generator	52	34	ICR36	0x464H	0x32CH	0x000FFF2CH	–
UART 0 RX	53	35	ICR37	0x465H	0x328H	0x000FFF28H	0
UART 0 TX	54	36	ICR38	0x466H	0x324H	0x000FFF24H	1
UART 1 RX	55	37	ICR39	0x467H	0x320H	0x000FFF20H	2
UART 1 TX	56	38	ICR40	0x468H	0x31CH	0x000FFF1CH	3
UART 2 RX	57	39	ICR41	0x469H	0x318H	0x000FFF18H	10
UART 2 TX	58	3A	ICR42	0x46AH	0x314H	0x000FFF14H	11
I²C *7	59	3B	ICR43	0x46BH	0x310H	0x000FFF10H	13
Alarm Comparator	60	3C	ICR44	0x46CH	0x30CH	0x000FFF0CH	–
RTC (Watchtimer) / Calibration Unit	61	3D	ICR45	0x46DH	0x308H	0x000FFF08H	–
DMA	62	3E	ICR46	0x46EH	0x304H	0x000FFF04H	–
Delayed interrupt activation bit	63	3F	ICR47	0x46FH	0x300H	0x000FFF00H	–
							–
System reserved *3	64	40	–	–	0x2FCH	0x000FFEFCH	–
System reserved *3	65	41	–	–	0x2F8H	0x000FFEF8H	–
Security vector	66	42	–	–	0x2F4H	0x000FFEF4H	–
System reserved	67	43	(ICR51)	0x473H	0x2F0H	0x000FFEF0H	–
System reserved	68	44	(ICR52)	0x474H	0x2ECH	0x000FFEECH	–
System reserved	69	45	(ICR53)	0x475H	0x2E8H	0x000FFEE8H	–
System reserved	70	46	(ICR54)	0x476H	0x2E4H	0x000FFEE4H	–
System reserved	71	47	(ICR55)	0x477H	0x2E0H	0x000FFEE0H	–
System reserved	72	48	(ICR56)	0x478H	0x2DCH	0x000FFEDCH	–

Interrupt	Interrupt Number		Interrupt Level *1		Interrupt Vector *2		RN
	Decimal	Hexa-decimal	Setting Register	Register Address	Offset	Default Vector Address	
System reserved	73	49	(ICR57)	0x479H	0x2D8H	0x000FFED8H	–
System reserved	74	4A	(ICR58)	0x47AH	0x2D4H	0x000FFED4H	–
System reserved	75	4B	(ICR59)	0x47BH	0x2D0H	0x000FFED0H	–
System reserved	76	4C	(ICR60)	0x47CH	0x2CCH	0x000FFECCH	–
System reserved	77	4D	(ICR61)	0x47DH	0x2C8H	0x000FFEC8H	–
System reserved	78	4E	(ICR62)	0x47EH	0x2C4H	0x000FFEC4H	–
System reserved	79	4F	(ICR63)	0x47FH	0x2C0H	0x000FFEC0H	–
Used by the INT instruction.	80 to 255	50 to FF	–	–	0x2BCH to 0x000H	0x000FFEBCH to 0x000FFC00H	–
							–
							–

*1: The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2: The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR). The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (0x000FFC00H). The TBR is initialized to this value by a reset.After execution of the internal boot ROM TBR is set to 0x00FFC00H.

*3: .....Used by REALOS

*4: ..... System reserved

*5: ..... Only available on CY91FV360GA

*6: USART5/6 in CY91F364G, UART1/2 in all other devices.

*7: DMA to/from the USARTs in CY91F364G is not implemented.

Remarks:

The 1-Kbyte area from the address specified in TBR is the EIT vector area.

Each vector consists of four bytes. The following formula shows the relationship between the vector number and vector address.

vctadr = TBR + vctofs
= TBR + (3FCH - 4 × vct)

vctadr: Vector address, vctofs: Vector offset, vct: Vector number

12. Peripheral Resources

12.1 Instruction Cache

This section describes the instruction cache memory included in FR50 Family members and it operation. This only applies to CY91FV360GA.

12.1.1 General Description

The instruction cache is temporary memory. When an external low-speed memory accesses an instruction code, the instruction cache stores the single-accessed code to increase the second and subsequent access speeds.Setting this memory to the RAM mode enables software to directly read and write instruction cache data RAM and tag RAM.

12.1.2 Main Body Structure

- FR basic instruction length: 2 bytes
- Block arrangement system: 2-way set associative system
- Block
  - One way consists of 128 blocks.
  - One block consists of 16 bytes (= 4 sub-blocks).
  - One sub-block consists of 4 bytes (= 1 bus access unit).

Figure 12-1. Instruction Cache Structure

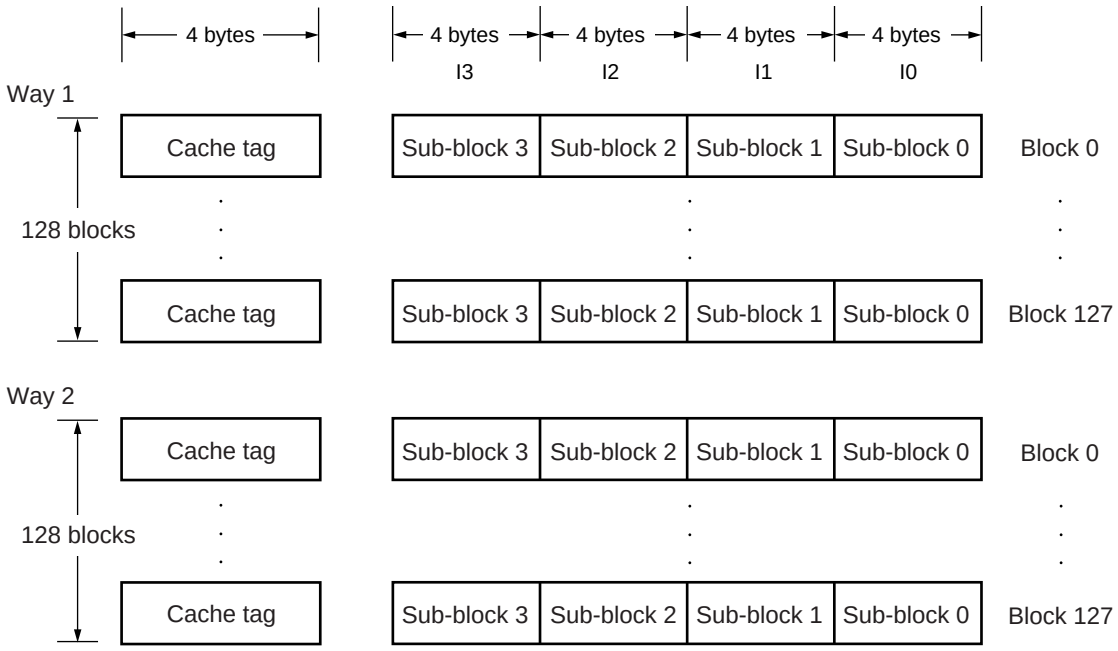
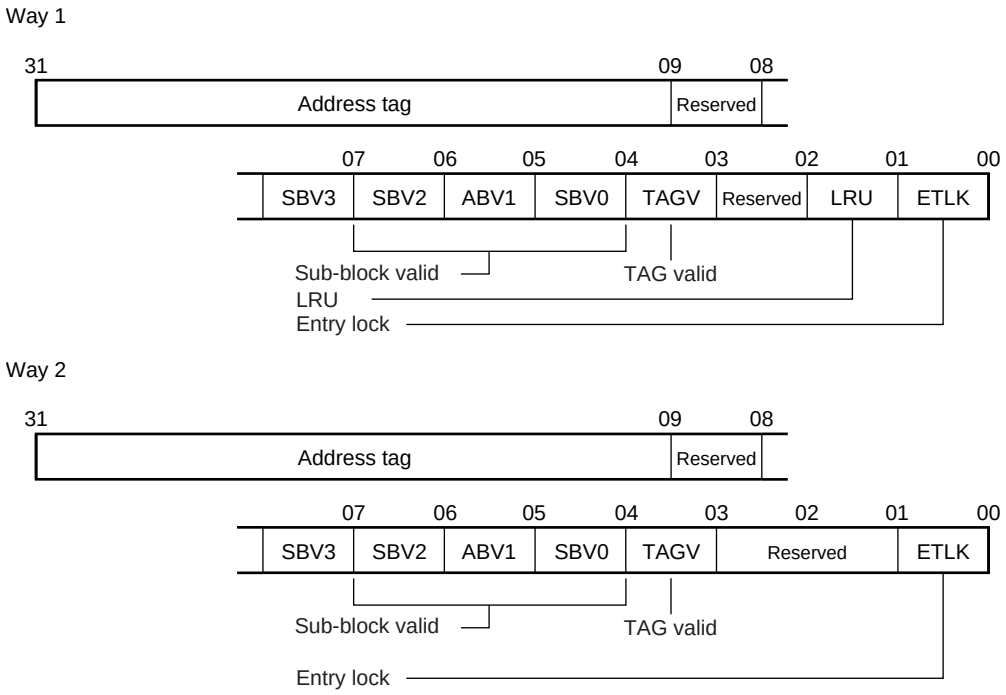


Figure 12-2. Instruction Cache Tag



12.0.1 Control Register Structure

IRBS (32 bits)
Address: 00000300H

31	30	29	28	27	26	25	24	Initial value
0	0	0	0	0	0	0	0	00000000B
R	R	R	R	R	R	R	R	

23	22	21	20	19	18	17	16	Initial value
0	0	0	0	0	0	0	1	00000001B
R	R	R	R	R	R	R	R	ICR26

Address: 00000302H

15	14	13	12	11	10	9	8	Initial value
IRBS	IRBS	IRBS	IRBS	—	—	—	—	0010 - - - -B
R/W	R/W	R/W	R/W	—	—	—	—	

7	6	5	4	3	2	1	0	Initial value
—	—	—	—	—	—	—	—	- - - - - - - - B
—	—	—	—	—	—	—	—	

IRBS [bits 15 to 12] These bits are used to set the base address of cache RAM at access in the RAM mode. Align cache RAM in units of 4K bytes. These bits are initialized by INIT. The initial value is the 00012000H address.

ISIZE (8 bits)

00000307H

7	6	5	4	3	2	1	0	Initial value
—	—	—	—	—	—	SIZE1	SIZE0	- - - - - - 11B
—	—	—	—	—	—	R/W	R/W	

The ICHCR (I-CacHe Control Register) controls the instruction cache operations.
Writing to the ICHCR does not affect caching of instructions fetched within three subsequent cycles.

ICHCR (8 bits)

000003E7H

7	6	5	4	3	2	1	0	Initial value
RAM	—	GBLK	ALFL	EOLK	ELKR	FLSH	ENAB	0 - 000000B
R/W	—	R/W	R/W	R/W	R/W	R/W	R/W	

12.1 Boot ROM

The Boot ROM is a fixed start-up routine which is located at FF000H (Reset entry) and will therefore be executed after every RST or INIT. The purpose of this ROM is to configure the device after a reset and to provide a simple serial bootloader for programming the embedded Flash memories.

The Boot ROM contains three logical parts:

12.1.1 Chip Initializations

Immediately after each reset, the following settings will be made:

CS0: 200000H…2FFFFFH, 32 Bit Bus, 1 wait-state (default external access)

CS7: 100000H…10FFFFH, 16 Bit Bus, 1 wait-state (CAN)

In addition, the Table-Base Register will be initialized to 1FFC00H (F361GA only) and the synchronous reset (see TBCR) will be enabled.

12.1.2 Check for Bootcondition

After the chip initialization, the “Security-Vector” will be checked (Vector #66). The purpose of this feature is to disable the bootstraploader due to security reasons.

The RSRR (reset cause register) will be read and saved. If no power-on reset (external INITX input, RSRR = 0x80) is indicated, a branch to the user application will be initiated (Branch to 1F4000H).

If INITX was detected and the “Security-Vector” check okay, the following conditions must be met in order to start the Bootstraploader:

Within a certain time, the start-up character “V” must be received via UART0 (9600, 8N1). The time-out is set to 200 ms.

12.1.3 Bootstraploader

If the Bootcondition was met, an acknowledge character “F” will be transmitted via UART0 to indicate that the Bootloader is ready to accept commands. 4 different commands are possible:

Receive and write to a specified memory block

Dump the contents of a specified memory block

Initiate a “CALL” to a certain location

Re-dump a calculated checksum for verification

12.1.4 Configuration Register (F362 mode register F362MD)

This register is used to control which pins of the external bus interface are active, where the pins for the external DMA channel are located and which I²C module is used.

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
00001FEH	ADRSWAP	ASYMCLKT	HIZ_D_A	HIZ_ECLK	HIZ_D_23_16	HIZ_D_15_0	DMASWP	IICSEL
access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

12.2 Clock Modulator

An important property of MCUs and other electronic devices is their electromagnetic compatibility - EMC. Besides a low susceptibility against external interferences, a low radiated emission is desired to avoid interference of adjacent devices.

Particularly the system clock and derived signals such as data- and address busses contribute significantly to the radiated emission. The purpose of the clock modulator is to spread the energy of these signals over a wide range of frequencies and thus reducing the amplitudes of the fundamental and harmonic frequencies.

With the use of an advanced frequency modulation algorithm, the Cypress built in clock modulator can achieve an attenuation of up to 20-25 dB compared to non modulated clock operation. Since the modulator is highly configurable, it can be optimally adjusted to the actual application in order to achieve minimal electromagnetic interference.

By default, the modulator is disabled and the MCU is running with unmodulated clock.

If you plan to use this feature, please contact Cypress.

12.3 I/O Ports

The I/O port registers consist of the “port data registers (PDR)”, the “data direction registers (DDR)” and the “port function registers (PFR)”.

The bits in PDRs correspond to the bits in DDRs and PFRs. Similarly, the register bits correspond to the port pins.

The port data registers contain the port I/O data and the data direction registers specify whether the corresponding bits (pins) are inputs or outputs. Bits set to “0” are inputs and bits set to “1” are outputs. The port function registers specify whether the port is used as peripheral port or as “I/O” port. Usually bits set to “0” mean I/O port and bits set to “1” mean functional port.

In case of analog peripherals there is additional circuitry to ensure that the digital logic is not disturbed by the analog signals. If the analog input function e.g. ADC is enabled the digital input is fixed to “0”.

- Input mode (DDR = “0”)

  PDR read: Reads the level on the corresponding external pin.
  PDR write: writes the PDR setting value.

- Output mode (DDR = “1”)

  PDR read: Reads the PDR value.
  PDR write: Outputs the PDR value to the corresponding external pins.

12.3.1 Register Configuration

Port Data Register

PDR7

Address: 00000007H

7	6	5	4	3	2	1	0	Initial value	Access
P77	P76	P75	P74	P73	P72	P71	P70	1111XXXXB	R/W

PDR8

Address: 00000008H

7	6	5	4	3	2	1	0	Initial value	Access
P87	P86	P85	P84	P83	P82	P81	P80	XXXXXXXXB	R/W

PDR9

Address: 00000009H

7	6	5	4	3	2	1	0	Initial value	Access
P97	P96	P95	P94	P93	P92	P91	P90	XXXXXXX1B	R/W

PDRB

Address: 0000000BH

7	6	5	4	3	2	1	0	Initial value	Access
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	XXXXXXXXB	R/W

PDRG

Address: 00000010H

7	6	5	4	3	2	1	0	Initial value	Access
PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	XXXXXXXXB	R/W

PDRH

Address: 00000011H

7	6	5	4	3	2	1	0	Initial value	Access
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	XXXXXXXXB	R/W

PDRI

Address: 00000012H

7	6	5	4	3	2	1	0	Initial value	Access
P17	—	—	—	PI3	—	—	—	X - - - X - - -B	R/W

PDRJ

Address: 00000013H

7	6	5	4	3	2	1	0	Initial value	Access
PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	XXXXXXXXB	R/W

PDRK

Address: 00000014H

7	6	5	4	3	2	1	0	Initial value	Access
PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	XXXXXXXXB	R/W

PDRL

Address: 00000015H

7	6	5	4	3	2	1	0	Initial value	Access
PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	XXXXXXXXB	R/W

PDRM

Address: 00000016H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	—	PM3	PM2	PM1	PM0	- - - - XXXXB	R/W

PDRN

Address: 00000017H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	PN5	PN4	PN3	PN2	PN1	PN0	- -XXXXXXB	R/W

PDRO

Address: 00000018H

7	6	5	4	3	2	1	0	Initial value	Access
PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	XXXXXXXXB	R/W

(Continued)

(Continued)

PDRP

Address: 00000019H

7	6	5	4	3	2	1	0	Initial value	Access
PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	XXXXXXXXB	R/W

PDRQ

Address: 0000001AH

7	6	5	4	3	2	1	0	Initial value	Access
—	—	PQ5	PQ4	PQ3	PQ2	PQ1	PQ0	--XXXXXXB	R/W

PDRR

Address: 0000001BH

7	6	5	4	3	2	1	0	Initial value	Access
PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	XXXXXXXXB	R/W

PDRS

Address: 0000001CH

7	6	5	4	3	2	1	0	Initial value	Access
PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	XXXXXXXXB	R/W

Data Direction Register (DDR)

DDR7
Address: 00000607H

7	6	5	4	3	2	1	0	Initial value	Access
P77	P76	P75	P74	P73	P72	P71	P70	00000000B	R/W

DDR8
Address: 00000608H

7	6	5	4	3	2	1	0	Initial value	Access
P87	P86	P85	P84	P83	P82	P81	P80	00000000B	R/W

DDR9
Address: 00000609H

7	6	5	4	3	2	1	0	Initial value	Access
P97	P96	P95	P94	P93	P92	P91	P90	00000000B	R/W

DDRB
Address: 0000600BH

7	6	5	4	3	2	1	0	Initial value	Access
PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	00000000B	R/W

DDRG
Address: 00000400H

7	6	5	4	3	2	1	0	Initial value	Access
PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	00000000B	R/W

DDRH
Address: 00000401H

7	6	5	4	3	2	1	0	Initial value	Access
PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	00000000B	R/W

DDRI
Address: 00000402H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	—	PI3	—	—	—	- - - - 0 - - -B	R/W

DDRJ
Address: 00000403H

7	6	5	4	3	2	1	0	Initial value	Access
PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	00000000B	R/W

DDRK
Address: 00000404H

7	6	5	4	3	2	1	0	Initial value	Access
PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	00000000B	R/W

DDRL
Address: 00000405H

7	6	5	4	3	2	1	0	Initial value	Access
PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000B	R/W

DDRM
Address: 00000406H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	—	—	PM3	PM2	PM1	PM0	- - - - 0000B	R/W

DDRN
Address: 00000407H

7	6	5	4	3	2	1	0	Initial value	Access
—	—	PN5	PN4	PN3	PN2	PN1	PN0	- -000000B	R/W

DDRO
Address: 00000408H

7	6	5	4	3	2	1	0	Initial value	Access
PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	00000000B	R/W

(Continued)

(Continued)

DDRP

Address: 00000409H

7	6	5	4	3	2	1	0
PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0

Initial value: 00000000B
Access: R/W

DDRQ

Address: 0000040AH

7	6	5	4	3	2	1	0
—	—	PQ5	PQ4	PQ3	PQ2	PQ1	PQ0

Initial value: --000000B
Access: R/W

DDRR

Address: 0000040BH

7	6	5	4	3	2	1	0
PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0

Initial value: 00000000B
Access: R/W

DDRS

Address: 0000040CH

7	6	5	4	3	2	1	0
PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0

Initial value: 00000000B
Access: R/W

Port Function Registers (PFR)

	7	6	5	4	3	2	1	0	Initial value	Access
PFR7 Address: 00000617H	P77	P76	P75	P74	P73	P72	P71	P70	00001111B	R/W
PFR8 Address: 00000618H	P87	P86	P85	P84	P83	P82	—	—	111110 --B	R/W
PFR9 Address: 00000619H	P97	P96	P95	P94	P93	P92	P91	P90	11110101B	R/W
PFRB Address: 0000061BH	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	00000000B	R/W
PFR27 Address: 00000627H	P277	P276	P275	P274	P273	P272	P271	P270	1111 - 00 -B	R/W
PFRG Address: 00000410H	PG7	PG6	PG5	PG4	PG3	PG2	PG1	PG0	00000000B	R/W
PFRH Address: 00000411H	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	00000000B	R/W
PFRI Address: 00000412H	—	—	—	—	PI3	—	—	—	----0 ---B	R/W
PFRJ Address: 00000413H	PJ7	PJ6	PJ5	PJ4	PJ3	PJ2	PJ1	PJ0	00000000B	R/W
PFRK Address: 00000414H	PK7	PK6	PK5	PK4	PK3	PK2	PK1	PK0	00000000B	R/W
PFRL Address: 00000415H	PL7	PL6	PL5	PL4	PL3	PL2	PL1	PL0	00000000B	R/W
PFRM Address: 00000416H	—	—	—	—	PM3	PM2	PM1	PM0	- - - - 0000B	R/W
PFRN Address: 00000417H	—	—	PN5	PN4	PN3	PN2	PN1	PN0	- - 000000B	R/W

(Continued)

(Continued)

PFRO

Address: 00000418H

7	6	5	4	3	2	1	0	Initial value	Access
PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	00000000B	R/W

PFRP

Address: 00000419H

7	6	5	4	3	2	1	0	Initial value	Access
PP7	PP6	PP5	PP4	PP3	PP2	PP1	PP0	00000000B	R/W

PFRQ

Address: 0000041AH

7	6	5	4	3	2	1	0	Initial value	Access
—	—	PQ5	PQ4	PQ3	PQ2	PQ1	PQ0	- - 000000B	R/W

PFRR

Address: 0000041BH

7	6	5	4	3	2	1	0	Initial value	Access
PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	00000000B	R/W

PFRS

Address: 0000041CH

7	6	5	4	3	2	1	0	Initial value	Access
PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	00000000B	R/W

12.4 DMA Controller (DMAC)

The DMAC module is used to implement direct memory access (DMA) transfer in FR50 family devices.

In a DMA transfer controlled by this module, various types of data can be transferred at high speed without involving the CPU, thus increasing system performance.

12.4.1 Hardware Configuration

The following are the main components of the DMAC module:

- Five independent DMA channels
- 5-channel independent access control circuit
- 32-bit address registers (Reload can be specified: Two registers for each channel.)
- 16-bit transfer count registers (Reload can be specified: One register for each channel.)
- 4-bit block count registers (One register for each channel)
- External transfer request input pins DREQ0, DREQ1, and DREQ2 (only ch0, ch1, and ch2)
- External transfer request acceptance output pins DACK0, DACK1, and DACK2 (only ch0, ch1, and ch2)
- DMA termination output pins DEOP0, DEOP1, and DEOP2 (only ch0, ch1, and ch2)
- Two-cycle transfer

12.4.2 Main Functions

The following are the main functions of data transfer performed by the module:

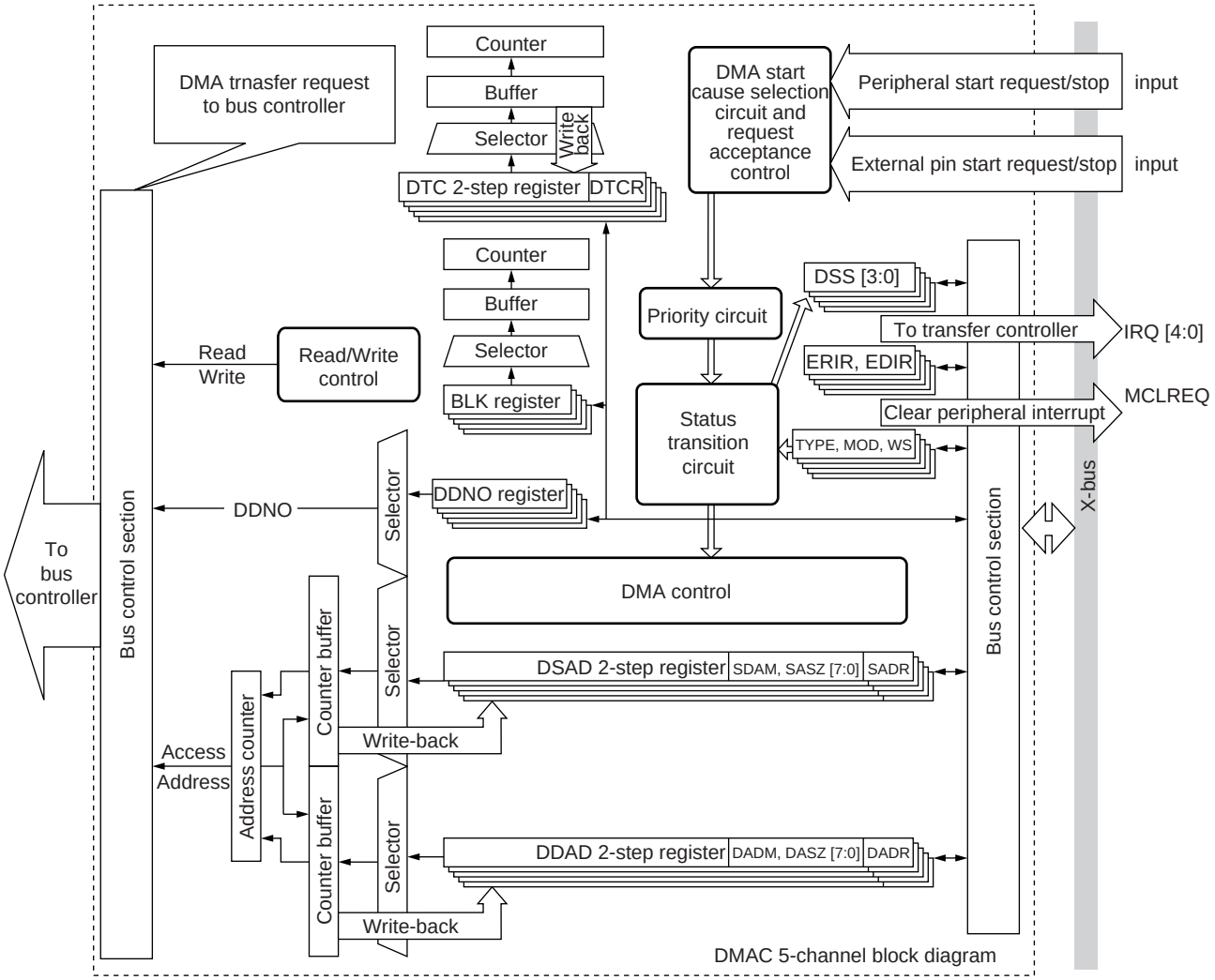
- Independent data transfer in multiple channels is enabled (5 channels).
  - a: Priority (ch0 > ch1 > ch2 > ch3 > ch4)
  - b: Priority can be alternated between ch0 and ch1.
  - c: DMAC start cause
    - External-only pin input (edge detection/level detection channels 0 to 2 only)
    - Internal peripheral request (interrupt request is shared, including external interrupts)
    - Software request (register write)
  - d: Transfer mode
    - Demand transfer, burst transfer, step transfer, block transfer
    - Addressing mode 32-bit full address specification (increase, decrease, fixed)
      (An address increment/decrement size of −255 to +255 can be specified.)
    - Data types of byte, halfword, and word lengths
    - Single-shot/reload selectable

12.4.3 Registers Configuration

Channel 0 control/status register A	DMACA0 0000200H	
Channel 0 control/status register B	DMACB0 0000204H	
Channel 1 control/status register A	DMACA1 0000208H	
Channel 1 control/status register B	DMACB1 000020CH	
Channel 2 control/status register A	DMACA2 0000210H	
Channel 2 control/status register B	DMACB2 0000214H	
Channel 3 control/status register A	DMACA3 0000218H	
Channel 3 control/status register B	DMACB3 000021CH	
Channel 4 control/status register A	DMACA4 0000220H	
Channel 4 control/status register B	DMACB4 0000224H	
Overall control register	DMACR 0000240H	

Channel 0 transfer source address register	DMASA0 0001000H	
Channel 0 transfer destination address register	DMADA0 0001004H	
Channel 1 transfer source address register	DMASA1 0001008H	
Channel 1 transfer destination address register	DMADA1 000100CH	
Channel 2 transfer source address register	DMASA2 0001010H	
Channel 2 transfer destination address register	DMADA2 0001014H	
Channel 3 transfer source address register	DMASA3 0001018H	
Channel 3 transfer destination address register	DMADA3 000101CH	
Channel 4 transfer source address register	DMASA4 0001020H	
Channel 4 transfer destination address register	DMADA4 0001024H	

12.4.4 Block Diagram



12.5 UART

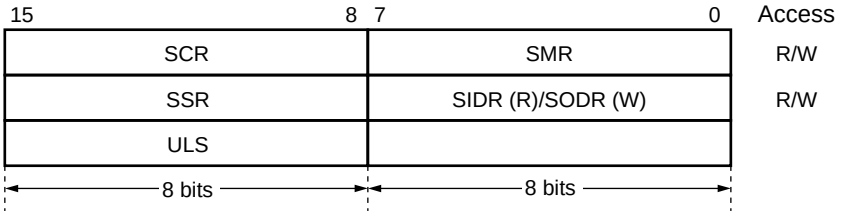
The UART is a serial I/O port for performing asynchronous (stop-start synchronization) communications. The CY91360G series contains three UART channels.

12.5.1 Features

- Full-duplex, double buffering
- Supports asynchronous (stop-start synchronization) communications
- Supports multi-processor mode
- Fully programmable baud rate
  The baud rate can be set using an internal timer. (See the U-TIMER section.)
- Supports flexible baud rate setting using an external clock
- Error detection function (parity, framing, overrun)
- Non return to zero (NRZ) transfer signal
- Supports DMA transfer activation using an interrupt

12.5.2 Register Configuration

Register structure



Serial input register (SIDR)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Serial output register (SODR)

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Serial status register (SSR)

7	6	5	4	3	2	1	0
PE	ORE	FRE	RDRF	TDRE	—	RIE	TIE

Serial mode register (SMR)

7	6	5	4	3	2	1	0
MD1	MD0	—	—	CS0	—	SCKE	—

Serial control register (SCR)

7	6	5	4	3	2	1	0
PEN	P	SBL	CL	A/D	REC	RXE	TXE

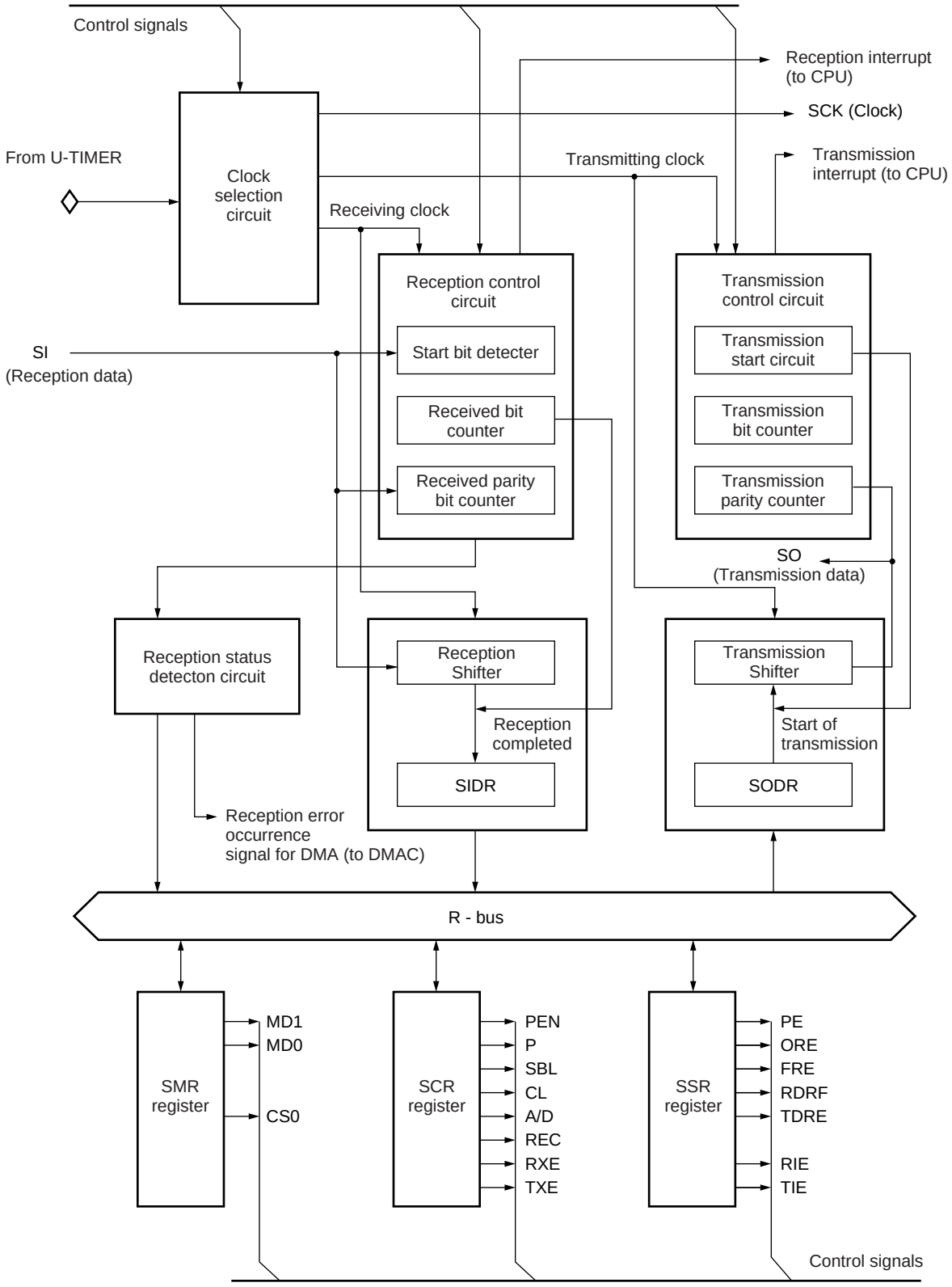
UART level select register (ULS)

7	6	5	4	3	2	1	0
—	—	—	—	NSDO	NSDI	UTDBL	UDBL

	Address	Bits	7	6	5	4	3	2	1	0	Initial value
SMR	0000 0063H 0000 006FH 0000 007BH		MD1	MD2	Reserved	Reserved	CS0	Reserved	Reserved	Reserved	00--0-00B
			R/W	R/W			W				← Access

	Address	Bits	7	6	5	4	3	2	1	0	Initial value
SCR	0000 0062H 0000 006EH 0000 007AH		PEN	P	SBL	CL	A/D	REC	RXE	TXE	00000100B
			R/W	R/W	R/W	R/W	R/W	W	R/W	R/W	← Access

12.5.3 Block Diagram

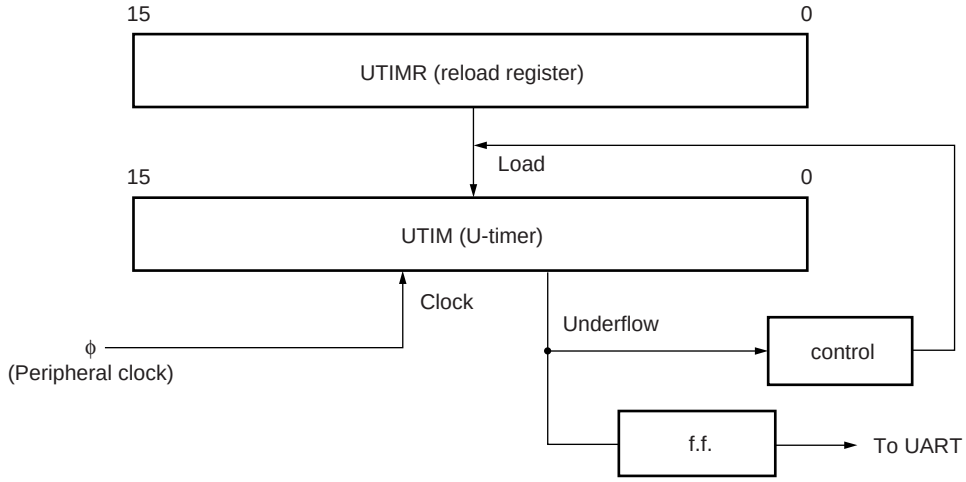


12.6 U-TIMER (16-bit Timer for UART Baud Rate Generation)

The U-timer (U-TIMER) is a 16-bit timer used to generate the baud rate for the UART. The operating frequency of the chip and the U-TIMER reload value can be combined to set a user-defined baud rate.

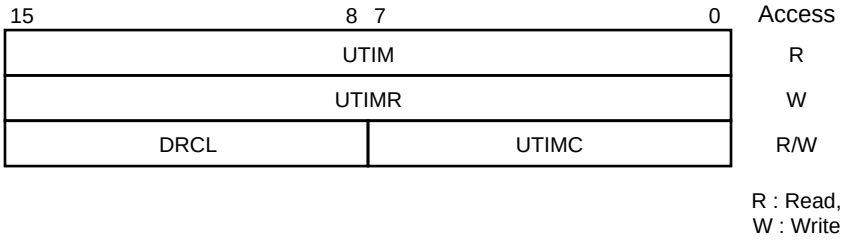
The CY91360G series contains three U-TIMER channels. The intervaltimers can count for a maximum of 216 × ϕ.

12.6.1 Block Diagram



12.6.2 Register Configuration

Register structure



UTIM	Address	Bits	15	14	----------	2	1	0	Initial value	Access
ch0	00000068H		b15	b14		b2	b1	b0	0	R
ch1	00000074H									
ch2	00000080H									

UTIMR Reload Register

UTIMR	Address	Bits	15	14	----------	2	1	0	Initial value	Access
ch0	00000068H		b15	b14		b2	b1	b0	0	W
ch1	00000074H									
ch2	00000080H									

UTIMC U Timer Control Register

UTIMC	Address	7	6	5	4	3	2	1	0	Initial value	Access
ch0	0000006BH	UCC1	—	—	—	UNDR	Reserved	UTST	UTCR	0---0001	R/W
ch1	00000077H										
ch2	00000083H										

12.7 PWM Timer

The PWM (Pulse Width Modulation) timer can output high-precision pulse waves at an arbitrary cycle and pulse width (duty ratio).

The CY91360G series contains eight PWM timer channels. Each of the channels consists of a 16-bit down-counter, cycle setting register, duty setting register, and pin controller.

The control status register for each channel is used to indicate the operation status of the PWM timer. General control registers 1 and 2 are common registers shared by four channels, serving for input and software triggering.

12.7.1 Features

- The count clock for the 16-bit down-counter can be selected from among the following four types:
  Internal clocks: ϕ, ϕ/4, ϕ/16, ϕ/64 (ϕ: Machine clock for peripherals)
- The counter can be initialized to "FFFF$_H$" by a reset or underflow.
  The 16-bit down-counter causes an underflow when it changes from "0000$_H$" to "FFFF$_H$".
- Each channel has PWM outputs.
  Eight channels: Eight output pins
- Registers
  Cycle setting register: Data reload register with buffer
  Data transfer from the buffer is performed either when an activation trigger is detected or when the down-counter causes an underflow (cycle match). The output is inverted at a cycle match.
  Duty setting register: Compare register with buffer.
  The value set in this register is compared to the counter value. The output is inverted when the values match (duty match).
- Pin control
  A duty match causes a reset to "1" (given priority).
  An underflow causes a reset to "0".
  The output value fix mode enables output of all "L" or all "H".
  The polarity can also be specified.
- Interrupt requests can be generated by selecting the following interrupt sources:
  Activation of the PWM timer (software trigger or trigger input)
  Occurrence of an underflow (cycle match)
  Occurrence of a duty match
  Occurrence of an underflow (cycle match) or duty match
- You can set simultaneous activation of two or more channels using software or another interval timer. You can also set restarting the PWM timer during operation.

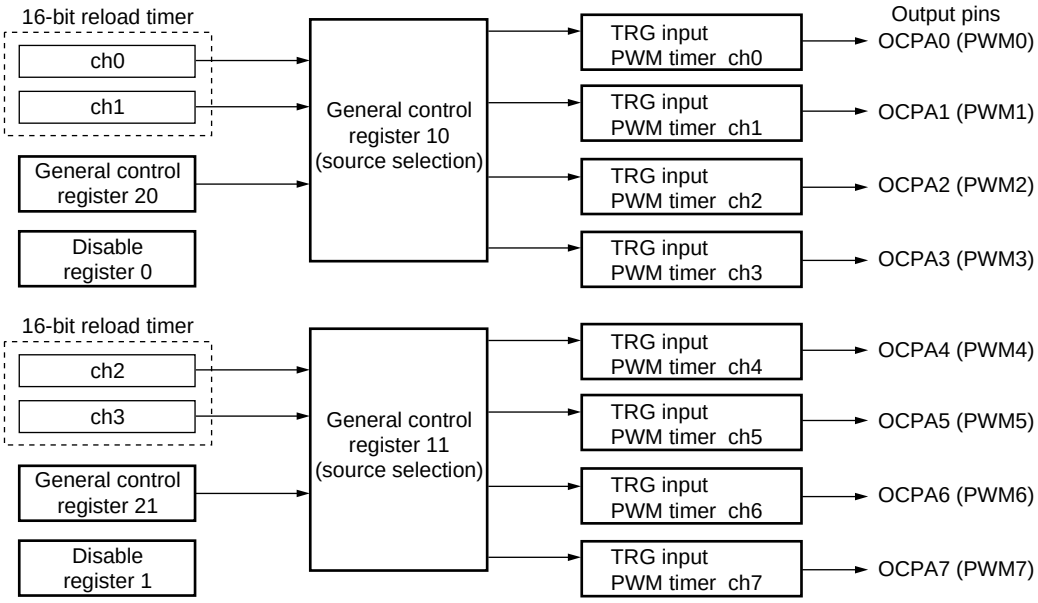
12.7.2 Register Configuration for ch 0 to ch 3

Address	Bits 15 8 7 0	Access	Register name
00000118H	GCN10	R/W	General control register 10
0000011AH	PDBL0 / GCN20	R/W	Disable/General control register 20
PWM timer ch 0			
00000120H	PTMR0	R	ch0 timer register
00000122H	PCSR0	W	ch0 cycle setting register
00000124H	PDUT0	W	ch0 duty setting register
00000126H	PCNH0 / PCNL0	R/W	ch0 control status registers
PWM timer ch 1			
00000128H	PTMR1	R	ch1 timer register
0000012AH	PCSR1	W	ch1 cycle setting register
0000012CH	PDUT1	W	ch1 duty setting register
0000012EH	PCNH1 / PCNL1	R/W	ch1 control status registers
PWM timer ch 2			
00000130H	PTMR2	R	ch2 timer register
00000132H	PCSR2	W	ch2 cycle setting register
00000134H	PDUT2	W	ch2 duty setting register
00000136H	PCNH2 / PCNL2	R/W	ch2 control status registers
PWM timer ch 3			
00000138H	PTMR3	R	ch3 timer register
0000013AH	PCSR3	W	ch3 cycle setting register
0000013CH	PDUT3	W	ch3 duty setting register
0000013EH	PCNH3 / PCNL3	R/W	ch3 control status registers

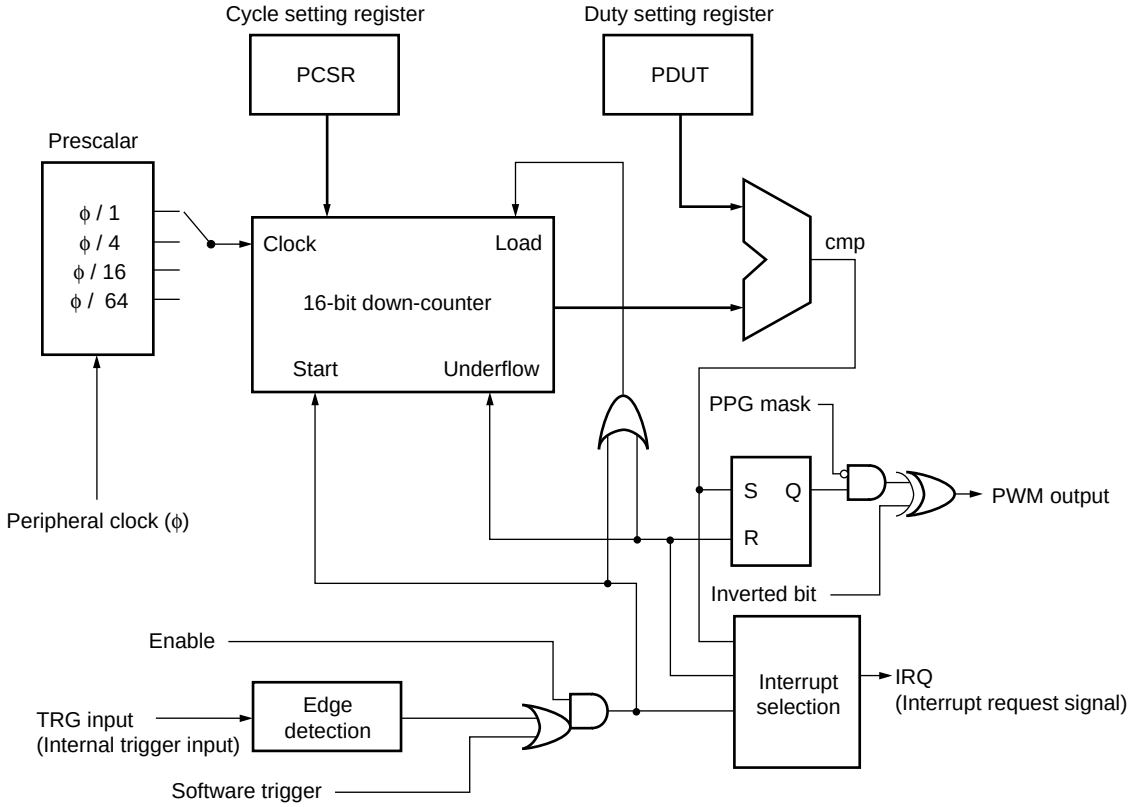
12.7.3 PWM Timer Registers for ch 4 to ch 7

Address	Bits 15 8 7 0	Access	Register name
0000011CH	GCN11	R/W	General control register 11
0000011EH	PDBL1 | GCN21	R/W	Disable/General control register 21
PWM timer ch 4			
00000140H	PTMR4	R	ch4 timer register
00000142H	PCSR4	W	ch4 cycle setting register
00000144H	PDUT4	W	ch4 duty setting register
00000146H	PCNH4 | PCNL4	R/W	ch4 control status registers
PWM timer ch 5			
00000148H	PTMR5	R	ch5 timer register
0000014AH	PCSR5	W	ch5 cycle setting register
0000014CH	PDUT5	W	ch5 duty setting register
0000014EH	PCNH5 | PCNL5	R/W	ch5 control status registers
PWM timer ch 6			
00000150H	PTMR6	R	ch6 timer register
00000152H	PCSR6	W	ch6 cycle setting register
00000154H	PDUT6	W	ch6 duty setting register
00000156H	PCNH6 | PCNL6	R/W	ch6 control status registers
PWM timer ch 7			
00000158H	PTMR7	R	ch7 timer register
0000015AH	PCSR7	W	ch7 cycle setting register
0000015CH	PDUT7	W	ch7 duty setting register
0000015EH	PCNH7 | PCNL7	R/W	ch7 control status registers

12.7.4 Configuration Diagram of the Entire PWM Timer



12.7.5 Configuration Diagram of PWM Timer 1 ch



12.8 16-bit Reload Timer

Each 16-bit reload timer consists of a 16-bit down-counter, a 16-bit reload register, a prescaler for generating the internal count clock, and a control register.

The 16-bit reload timer can also activate DMA transfer using interrupts.

The CY91360G series contains six 16-bit reload timer channels.

12.8.1 16-bit Reload Timer Register Configuration

Control status register (TMCSR)

15	14	13	12	11	10	9	8
—	—	—	—	CSL1	CSL0	—	—

7	6	5	4	3	2	1	0
—	—	—	RELD	INTE	UF	CNTE	TRG

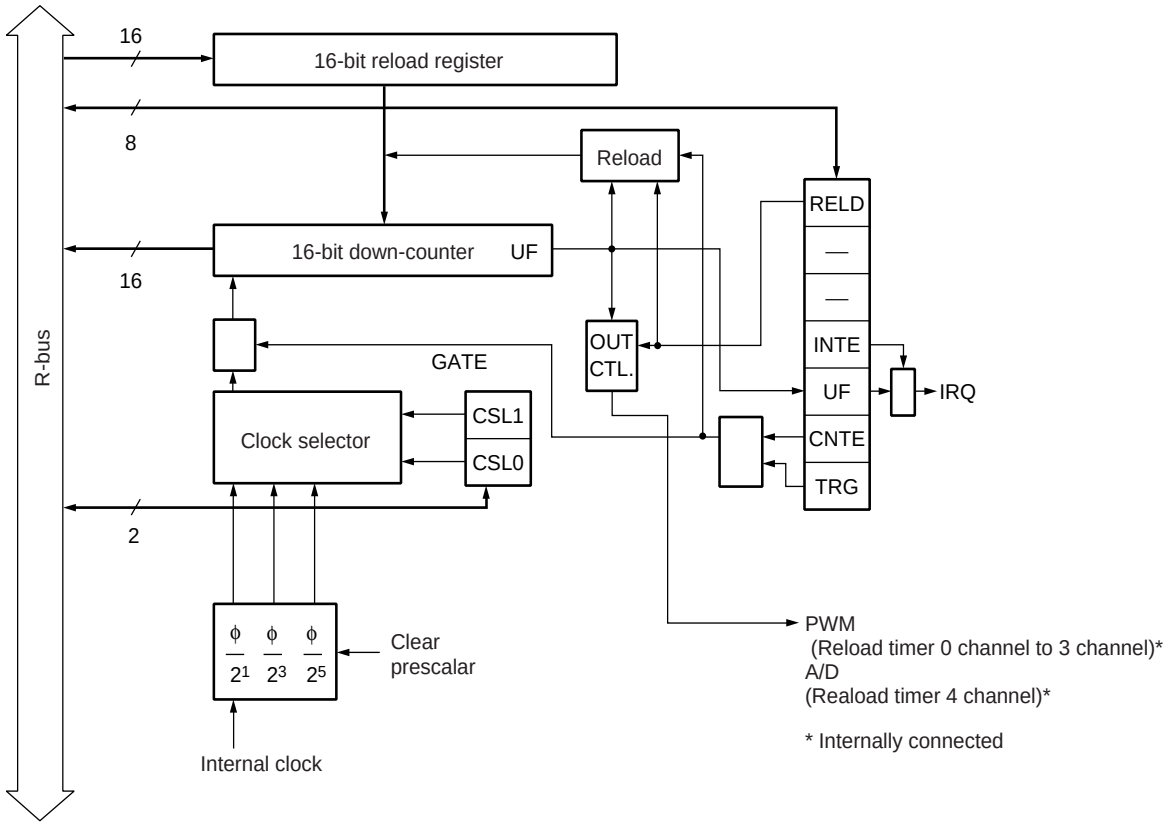
16-bit timer register (TMR)

15	0

16-bit reload register (TMRLR)

15	0

12.8.2 Block Diagram



12.9 Bit Search Module

The bit search module searches for a “0”, “1”, or change-point in the data written to the input register and returns the position of the detected bit.

This section describes the data register for detecting zeros (BSD0), data register for detecting ones (BSD1), data register for detecting change-points (BSDC), and detection result register (BSRR).

a: **Data register for detecting zeros** (**BSD0**)

Address	31 Register structure 0	Initial value	Access
0000 03F0H		Indeterminate	W

b: **Date register for detecting ones** (**BSD1**)

Address	31 Register structure 0	Initial value	Access
0000 03F4H		Indeterminate	R/W

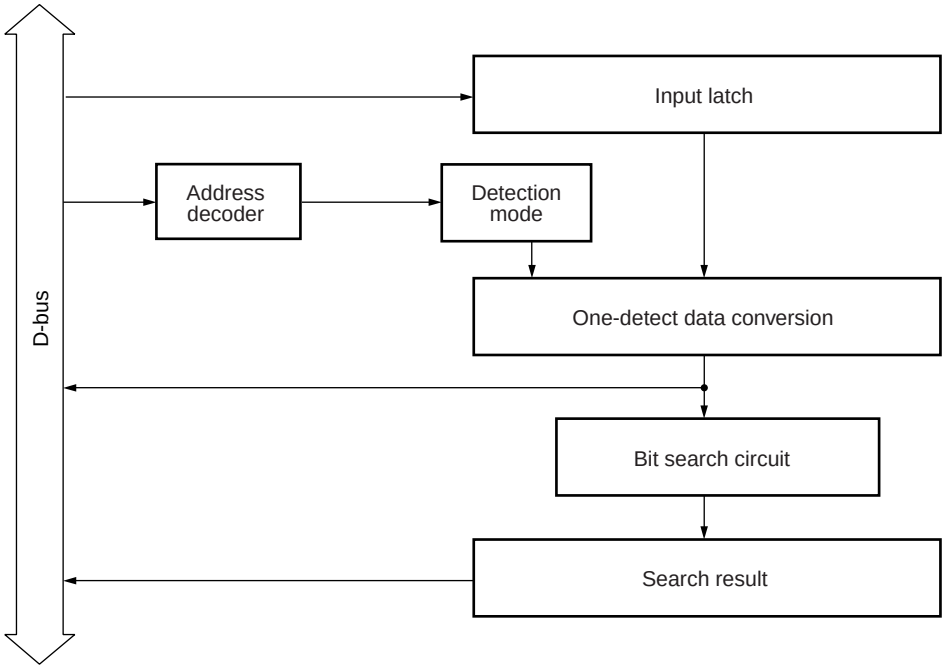
c: **Data register for detecting change points** (**BSDC**)

Address	31 Register structure 0	Initial value	Access
0000 03F8H		Indeterminate	W

d: **Detection Result Register** (**BSRR**)

Address	31 Register structure 0	Initial value	Access
0000 03FCH		Indeterminate	R

12.9.1 Block Diagram of the Bit Search Module

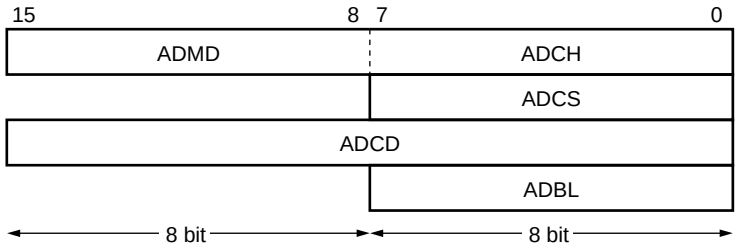


12.10 10-bit A/D Converter (Successive Approximation Conversion Type)

This section provides an overview of the A/D converter, describes the register structure and functions, and describes the operation of the A/D converter.

A/D Converter converts analog input voltage into digital values, and provides the following features.

- Conversion time: minimum 178 cycles (32 MHz: 5.6 μs, 24 MHz: 7.4 μs, 16 MHz: 11.2 μs) per channel
- RC type successive approximation conversion with sample & hold circuit
- 10-bit resolution
- Program selection analog input from 16 channels
  - Single conversion mode: conversion of one selected channel
  - Scan conversion mode: continuous conversion of multiple channels, programmable for up to 16 channels
  - Single conversion mode: Convert the specified channel once only.
- Continuous mode: Repeatedly convert the specified channels.
- Stop mode: Convert one channel then temporarily halt until the next activation. (Enables synchronization of the conversion start timing.)
- A/D conversion can be followed by an A/D conversion interrupt request to CPU. This interrupt, an option that is ideal for continuous processing can be used to start a DMA transfer of the results of A/D conversion to memory.
- Startup may be by software, external trigger (falling edge) or timer (rising edge)



Channel setting register (ADCH)

bit	7	6	5	4	3	2	1	0
Address: 00009D$_H$	ANS3	ANS2	ANS1	ANS0	ANE3	ANE2	ANE1	ANE0

Mode register (ADMD)

bit	15	14	13	12	11	10	9	8
Address: 00009C$_H$	—	—	—	—	MOD1	MOD0	STS1	STS0

Control status register (ADCS)

bit	7	6	5	4	3	2	1	0
Address: 00009F$_H$	BUSY	INT	INTE	PAUS	—	—	STRT	Reserved

Data register (ADCD)

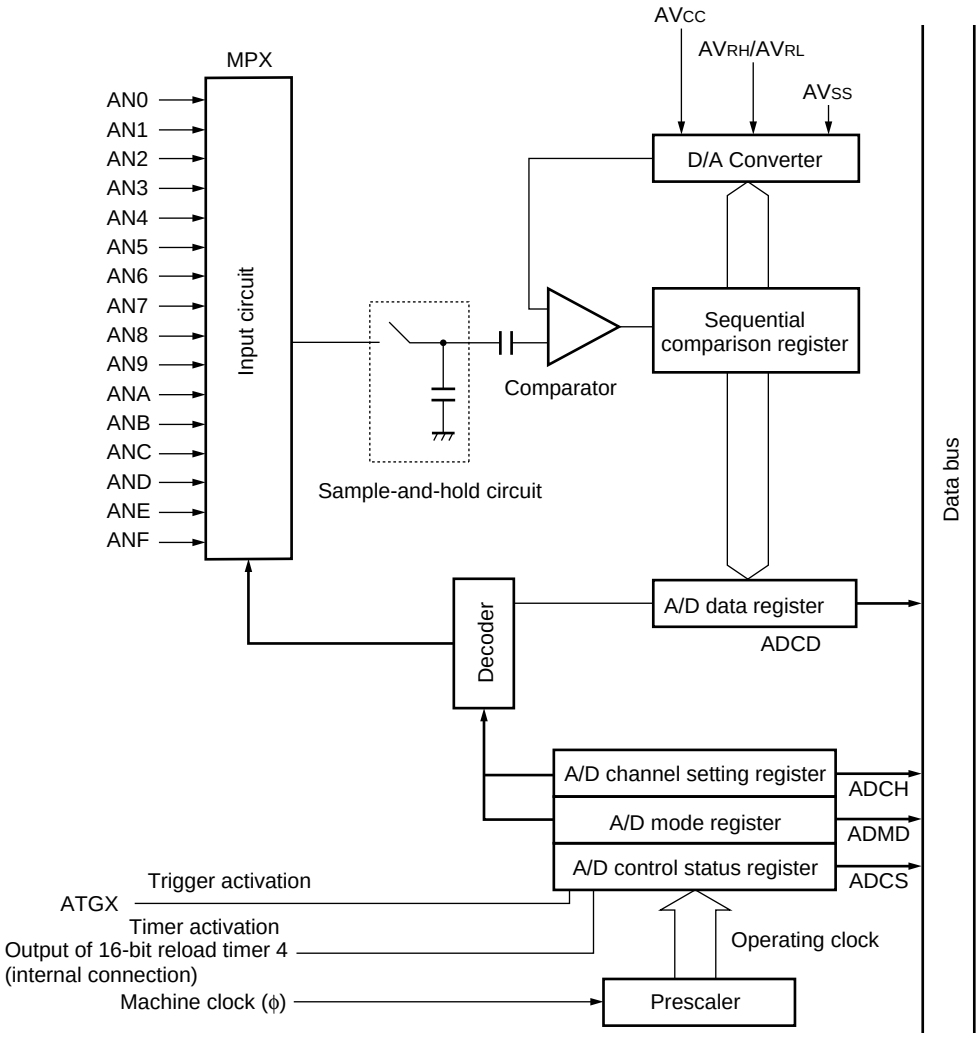
bit	7	6	5	4	3	2	1	0
Address: 0000A1$_H$	D7	D6	D5	D4	D3	D2	D1	D0

bit	15	14	13	12	11	10	9	8
Address: 0000A0$_H$	—	—	—	—	—	—	D9	D8

Disable register (ADBL)

bit	15	14	13	12	11	10	9	8
Address: 0000A3$_H$	—	—	—	—	—	—	—	DBL

12.10.1 Block Diagram



12.11 Interrupt Controller

An interrupt controller controls interrupt acceptance and arbitration processing.

Hardware Configuration

This module consists of the following:

- ICR register
- Interrupt priority evaluation circuit
- Interrupt level and interrupt number (vector) generator
- Hold request cancel request generator

Major Functions

This module has the following major functions:

- Detecting an NMI request or interrupt request
- Priority evaluation (using the level or number)
- Transferring the level of the interrupt cause in the evaluation result (to the CPU)
- Transferring the number of the interrupt cause in the evaluation result (to the CPU)
- Instructing recovery from stop mode due to an NMI or interrupt level other than 11111 (to the CPU)
- Generating a hold request cancel request for the bus master

12.11.1 Register Configuration

		bit 7	6	5	4	3	2	1	0	
Address:	00000440H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR00
Address:	00000441H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR01
Address:	00000442H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR02
Address:	00000443H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR03
Address:	00000444H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR04
Address:	00000445H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR05
Address:	00000446H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR06
Address:	00000447H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR07
Address:	00000448H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR08
Address:	00000449H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR09
Address:	0000044AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR10
Address:	0000044BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR11
Address:	0000044CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR12
Address:	0000044DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR13
Address:	0000044EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR14
Address:	0000044FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR15
Address:	00000450H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR16
Address:	00000451H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR17
Address:	00000452H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR18
Address:	00000453H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR19
Address:	00000454H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR20
Address:	00000455H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR21
Address:	00000456H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR22
Address:	00000457H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR23
Address:	00000458H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR24
Address:	00000459H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR25
Address:	0000045AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR26
Address:	0000045BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR27
Address:	0000045CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR28
Address:	0000045DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR29
Address:	0000045EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR30
Address:	0000045FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR31
					R	R/W	R/W	R/W	R/W	

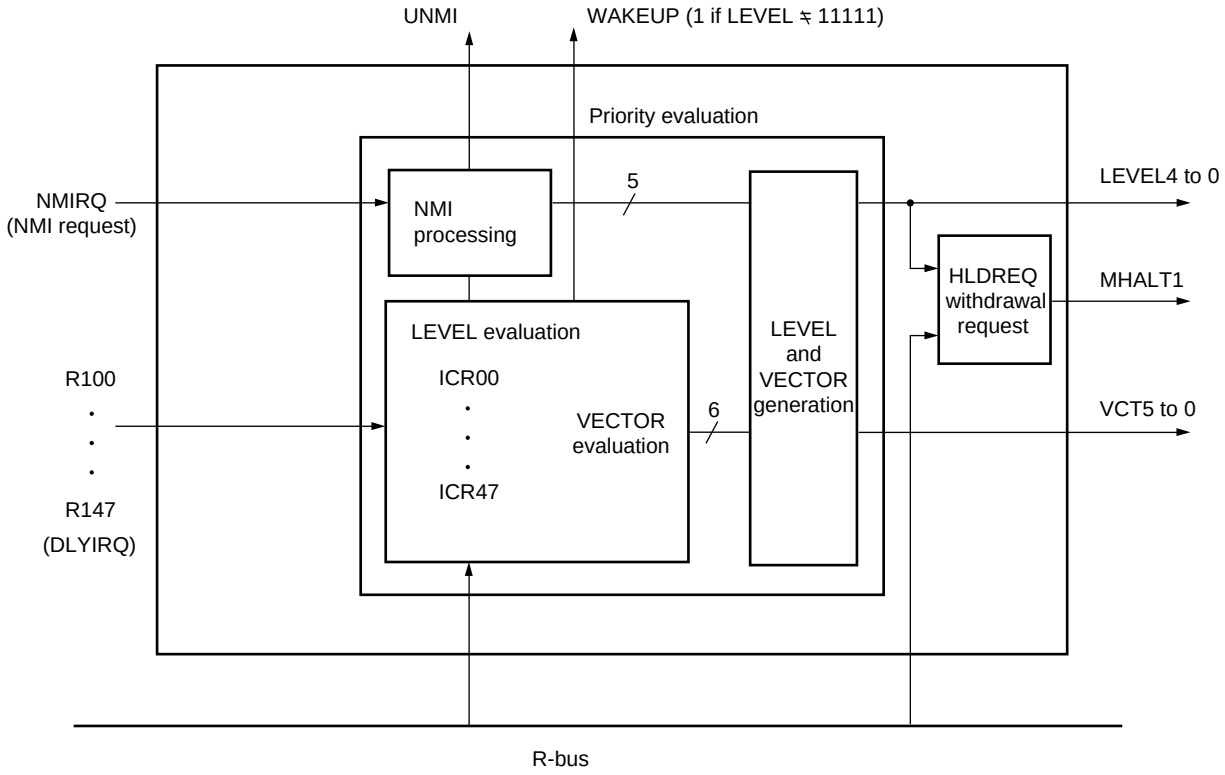
(Continued)

(Continued)

	bit 7	6	5	4	3	2	1	0	
Address: 00000460H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR32
Address: 00000461H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR33
Address: 00000462H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR34
Address: 00000463H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR35
Address: 00000464H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR36
Address: 00000465H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR37
Address: 00000466H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR38
Address: 00000467H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR39
Address: 00000468H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR40
Address: 00000469H	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR41
Address: 0000046AH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR42
Address: 0000046BH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR43
Address: 0000046CH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR44
Address: 0000046DH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR45
Address: 0000046EH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR46
Address: 0000046FH	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR47
				R	R/W	R/W	R/W	R/W	

Address: 00000045H	MHALTI	—	—	LVL4	LVL3	LVL2	LVL1	LVL0	HRCL
	R/W			R	R/W	R/W	R/W	R/W	

12.11.2 Block Diagram



12.12 External Interrupt/NMI Control Block

The external interrupt/NMI controller controls external interrupt requests input from the NMIX and INT0 to INT7 pins.
Detection of “H” levels, “L” levels, rising edges, or falling edges can be selected (except for the NMI).
The external interrupt/NMI controller can also be used for DMA requests.
This section lists the registers of the controller and provides its block diagram.

12.12.1 Register Configuration of the External Interrupt NMI Controller

External interruption permission register (ENIR)

Bit	7	6	5	4	3	2	1	0
	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0

External interruption factors register (EIRR)

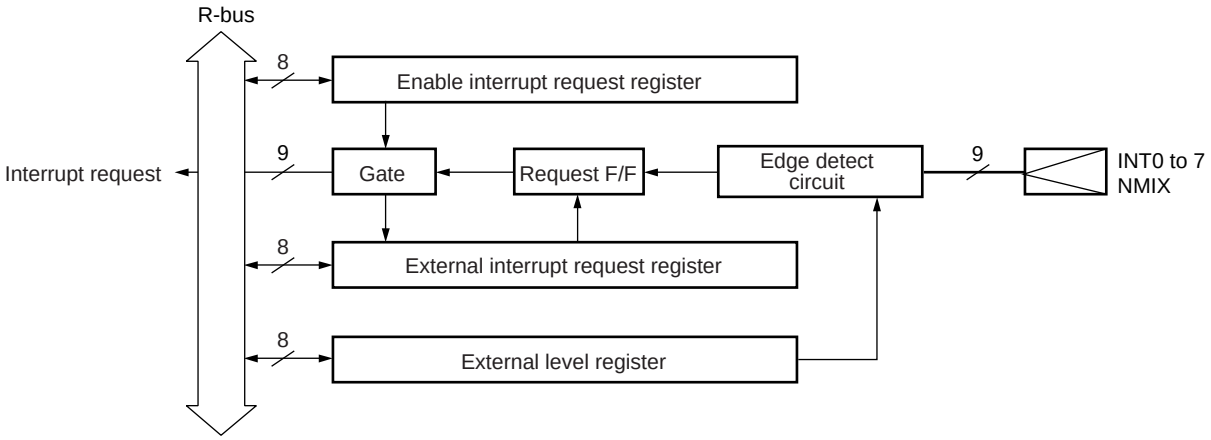
Bit	15	14	13	12	11	10	9	8
	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0

Request level setting register (ELVR)

Bit	15	14	13	12	11	10	9	8
	LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4

Bit	7	6	5	4	3	2	1	0
	LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0

12.12.2 Block Diagram



12.13 Delayed Interrupt

12.13.1 Delayed interrupt control register (DICR)

The delayed interrupt control register (DICR) is a delayed interrupt generator register and is used to generate the task switching interrupt.

Structure of the DICR

Address	Bits	7	6	5	4	3	2	1	0	Initial value
00000044H		—	—	—	—	—	—	—	DLYI	- - - - - - - 0
									R/W	← Access

12.14 Clock Generation

The CY91360G series generates internal operating clocks as follows:

- Base clock generation: Device scales clock source input by 2 (X clock) or oscillates base clock with PLL to generate basic clock (PLL clock)
- Generation of each internal clock: Device scales base clock to generate clocks supplied to each block

Generation and control of each clock are explained below.

Some devices allow the operation of the RTC module based on a separate 32 kHz subclock. See the section “27. Subclock” for more details.

12.14.1 Register Configuration

RSRR: Reset source register, Watchdog timer control register

bit	15	14	13	12	11	10	9	8
address: 00000480H	INIT	HSTB	WDOG	ERST	SRST	—	WT1	WT0
access	R	R	R	R	R	—	R/W	R/W
Initial Value (INITX)	1	0	0	0	0	—	0	0
Initial Value (INIT)	*	*	*	X	X	—	0	0
Initial Value (RST)	X	X	X	*	*	—	0	0
After Boot ROM **	0	0	0	0	0	0	0	0

*: varies with reset factor
x: not initialized

**: After execution of the program in the internal boot ROM the reset source is visible

STCR: Standby control register

bit	7	6	5	4	3	2	1	0
address: 00000481H	STOP	SLEEP	HIZ	SRST	OS1	OS0	OSCD2	OSCD1
access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (INITX)	0	0	1	1	0	0	1	1
Initial Value (HSTX) *	0	0	1	1	1	1	1	1
Initial Value (INIT)	0	0	1	1	X	X	1	1
Initial Value (RST)	0	0	X	1	X	X	X	X

*: Valid only when this initialization is performed simultaneously with initialization by INITX: others same as INIT.

(Continued)

TBCR: **Time-based counter control register**

bit	15	14	13	12	11	10	9	8
address: 00000482H	TBIF	TBIE	TBC2	TBC1	TBC0	—	SYNCR	SYNCS
Initial Value (INIT)	0	0	X	X	X	X	0	0
Initial Value (RST)	0	0	X	X	X	X	X	X
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CTBR: **Time-based counter clear register**

bit	7	6	5	4	3	2	1	0
address: 00000483H	D7	D6	D5	D4	D3	D2	D1	D0
Initial Value (INIT)	X	X	X	X	X	X	X	X
Initial Value (RST)	X	X	X	X	X	X	X	X
	W	W	W	W	W	W	W	W

CLKR: **Clock source control register**

bit	15	14	13	12	11	10	9	8
address: 00000484H	PLL2S0	PLL1S2	PLL1S1	PLL1S0	PLL2EN	PLL1EN	CLKS1	CLKS0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (INIT)	0	0	0	0	0	0	0	0
Initial Value (RST)	X	X	X	X	X	X	X	X

WPR Watchdog reset generation postponement register

bit	7	6	5	4	3	2	1	0
address: 00000485H	D7	D6	D5	D4	D3	D2	D1	D0
	W	W	W	W	W	W	W	W
Initial Value (INIT)	X	X	X	X	X	X	X	X
Initial Value (RST)	X	X	X	X	X	X	X	X

DIVR0: **Base clock division setting register 0**

bit	7	6	5	4	3	2	1	0
address: 00000486H	B3	B2	B1	B0	P3	P2	P1	P0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (INIT)	0	0	0	0	0	0	1	1
Initial Value (RST)	X	X	X	X	X	X	X	X

DIVR1: **Base clock division setting register 1**

bit	7	6	5	4	3	2	1	0
address: 00000487H	T3	T2	T1	T0	S3	S2	S1	S0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial Value (INIT)	0	0	0	0	0	0	0	0
Initial Value (RST)	X	X	X	X	X	X	X	X

(Continued)

(Continued)

CMCR: Clock control for CAN modules

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	initial
0164H	PRE7	PRE6	PRE5	PRE4	PRE3	PRE2	PRE1	PRE0	11111111
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	1	1	1	1	1	1	1	1	

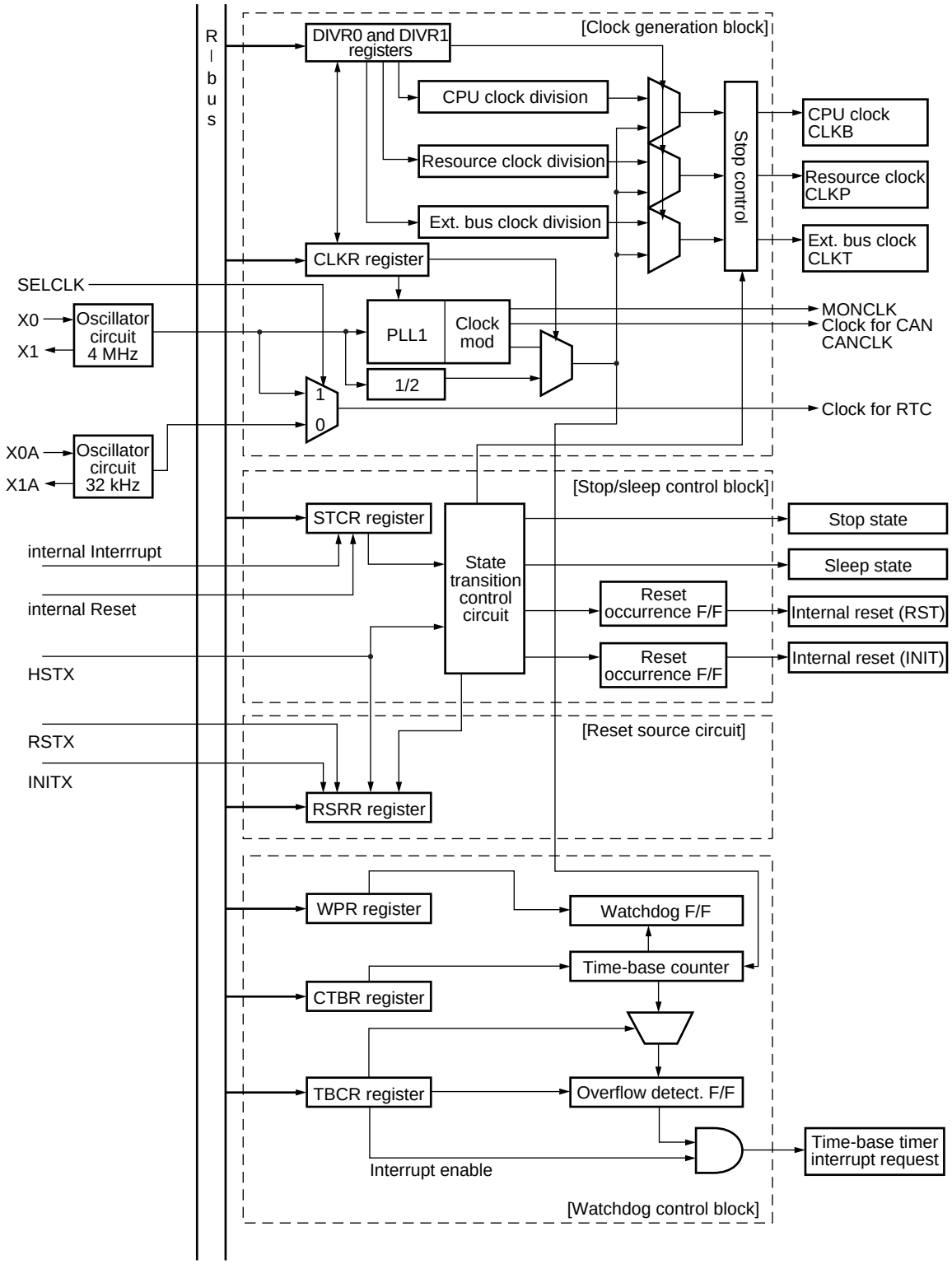
address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	initial
0165H	PRES	CDSELE	IRNG	CAL	MSEL	MTST	SCLK	MSRT	00000000
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	0	0	0	0	0	0	0	0	

Subclock RTC32 (CLKR2)

This register is used to control the RTC32 mode bit for use in subclock system.

address	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
000046H	—	—	—	—	—	—	—	RTC32
access	—	—	—	—	—	R/W	R/W	R/W
initial value	—	—	—	—	—	0	0	0

12.14.2 Block Diagram



12.15 Bus Interface

The external bus interface controls the interfaces with the external memory and external I/Os.

- Up to 32-bit (4 GB) address output.
- Up to eight independent banks provided by chip-select function

  The banks can be set in 64-KB (minimum) at any position in the logic address space.
  Can be set to no area
- 32/16/8 bit bus width setup can be performed for each chip-select area.
- Programmable automatic memory wait (up to 7 cycles) insertion
- Unused address/data pins can be used as I/O ports. (But see notes below)

Note: Chip Select Area CS7 is used for the internal CAN modules. The necessary register settings are done by an internal boot routine. Take care not to overwrite register bits related to this CS area.
If the CAN macros which are connected internally to the external bus (also called User Logic Bus) are used, a certain number of data, address and control ports of the external bus interface cannot be configured as general purpose I/O ports.

12.15.1 Register Configuration

Area select registers (ASR0 to ASR7)

	15	14	13	12 ...	2	1	0	Initial value INIT	Initial value RST	Access
ASR0 00000640H	A31	A30	A29	... ...	A18	A17	A16	0000H	0000H	W
ASR1 00000644H	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
ASR2 00000648H	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
ASR3 0000064CH	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
ASR4 00000650H	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
ASR5 00000654H	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
ASR6 00000658H	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
ASR7 0000065CH	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W

Note: After execution of the code in the initial boot ROM ASR0 is set to “0x20”, and ASR7 to “0x10”.

(Continued)

(Continued)

Area mask register (**AMR0** to **AMR7**)

	15	14	13	12 ...	2	1	0	Initial value INIT	Initial value RST	Access
AMR0 00000642H	A31	A30	A29	... ...	A18	A17	A16	FFFFH	FFFFH	W
AMR1 00000646H	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
AMR2 0000064AH	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
AMR3 0000064EH	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
AMR4 0000652H	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
AMR5 00000656H	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
AMR6 0000065AH	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W
AMR7 0000065EH	A31	A30	A29	... ...	A18	A17	A16	0000H	XXXXH	W

Area mode registers (**AMD0** to **AMD7**)

	7	6	5	4	3	2	1	0	INIT	RST	
00000660H 00000661H 00000662H to 00000667H	—	—	RDYE	BW1	BW0	WTC2	WTC1	WTC0	-0000111B -0000000B --000000B to --000000B	-00XX111B -XXXXXXXB --XXXXXXB to --XXXXXXB	R/W

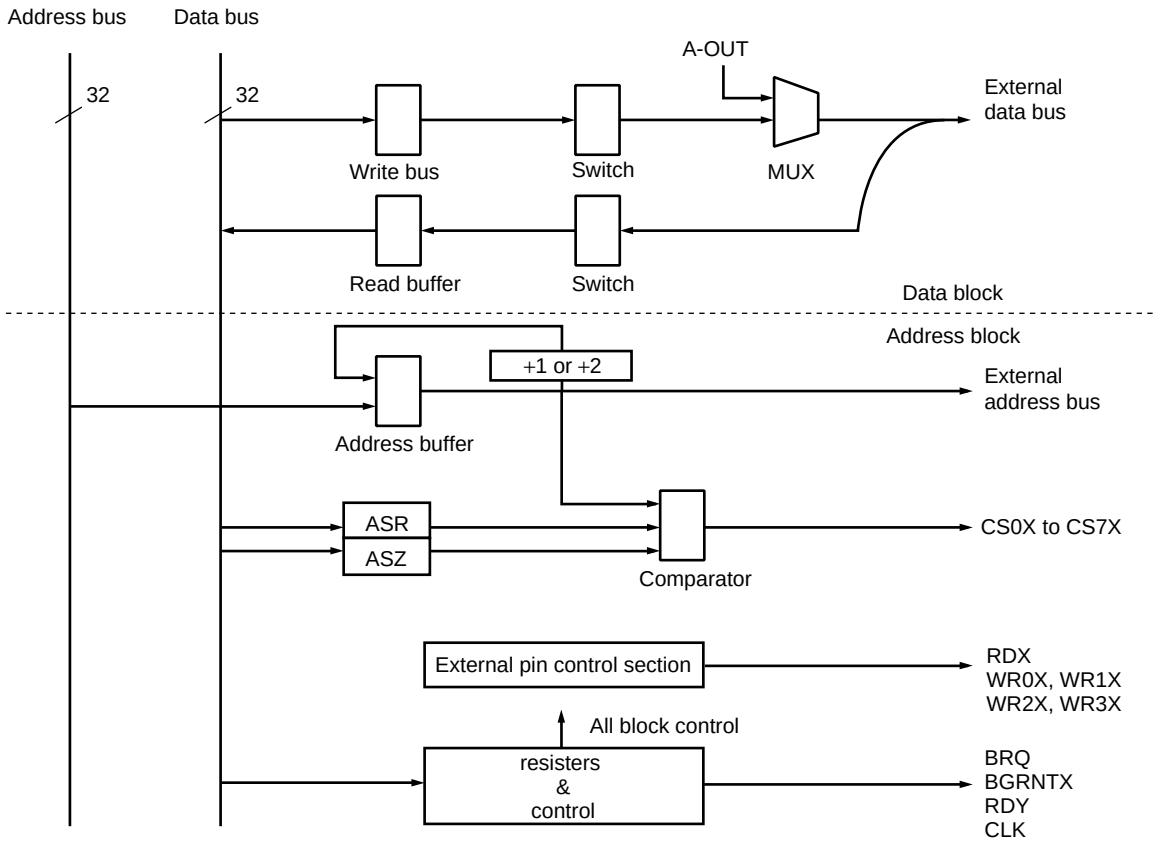
CHE (**CacHe Enable register**)

	7	6	5	4	3	2	1	0		
00000670H	CHE7	CHE6	CHE5	CHE4	CHE3	CHE2	CHE1	CHE0	11111111B	R/W

CSE (**Chip Select Enable register**)

	7	6	5	4	3	2	1	0		
00000668H	CSE7	CSE6	CSE5	CSE4	CSE3	CSE2	CSE1	CSE0	00000001B	R/W

12.15.2 Block Diagram



12.16 CAN Controller

This section provides an overview of the CAN Interface, describes the register structure and functions, and describes the operation of the CAN Interface.

The CAN controller is a module built into a CY91360G series. The CAN (Controller Area Network) is the standard protocol for serial communication between automobile controllers and is widely used in industrial applications.

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - Supports transmission/reception in standard frame and extended frame formats
- Supports transmitting of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Supports full-bit comparison, full-bit mask and partial bit mask filtering.
  - Two acceptance mask registers in either standard frame format or extended frame formats
- Bit rate programmable from 10 Kbits/s to 1 Mbits/s (when input clock is at 16 MHz)

The following sections only describe CAN 0. For the addresses of the registers of the other CAN channels see the I/O map.

The address shown assume that the CS7 area is defined as described in the chapter about the internal Boot ROM.

12.16.1 List of Control Registers

Table 12-1. List of Control Registers

Address CAN0	Register	Abbreviation	Access	Initial Value
100000H	Message buffer valid register	BVALR0	R/W	00000000 00000000
100001H				
100002H	Transmit request register	TREQR0	R/W	00000000 00000000
100003H				
100004H	Transmit cancel register	TCANR0	W	00000000 00000000
100005H				
100006H	Transmit complete register	TCR0	R/W	00000000 00000000
100007H				
100008H	Receive complete register	RCR0	R/W	00000000 00000000
100009H				
10000AH	Remote request receiving register	RRTRR0	R/W	00000000 00000000
10000BH				
10000CH	Receive overrun register	ROVRR0	R/W	00000000 00000000
10000DH				
10000EH	Receive interrupt enable register	RIER0	R/W	00000000 00000000
10000FH				
100010H	Control status register	CSR0	R/W, R	00---000 0----0-1
100011H				
100012H	Last event indicator register	LEIR0	R/W	-------- 000-0000
100013H				

Table 12-1. List of Control Registers *(continued)*

Address CAN0	Register	Abbreviation	Access	Initial Value
100014H	Receive/transmit error counter	RTEC0	R	00000000 00000000
100015H				
100016H	Bit timing register	BTR0	R/W	-1111111 11111111
100017H				
100018H	IDE register	IDER0	R/W	XXXXXXXX XXXXXXXX
100019H				
10001AH	Transmit RTR register	TRTRR0	R/W	00000000 00000000
10001BH				
10001CH	Remote frame receive waiting register	RFWTR0	R/W	XXXXXXXX XXXXXXXX
10001DH				
10001EH	Transmit interrupt enable register	TIER0	R/W	00000000 00000000
10001FH				
100020H	Acceptance mask select register	AMSR0	R/W	XXXXXXXX XXXXXXXX
100021H				
100022H				XXXXXXXX XXXXXXXX
100023H				
100024H	Acceptance mask register 0	AMR00	R/W	XXXXXXXX XXXXXXXX
100025H				
100026H				XXXXX - - - XXXXXXXX
100027H				
100028H	Acceptance mask register 1	AMR10	R/W	XXXXXXXX XXXXXXXX
100029H				
10002AH				XXXXX - - - XXXXXXXX
10002BH				

12.16.2 Message Buffers

Table 12-2. List of Message Buffers (ID Registers)

Address CAN0	Register	Abbreviation	Access	Initial Value
10002CH to 10004BH	General-purpose RAM	–	R/W	XXXXXXXX to XXXXXXXX
10004CH	ID register 0	IDR00	R/W	XXXXXXXX XXXXXXXX
10004DH				
10004EH				XXXXX - - - XXXXXXXX
10004FH				

Table 12-2. List of Message Buffers (ID Registers) *(continued)*

Address CAN0	Register	Abbreviation	Access	Initial Value
100050H	ID register 1	IDR10	R/W	XXXXXXXX XXXXXXXX
100051H				
100052H				XXXXX--- XXXXXXXX
100053H				
100054H	ID register 2	IDR20	R/W	XXXXXXXX XXXXXXXX
100055H				
100056H				XXXXX--- XXXXXXXX
100057H				
100058H	ID register 3	IDR30	R/W	XXXXXXXX XXXXXXXX
100059H				
10005AH				XXXXX--- XXXXXXXX
10005BH				
10005CH	ID register 4	IDR40	R/W	XXXXXXXX XXXXXXXX
10005DH				
10005EH				XXXXX--- XXXXXXXX
10005FH				
100060H	ID register 5	IDR50	R/W	XXXXXXXX XXXXXXXX
100061H				
100062H				XXXXX--- XXXXXXXX
100063H				
100064H	ID register 6	IDR60	R/W	XXXXXXXX XXXXXXXX
100065H				
100066H				XXXXX--- XXXXXXXX
100067H				
100068H	ID register 7	IDR70	R/W	XXXXXXXX XXXXXXXX
100069H				
10006AH				XXXXX--- XXXXXXXX
10006BH				
10006CH	ID register 8	IDR80	R/W	XXXXXXXX XXXXXXXX
10006DH				
10006EH				XXXXX--- XXXXXXXX
10006FH				
100070H	ID register 9	IDR90	R/W	XXXXXXXX XXXXXXXX
100071H				
100072H				XXXXX--- XXXXXXXX
100073H				

Table 12-2. List of Message Buffers (ID Registers) *(continued)*

Address CAN0	Register	Abbreviation	Access	Initial Value
100074H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXX
100075H				
100076H				XXXXX--- XXXXXXXX
100077H				
100078H	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXX
100079H				
10007AH				XXXXX--- XXXXXXXX
10007BH				
10007CH	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXX
10007DH				
10007EH				XXXXX--- XXXXXXXX
10007FH				
100080H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXX
100081H				
100082H				XXXXX--- XXXXXXXX
100083H				
100084H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXX
100085H				
100086H				XXXXX--- XXXXXXXX
100087H				
100088H	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXX
100089H				
10008AH				XXXXX--- XXXXXXXX
10008BH				

Table 12-3. List of Message Buffers (DLC Registers and Data Registers)

Address CAN0	Register	Abbreviation	Access	Initial Value
10008CH	DLC register 0	DLCR00	R/W	----XXXX
10008DH				
10008EH	DLC register 1	DLCR10	R/W	----XXXX
10008FH				
100090H	DLC register 2	DLCR20	R/W	----XXXX
100091H				
100092H	DLC register 3	DLCR30	R/W	----XXXX
100093H				
100094H	DLC register 4	DLCR40	R/W	----XXXX
100095H				

Table 12-3. List of Message Buffers (DLC Registers and Data Registers) *(continued)*

Address CAN0	Register	Abbreviation	Access	Initial Value
100096H	DLC register 5	DLCR50	R/W	----XXXX
100097H				
100098H	DLC register 6	DLCR60	R/W	----XXXX
100099H				
10009AH	DLC register 7	DLCR70	R/W	----XXXX
10009BH				
10009CH	DLC register 8	DLCR80	R/W	----XXXX
10009DH				
10009EH	DLC register 9	DLCR90	R/W	----XXXX
10009FH				
1000A0H	DLC register 10	DLCR100	R/W	----XXXX
1000A1H				
1000A2H	DLC register 11	DLCR110	R/W	----XXXX
1000A3H				
1000A4H	DLC register 12	DLCR120	R/W	----XXXX
1000A5H				
1000A6H	DLC register 13	DLCR130	R/W	----XXXX
1000A7H				
1000A8H	DLC register 14	DLCR140	R/W	----XXXX
1000A9H				
1000AAH	DLC register 15	DLCR150	R/W	----XXXX
1000ABH				
1000ACH to 1000B3H	Data register 0 (8 bytes)	DTR00	R/W	XXXXXXXX to XXXXXXXX
1000B4H to 1000BBH	Data register 1 (8 bytes)	DTR10	R/W	XXXXXXXX to XXXXXXXX
1000BCH to 1000C3H	Data register 2 (8 bytes)	DTR20	R/W	XXXXXXXX to XXXXXXXX
1000C4H to 1000CBH	Data register 3 (8 bytes)	DTR30	R/W	XXXXXXXX to XXXXXXXX
1000CCH to 1000D3H	Data register 4 (8 bytes)	DTR40	R/W	XXXXXXXX to XXXXXXXX
1000D4H to 1000DBH	Data register 5 (8 bytes)	DTR50	R/W	XXXXXXXX to XXXXXXXX
1000DCH to 1000E3H	Data register 6 (8 bytes)	DTR60	R/W	XXXXXXXX to XXXXXXXX

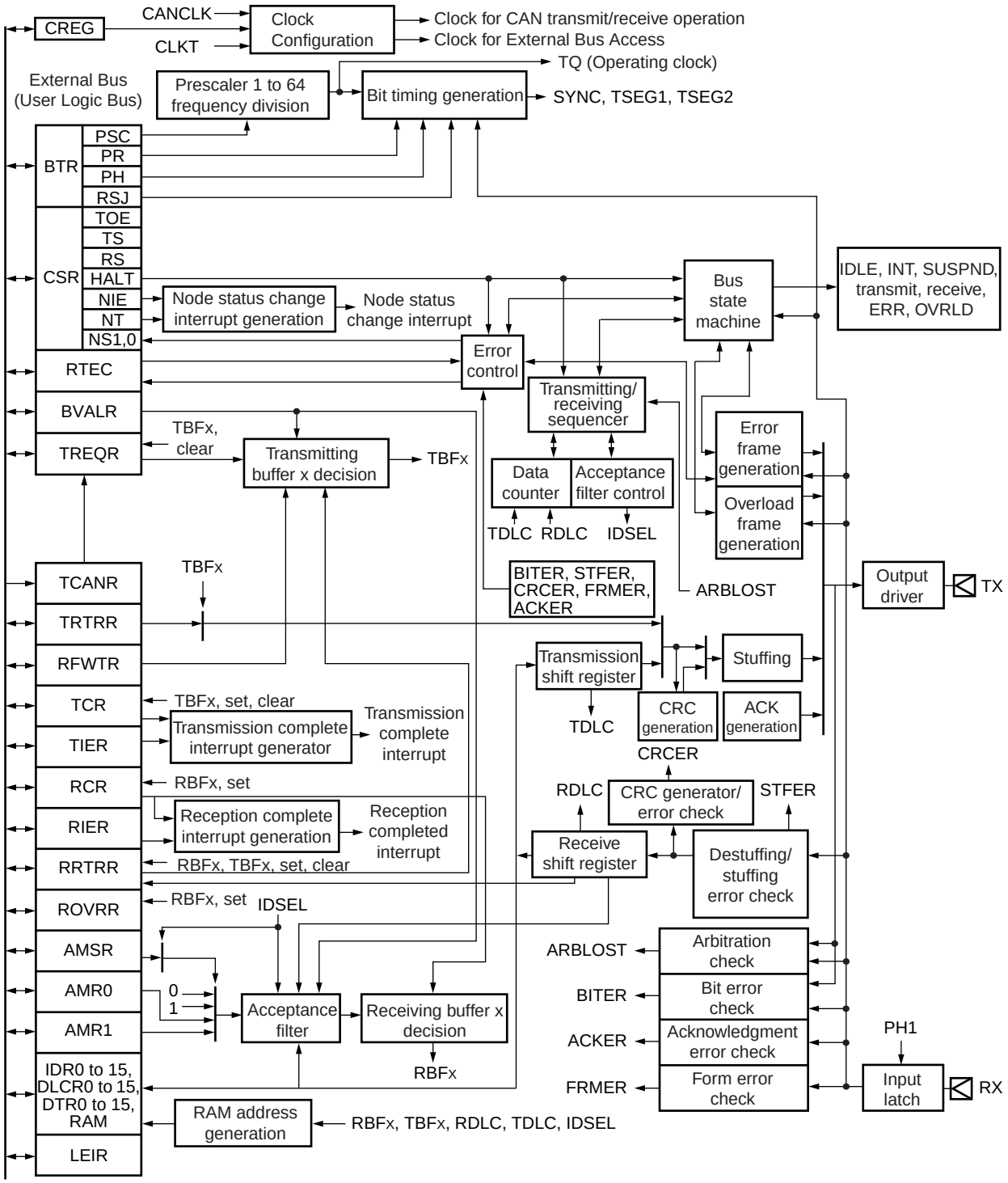
Table 12-3. List of Message Buffers (DLC Registers and Data Registers) *(continued)*

Address CAN0	Register	Abbreviation	Access	Initial Value
1000E4H to 1000EBH	Data register 7 (8 bytes)	DTR70	R/W	XXXXXXXX to XXXXXXXX
1000ECH to 1000F3H	Data register 8 (8 bytes)	DTR80	R/W	XXXXXXXX to XXXXXXXX
1000F4H to 1000FBH	Data register 9 (8 bytes)	DTR90	R/W	XXXXXXXX to XXXXXXXX
1000FCH to 100103H	Data register 10 (8 bytes)	DTR100	R/W	XXXXXXXX to XXXXXXXX
100104H to 10010BH	Data register 11 (8 bytes)	DTR110	R/W	XXXXXXXX to XXXXXXXX
10010CH to 100113H	Data register 12 (8 bytes)	DTR120	R/W	XXXXXXXX to XXXXXXXX
100114H to 10011BH	Data register 13 (8 bytes)	DTR130	R/W	XXXXXXXX to XXXXXXXX
10011CH to 100123H	Data register 14 (8 bytes)	DTR140	R/W	XXXXXXXX to XXXXXXXX
100124H to 10012BH	Data register 15 (8 bytes)	DTR150	R/W	XXXXXXXX to XXXXXXXX

Table 12-4. Configuration Register (CREG)

Address CAN0	Register	Abbreviation	Access	Initial Value
10012CH 10012DH	Configuration register	CREG0	R/W	00000000 00000110

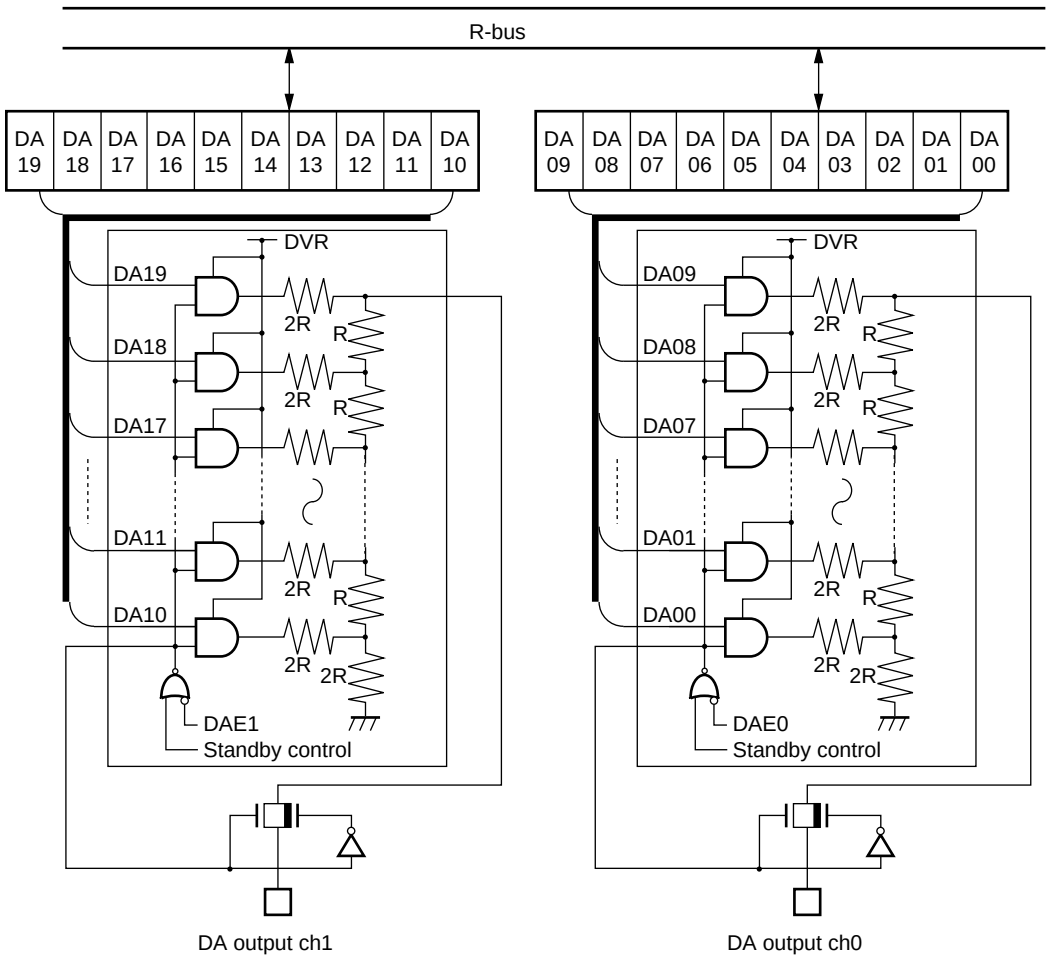
12.16.3 Block Diagram



12.17 D/A Converter

This section provides an overview of the D/A converter, describes the register structure and functions, and describes the operarton of D/A converter.This block is an R-2R format D/A converter, having ten-bit resolution. The D/A converter has two channels.Output control can be performed independently for the two channels using the D/A control register.

12.17.1 Block Diagram



12.17.2 Registers

D/A control register (DACR)

bit	7	6	5	4	3	2	1	0
Address: 0000A5H	—	—	—	—	—	MODE	DAE1	DAE0

D/A converter data register (ch 0) (DADR0)

bit	15	14	13	12	11	10	9	8
Address: 0000A6H	—	—	—	—	—	—	DA09	DA08

bit	7	6	5	4	3	2	1	0
Address: 0000A7H	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00

D/A converter data register (ch 1) (DADR1)

bit	15	14	13	12	11	10	9	8
Address: 0000A8H	—	—	—	—	—	—	DA19	DA18

bit	7	6	5	4	3	2	1	0
Address: 0000A9H	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10

D/A clock control (DDBL)

bit	7	6	5	4	3	2	1	0
Address: 0000ABH	—	—	—	—	—	—	—	DBL

12.18 400 kHz I²C Interface

This section describes the functions and operation of the fast I²C interface.

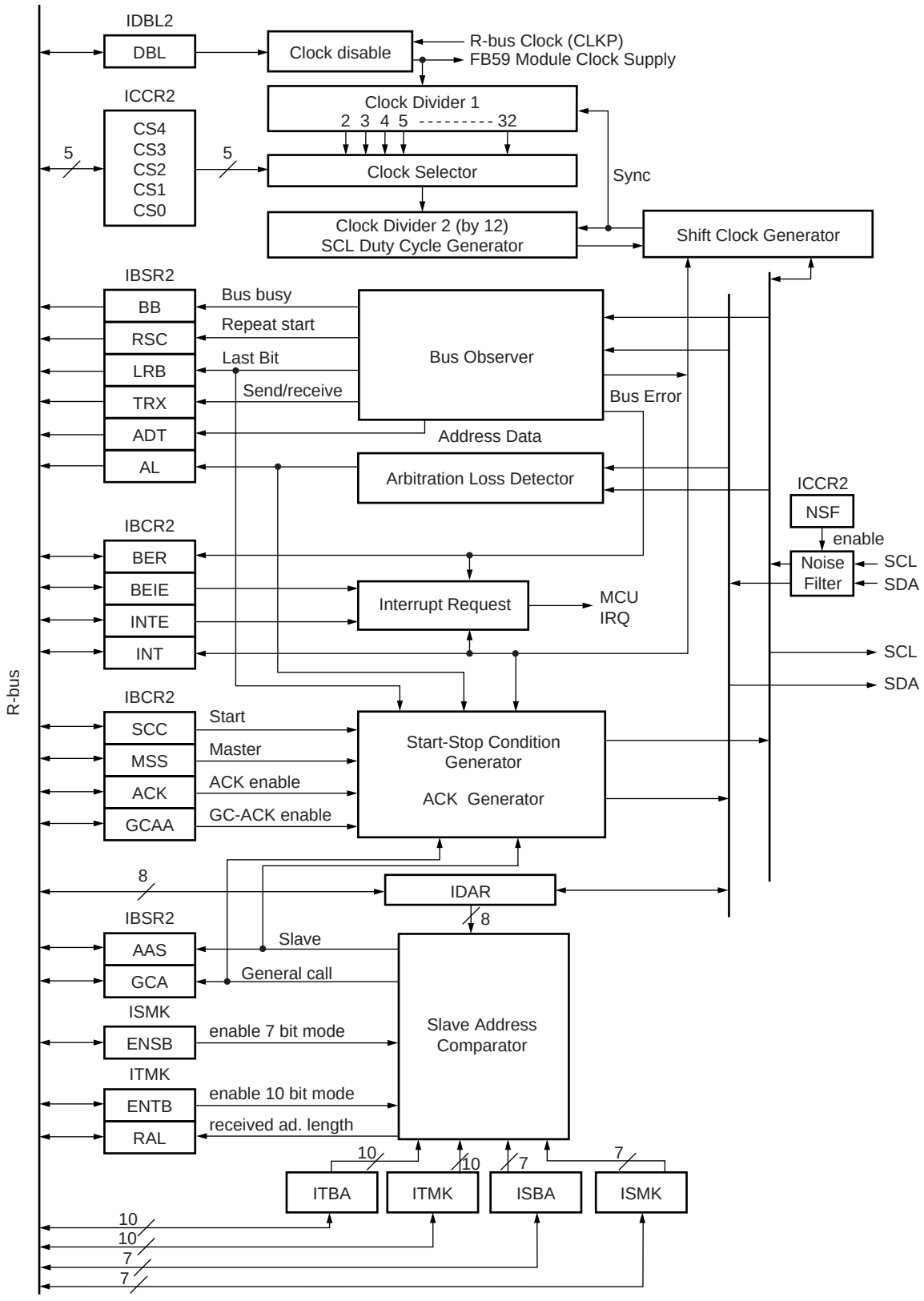
The I²C interface is a serial I/O port supporting the Inter IC bus, operating as a master/slave device on the I²C bus.

12.18.1 Features

- Master/slave transmitting and receiving functions
- Arbitration function
- Clock synchronization function
- General call addressing support
- Transfer direction detection function
- Repeated start condition generation and detection function
- Bus error detection function
- 7 bit addressing as master and slave
- 10 bit addressing as master and slave
- Possibility to give the interface a seven and a ten bit slave address
- Acknowledging upon slave address reception can be disabled (Master-only operation)
- Address masking to give interface several slave addresses (in 7 and 10 bit mode)
- Up to 400 KBit transfer rate
- Possibility to use built-in noise filters for SDA and SCL
- Can receive data at 400 KBit if R-bus-Clock is higher than 6 MHz regardless of prescaler setting
- Can generate MCU interrupts on transmission and bus error events
- Supports being slowed down by a slave on bit and byte level

The I²C interface does not support SCL clock stretching on bit level since it can receive the full 400 KBit datarate if the R-bus-Clock (CLKP) is higher than 6 MHz regardless of the prescaler setting. However, clock stretching on byte level is performed since SCL is pulled low during an interrupt (INT = “1” in IBCR register).

12.18.2 Block Diagram



12.18.3 I²C Interface Registers

a: **Bus control register** (**IBCR2**)

bit	15	14	13	12	11	10	9	8
Address: 000184H	BER	BEIE	SCC	MSS	ACK	GCAA	INTE	INT
Read/write ⇨	(R/W)	(R/W)	(W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

b: **Bus status register** (**IBSR2**)

bit	7	6	5	4	3	2	1	0
Address: 000185H	BB	RSC	AL	LRB	TRX	AAS	GCA	ADT
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

c: **Ten bit slave address register** (**ITBAH**, **ITBAL**)

Ten Bit Address high byte

bit	15	14	13	12	11	10	9	8
Address: 000186H	—	—	—	—	—	—	TA9	TA8
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Ten Bit Address low byte

bit	7	6	5	4	3	2	1	0
Address: 000187H	TA7	TA6	TA5	TA4	TA3	TA2	TA1	TA0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

d: **Ten bit slave address mask register** (**ITMKH**, **ITMKL**)

Ten Bit Address Mask high byte

bit	15	14	13	12	11	10	9	8
Address: 000188H	ENTB	RAL	—	—	—	—	TM9	TM8
Read/write ⇨	(R/W)	(R)	(—)	(—)	(—)	(—)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(1)	(1)	(1)	(1)	(1)	(1)

Ten Bit Address Mask low byte

bit	7	6	5	4	3	2	1	0
Address: 000189H	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(1)	(1)	(1)	(1)	(1)	(1)	(1)	(1)

e: **Seven bit slave address register** (**ISBA**)

bit	7	6	5	4	3	2	1	0
Address: 00018BH	—	SA6	SA5	SA4	SA3	SA2	SA1	SA0
Read/write ⇨	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

(Continued)

(Continued)

f: **Seven bit slave address mask register** (**ISMK**)

bit	15	14	13	12	11	10	9	8
Address: 00018AH	ENSB	SM6	SM5	SM4	SM3	SM2	SM1	SM0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(1)	(1)	(1)	(1)	(1)	(1)	(1)

g: **Data register** (**IDARH**, **IDAR2**)

Data register high byte

bit	15	14	13	12	11	10	9	8
Address: 00018CH	—	—	—	—	—	—	—	—
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(—)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Data register

bit	7	6	5	4	3	2	1	0
Address: 00018DH	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

h: **Clock control register** (**ICCR2**)

bit	15	14	13	12	11	10	9	8
Address: 00018EH	—	NSF	EN	CS4	CS3	CS2	CS1	CS0
Read/write ⇨	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(1)	(1)	(1)	(1)	(1)

i: **Clock disable register** (**IDBL2**)

bit	7	6	5	4	3	2	1	0
Address: 00018FH	—	—	—	—	—	—	—	DBL
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

12.19 16-bit I/O Timer

The CY91360G Series contains two 16-bit free-running timer modules, two output compare modules, and two input capture modules and supports four input channels and four output channels. The following sections only describes the 16-bit free-running timer, Output Compare 0/1 and Input Capture 0/1.
The remaining modules have the identical functions and the register addresses should be found in the I/O map.

12.19.1 Function overview

a: **16-bit Free-running Timer**

The 16-bit free-run timer consists of a 16-bit up counter, control register, and prescaler. The values output from this timer counter are used as the base timer for input capture and output compare.

- Four counter clocks are available.
  Internal clock: ϕ/4, ϕ/16, ϕ/32, ϕ/64
- An interrupt can be generated upon a counter overflow or a match with compare register 0.
- The counter value can be initialized to “0000H” upon a reset, software clear, or match with compare register 0.

b: **Output Compare** (**2 channels per one module**)

The output compare module consists of two 16-bit compare registers, compare output latch, and control register.

When the 16-bit free-running timer value matches the compare register value, the output level is reversed and an interrupt is issued.

- The two compare registers can be used independently.
  Output pins and interrupt flags corresponding to compare registers
- Output pins can be controlled based on pairs of the two compare registers.
  Output pins can be reversed by using the two compare registers.
- Initial values for output pins can be set.
- Interrupts can be generated upon a compare match.

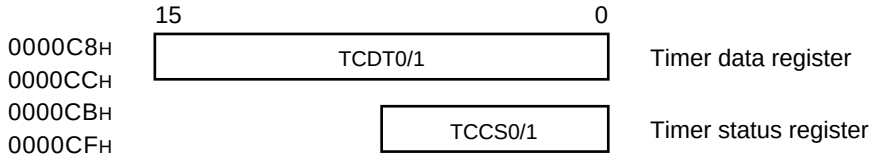
c: **Input Capture** (**2 channels per one module**)

The input capture module consists of two 16-bit capture registers and control registers corresponding to two independent external input pins. The 16-bit free-running timer value can be stored in the capture register and an interrupt is issued simultaneously upon detection of an edge of a signal input from an external input pin.

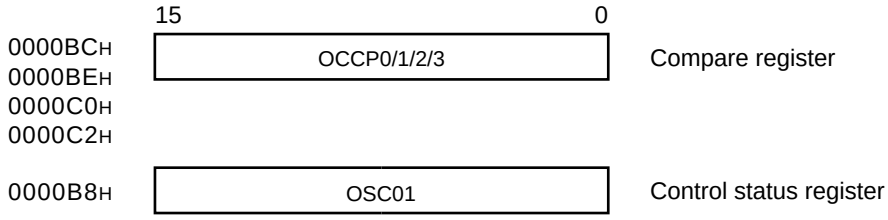
- The detection edge of an external input signal can be specified.
  Rising, falling, or both edges
- Two input channels can operate independently.
- An interrupt can be issued upon a valid edge of an external input signal.

12.19.2 Registers

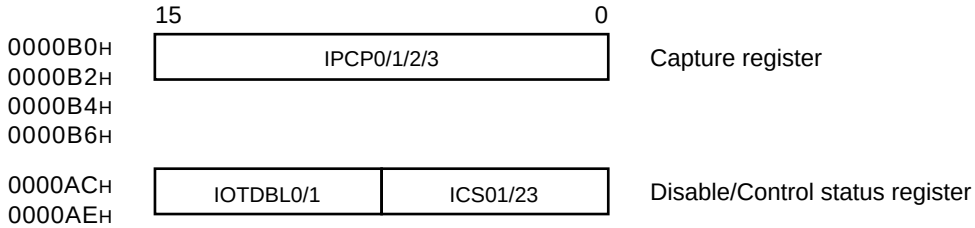
a: **16-bit free-running timer**



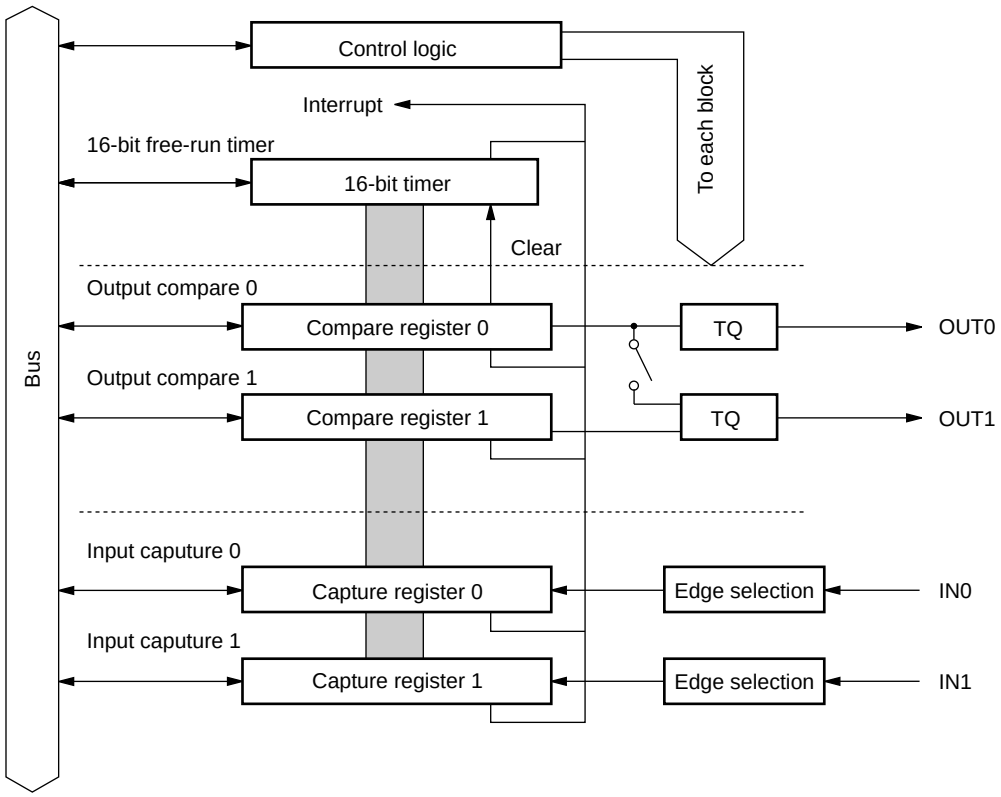
b: **16-bit output compare**



c: **16-bit input capture**



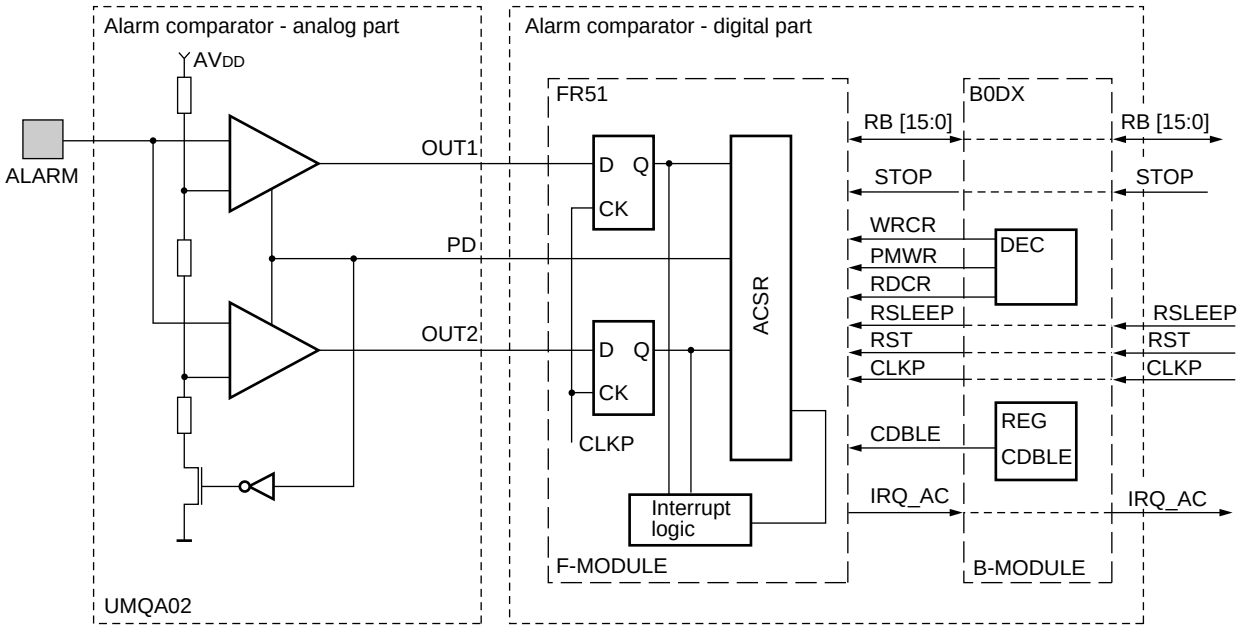
12.19.3 Block Diagram



12.20 Alarm Comparator

This section provides an overview of the Alarm Comparator (Also called Under/Overvoltage Detection), describes the register structure and functions, and describes the operation of the Alarm Comparator.

12.20.1 Block Diagram



12.20.2 Registers

Alarm comparator clock disable register (ACCDBL)

Address	Bits	7	6	5	4	3	2	1	0	Initial value
00000180H		—	—	—	—	—	—	—	CDBLE	- - - - - - - 0B
									R/W	← Access

Alarm comparator status disable register (ACSR)

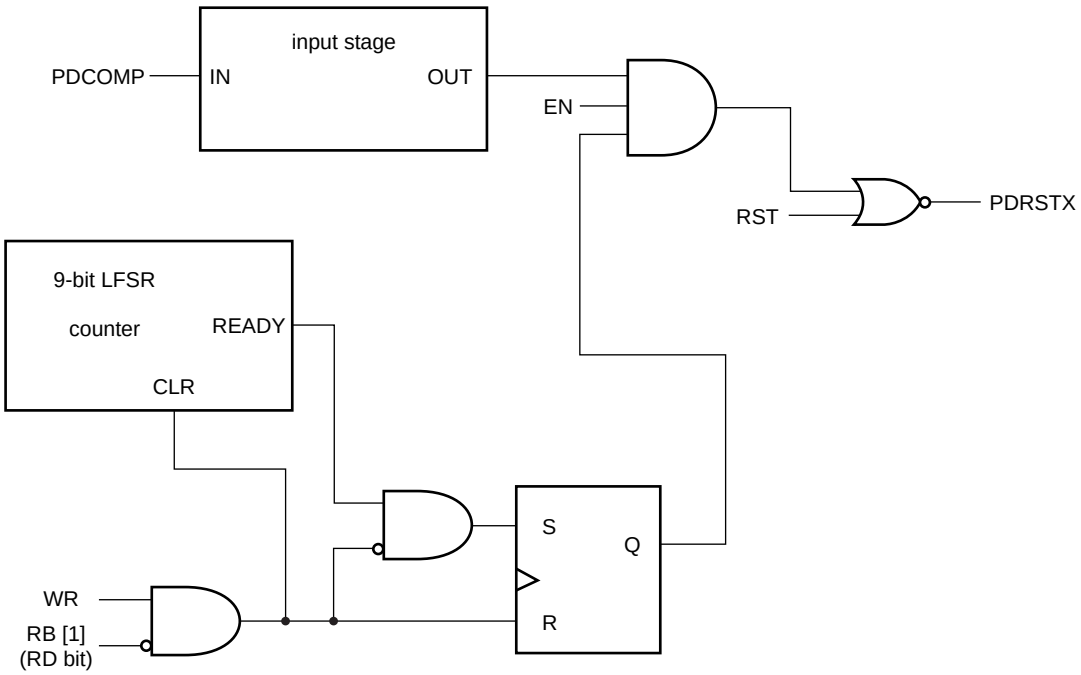
Address	Bits	7	6	5	4	3	2	1	0	Initial value
00000181H		—	OV_EN	UV-EN	OUT2	OUT1	IRQ	IEN	PD	-11xxx00B
			R/W	R/W	R	R	R/W	R/W	R/W	← Access

12.21 Power Down Reset

This section provides an overview of the Power Down Reset, and describes the register structure.

The power down reset module performs a system reset when V_{CC} goes below a threshold voltage. The reset signal is be disabled and enabled by setting the power down reset control register (PDRCR). For low power applications the digital and the analog part of the power down reset control circuit can be disabled.

12.21.1 Block Diagram



12.21.2 Register

	7	6	5	4	3	2	1	0
PDRCR 00017DH	—	—	—	—	—	CDSBLE	PD	EN
access	—	—	—	—	—	R/W	R/W	R/W
initial value (INIT)	—	—	—	—	—	0	0	0
initial value (RST)	X	X	X	X	X	X	X	X

12.22 Serial I/O Interface (SIO)

This section provides an overview of the Serial I/O Interface (SIO), and describes the register structure.

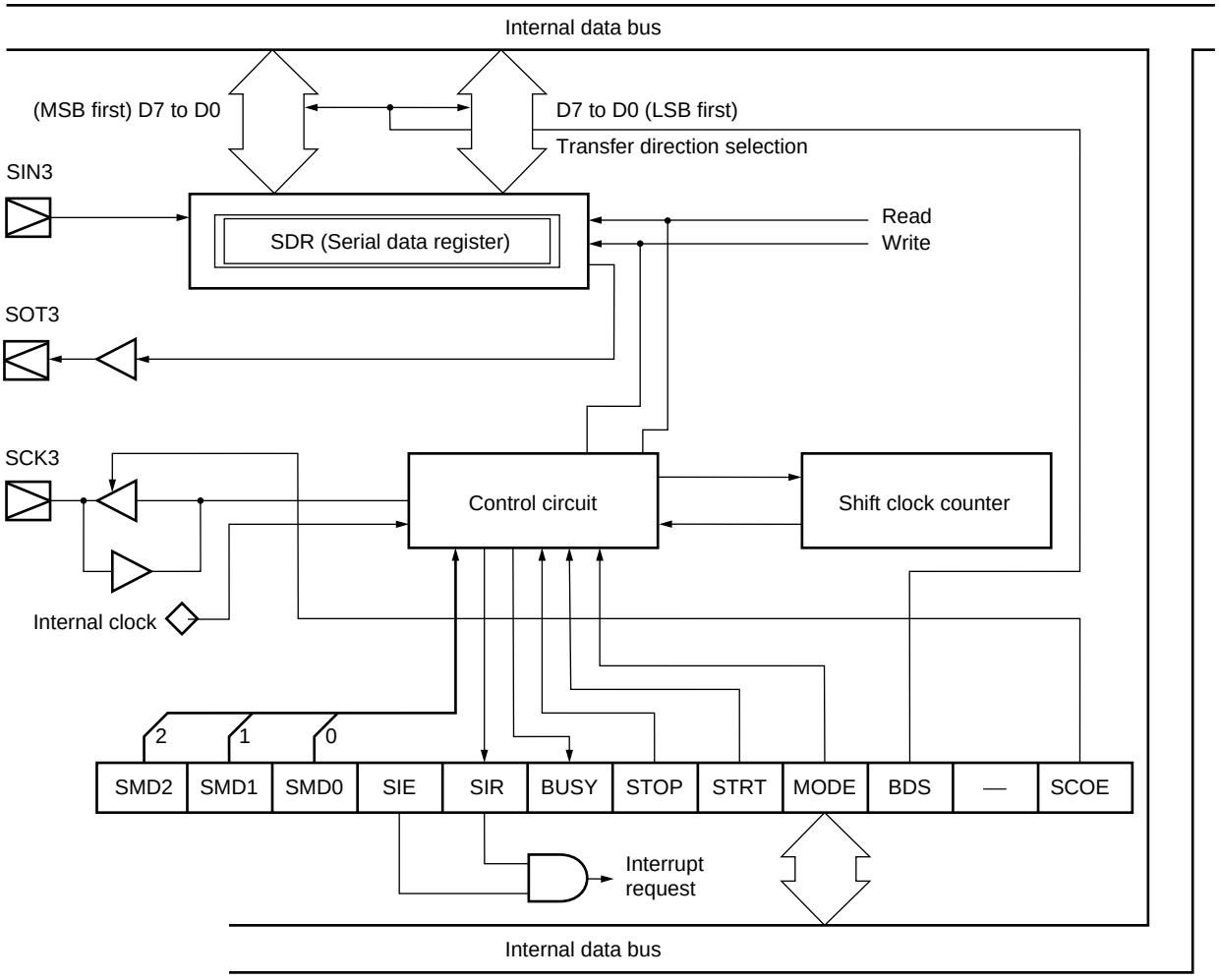
12.22.1 Block Diagram

This block is a serial I/O interface that allows data transfer using clock synchronization. The interface consists of a single eight-bit channel. Data can be transferred from the LSB or MSB.

CY91360G series contains two Serial I/O units SIO0 and SIO1. This section only describes SIO0. Please see the I/O map for the register addresses of SIO1.

The serial I/O interface operates in two modes:

- Internal shift clock mode: Data is transferred in synchronization with the internal clock.
- External shift clock mode: Data is transferred in synchronization with the clock supplied via the external pin (SCK). By manipulating the general-purpose port sharing the external pin (SCK), data can also be transferred by a CPU instruc tion in this mode.



12.22.2 Registers

Serial mode control status register (SMCS)

	15	14	13	12	11	10	9	8
Address: 000084H	SMD2	SMD1	SMD0	SIE	SIR	BUSY	STOP	STRT

	7	6	5	4	3	2	1	0
Address: 000085H	—	—	—	—	MODE	BDS	—	SCOE

SIO edge selection/clock disable register (SES)

	15	14	13	12	11	10	9	8
Address: 000086H	—	—	—	—	—	—	DBL	NEG

Serial data register (SDR)

	7	6	5	4	3	2	1	0
Address: 000087H	D7	D6	D5	D4	D3	D2	D1	D0

12.23 Sound Generator

This section provides an overview of the Sound Generator, and describes the register structure.

The Sound Generator consists of the Sound Control register, Frequency Data register, Amplitude Data register, Decrement Grade register, Tone Count register, Sound Disable register, PWM pulse generator, Frequency counter, Decrement counter and Tone Pulse counter.

12.23.1 Registers

Sound control register (SGCR)

bit	7	6	5	4	3	2	1	0
Address: 0000EF$_H$	S1	S0	TONE	—	—	INTE	INT	ST
Read/write ⇨	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(—)	(—)	(0)	(0)	(0)

bit	15	14	13	12	11	10	9	8
Address: 0000EE$_H$	TST	—	—	—	—	—	BUSY	DEC
Read/write ⇨	(R/W)	(—)	(—)	(—)	(—)	(—)	(R)	(R/W)
Default value ⇨	(0)	(—)	(—)	(—)	(—)	(—)	(0)	(0)

Frequency data register (SGFR)

bit	7	6	5	4	3	2	1	0
Address: 0000F1$_H$	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

Amplitude data register (SGAR)

bit	15	14	13	12	11	10	9	8
Address: 0000F0$_H$	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Decrement grade register (SGDR)

bit	7	6	5	4	3	2	1	0
Address: 0000F3$_H$	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

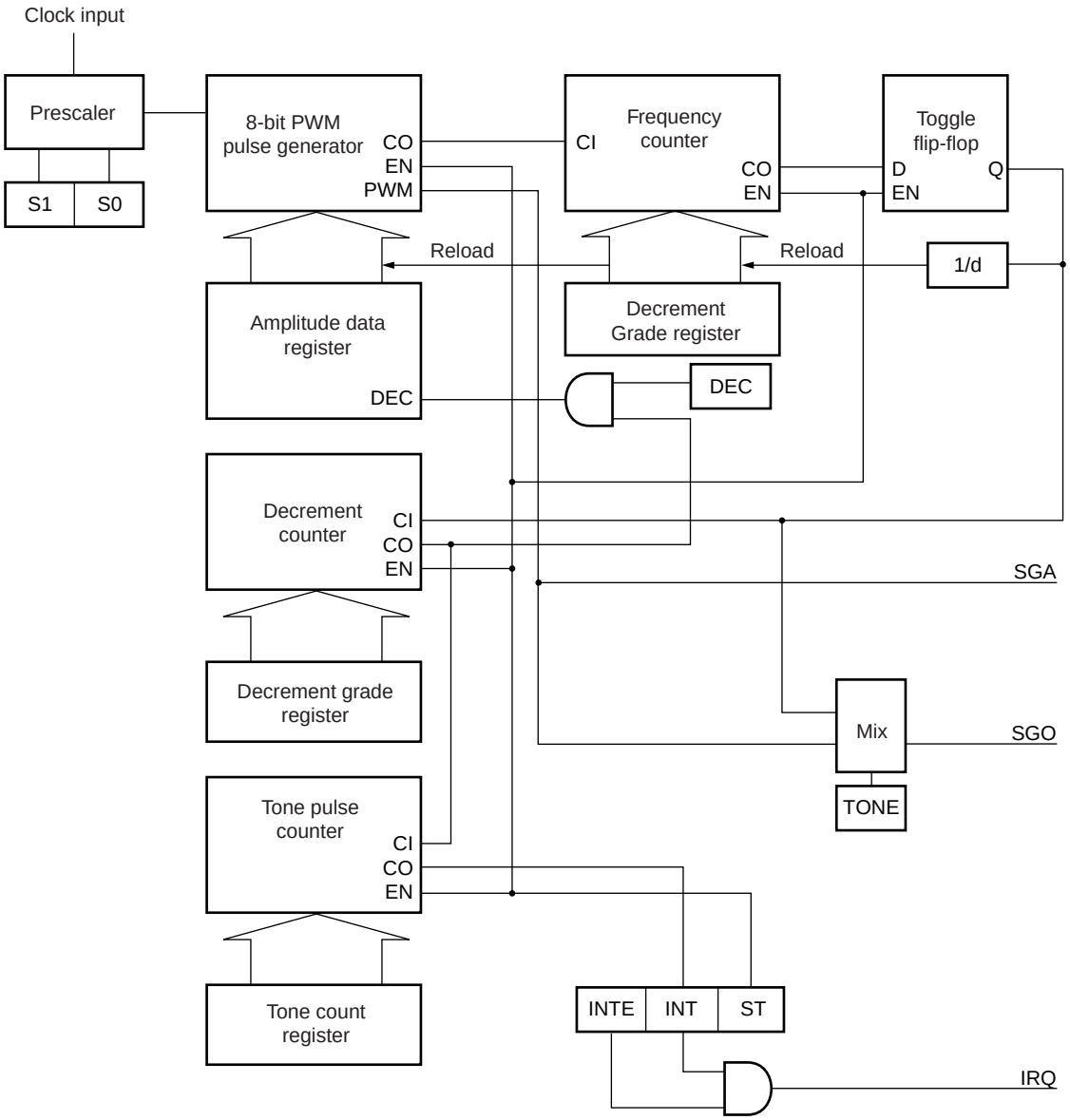
Tone count register (SGTR)

bit	15	14	13	12	11	10	9	8
Address: 0000F2$_H$	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

Sound disable register (SGDBL)

bit	7	6	5	4	3	2	1	0
Address: 0000ED$_H$	—	—	—	—	—	—	—	DBL
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)
Default value ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)

12.23.2 Block Diagram



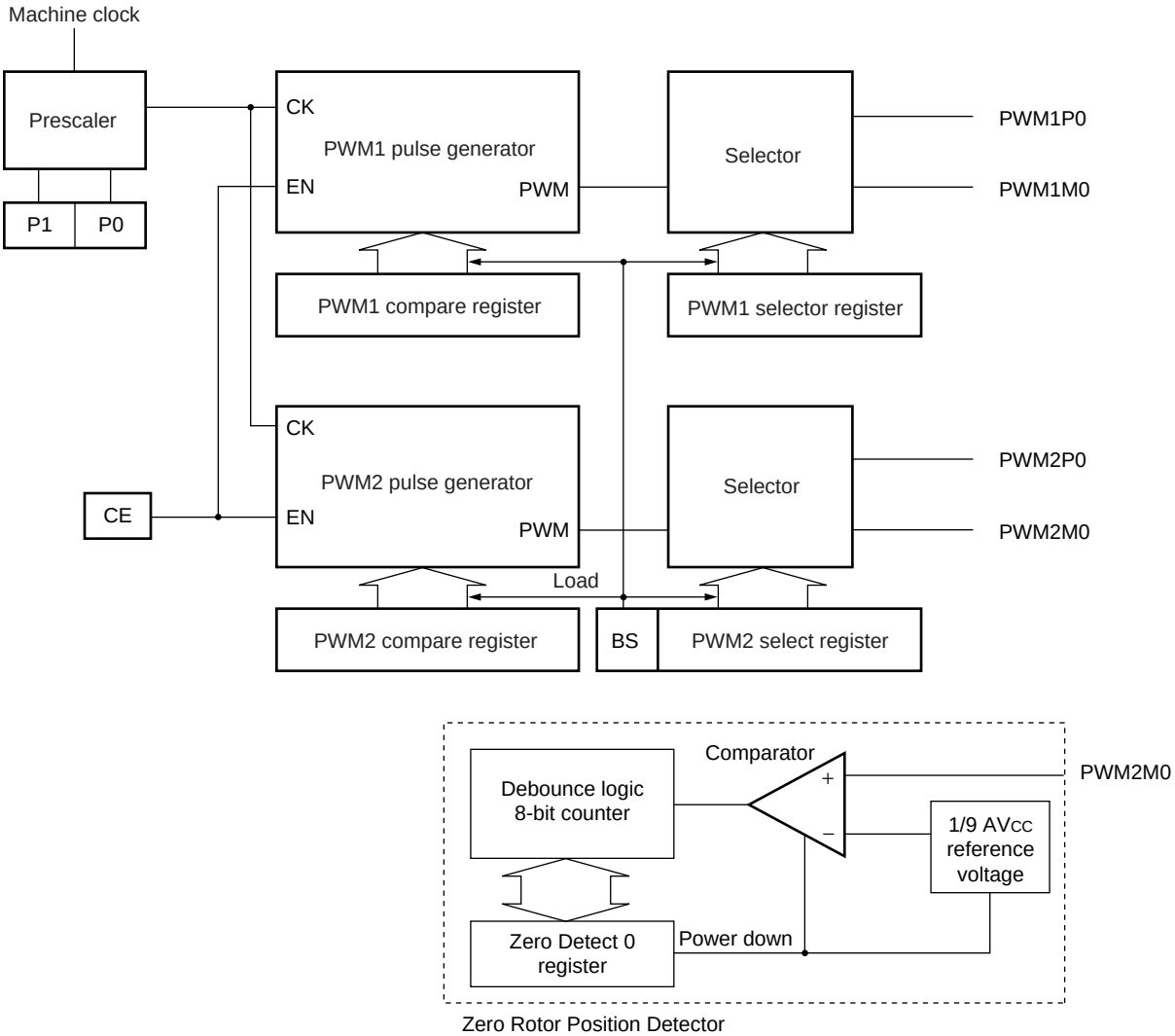
12.24 Stepper Motor Controller

This section provides an overview of the Stepper Motor Control Module, and describe the register structure.

The Stepping Motor Controller consists of two PWM Pulse Generators, four motor drivers, Selector Logic and the Zero Rotor Position Detector. The four motor drivers have high output drive capabilities and they can be directly connected to the four ends of two motor coils. The combination of the PWM Pulse Generators and Selector Logic is designed to control the rotation of the motor. A Synchronization mechanism assures the synchronous operations of the two PWMs. The Zero Rotor Position Detector helps CPU obtain feed back information of the rotor movements. The following sections describe the Stepping Motor Controller 0 only. The other controllers have the same functions. The register addresses are found in the I/O map.

Note: The Rotor Zero Position Detection capability is protected by a patent from siemens VDO automatic AG and may only be used with VDO's prior approval.

12.24.1 Block Diagram



12.24.2 Registers

PWM control 0 register (PWC0)

bit	7	6	5	4	3	2	1	0
Address: 0000D1H	—	—	P1	P0	CE	—	—	TST
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(—)	(—)	(R/W)
Default value ⇨	(—)	(—)	(0)	(0)	(0)	(—)	(—)	(0)

Zero detect 0 register (ZPD0)

bit	15	14	13	12	11	10	9	8
Address: 0000D0H	S1	S0	TS	T2	T1	T0	PD	RS
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(1)	(0)

PWM1 compare 0 register (PWC10)

bit	7	6	5	4	3	2	1	0
Address: 0000D9H	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

PWM2 compare 0 register (PWC20)

bit	15	14	13	12	11	10	9	8
Address: 0000D8H	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

PWM1 select register (PWS10)

bit	7	6	5	4	3	2	1	0
Address: 0000DBH	—	—	P2	P1	P0	M2	M1	M0
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(—)	(—)	(0)	(0)	(0)	(0)	(0)	(0)

PWM2 select register (PWS20)

bit	15	14	13	12	11	10	9	8
Address: 0000DAH	—	BS	P2	P1	P0	M2	M1	M0
Read/write ⇨	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(—)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

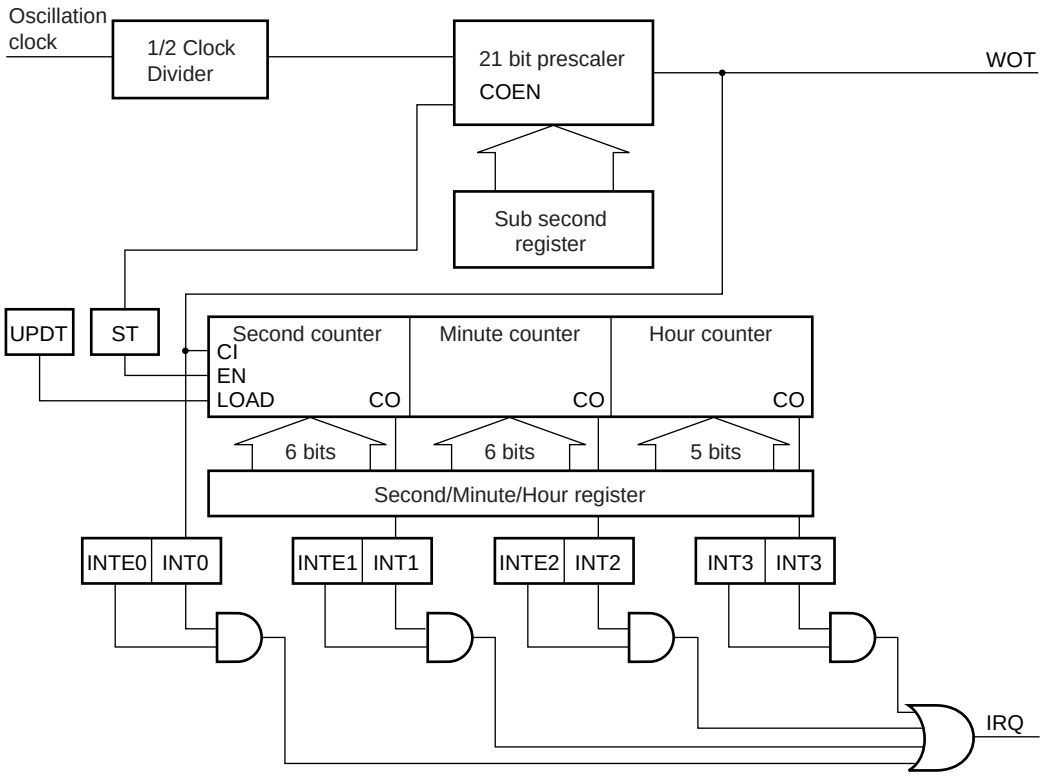
PWM clock disable register (SMDBL0)

bit	7	6	5	4	3	2	1	0
Address: 0000E8H	—	—	—	—	—	—	—	DBL
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)
Default value ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)

12.25 Real Time Clock

This section provides an overview of the Real Time Clock (also called WatchTimer), describes the register structure and functions.The Real Time Clock (Watch Timer) consists of the Timer Control register, Sub-second register, Second/Minute/Hour registers, 1/2 clock divider, 21bit prescaler and Second/Minute/Hour counters. The Real Time Clock operates as the real-world timer and provides the real-world time information.

12.25.1 Block Diagram



12.25.2 Registers

Timer disable register (WTDBL)

bit	7	6	5	4	3	2	1	0
Address: 0000F5H	—	—	—	—	—	—	—	DBL
Read/write ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(R/W)
Default value ⇨	(—)	(—)	(—)	(—)	(—)	(—)	(—)	(0)

Timer control register (WTCR)

bit	7	6	5	4	3	2	1	0
Address: 0000F7H	TST2	TST1	TST0	—	RUN	UPDT	—	ST
Read/write ⇨	(R/W)	(R/W)	(R/W)	(—)	(R)	(R/W)	(—)	(R/W)
Default value ⇨	(0)	(0)	(0)	(—)	(0)	(0)	(—)	(0)

bit	15	14	13	12	11	10	9	8
Address: 0000F6H	INTE3	INT3	INTE2	INT2	INTE1	INT1	INTE0	INT0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

Sub-second register (WTBR)

bit	7	6	5	4	3	2	1	0
Address: 0000FBH	D7	D6	D5	D4	D3	D2	D1	D0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

bit	15	14	13	12	11	10	9	8
Address: 0000FAH	D15	D14	D13	D12	D11	D10	D9	D8
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(X)	(X)	(X)	(X)	(X)	(X)	(X)	(X)

bit	7	6	5	4	3	2	1	0
Address: 0000F9H	—	—	—	D20	D19	D18	D17	D16
Read/write ⇨	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(—)	(—)	(—)	(X)	(X)	(X)	(X)	(X)

Second register (WTSR)

bit	15	14	13	12	11	10	9	8
Address: 0000FEH	—	—	S5	S4	S3	S2	S1	S0
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(—)	(—)	(X)	(X)	(X)	(X)	(X)	(X)

(Continued)

(Continued)

Minute register (WTMR)

bit	7	6	5	4	3	2	1	0
Address: 0000FD$_H$	—	—	M5	M4	M3	M2	M1	M0
Read/write ⇨	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(—)	(—)	(X)	(X)	(X)	(X)	(X)	(X)

Hour register (WTHR)

bit	15	14	13	12	11	10	9	8
Address: 0000FC$_H$	—	—	—	H4	H3	H2	H1	H0
Read/write ⇨	(—)	(—)	(—)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(—)	(—)	(—)	(X)	(X)	(X)	(X)	(X)

12.26 Subclock

The Subclock System provides various power saving modes. The key of the concept is to supply the 32 kHz clock signal only to the Real Time Clock RTC) Module, while the rest of the MCU is provided with 4 MHz clock signal in order to achieve lower power supply current in the RTC32K mode.

This behavior can be altered by the configuration input, SELCLK pin to switch the RTC module to operate with the 4 MHz clock. The following sections describe the operation with SELCLK connected to “0” and SELCLK connected to “1” respectively.

Note: On CY91F362GB SELCLK should always be connected to “1”, subclock operation is not implemented on those devices.

12.26.1 Operation of Subclock (SELCLK = 0)

The next table summarizes the operation states of the components related to the Subclock System.To simplify this table SLEEP modes are not listed but the operation is the same as for RUN modes except that the CPU is stopped.

Mode	Power Dissipation	Operation of Components				
		4 M Osc.	32 K Osc.	RTC	CPU & Peripheral	PLL
RUN	High	Run	Run	Run	Run	Stop/Run
RTC4M32K	Medium Low	Run	Run	Run	Stop	Stop
RTC32K	Low	Stop	Run	Run	Stop	Stop
STOP	Lowest	Stop	Stop	Stop	Stop	Stop

The following table summarizes those operation modes and necessary software settings.

Mode	Software Setting					
	STOP	PLL1EN	PLL2EN	OSCD1	OSCD2	RTC32
RUN	0	0 or 1	1	Don’t Care	Don’t Care	Don’t Care
RTC4M32K	1	Don’t Care	1	0	0	Don’t Care
RTC32K	1	Don’t Care	1	1	0	1
STOP	1	Don’t Care	Don’t Care	1	1	Don’t Care

It is recommended that PLL2EN is set to “1” after the initialization to start the 32 kHz oscillation and this bit should be kept at “1” during the operation. Otherwise the 32 kHz oscillator does not start. Also bits 9 and 10 of the CLKR register (address 0046_H) should always be set to “0” during operation.

12.26.2 4 MHz Real Time Clock Configuration (SELCLK = 1)

When the SELCLK pad is connected logic level 1, the 32 kHz oscillation is disabled regardless of the software setting. In this configuration, the Real Time Clock Module is supplied with the 4 MHz oscillation clock signal.

The following table summaries the modes available in this configuration.

Mode	Power Dissipation	Operation of Components				
		4 M Osc.	32 K Osc.	RTC	CPU & Peripheral	PLL
RUN	High	Run	Stop	Run	Run	Stop/Run
RTC4M	Medium Low	Run	Stop	Run	Stop	Stop
STOP	Lowest	Stop	Stop	Stop	Stop	Stop

Mode	Software Setting					
	STOP	PLL1EN	PLL2EN	OSCD1	OSCD2	RTC32
RUN	0	0 or 1	Don't Care	Don't Care	Don't Care	Don't Care
RTC4M	1	Don't Care	Don't Care	0	Don't Care	Don't Care
STOP	1	Don't Care	Don't Care	1	Don't Care	Don't Care

12.26.3 Use of Real Time Clock Module

There is some additional consideration needed to operate the RTC module to achieve the desired functionality.

Because the RTC module is directly connected to the 32 kHz oscillation clock, the oscillation stabilization time has to be taken care of by the software.This can be achieved by using another timer (e.g the Time Base Timer) to trigger the software to start the RTC module (Setting of ST bit to "1").

It is also important to stop the RTC module before entering the STOP mode. Otherwise, the reactivation from STOP mode results in unpredictable operation of the RTC module.

After the reactivation, the oscillation stabilization time has to be measured again by the software, then the RTC module can be restarted.

12.27 32 kHz Clock Calibration Unit

The 32 kHz Clock Calibration Module provides possibilities to calibrate the 32 kHz oscillation clock with respect to the 4 MHz oscillation clock.

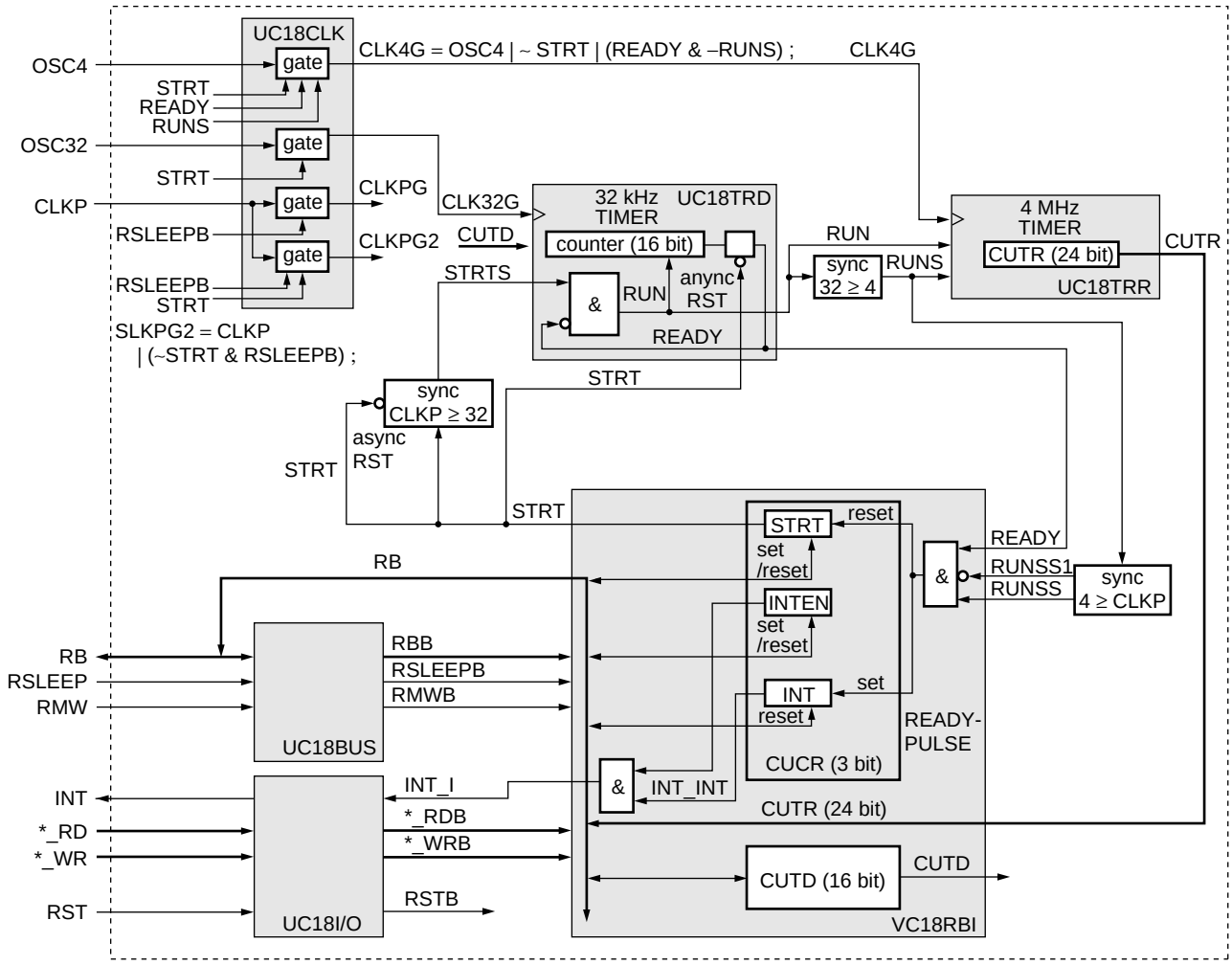
12.27.1 Description

This hardware allows the software to measure time generated by the 32 kHz clock with the 4 MHz clock.

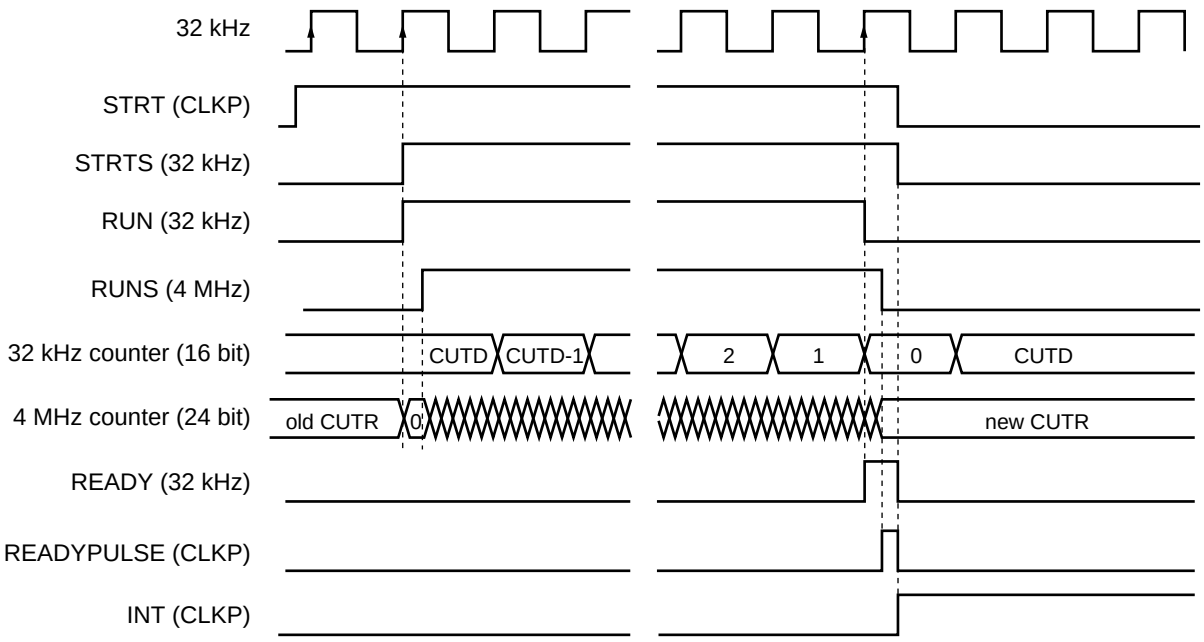
By utilizing this hardware in conjunction with software processing, the accuracy of the 32 kHz clock can come closer to that of the 4 MHz clock. The measurement result from the 32 kHz Clock Calibration Module can be processed by the software and the setting required for the Real Time Clock Module can be obtained.

This module consists of two timers, one operating with the 32 kHz clock and the other operating with the 4 MHz clock. The 32 kHz timer triggers the 4 MHz timer and resulting 4 MHz timer value is stored in a register. The value stored in this register can be used for the subsequent software processing to calculate the desired Real Time Clock module's setting.

12.27.2 Block Diagram



12.27.3 Timing



12.27.4 Clocks

The module operates with 3 different clocks: The 4 MHz clock OSC4, the 32 kHz clock OSC32 and the R-bus clock CLKP. Synchronization circuits adapt the different domains.

All 3 clocks are gated. The 32 kHz and the 4 MHz clock are switched off if STRT is 0. CLKPG is gated by RSLEEP and CLKPG2 by RSLEEP and STRT for the 2 bits, which are set/reset by hardware.

The clock frequencies have to fulfill the following requirements:

1.) Clock ratio

$T_{OSC32} > 2 \times T_{OSC4} + 3 \times T_{CLKP}$
$T_{OSC4} < 1 / 2 \times T_{OSC32} - 3 / 2 \times T_{CLKP}$
$T_{CLKP} < 1 / 3 \times T_{OSC32} - 2 / 3 \times T_{OSC4}$

2.) The input frequencies must not exceed the values given in next table.

Table 12-5. Maximum Operation Frequencies

	CLKP		OSC32		OSC4	
Maximum	32 MHz	31.25 ns	4 MHz	250 ns	13 MHz	76.9 ns

Table 12-6. Examples of Valid Clock Ratios which Fulfill Requirements 1 and 2

	OSC32		OSC4		CLKP	
Maximum operation speed	4 MHz	250 ns	13 MHz	76.9 ns	32 MHz	31.25 ns
Standard TDIR mode	500 kHz	2000 ns	4 MHz	250 ns	4 MHz	250 ns
Normal operation	32 kHz	31.25 us	4 MHz	250 ns	> 2 MHz	500 ns

12.27.5 Register Description

a: Calibration unit control register (CUCR)

Control register low byte (CUCRL)

bit	7	6	5	4	3	2	1	0
Address: 000191H	—	—	—	STRT	—	—	INT	INTEN
Read/write ⇨	(R)	(R)	(R)	(R/W)	(R)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

b: 32 kHz timer data register (CUTD)

32 kHz timer data register high byte (CUTDH)

bit	15	14	13	12	11	10	9	8
Address: 000192H	TDD15	TDD14	TDD13	TDD12	TDD11	TDD10	TDD9	TDD8
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(1)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

32 kHz timer data register low byte (CUTDL)

bit	7	6	5	4	3	2	1	0
Address: 000193H	TDD7	TDD6	TDD5	TDD4	TDD3	TDD2	TDD1	TDD0
Read/write ⇨	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)	(R/W)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

c: 4 MHz timer data register (CUTR)

4 MHz timer data register1 high byte (CUTR1H)

bit	15	14	13	12	11	10	9	8
Address: 000194H	—	—	—	—	—	—	—	—
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

4 MHz timer data register1 low byte (CUTR1L)

bit	7	6	5	4	3	2	1	0
Address: 000195H	TDR23	TDR22	TDR21	TDR20	TD19	TDR18	TDR17	TDR16
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

4 MHz timer data register2 high byte (CUTR2H)

bit	15	14	13	12	11	10	9	8
Address: 000196H	TDR15	TDR14	TDR13	TDR12	TDR11	TDR10	TDR9	TDR8
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

4 MHz timer data register2 low byte (CUTR2L)

bit	7	6	5	4	3	2	1	0
Address: 000197H	TDR7	TDR6	TDR5	TDR4	TD3	TDR2	TDR1	TDR0
Read/write ⇨	(R)	(R)	(R)	(R)	(R)	(R)	(R)	(R)
Default value ⇨	(0)	(0)	(0)	(0)	(0)	(0)	(0)	(0)

12.28 Flash Memory

CY91360G series devices feature 512 Kbyte of embedded flash memory unit derived from the MB29LV400C and the FLASH Memory interface circuit.

12.28.1 Out Line of Flash Memory

The Flash Memory consists of a flash memory unit derived from the MBM29LV400C and a flash memory interface circuit.

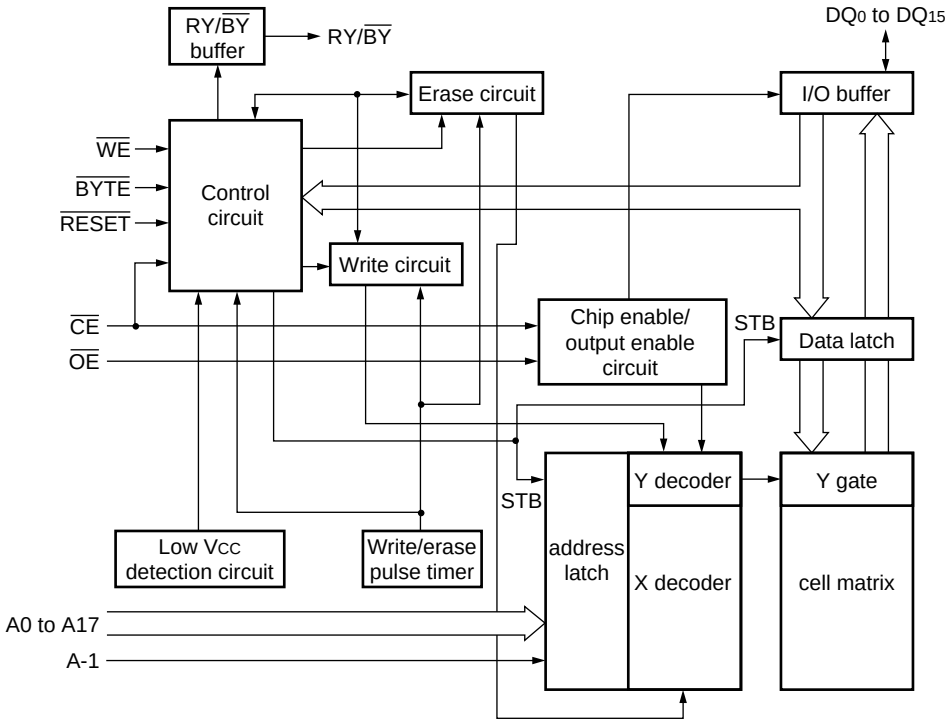
- 512 Kword × 8 bit/256 Kword × 16 bit/128 Kword × 32 bit
  (64 Kbyte × 3 + 32 Kbyte + 8 Kbyte × 2 + 16 Kbyte) sectors
- Uses automatic program algorithm (Embedded Algorithm™*)
- Erase pause/restart function
- Detects completion of writing/erasing using data polling or toggle bit functions
- Detects completion of writing/erasing by RY/BY pin
- Compatible with JEDEC standard commands
- Performs minimum of 10,000 write/erase operations
- Sector erase function (any combination of sectors)
- Sector protect function
- Temporary sector protect cancellation function
- Allows flash memory interface circuit to write to/erase flash memory both under control of external pin by writer and under control of internal bus by CPU.

*: Embedded Algorithm™ is a registered trademark of Advanced Micro Devices, Inc.

12.28.2 Block Diagrams of Flash Memory

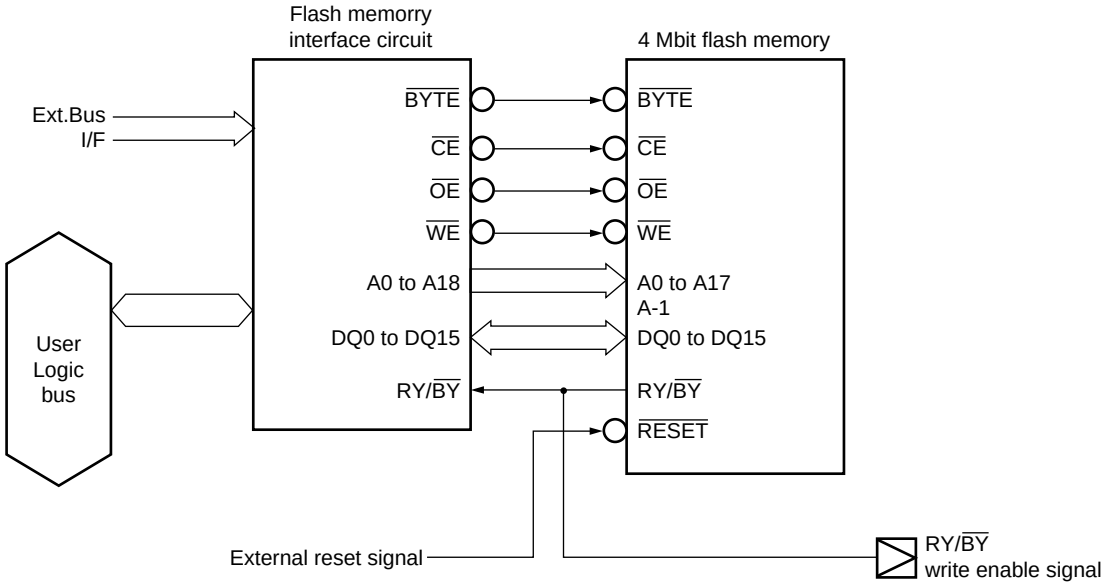
a: Block Diagram of Flash Memory

Figure shows the block diagram of the flash memory unit, which has almost the same configuration as the MBM29LV400C.



b: Entire Block Diagram of Flash Memory

Figure shows the entire block diagram of the flash memory with the flash memory interface circuit.



c: Sector Configuration

Table 12-7. Write, Byte Read, Half Word Read

		Flash Memory Mode	Other Modes
8 bit × 2		$7FFFF_H$	$FFFFF_H$
Sector 13	16 KB	$7C000_H$	$FC000_H$
Sector 12	8 KB	$7A000_H$	$FA000_H$
Sector 11	8 KB	78000_H	$F8000_H$
Sector 10	32 KB	70000_H	$F0000_H$
Sector 9	64 KB	60000_H	$E0000_H$
Sector 8	64 KB	50000_H	$D0000_H$
Sector 7	64 KB	40000_H	$C0000_H$
Sector 6	16 KB	$3C000_H$	$BC000_H$
Sector 5	8 KB	$3A000_H$	$BA000_H$
Sector4	8 KB	38000_H	$B8000_H$
Sector 3	32 KB	30000_H	$B0000_H$
Sector 2	64 KB	20000_H	$A0000_H$
Sector 1	64 KB	10000_H	90000_H
Sector 0	64 KB	00000_H	80000_H

Table 12-8. Long Word Read

MSB		LSB		Flash Memory Mode	Other Modes
8 bit × 2		8 bit × 2		$7FFFF_H$	$FFFFF_H$
Sector 13	16 KB	Sector 6	16 KB	78000_H	$F8000_H$
Sector 12	8 KB	Sector 5	8 KB	74000_H	$F4000_H$
Sector 11	8 KB	Sector 4	8 KB	70000_H	$F0000_H$
Sector 10	32 KB	Sector 3	32 KB	60000_H	$E0000_H$
Sector 9	64 KB	Sector 2	64 KB	40000_H	$C0000_H$
Sector 8	64 KB	Sector 1	64 KB	20000_H	$A0000_H$
Sector 7	64 KB	Sector 0	64 KB	00000_H	80000_H

12.28.3 Write/Erase Modes

The flash memory can be accessed in two different ways; the flash memory mode allowing write/erase directly from the external pins, and the other modes allowing write/erase from the CPU via the internal bus. These modes are selected by the external mode pins.

a: **Flash Memory Mode**

The CPU stops when the mode pins are set to 111 while the INITX signal is asserted. The flash memory interface circuit is directly connected to the external bus interface, allowing direct control by the external pins. This mode makes the MCU seem like a standard flash memory at the external pins, and write/erase can be performed using a flash memory programmer.

In the flash memory mode all the operations supported by the flash memory automatic algorithm can be used.

b: **Other Modes**

The flash memory is located in the CS1X area of the CPU memory space and like ordinary mask ROM can be read-accessed and program-accessed from the CPU through the flash memory interface circuit.

Writing/erasing the flash memory is performed by instructions from the CPU via the flash memory interface circuit. Therefore, this mode allows rewriting even when the MCU is soldered on the target board.

The sector protect operations can not be performed in these modes.

c: **Control Signals of Flash Memory**

Next table lists the flash memory control signals in the flash memory mode.

There is almost a one-to-one correspondence between the flash memory control signals and the external pins of the MBM291V400TA. The V_{ID} (12 V) pins required by the sector protect operations are MD0, MD1 and MD2 instead of A9, RESET and OE for the MBM29LV400C.

In the flash memory mode, the width of the external data bus can be 8 or 16 bit.

12.28.4 Flash Control Status Register (FMCS)

Flash Memory Macros used in devices: Normal Flash Macro used in: CY91F362GB
Fast Flash Macro used in: CY91FV360GA

	Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
FV360GA, F362GB:	00007000H	FACCEN	—	—	RDYEG*	RDY	RDYI	WE	LPM
	Access	R/W	R/W	R/W	R	R	R/W	R/W	R/W
	Initial value	1	1	1	0	X	0	0	0
	value after Boot ROM	0	1	1	0	X	0	0	0

*: It is not allowed to use RDYEG.

12.28.5 Read/Write Access

In the flash memory mode, read/write access to the flash memory must be under control of the external pins. However, with the CPU access, there are no special timing constraints on read/write access because the flash memory is controlled by the flash memory interface circuit.

In this section, “write access” does not directly mean “program flash memory”. It implies “activation of the flash commands”.

a: **Read/Write Access in Flash Memory Mode**

Next table gives the setting of pins for read/write access in the Flash Memory mode. There is no special problem with control of these pins if connected to a flash memory writer. However, in other cases, timing specifications must be met.

Table 12-9. Setting Conditions of Pins for Read/Write Access in Flash Memory Mode

Operations	BGRNTX ($\overline{CE}$)	RDY ($\overline{OE}$)	CS4X ($\overline{WE}$)	A0 to A18	D16 to D31	INIT
Read	L	L	H	Read address	D_{OUT}	H
Write	L	H	L	Write address	D_{IN}	H
Output disable	L	H	H	x	High-Z	H
Standby	H	x	x	x	High-Z	H
Hardware reset	x	x	x	x	High-Z	L

Note: This table uses pin names from F362GB. Check corresponding pin names of other devices.

b: **Read Access with CPU**

Flash Wait Control Register (**FMWT**)

Address	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00007004_H	—	—	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0
Access	—	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value value after Boot ROM Normal Flash Macro	—	0	0	0	0	0	1	1
Initial value value after Boot ROM Fast Flash Macro	—	0	0	1	0	0	1	1

Normal Flash Macro: Recommended Settings

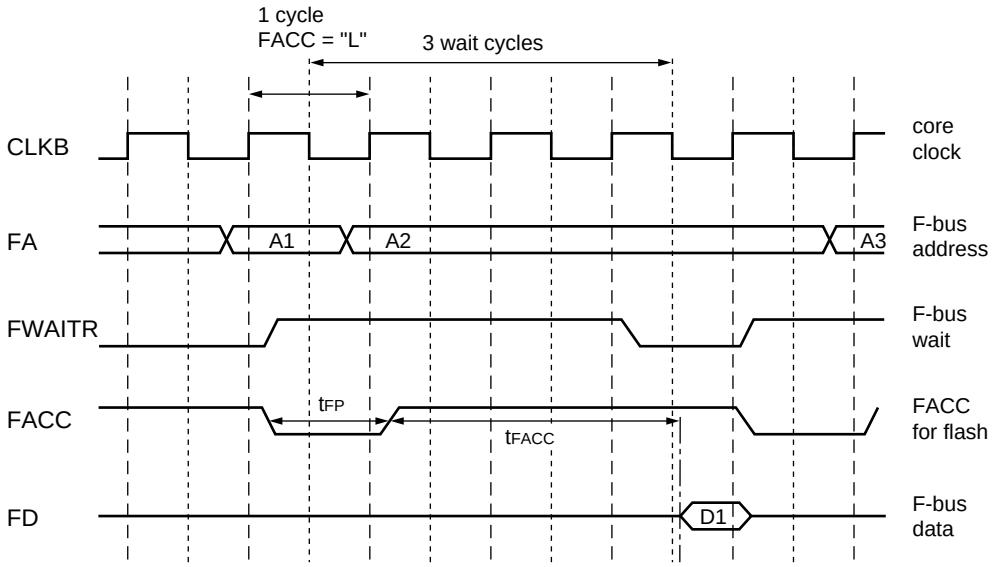
Table 12-10. Without Applying Clock Modulation

CLKB Unmodulated Core Clock Frequency [MHz]	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	FACC Low Cycles/Wait Cycles	FMWT
64	0	1	0	0	1	1	1 / 3	13_H
48	0	1	0	0	1	1	1 / 3	13_H
40	0	1	0	0	1	0	1 / 2	12_H
32	0	0	0	0	1	0	0.5 / 2	02_H
24	0	0	0	0	0	1	0.5 / 1	01_H
16	0	0	0	0	0	1	0.5 / 1	01_H

Table 12-11. When Applying Clock Modulation

CLKB Core Clock Frequency [MHz]	Peak Max Frequency	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	FACC Low Cycles/Wait Cycles	FMWT
48	64	0	1	0	0	1	1	1 / 3	13_H
32	48	0	1	0	0	1	1	1 / 3	13_H
24	40	0	1	0	0	1	0	1 / 2	12_H
24	32	0	0	0	0	1	0	0.5 / 2	02_H
16	24	0	0	0	0	0	1	0.5 / 1	01_H

Example for flash memory read access with 1 cycle for the low time of FACC and 3 wait cycles



The minimum value for t_{FP} is 15 ns, for t_{FACC} it is 40 ns.

Fast Flash Macro: Recommended Settings

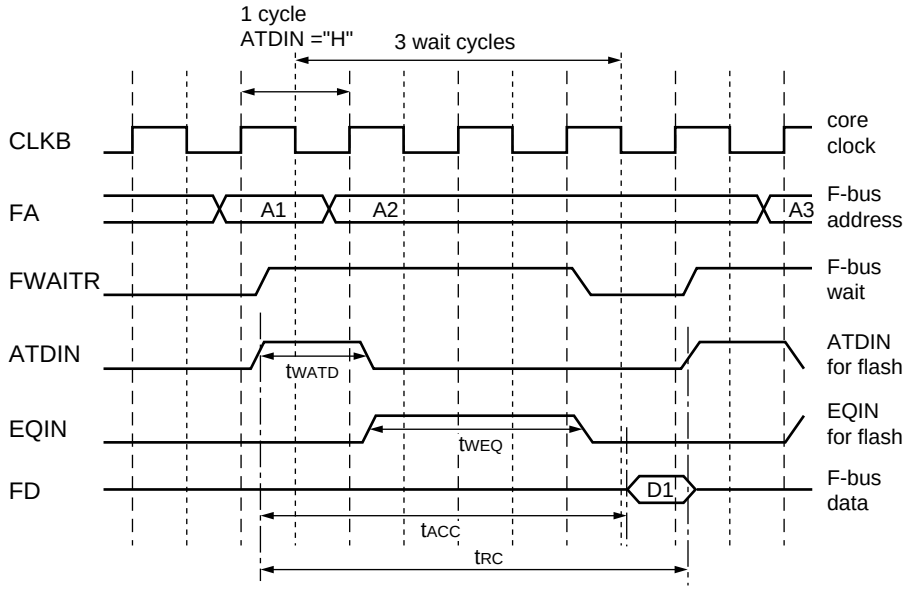
Table 12-12. Without Applying Clock Modulation

CLKB Unmodulated Core Clock Frequency [MHz]	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	ATDIN High Cycles/Wait Cycles	FMWT
64	0	1	0	0	1	1	1 / 3	13_H
48	0	0	0	0	1	0	0.5 / 2	02_H
40	0	0	0	0	1	0	0.5 / 2	02_H
32	0	0	1	0	0	1	0.5 / 1	09_H
24	0	0	0	0	0	1	0.5 / 1	01_H
16	0	0	0	0	0	1	0.5 / 1	01_H

Table 12-13. When Applying Clock Modulation

CLKB Core Clock Frequency [MHz]	Peak Max Frequency	FAC1	FAC0	EQINH	WTC2	WTC1	WTC0	ATDIN High Cycles/Wait Cycles	FMWT
48	64	0	1	0	0	1	1	1 / 3	13_H
32	48	0	0	0	0	1	0	0.5 / 2	02_H
24	40	0	0	0	0	1	0	0.5 / 2	12_H
24	32	0	0	1	0	0	1	0.5 / 1	09_H
16	24	0	0	0	0	0	1	0.5 / 1	01_H

Example for flash memory read access with 1 cycle for the high time of ATDIN and 3 wait cycles



The minimum value for t_{WATD} is 10 ns, the minimum value for t_{WEQ} is 20 ns.

The minimum value for t_{RC} is 40 ns.

The maximum value for t_{ACC} is $t_{WATD} + t_{WEQ} + 5$ ns.

c: **Write Access with CPU**

Recommended settings for WTC2 to WTC0 for write access to the flash memory, FACCEN of FMCS should be set to 1 for writing, so FAC1, FAC0, EQINH bit settings then have no meaning for the write operation

Table 12-14. Without Applying Clock Modulation

CLKB Unmodulated Core Clock Frequency [MHz]	WTC2	WTC1	WTC0	Wait Cycles	FMWT
64	setting not allowed for writing				
48	1	0	0	4	X4H
40	1	0	0	4	X4H
32	0	1	0	2	X2H
24	0	1	0	2	X2H
16	0	0	1	1	X1H

Table 12-15. When Applying Clock Modulation

CLKB Core Clock Frequency [MHz]	Peak Max Frequency	WTC2	WTC1	WTC0	Wait Cycles	FMWT
48	64	setting not allowed for writing				
32	48	1	0	0	4	X4H
24	40	1	0	0	4	X4H
24	32	0	1	0	2	X2H
16	24	0	1	0	2	X2H

12.28.6 Automatic Write/Erase

Irrespective of the Flash Memory mode or other modes, writing to/erasing the flash memory unit is performed by starting the flash memory automatic algorithm.

To start the automatic algorithm, various sequences of write accesses are executed in 1 to 6 cycles. They are called Flash commands.

a: **Flash Commands**

There are four commands for starting the automatic algorithm of the Flash Memory unit; Read/Reset, Write, Chip Erase, and Sector Erase. There are also Erase Suspend and Erase Resume commands for the sector erase operation.

Next tables give the command sequence lists in the flash memory and other modes.

b: **Command Sequence**

Table 12-16. Command Sequence List (CPU access)

Command Sequence	Write Cycle of Bus	Write Cycle of First Bus		Write Cycle of Second Bus		Write Cycle of Third Bus		Read/ Write Cycle of Fourth Bus		Write Cycle of Fifth Bus		Write Cycle of Sixth Bus	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read/ Reset [a]	1	**xxxx	xxF0	–	–	–	–	–	–	–	–	–	–
Read/ Reset [a]	4	**5554	xxAA	**aaa8	xx55	**5554	xxF0	RA	RD	–	–	–	–
Write	4	**5554	xxAA	**aaa8	xx55	**5554	xxA0	PA (even)	PD (half word)	–	–	–	–
Chip Erase	6	**5554	xxAA	**aaa8	xx55	**5554	xx80	**5554	xxAA	**aaa8	xx55	**5554	xx10
Sector Erase	6	**5554	xxAA	**aaa8	xx55	**5554	xx80	**5554	xxAA	**aaa8	xx55	SA (even)	xx30
Sector Erase Suspend		Input of address **xxxx or data ($xxB0_H$) suspends sector erasing.											
Sector Erase Resume		Input of address **xxxx or data ($xx30_H$) suspends and resumes sector erasing.											

a. Two Read/Reset commands reset Flash memory to the read mode.

Addresses in the table are the values in the CPU memory space. All addresses and data are hexadecimal values, where x is any value and ** may be 08 to 0F.

Table 12-17. Command Sequence List (Flash Memory Mode)

Command Sequence	Write Cycle of Bus	Write Cycle of First Bus		Write Cycle of Second Bus		Write Cycle of Third Bus		Read/ Write Cycle of Fourth Bus		Write Cycle of Fifth Bus		Write Cycle of Sixth Bus	
		Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read/ Reset [a]	1	nxxxx	F0	–	–	–	–	–	–	–	–	–	–
Read/ Reset [a]	4	naaaa	AA	n5554	55	naaaa	F0	RA	RD	–	–	–	–
Write	4	naaaa	AA	n5554	55	naaaa	A0	PA (even)	PD (word)	–	–	–	–
Chip Erase	6	naaaa	AA	n5554	55	naaaa	80	naaaa	AA	n5554	55	naaaa	10
Sector Erase	6	naaaa	AA	n5554	55	naaaa	80	naaaa	AA	n5554	55	SA (even)	30
Sector Erase Suspend		Input of address nxxxx or data ($B0_H$) suspends sector erasing.											
Sector Erase Resume		Input of address nxxxx or data (30_H) suspends and resumes sector erasing.											

a. Two Read/Reset commands reset Flash memory to the read mode.

Addresses in the table are values for writer addresses. All addresses and data are hexadecimal values, where x is any value and n may be 0 to 7.

RA: Read address

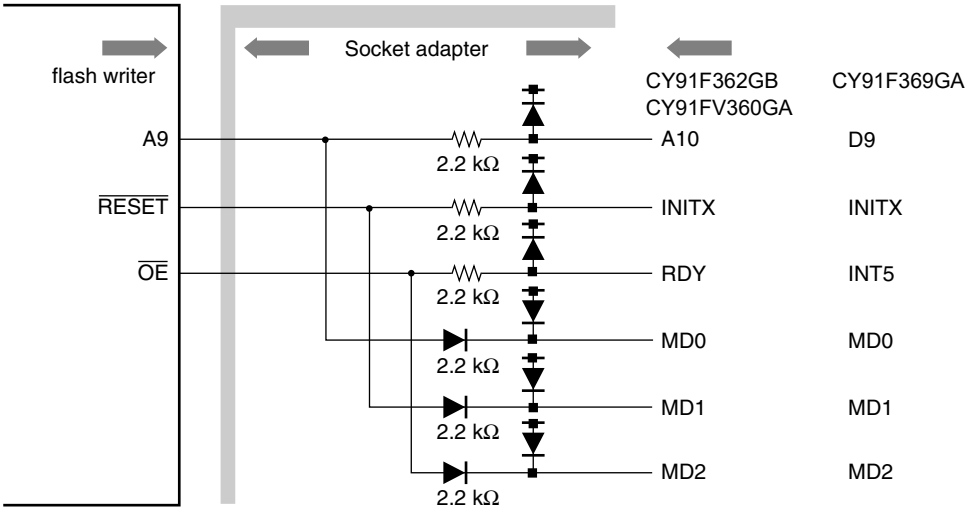
PA: Write address. Only even addresses can be specified.
SA: Sector address (See next table). Only even addresses can be specified.
RD: Read data
PD: Write data. Only word data can be specified.

Table 12-18. Sector Address for Half Word Mode

Sector	A18	A17	A16	A15	A14	A13	Address Range
SA13	1	1	1	1	1	–	$7C000_H$ to $7FFFF_H$
SA12	1	1	1	1	0	1	$7A000_H$ to $7BFFF_H$
SA11	1	1	1	1	0	0	78000_H to $79FFF_H$
SA10	1	1	1	0	–	–	70000_H to $77FFF_H$
SA9	1	1	0	–	–	–	60000_H to $6FFFF_H$
SA8	1	0	1	–	–	–	50000_H to $5FFFF_H$
SA7	1	0	0	–	–	–	40000_H to $4FFFF_H$
SA6	0	1	1	1	1	–	$3C000_H$ to $3FFFF_H$
SA5	0	1	1	1	0	1	$3A000_H$ to $3BFFF_H$
SA4	0	1	1	1	0	0	38000_H to $39FFF_H$
SA3	0	1	1	0	–	–	30000_H to $37FFF_H$
SA2	0	1	0	–	–	–	20000_H to $2FFFF_H$
SA1	0	0	1	–	–	–	10000_H to $1FFFF_H$
SA0	0	0	0	–	–	–	00000_H to $0FFFF_H$

12.28.7 Connection to Flash Memory

The Flash Memory mode of the CY91360G series devices is intended mainly for external connection to a flash memory writer. As indicated in Table Flash Control Signals, there is a slight difference between the external pins of the CY91360G series devices and the MBM29LV400C (4 Mbit flash memory). Connection to an MBM29LV400C writer requires the socket adapter.



12.28.8 Notes to Use of Flash Memory

Notes on the flash memory in CY91360G series devices are given below.

a: **Input of Hardware Reset** (INITX)

To input a hardware reset when the automatic algorithm is not started, where reading is in progress, a minimum of 500 ns should be taken at a low-level width. In this case, a maximum of 500 ns is required until data can be read from the flash memory after a hardware reset has been activated.

Similarly, to input a hardware reset when the automatic algorithm is activated, where writing/erasing is in progress, a minimum of 50 ns should be taken in a low-level width. In this case, 20 μs are required until data can be read after the executing operation has been terminated to initialize the flash memory.

A hardware reset during writing undefined data being written. A hardware reset during erasing may make the sector being erased unusable.

b: **Canceling Software Reset**, **Watchdog Timer Reset**, **and Hardware Standby**

When writing/erasing the flash memory with the CPU access and if reset conditions occur while the automatic algorithm is active, the CPU may run away. This occurs because these reset conditions cause the automatic algorithm to continue without initializing the flash memory unit, possibly preventing the flash memory unit from entering the read state when the CPU starts the sequence after the reset has been deasserted. These reset conditions should be inhibited during writing/erasing the Flash Memory.

c: **Program Access to Flash Memory**

When the automatic algorithm is operating, read access to the flash memory is disabled. With the memory access mode of the CPU set to the internal ROM mode, writing/erasing should be started after switching the program area to another area such as RAM.

In this case, when sectors containing interrupt vectors are erased, interrupt processing cannot be executed.

For the same reason, all interrupt sources should be disabled while the automatic algorithm is operating.

d: **Hold Function**

When the CPU accepts a hold request, the Write signal $\overline{WE}$ of the flash memory unit may be skewed and many cause erroneous writing/erasing. When the acceptance of a hold request is enabled, ensure that the WE bit of the FLASH control status register (FMCS) is 0.

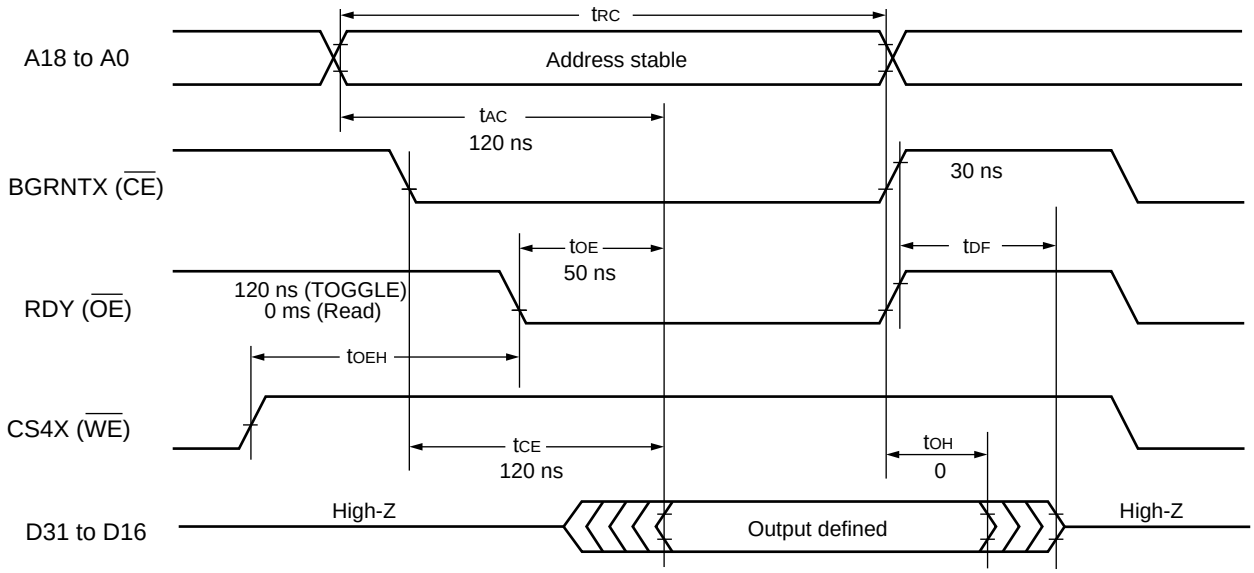
e: **Applying V_{ID}**

Applying V_{ID} required for the sector protect operation should always be started and terminated when the supply voltage is on.

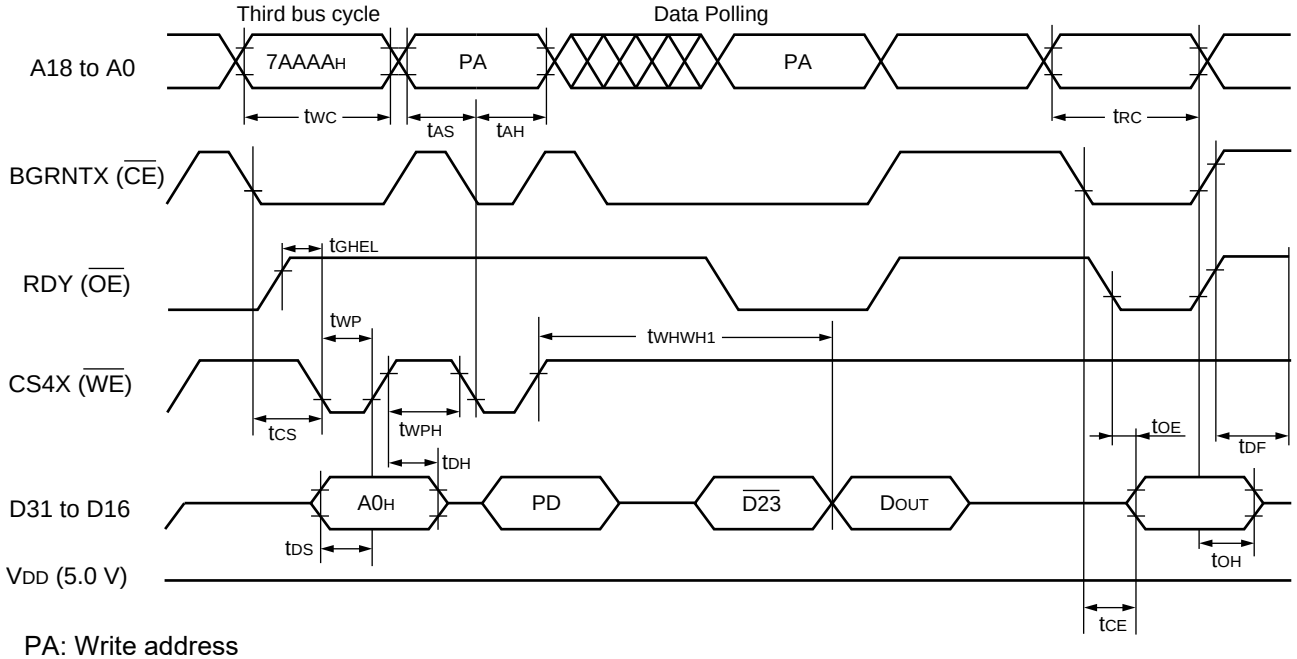
12.28.9 Timing Diagrams in Flash Mode

Each timing diagram for the external pins of the CY91360G series in the Flash Memory mode is shown below.

a: **Data read by Read Access**



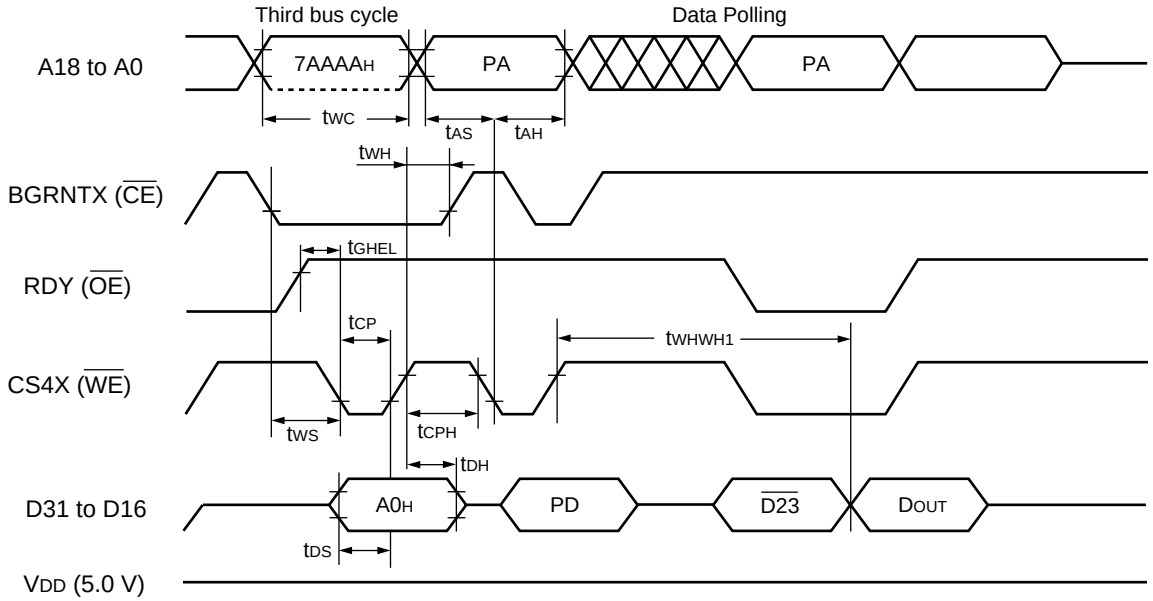
b: **Write Data Polling Read (WE control)**



PA: Write address
PD: Write data
D23: Reverse output of write data
DOUT: Output of write data

Note: The last two bus cycle sequences out of the four are described.

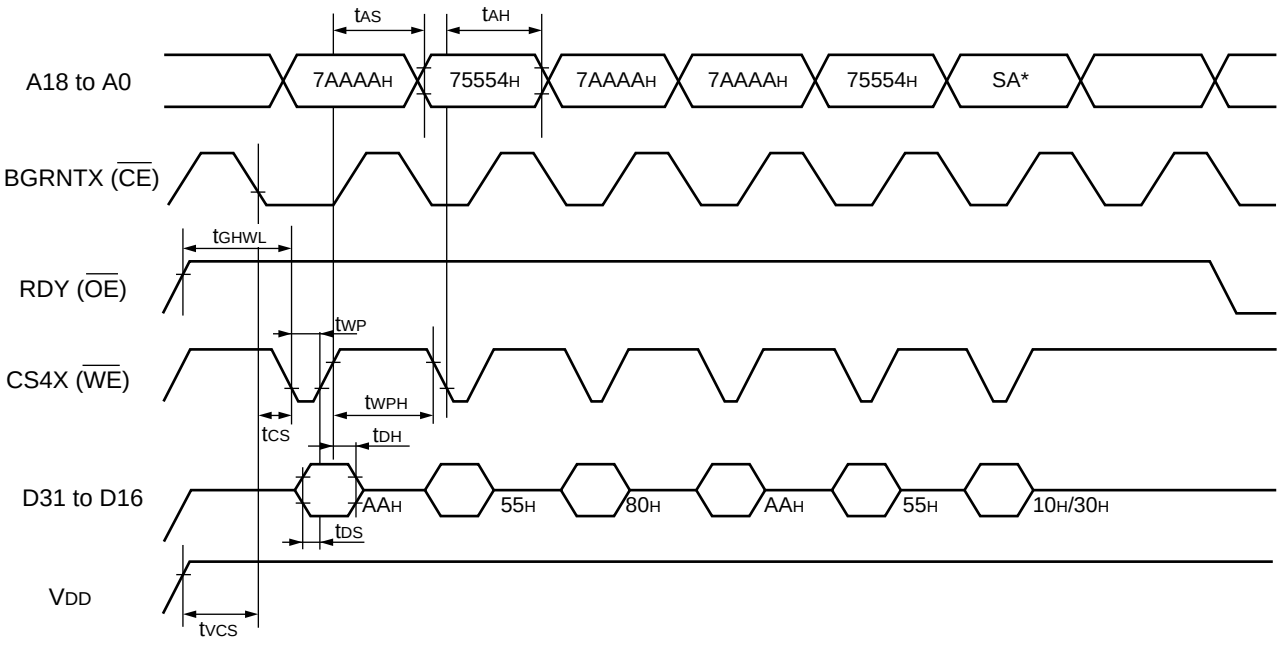
c: **Write Data Polling Read (CE control)**



PA: Write address
PD: Write data
D23: Reverse output of write data
DOUT: Output of write data

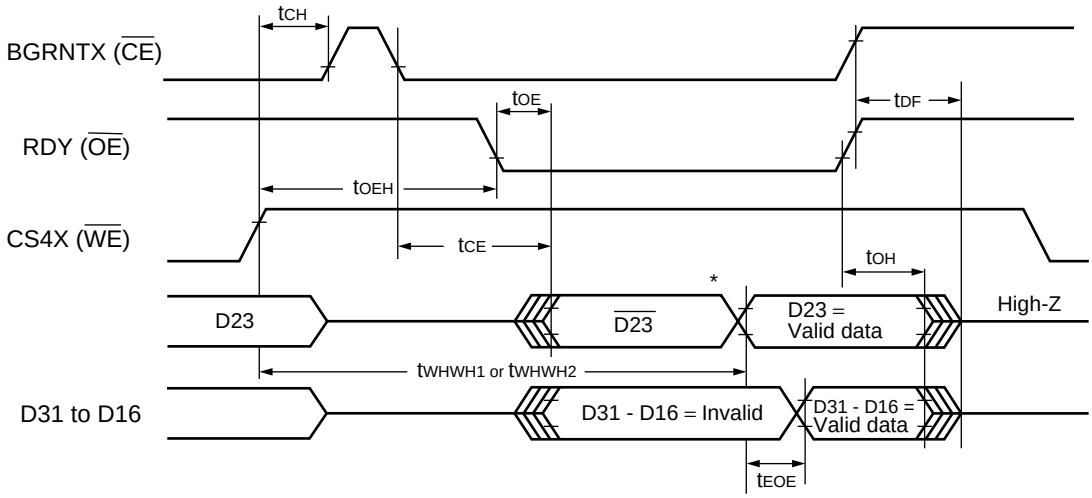
Note: The last two bus cycle sequences out of the four are described.

d: **Chip Erase/Sector Erase Command Sequence**



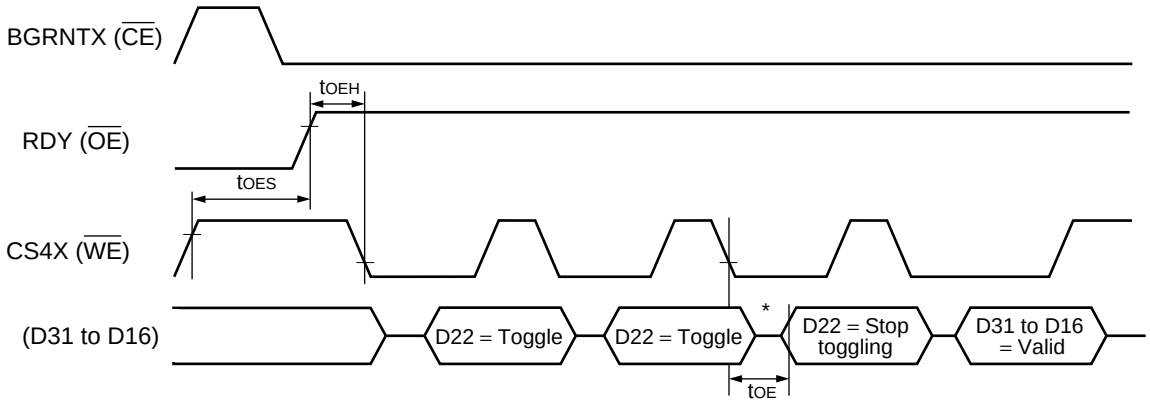
Note: SA is the sector address at sector erasing. 7AAAAH (or 6AAAAH) is the address at chip erasing.

e: **Data Polling**



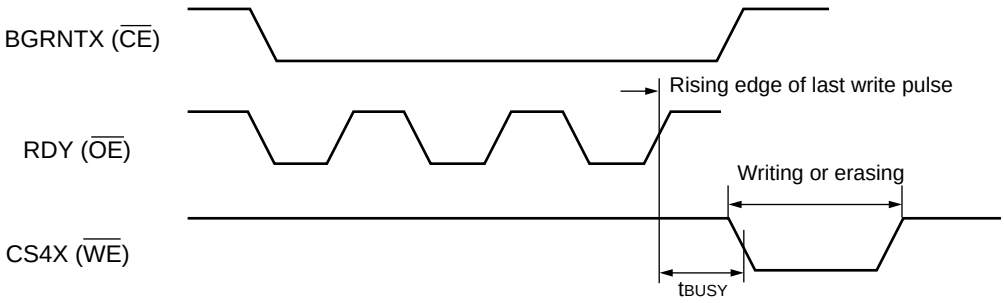
*: DQ7 is valid data (The device terminates automatic operation).

f: **Toggle Bit**

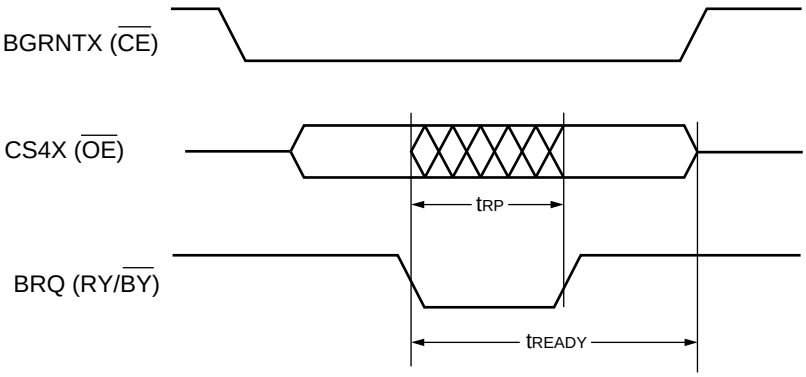


*: DQ6 stops toggling (The device terminates automatic operation).

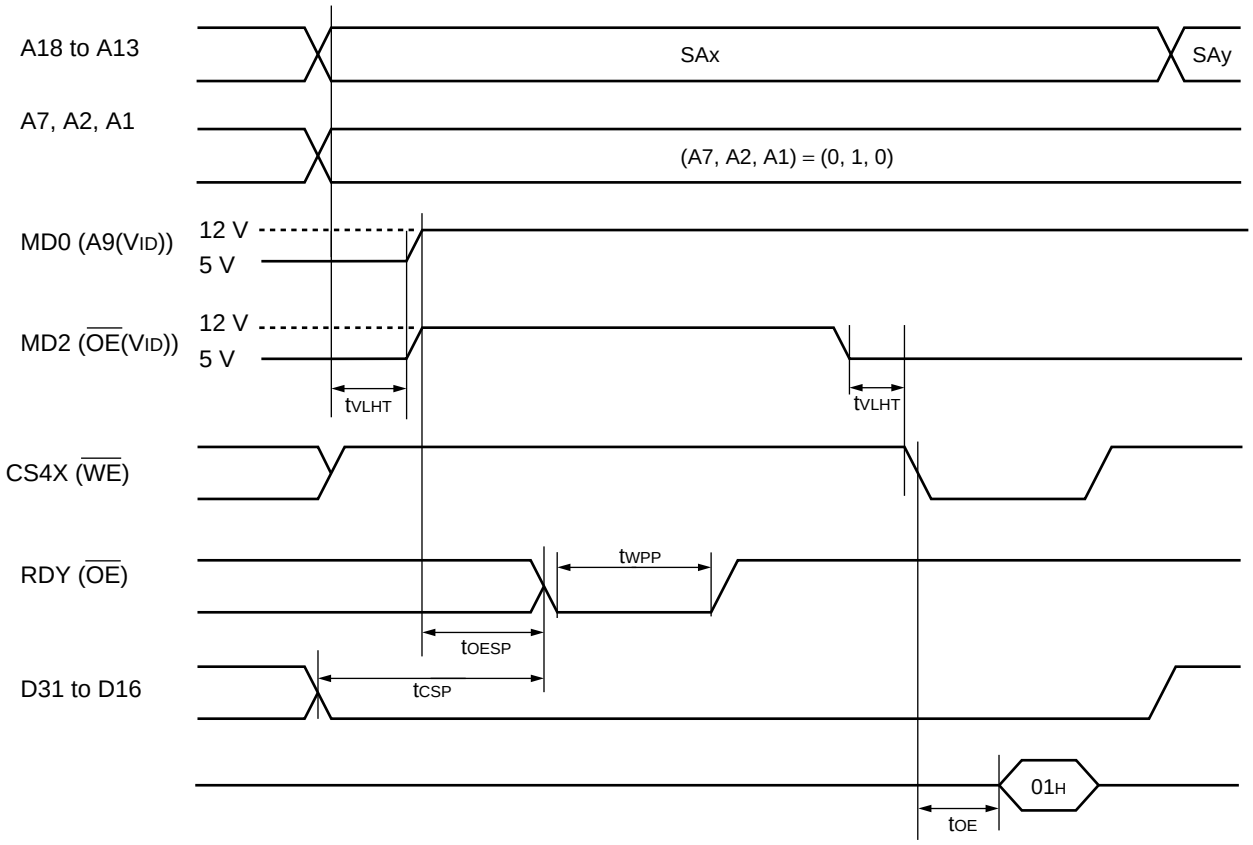
g: **RY/BY Timing during Writing/Erasing**



h: **INITX and RY/BY Timing**

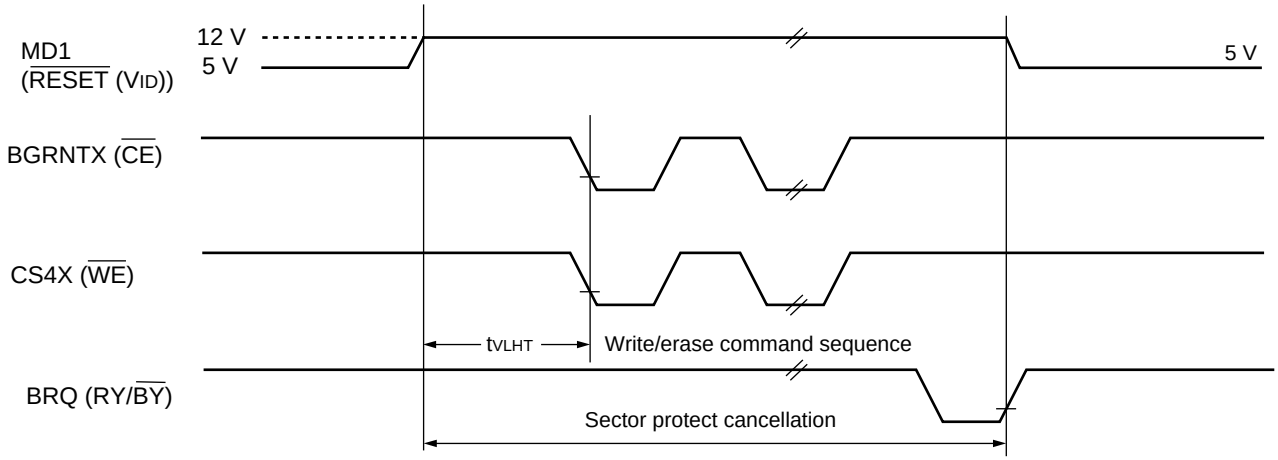


i: Enable Sector Protect/Verify Sector Protect



SA_x: First sector address
SA_y: Next sector address

j: **Temporary Sector Protect Cancellation**



12.28.10 AC Characteristics in Flash Memory Mode

The AC specifications for the external pins of the CY91360G series in the Flash Memory mode are shown below. They apply to the case where the user performs read/write access in the Flash Memory mode. They are not needed for access in the normal mode and for use of a flash memory writer.

The values are subject to change without prior notice.

a: **Read Access**

Table 12-19. AC Characteristics for Read Access

(Under recommended conditions)

Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Read cycle time	t_{RC}	–	120	–	–	ns
Address access time	t_{ACC}	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	–	–	120	ns
$\overline{CE}$ to data output	t_{CE}	$\overline{OE} = V_{IL}$	–	–	120	ns
$\overline{OE}$ to data output	t_{OE}	–	–	–	50	ns
$\overline{CE}$ to output floating	t_{DF}	–	–	–	30	ns
$\overline{OE}$ to output floating	t_{DF}	–	–	–	30	ns
Previous cycle data output hold time	t_{OH}	–	0	–	–	ns
INITX pin to return to read mode	t_{Ready}	–	–	–	20	µs

b: **Write [write/erase command] access ($\overline{WE}$ control)**

Table 12-20. AC Characteristics for Write Access ($\overline{WE}$ Control)

(Under recommended conditions)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Write cycle time		t_{WC}	120	–	–	ns
Address setup time		t_{AS}	0	–	–	ns
Address hold time		t_{AH}	50	–	–	ns
Data setup time		t_{DS}	50	–	–	ns
Data hold time		t_{DH}	0	–	–	ns
Output enable setup time		t_{OES}	0	–	–	ns
Output enable hold time	Read	t_{OEH}	0	–	–	ns
	Toggle and data polling		10	–	–	ns
Read recovery time before write		t_{GHWL}	0	–	–	ns
$\overline{CE}$ setup time		t_{CS}	0	–	–	ns
$\overline{CE}$ hold time		t_{CH}	0	–	–	ns
Write pulse width		t_{WP}	50	–	–	ns
Write pulse width High level		t_{WPH}	20	–	–	ns
Write continuation time		t_{WHWH1}	–	8	–	µs
Sector erase continuation time*[1]		t_{WHWH2}	–	1	15	s
V_{CC} setup time		t_{VCS}	50	–	–	µs

Table 12-20. AC Characteristics for Write Access ($\overline{WE}$ Control)

(Under recommended conditions)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Voltage transition time*2	t_{VLHL}	4	–	–	µs
Write pulse width*2	t_{WPP}	100	–	–	µs
OE setup time for validating $\overline{WE}$*2	t_{OESP}	4	–	–	µs
CE setup time for validating $\overline{WE}$*2	t_{CSP}	4	–	–	µs
$\overline{INIT}$ pulse width	t_{RP}	500	–	–	ns
RY/$\overline{BY}$ delay until write/erase is enabled	t_{BUSY}	50	–	–	ns

*1: The internal preprogramming time before erasing is not included.

*2: Applies only to sector protection

c: Write [write/erase command] access ($\overline{CE}$ control)

Table 12-21. AC Characteristics for Write Access ($\overline{CE}$ Control)

(Under recommended conditions)

Parameter		Symbol	Value			Unit
			Min	Typ	Max	
Write cycle time		t_{WC}	120	–	–	ns
Address setup time		t_{AS}	0	–	–	ns
Address hold time		t_{AH}	50	–	–	ns
Data setup time		t_{DS}	50	–	–	ns
Data hold time		t_{DH}	0	–	–	ns
Output enable setup time		t_{OES}	0	–	–	ns
Output enable hold time	Read	t_{OEH}	0	–	–	ns
	Toggle and data polling		10	–	–	ns
Read recovery time before write		t_{GHWL}	0	–	–	ns
$\overline{WE}$ setup time		t_{WS}	0	–	–	ns
$\overline{WE}$ hold time		t_{WH}	0	–	–	ns
$\overline{CE}$ pulse width		t_{CP}	50	–	–	ns
$\overline{CE}$ pulse width High level		t_{CPH}	20	–	–	ns
Write continuation time		t_{WHWH1}	–	16	–	µs
Sector erase continuation time*		t_{WHWH2}	–	1.5	30	s
V_{CC} setup time		t_{VCS}	50	–	–	µs
$\overline{INIT}$ pulse width		t_{RP}	500	–	–	ns
RY/$\overline{BY}$ delay until write/erase is enabled		t_{BUSY}	50	–	–	ns

*: The internal preprogramming time before erasing is not included.

13. Flash Memory Mode Signal Assignment

CY91FV360GA/F362GB/F364G/F369GA

Table 13-1. Pins Used in Flash Memory Mode

MBM29LV 400C	CY91FV360GA		CY91F362GB		CY91F364G		CY91F369GA		Remarks
	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	
A-1	202	A0	9	A0	92	PR0	157	A0	Address A(0)
A0	310	A1	10	A1	93	PR1	158	A1	Address A(1)
A1	201	A2	11	A2	94	PR2	159	A2	Address A(2)
A2	357	A3	12	A3	95	PR3	160	A3	Address A(3)
A3	257	A4	13	A4	96	PR4	136	D15	Address A(4)
A4	144	A5	14	A5	97	PR5	135	D14	Address A(5)
A5	309	A6	15	A6	98	PR6	134	D13	Address A(6)
A6	256	A7	16	A7	99	PR7	133	D12	Address A(7)
A7	200	A8	17	A8	102	LED0	132	D11	Address A(8)
A8	356	A9	18	A9	103	LED1	131	D10	Address A(9)
A9	308	A10	19	A10	104	LED2	130	D9	Address A(10)
A10	92	A11	20	A11	105	LED3	129	D8	Address A(11)
A11	44	A12	21	A12	107	LED4	128	D7	Address A(12)
A12	255	A13	22	A13	108	LED5	127	D6	Address A(13)
A13	143	A14	23	A14	109	LED6	126	D5	Address A(14)
A14	199	A15	24	A15	110	LED7	125	D4	Address A(15)
A15	307	A16	27	A16	113	PO4	124	D3	Address A(16)
A16	91	A17	28	A17	114	PO5	123	D2	Address A(17)
A17	142	A18	29	A18	115	PO6	122	D1	Address A(18)
A18	–	–	–	–	–	–	121	D0	See notes
[A20]	–	–	–	–	117	DA0	–	–	See notes
WE	140	CS4X	32	CS4X	116	PO7	72	INT4	Write enabled
BYTE	196	CS5X	33	CS5X	2	AN1	71	INT3	Byte access
OE	305	RDY	35	RDY	54	TESTX	73	INT5	Output enabled
CE	139	BGRNTX	36	BGRNTX	55	CPUTESTX	69	INT1	Chip enabled
RY/$\overline{BY}$	88	BRQ	37	BRQ	56	ATGX	68	INT0	Ready/$\overline{Busy}$ (open drain)
A9 (V_{ID})	293	MD0	111	MD0	57	MD0	58	MD0	VDA9 High voltage
$\overline{RESET}$ (V_{ID})	31	MD1	112	MD1	58	MD1	59	MD1	VDRS High voltage
$\overline{OE}$ (V_{ID})	239	MD2	113	MD2	59	MD2	60	MD2	VDOE High voltage
RESET	30	INITX	115	INITX	60	INITX	62	INITX	Reset
DQ0	46	D16	201	D16	44	IN0	139	D16	Data I/O
DQ1	95	D17	202	D17	45	IN1	140	D17	Data I/O

Table 13-1. Pins Used in Flash Memory Mode *(continued)*

MBM29LV 400C	CY91FV360GA		CY91F362GB		CY91F364G		CY91F369GA		Remarks
	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	
DQ2	1	D18	203	D18	46	IN2	141	D18	Data I/O
DQ3	148	D19	204	D19	47	IN3	142	D19	Data I/O
DQ4	205	D20	205	D20	48	OUT0	143	D20	Data I/O
DQ5	45	D21	206	D21	49	OUT1	144	D21	Data I/O
DQ6	94	D22	207	D22	50	OUT2	145	D22	Data I/O
DQ7	260	D23	208	D23	51	OUT3	146	D23	Data I/O
DQ8	312	D24	1	D24	34	INT0	147	D24	Data I/O
DQ9	204	D25	2	D25	35	INT1	148	D25	Data I/O
DQ10	147	D26	3	D26	36	INT2	149	D26	Data I/O
DQ11	93	D27	4	D27	37	INT3	150	D27	Data I/O
DQ12	259	D28	5	D28	38	INT4	151	D28	Data I/O
DQ13	203	D29	6	D29	39	INT5	152	D29	Data I/O
DQ14	146	D30	7	D30	40	INT6	153	D30	Data I/O
DQ15	258	D31	8	D31	41	INT7	154	D31	Data I/O
[$\overline{\text{TMODX}}$]	89	CS6X	34	CS6X	118	DA1	70	INT2	Test mode Pull-up
[ATDIN]	253	DREQ2	–	–	1	AN0	74	INT6	ATD test Pull-down
[EQIN]	42	A26	–	–	90	LTESTX	75	INT7	EQ test Pull-down

Notes:

- CY91F362GB:

  A19 (pin 30) and A20 (pin 32) must be pulled “L” level in Flash Memory Mode.
  At reading from Flash memory, D0 to D15 (p183 to pin 197, pin 200) are switched to the output mode.
  See “Pins not used in flash memory mode (CY91F362GB) ”.

- CY91F364G:

  DA0 (pin 117) must be pulled “H” level in Flash Memory Mode.

- CY91F369GA: Pin 70 must be pulled “H” level in Flash Memory Mode. Also, pin 74 and pin 75 must be pulled “L” level in Flash Memory Mode.
  ALARM (pin 54) must be pulled “L” level.
  The other pins should be set to open at Flash Memory Mode.

Table 13-2. Pins Not Used in Flash Memory Mode (CY91F362GB)

CY91F362GB			Remarks
Pin No.	Normal Function	Flash Memory Mode	
75, 76	DA0, DA1	Output	Open
77	ALARM	Input	Pull-down
81 to 83	TESTX, CPUTESTX, LTESTX	Input	Pull-up or open (Initial pull-up)
114	HSTX	Input	Pull-up or open (Initial pull-up)
116	MONCLK	Output	Open
117	SELCLK	Input	Pull-up
119, 121	X0, X0A	Input	Pull-down
120, 122	X1, X1A	Output	Open
124	CPO	Output	Open
125	VCI	Input	Pull-down
Other signal		Input	Pull-up

CY91F365GB/F366GB/F367GB/F368GB/F376G

Table 13-3. Pins Used in Flash Memory Mode

MBM29LV 400C	CY91F365GB/ CY91F366GB		CY91F367GB/ CY91F368GB		CY91F376G		Remarks
	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	
A-1	96	PWM1P0	96	PR0	96	PWM1P0	Address A(0)
A0	97	PWM1M0	97	PR1	97	PWM1M0	Address A(1)
A1	98	PWM2P0	98	PR2	98	PWM2P0	Address A(2)
A2	99	PWM2M0	99	PR3	99	PWM2M0	Address A(3)
A3	101	PWM1P1	101	PR4	101	PWM1P1	Address A(4)
A4	102	PWM1M1	102	PR5	102	PWM1M1	Address A(5)
A5	103	PWM2P1	103	PR6	103	PWM2P1	Address A(6)
A6	104	PWM2M1	104	PR7	104	PWM2M1	Address A(7)
A7	106	PWM1P2	106	PS0	106	PWM1P2	Address A(8)
A8	107	PWM1M2	107	PS1	107	PWM1M2	Address A(9)
A9	108	PWM2P2	108	PS2	108	PWM2P2	Address A(10)
A10	109	PWM2M2	109	PS3	109	PWM2M2	Address A(11)
A11	111	PWM1P3	111	PS4	111	PWM1P3	Address A(12)
A12	112	PWM1M3	112	PS5	112	PWM1M3	Address A(13)
A13	113	PWM2P3	113	PS6	113	PWM2P3	Address A(14)
A14	114	PWM2M3	114	PS7	114	PWM2M3	Address A(15)
A15	91	PG3	91	PG3	91	PG3	Address A(16)
A16	92	PG4	92	PG4	92	PG4	Address A(17)
A17	93	PG5	93	PG5	93	PG5	Address A(18)
A18	–	–	–	–	89	PG1	Address A(19)
[A20]	–	–	–	–	88	PG0	Pull-up See note
WE	31	BOOT	31	BOOT	31	BOOT	Write enabled
BYTE	32	TESTX	32	TESTX	32	TESTX	Byte access
OE	51	IN1	51	IN1	51	IN1	Output enabled
CE	50	IN0	50	IN0	50	IN0	Chip enabled
RY/$\overline{BY}$	38	MONCLK	38	MONCLK	38	MONCLK	Ready/$\overline{Busy}$ (open drain)
A9 (V_{ID})	57	MD0	57	MD0	57	MD0	VDA9 High voltage
$\overline{RESET}$ (V_{ID})	58	MD1	58	MD1	58	MD1	VDRS High voltage
$\overline{OE}$ (V_{ID})	59	MD2	59	MD2	59	MD2	VDOE High voltage
RESET	60	INITX	60	INITX	60	INITX	Reset
DQ0	117	PJ0	117	PJ0	117	PJ0	Data I/O
DQ1	118	PJ1	118	PJ1	118	PJ1	Data I/O
DQ2	119	PJ2	119	PJ2	119	PJ2	Data I/O
DQ3	120	PJ3	120	PJ3	120	PJ3	Data I/O

Table 13-3. Pins Used in Flash Memory Mode

MBM29LV 400C	CY91F365GB/ CY91F366GB		CY91F367GB/ CY91F368GB		CY91F376G		Remarks
	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	
DQ4	52	IN2	52	IN2	52	IN2	Data I/O
DQ5	53	IN3	53	IN3	53	IN3	Data I/O
DQ6	54	OUT0	54	OUT0	54	OUT0	Data I/O
DQ7	55	OUT1	55	OUT1	55	OUT1	Data I/O
DQ8	39	INT0	39	INT0	39	INT0	Data I/O
DQ9	40	INT1	40	INT1	40	INT1	Data I/O
DQ10	41	INT2	41	INT2	41	INT2	Data I/O
DQ11	42	INT3	42	INT3	42	INT3	Data I/O
DQ12	43	INT4	43	INT4	43	INT4	Data I/O
DQ13	44	INT5	44	INT5	44	INT5	Data I/O
DQ14	45	INT6	45	INT6	45	INT6	Data I/O
DQ15	46	INT7	46	INT7	46	INT7	Data I/O
[$\overline{\text{TMODX}}$]	33	CPUTESTX	33	CPUTESTX	33	CPUTESTX	Test mode Pull-up
[ATDIN]	63	SOT4	63	SOT4	63	SOT4	ATD test Pull-down
[EQIN]	90	PG2	90	PG2	90	PG2	EQ test Pull-down

Note: CY91F376G: At using for 768KB Flash macro, A18 is used as the append input pin of Flash macro. Line (A20) which is connected to pin 88 (PG0) should be set to “H” level.

Table 13-4. Pins Not Used in Flash Memory Mode (CY91F365GB/F366GB/F367GB/F368GB/F376G)

CY91F365GB/F366GB/F367GB/F368GB/F376G			Remarks
Pin No.	Normal Function	Pin State	
35	X0	Input	Pull-up
36	X1	Output	Open
66	SIN3	Output	Open
67	SOT3	Output	Open
68	SCK3	Output	Open
27	DA0/X0A	Output/Input	Open/Pull-up
28	DA1/X1A	Output	Open
29	ALARM	Input	Pull-up
Other signal		Input	Pull-up

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Condition
		Min	Max		
Digital supply voltage	V_{DD}-V_{SS}	–0.3	+6.0	V	
External interface supply	V_{DD}35-V_{SS}	–0.3	+6.0	V	*4
Stepper motor control supply voltage	HV_{DD}-HV_{SS}	–0.3	+6.5	V	
Storage temperature	Tstg	–55	+125	°C	
Power consumption	P_{TOT}	–	*3	W	T_A = +25°C
Digital input voltage	V_{IDIG}	–0.3*1	+5.8	V	V_{SS} = 0 V, V_{DD} = 5 V
Analog input voltage	V_{IA}	–0.3	+5.8	V	AV_{SS} = 0 V, AV_{CC} = 5 V
Analog supply voltage	AV_{CC}-AV_{SS}	–0.3	+5.8	V	AV_{SS} = 0 V
Analog reference voltage	$V_{REFH/L}$-V_{SSA}	–0.3	+5.8	V	AV_{SS} = 0 V
Static DC current into digital I/O	$I_{I/ODC}$	–2.0	+2.0	mA	$\Sigma I_{I/ODC} < I_{SRUN}$, *2
Static total DC current into digital I/O	$\Sigma \lvert I_{I/ODC} \rvert$	–	20	mA	*2

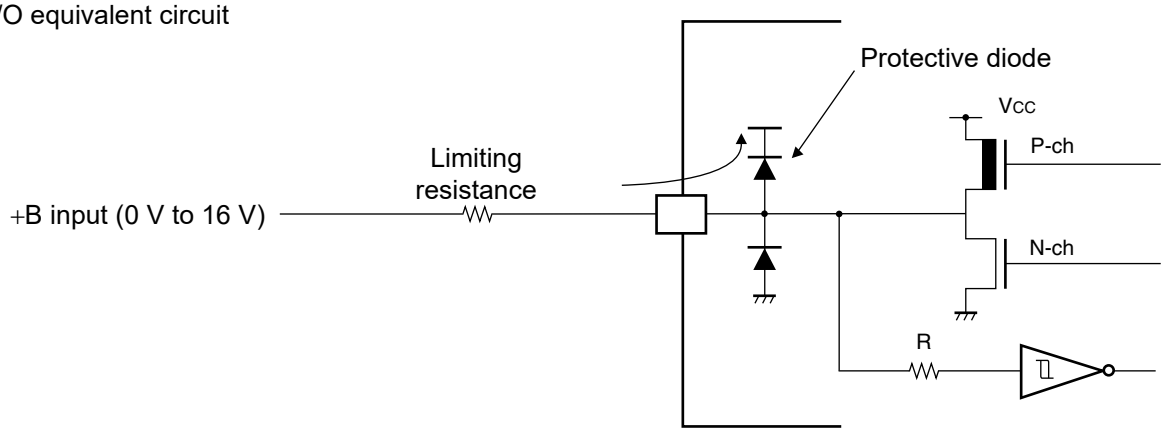
*1: Making full use of the allowed static DC correct into digital I/O will lead to lower values for V_{IDIG} Min.

*2:

- Applicable to pins: D0 to D31, A0 to A20, CS0X to CS6X, RDY, BGRNTX, BRQ, RDX, WR0X to WR3X, AS, ALE, CLK, DREQ0, DACK0, DEOP0, INT0 to INT7, SGO, SGA, SDA, SCL, SOT0, SIN0, SCK0, OCPA0 to OCPA3, TX0, TX1, RX0, RX1, SOT3, SOT4, SIN3, SIN4, SCK3, SCK4, LED0 to LED7 (CY91F362GB only), IN0 to IN3 (CY91F362GB only), OUT0 to OUT3 (CY91F362GB only), OCPA4 to OCPA7 (CY91F362GB only), SOT1, SOT2 (CY91F362GB only), SIH1, SIH2 (CY91F362GB only), SCK1, SCK2 (CY91F362GB only), PWM1P0 to PWM1P3 (CY91F362GB only), PWM1M0 to PWM1M3 (CY91F362GB only), PWM2P0 to PWM2P3 (CY91F362GB only), PWM2M0 to PWM2M3 (CY91F362GB only)
- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.

■ Sample recommended circuits

•I/O equivalent circuit



*3: Dependent on each product (see Maximum power consumption)

*4: The external interface on CY91F362GB and CY91F369GA can be operated with low voltage (typical 3.3 V) at the V_{DD}35 pins.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Table 14-1. Maximum Power Consumption

Device	Maximum Power Consumption
CY91FV360GA	2.5 W
CY91F362GB	2.5 W
CY91F364G	1.2 W
CY91F376G	1.2 W
CY91F369GA	2.5 W

Device	Maximum Power Consumption
CY91F365GB	1.3 W
CY91F366GB	1.3 W
CY91F367GB	1.3 W
CY91F368GB	1.3 W
CY91366GA	1.3 W

Table 14-2. Absolute Maximum I/O Output Current

Parameter	Symbol	Rating		Unit	I/O Circuit Type/ Remark
		Min	Max		
"L" level maximum output current *1	IOL1	–	15	mA	*3
	IOL2	–	35	mA	J (LED)
	IOL3	–	40	mA	K, M (SMC)
	IOL4	–	10	mA	Y, TA (I^2C)
	IOL5	–	20	mA	Q1 (MONCLK)
"L" level average output current *2	IOLAV1	–	4	mA	*3
	IOLAV2	–	24	mA	J (LED)
	IOLAV3	–	30	mA	K, M (SMC)
	IOLAV4	–	3	mA	Y, TA (I^2C)
	IOLAV5	–	8	mA	Q1 (MONCLK)

Table 14-2. Absolute Maximum I/O Output Current *(continued)*

Parameter	Symbol	Rating		Unit	I/O Circuit Type/ Remark
		Min	Max		
"L" level total output current	ΣIOL1	–	100	mA	*3
	ΣIOL2	–	100	mA	J (LED)
	ΣIOL3	–	240	mA	K, M (SMC)
	ΣIOL4	–	–	mA	Y, TA (I^2C) *4
	ΣIOL5	–	–	mA	Q1 (MONCLK) *4
"L" level total average output current *2	ΣIOLAV1	–	50	mA	*3
	ΣIOLAV2	–	50	mA	J (LED)
	ΣIOLAV3	–	155	mA	K, M (SMC)
	ΣIOLAV4	–	–	mA	Y, TA (I^2C) *4
	ΣIOLAV5	–	–	mA	Q1 (MONCLK) *4
"H" level maximum output current *1	IOH1	–	–15	mA	*3
	IOH2	–	–25	mA	J (LED)
	IOH3	–	–40	mA	K, M (SMC)
	IOH4	–	–10	mA	Y, TA (^2C) *4
	IOH5	–	–20	mA	Q1 (MONCLK) *4
"H" level average output current *2	IOHAV1	–	–4	mA	*3
	IOHAV2	–	–14	mA	J (LED)
	IOHAV3	–	–30	mA	K, M (SMC)
	IOHAV4	–	–3	mA	Y, TA (I^2C)
	IOHAV5	–	–8	mA	Q1 (MONCLK)
"H" level total output current	ΣIOH1	–	–100	mA	*3
	ΣIOH2	–	–50	mA	J (LED)
	ΣIOH3	–	–240	mA	K, M (SMC)
	ΣIOH4	–	–	mA	Y, TA (I^2C) *4
	ΣIOH5	–	–	mA	Q1 (MONCLK) *4
"H" level total average output current *2	ΣIOHAV1	–	–50	mA	*3
	ΣIOHAV2	–	–25	mA	J (LED)
	ΣIOHAV3	–	–155	mA	K, M (SMC)
	ΣIOHAV4	–	–	mA	Y, TA (I^2C) *4
	ΣIOHAV5	–	–	mA	Q1 (MONCLK) *4

*1: Maximum output current means peak current.

*2: Average output current = operating current x operating efficiency

*3: All I/O circuit types not specially mentioned.

*4: No total current values because there are only 2 pins for I^2C and one for MONCLK.
For an overview of the I/O circuit types, see I/O Circuit Type.

14.2 Recommended Operating Conditions

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Operating temperature		T_A	–40	–	+85	°C	Other than CY91F364G
			–40	–	+105		CY91F364G, *2
Supply voltage (Internal voltage regulator)	Digital supply	V_{DD} - V_{SS}	4.25*1	5	5.25	V	V_{DDCORE} = 3.3 V
	Stepper motor control supply	HV_{DD} - HV_{SS}	4.75	5	5.25	V	HV_{SS} = 0 V
	Analog supply	V_{DDA} - V_{SSA}	4.9	5	5.1	V	V_{SSA} = 0 V
	External interface supply	V_{DD35} - V_{SS}	3.0	3.5	3.6	V	*3
			4.25	5	5.25		
RAM data retention voltage		V_{DD} - V_{SS}	3.0	–	–	V	

*1: This is only valid if the integrated power-down reset circuit is switched-off, else a reset can be triggered at voltages less or equal than 4.5 V.
The minimum voltage is 4.75 V during operation at 64 MHz.

*2: The external interface on CY91F362GB and CY91F369GA can be operated with low voltage (typical 3.3 V) at the V_{DD}35 pins.

*3: CY91F364G can be used at T_A = +85 °C to +105 °C under the following conditions.

- The maximum frequency of core clock (f_{CLKS}) must not exceed 48 MHz.
- The total current consumption inclusive pads must not exceed 125 mA (The core current needs approx. 90 mA at 48 MHz).

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their Cypress representatives beforehand.

14.3 DC Characteristics

Parameter			Symbol	Value			Unit	Condition
				Min	Typ	Max		
Current consumption	Run mode		I_{srun}	–	–	*1	mA	T_A = +25 °C
	Sleep mode	CY91F 364G	I_{ssleep}	–	50 40	80 60	mA mA	64 MHz, T_A = +25 °C, *4 48 MHz, T_A = +25 °C, *5
		CY91F 376G	I_{ssleep}	–	60 50	120 *6 100 *6	mA mA	64 MHz, T_A = +25 °C, *4 48 MHz, T_A = +25 °C, *5
		CY91FV3 60GA	I_{ssleep}	–	200 165	250 200	mA mA	64 MHz, T_A = +25 °C, *4 48 MHz, T_A = +25 °C, *5
		all other devices	I_{ssleep}	–	145 110	170 140	mA mA	64 MHz, T_A = +25 °C, *4 48 MHz, T_A = +25 °C, *5
	RTC mode		I_{sRTC}	–	0.5 –	1.25 500	mA µA	Main clock frequency = 4 MHz T_A = +25 °C Subclock frequency = 32 kHz T_A = +25 °C
	Stop mode		I_{sstop}	–	10	200	µA	Oscillation stop T_A = +25 °C At Software Standby
Stepper motor control	H-port output voltage		V_{OHH}	HV_{DD} – 500	–	HV_{DD} – 125	mV	I_{ol} = ±30 mA, T_C = +25 °C
			V_{OHL}	HV_{SS} + 125	–	HV_{SS} + 500	mV	I_{ol} = ±30 mA, T_C = +25 °C
			V_{OHH}	HV_{DD} – 500	–	HV_{DD} – 125	mV	I_{ol} = ±27 mA, T_C = +85 °C
			V_{OHL}	HV_{SS} + 125	–	HV_{SS} + 500	mV	I_{ol} = ±27 mA, T_C = +85 °C
			V_{OHH}	HV_{DD} – 500	–	HV_{DD} – 125	mV	I_{ol} = ±30 mA, T_C = –40 °C
			V_{OHL}	HV_{SS} + 125	–	HV_{SS} + 500	mV	I_{ol} = ±30 mA, T_C = –40 °C
	SMC comparator threshold voltage		V_{THcomp}	HV_{DD} / 9 – 70	HV_{DD} / 9	HV_{DD} / 9 + 70	mV	
	Slew rate		–	–	40	–	ns	Cload = 0 pF
Alarm comparator	Threshold voltage	Over-voltage	V_{TAH}	$^4/_5$ V_{DDA} – 5%	$^4/_5$ V_{DDA}	$^4/_5$ V_{DDA} + 5%	V	(external 4 : 1 divider)
		Under-voltage	V_{TAL}	$^2/_5$ V_{DDA} – 5%	$^2/_5$ V_{DDA}	$^2/_5$ V_{DDA} + 5%	V	
	Switching hysteresis		V_{TAHYS}	12.5	25	50	mV	
	Alarm sense time		t_{AS}	–	–	10	µs	
	Input resistance		R_{in}	5	–	–	MΩ	at V_{TAH}, V_{TAL}
Power down Reset	Threshold voltage		V_{TPOR}	3.5	4.0	4.5	V	
	Switching hysteresis		$V_{TPORHYS}$	20	50	80	mV	
	Reset sense time		t_{RS}	–	–	10	µs	
Digital outputs	Output “H” voltage		V_{OH}	V_{DD} – 0.5	–	V_{DD}	V	I_{load} = –4 mA
			V_{OH35}	V_{DD35} – 0.8	–	V_{DD35}	V	I_{load} = –4 mA, *3
				V_{DD35} – 0.5	–	V_{DD35}	V	I_{load} = –2.5 mA
	Output “L” voltage		V_{OL}	V_{SS}	–	V_{SS} + 0.4	V	I_{load} = 4 mA
			V_{OL35}	V_{SS}	–	V_{SS} + 0.7 V_{SS} + 0.4	V	I_{load} = 4 mA, *3 I_{load} = 2.5 mA

Parameter			Symbol	Value			Unit	Condition
				Min	Typ	Max		
Digital Inputs*2	CMOS (Type: Q, S, Y, T)	High voltage range	V_{IH}	0.65 × V_{DD}	–	V_{DD}	V	
			V_{IH35}	0.65 × V_{DD35}	–	V_{DD35}	V	V_{DD35} < 4.25 V, *3
		Low voltage range	V_{IL}	V_{SS}	–	0.25 × V_{DD}	V	
			V_{IL35}	V_{SS}	–	0.25 × V_{DD35}	V	V_{DD35} < 4.25 V, *3
	CMOS Schmitt-Trigger (Types: E, F, U)	High voltage range	V_{IH}	0.8 × V_{DD}	–	V_{DD}	V	
		Low voltage range	V_{IL}	V_{SS}	–	0.2 × V_{DD}	V	
	CMOS Automotive level Schmitt-Trigger (Types: A, B, K1, M1, J)	High voltage range	V_{IH}	0.8 × V_{DD}	–	V_{DD}	V	
			V_{IH35}	0.8 × V_{DD35}	–	V_{DD35}	V	V_{DD35} < 4.25 V, *3
		Low voltage range	V_{IL}	V_{SS}	–	0.5 × V_{DD}	V	V_{DD}min = 4.25 V
			V_{IL35}	V_{SS}	–	0.4 × V_{DD35}	V	V_{DD35} < 4.25 V, *3
		hysteresis voltage	–	–	0.5	–	V	
	CMOS 3/5 V (Type: L, N, O)	High voltage range	V_{IH}	0.65 × V_{DD}	–	V_{DD}	V	
		Low voltage range	V_{IL}	V_{SS}	–	0.25 × V_{DD}	V	
	CMOS 3 V (Type: P, W)	High voltage range	V_{IH}	0.65 × V_{DD}	–	V_{DD}	V	
		Low voltage range	V_{IL}	V_{SS}	–	0.25 × V_{DD}	V	
		Input capacitance	C_{IN}	–	–	16	pF	
		Input leakage current	I_{IL}	–1	–	+1	µA	T_A = +25 °C
		Pull up resistor	R_{up1} R_{up2}	–	50 10	–	kΩ kΩ	Types: E, U Type: S
ADC inputs	Reference voltage input		V_{REFH} V_{REFL}	V_{REFL} + 3 V_{SSA}	–	V_{DDA} V_{REFH} – 3	V V	
	Input voltage range		V_{imax} V_{imin}	V_{REFL} –	–	V_{REFH} –	V V	
	Input resistance		R_I	–	–	3.6	kΩ	
	Input capacitance		C_I	–	–	30	pF	
	Input leakage current		I_{IL}	–1	–	+1	µA	
	Impedance of external output driving the ADC input		–	–	–	4.0	kΩ	at sampling time of 1.6 µs

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
DAC analog outputs	Output voltage	V_{out}	V_{SSA}	–	V_{DDA}	V	
	Output impedance	R_{out}	2.0	2.9	4.0	kΩ	external voltage follower required
	Output capacitance	C_{out}	–	–	20	pF	
Sound generator	Output voltage	$V_{outHIGH}$ V_{outLOW}	$V_{DD} - 0.5$ V_{SS}	–	V_{DD} $V_{SS} + 0.4$	V V	
	Output current	I_{out}	4	–	–	mA	
PPG	Output voltage	$V_{outHIGH}$ V_{outLOW}	$V_{DD} - 0.5$ V_{SS}	–	V_{DD} $V_{SS} + 0.4$	V V	
	Output current	I_{out}	4	–	–	mA	
LED	Output voltage	$V_{outHIGH}$ V_{outLOW}	$V_{DD} - 0.8$ –	–	– $V_{SS} + 0.8$	V V	$I_{outHIGH}$ = 12 mA I_{outLOW} = 24 mA
I^2C Bus Interface (Open Drain Output)	Output voltage	$V_{outHIGH}$ V_{outLOW}	– V_{SS}	–	V_{DD} $V_{SS} + 0.4$	V V	I_{outLOW} = 3 mA
	Output current	I_{out}	3	–	–	mA	I_{outLOW} = 3 mA
Lock-up time PLL1 (4 MHz →16 MHz to 64 MHz)		–	–	0.1	1	ms	
ESD Protection (Human body model AEC-Q100 compliant)		V_{surge}	1	–	–	kV	$R_{discharge}$ = 1.5 kΩ $C_{discharge}$ = 100 pF

*1: See “4. Run Mode Current/Power Consumption”.

*2: ..... Valid for bidirectional tristate I/O PAD cell.

*3: The external interface on CY91F362GB and CY91F369GA can be operated with low voltage (typical 3.3 V) at the $V_{DD}35$ pins. The parameters are tested at $V_{DD}35$ = (4.25 V to 5.5 V). The parameters at lower voltage are guaranteed by design.

*4: Sleep mode current consumption given for CLKB : CLKP : CLKT = 64 : 32 : 4 MHz, V_{DD} = 5.25 V.

*5: Sleep mode current consumption given for CLKB : CLKP : CLKT = 48 : 24 : 4 MHz, V_{DD} = 5.25 V.

*6: The current consumption values of CY91F376G are currently under evaluation.

14.4 Run Mode Current/Power Consumption

The power dissipation during normal operation is determined by the total power dissipation of the internal logic P_C, the dissipation from analog modules P_A and the power dissipation P_{IO} of the I/O buffers. Among the I/O buffers the dissipation caused by the stepper motor drivers P_{SMC} should be taken into special consideration.

So the overall power consumption P_D will be calculated as a sum of $Pc + P_A + P_{SMC} + P_{IO}$.

14.4.1 Logic Power Consumption

The following formula can be used to calculate the maximum core current consumption when the PLL is used depending on the frequency settings for the internal clocks:

$I_{CC} = B \times CLKB\ [MHz] + P \times CLKP\ [MHz] + T \times CLKT\ [MHz] + 35.5\ [mA]$

The factors B, P, and T depend of the device, see table “Current consumption factors”.

If clock modulation is used the following value must be added to this result: 0.24 [mA/MHz] × CLKB [MHz].

This results in the following values (higher clock settings are not allowed):

Table 14-3. Current Consumption Factors

Product	B [mA/MHz]	T [mA/MHz]	P [mA/MHz]	Remarks
CY91FV360GA CY91F362GB	3.45	2.52	0.72	
CY91F364G	1.25	1.70	0.40	
CY91F365GB CY91F366GB CY91F367GB CY91F368GB	2.30	2.70	0.50	
CY91366GA	2.30	2.70	0.50	
CY91F376G	1.25	1.70	0.40	
CY91F369GA	2.30	2.70	0.50	

Clock Frequencies [MHz]			Logic Current Consumption at 5.25 V [mA]	Logic Power Consumption PC at 5.25 V [W]	Remarks
CLKB	CLKP	CLKT			
64	16	16	308	1.62	no clock modulation possible
48	24	24	290	1.52	
48	16	16	264	1.39	
32	32	32	257	1.35	
32	16	16	205	1.08	
24	24	24	202	1.06	
24	12	12	163	0.86	
16	16	16	146	0.77	
2	2	2	40	0.21	no PLL, no clock modulation
0.125	0.125	0.125	30	0.16	no PLL, no clock modulation

In addition to this power consumption of the MCU core logic the following contributions to the overall power consumption have to be considered:

- Analog power consumption
- I/O and SMC power consumption

See the following sections.

14.4.2 Analog Power Consumption

Module	Typical Current Consumption	Maximum Current Consumption	Remarks
DAC		1 mA / channel	current at AV_{CC}
ADC	3 mA	7 mA	current at AV_{CC}
	1.6 mA	2.6 mA	current at AVRH
Power down reset	0.26 mA	0.5 mA	current at V_{DD}
Alarm Comparator	0.31 mA	0.5 mA	current at AV_{CC}
Zero point detection	0.13 mA	0.25 mA	current at AV_{CC}

To calculate the analog power consumption P_A, the current contributions of the active modules have to be multiplied by the maximum analog supply voltage of 5.1 V-or by the maximum digital supply voltage as in case of the Power down reset.

14.4.3 I/O and SMC Power Consumption

SMC Drivers:

The average current consumption per SMC channel is 38.2 mA, for four channels this results in 152.8 mA.
At 2 × 0.5 V this results in 153 mW power consumption P_{SMC} for four channels of stepper motor drivers.

Other I/O Buffers:

The power dissipation (P_{IO}) (at 5.25 V) of the I/O buffers is represented as the sum of the dynamic power dissipation (P_{AC5V}, P_{AC3V}) and the static power consumption (P_{DC}).

$$P_{IO} = P_{AC5V} \times 1.1 + P_{AC3V} \times 1.2 + P_{DC}$$

The following table lists values for P_{AC5V} and P_{AC3V}:

Buffer Type	Dynamic Power Dissipation P_{AC5V} P_{IB}/P_{OB} at 5V	Dynamic Power Dissipation P_{AC3V} P_{IB}/P_{OB} at 3.3V	Unit
Normal Input	12.4	12.4	µW/MHz (pF in C_L)
Bidirectional Input			
4 mA Bidirectional Output	194 + 25 C_L	85.5 + 11 C_L	
4 mA Output			
8 mA Bidirectional Output	353 + 25 C_L	154 + 11 C_L	
8 mA Output			

$P_{AC} = P_{IB} \times In \times f \times$ operating rate $+ P_{OB} \times On \times f \times$ operating rate

P_{IB}:	Power Consumption of Input Buffers and Bidirectional Inputs
P_{OB}:	Power Consumption of Output Buffers and Bidirectional Outputs
In:	Total number of input buffers and bidirectional buffer inputs
On:	Total number of output buffers and bidirectional buffer outputs
f:	System frequency
Operating rate:	1.0 if all buffers are switched simultaneously at system frequency

P_{DC} is the caused by off chip loads which are drawing static currents.

$P_{DC} = VO \times IO \times DC_N$

VO:	Output voltage drop - usually 0.4 V
IO:	Output current - usually 4 mA
DC_N:	Number of output buffers and bidirectional buffers driving off chip loads causing static currents.

14.5 Clock Settings

Clock Domain	Clock Name	Max Frequency Setting	Remark
Core	CLKB	64 MHz	under normal operating conditions
		32 MHz	
Resource bus	CLKP	32 MHz	
Ext. Bus	CLKT	32 MHz	
Clock for CAN	CANCLK	32 MHz	

14.6 Converter Characteristics

14.6.1 A/D Converter

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Resolution	–	–	–	10	Bit	
Total error	–	–	–	±5.0	LSB	overall error
Non-linearity error	–	–	–	±2.5	LSB	
Differential Non-linearity error	–	–	–	±1.9	LSB	
Zero Reading voltage	V_{0T}	AVRL – 3.5	AVRL + 0.5	AVRL + 4.5	LSB	
Full scale reading voltage	V_{FST}	AVRH – 5.5	AVRH – 1.5	AVRH + 2.5	LSB	
Input current	IA	–	3.0	7.0	mA	
Reference voltage current	IR	–	1.6	2.6	mA	
Conversion time	–	178 cycles CLKP	–	1 ms		
Ripple of supply voltage	–	–	–	±5.0	mV	

14.6.2 D/A Converter

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Resolution	–	–	–	10	Bit	
Differential linearity error	–	–0.9	–	+0.9	LSB	
Conversion time	–	–	3	–	µs	100pF external load

14.7 A/D Converter Glossary

■ **Resolution**

The smallest change in analog voltage detected by A/D converter.

■ **Linearity Error**

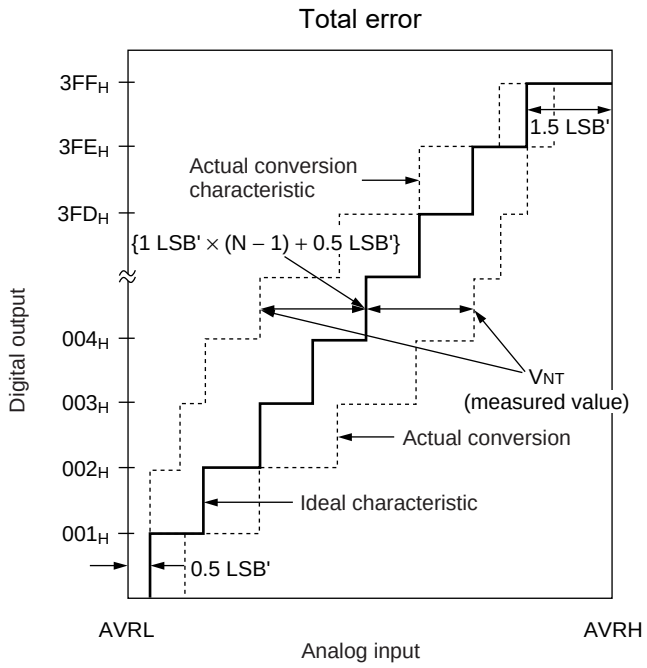
A deviation of actual conversion characteristic from a line connecting the zero-traction point (between “00 0000 0000” ↔ “00 0000 0001”) to the full-scale transition point (between “11 1111 1110” ↔ “11 1111 1111”).

■ **Differential Linearity Error**

A deviation of a step voltage for changing the LSB of output code from ideal input voltage.

■ **Total Error**

A difference between actual value and theoretical value. The overall error includes zero-transition error, full-scale transition error and linearity error.



$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB'} \times (N - 1) + 0.5\ \text{LSB'}\}}{1\ \text{LSB'}}\ [\text{LSB}]$$

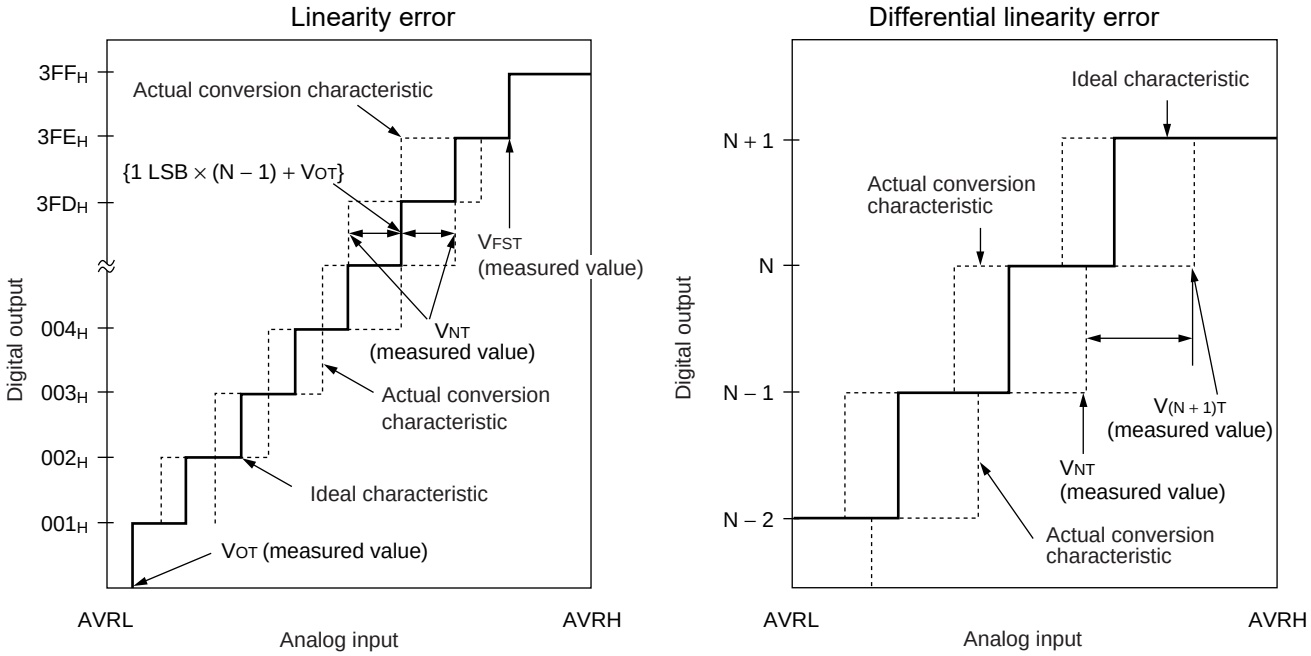
V_{OT}' (Ideal value) = AVRL + 0.5 LSB' [V]

V_{FST}' (Ideal value) = AVRH – 1.5 LSB' [V]

V_{NT}: A voltage for causing transition of digital output from (N – 1) to N

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N-1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}'} - 1\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

$$1\ \text{LSB'}\ (\text{ideal value}) = \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

V_{OT}: A voltage for causing transition of digital output from $(000)_H$ to $(001)_H$

V_{FST}: A voltage for causing transition of digital output from $(3FE)_H$ to $(3FF)_H$

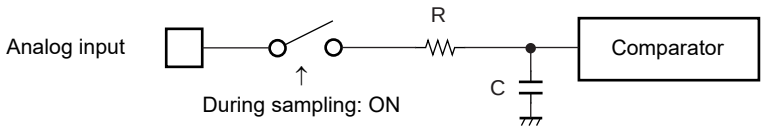
V_{NT}: A voltage for causing transition of digital output from $(N-1)_H$ to N_H

14.8 Notes on Using A/D Converter

14.8.1 About the External Impedance of Analog Input and its Sampling Time

■ A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

- Analog input circuit model



	R	C
Mask products*1	3.6 kΩ (Max)	30.0 pF (Max)
Flash products*2	3.6 kΩ (Max)	24.0 pF (Max)

*1: CY91366GA

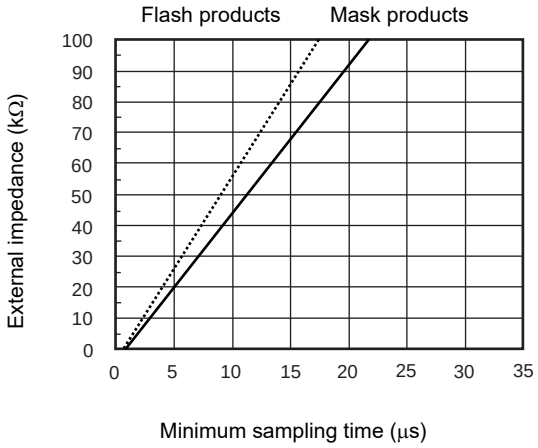
*2: CY91FV360GA/F362GB/F364G/F369GA/F365GB/F366GB/F367GB/F368GB/F376G

Note: The values are reference values.

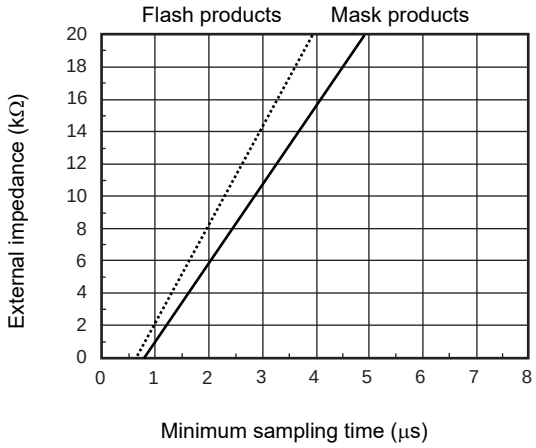
■ To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

- The relationship between the external impedance and minimum sampling time

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]



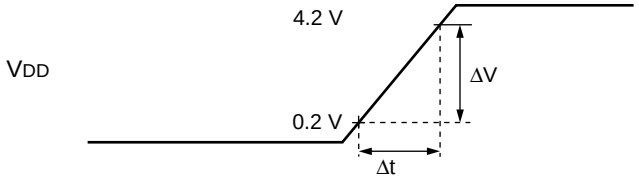
■ If the sampling time cannot be sufficient, connect a capacitor of about 0.1 μF to the analog input pin.

14.8.2 About Errors

As |AVRH − AVSS| becomes smaller, values of relative errors grow larger.

14.9 Time for Power Supply

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply raising slope	$\Delta V/\Delta t$	–	–	0.05	V/µs
Power supply raising slope	t_R	80	–	–	µs



14.10 Flash Memory

Table 14-4. Erase and Programming Performance

Parameter	Condition	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C, V_{DD} = 5.0 V	–	1	15*	s	Excludes 00H programming prior erasure
Chip erase time		–	14	–	s	Excludes 00H programming prior erasure
Half word (16-bit) programming time		–	16	3,600*	µs	Excludes system-level overhead
Erase/Program cycle	–	10,000	–	–	cycle	
Data retention time	–	100,000	–	–	h	

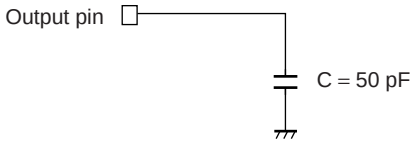
*: T_A = + 85 °C, V_{DD} = 5.0 V

14.11 AC Characteristics

14.11.1 Measurement Conditions

Parameter	Symbol	Value	Unit	Conditions
"H" level input voltage	V_{IH}	according to I/O spec	V	V_{DD} = 4.25 to 5.25 V, T_A = –40 to +85 °C
"L" level input voltage	V_{IL}		V	
"H" level output voltage	V_{OH}	0.5 × V_{DD}	V	
"L" level output voltage	V_{OL}	0.5 × V_{DD}	V	
"H" level input voltage	V_{IH}	3.0	V	V_{DD} = 3.0 to 3.6 V, T_A = –40 to +85 °C
"L" level input voltage	V_{IL}	0	V	
"H" level output voltage	V_{OH}	0.5 × V_{DD}	V	
"L" level output voltage	V_{OL}	0.5 × V_{DD}	V	

Load conditions

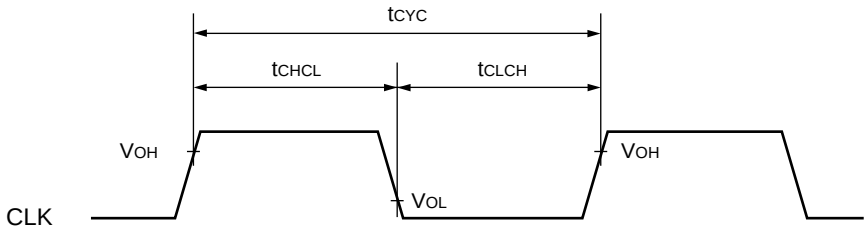


14.11.2 External Bus Clock

(V_{DD} = 4.25 V to 5.25 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
CLK cycle	t_{CYC}	CLK	t_{CPT}	–	ns
CLK rise → CLK fall	t_{CHCL}	CLK	t_{CYC} / 2 – 10	t_{CYC} / 2 + 10	ns
CLK fall → CLK rise	t_{CLCH}	CLK	t_{CYC} / 2 – 10	t_{CYC} / 2 + 10	ns

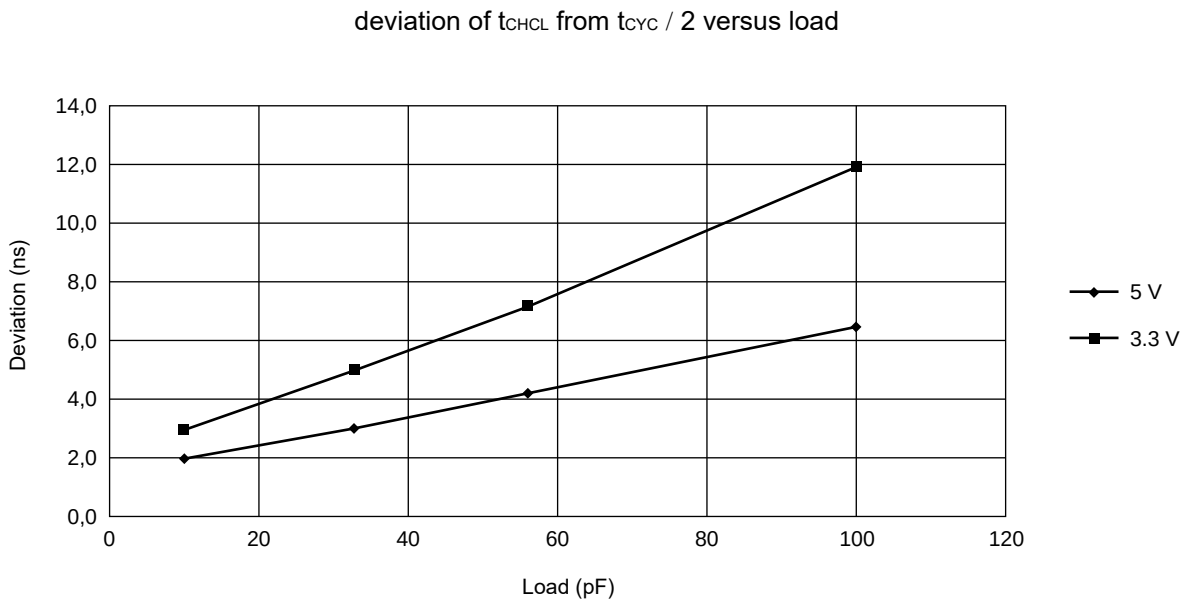
Note: This is only valid for operation without clock modulator



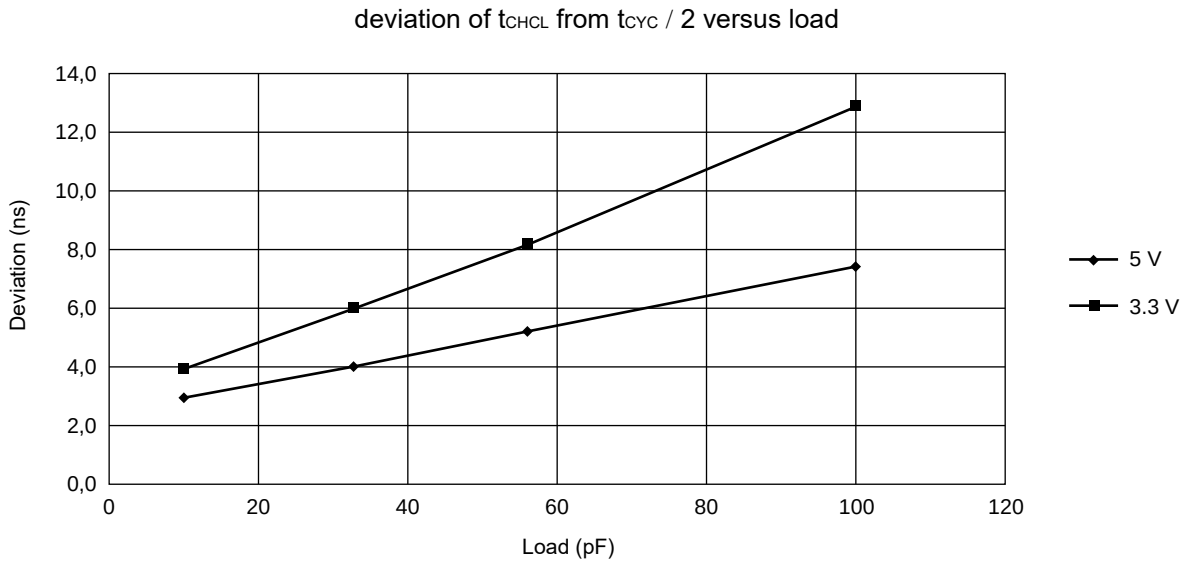
The values for t_{CHCL} and t_{CLCH} are heavily dependent on the load connected to the CLK pin. The following diagrams show this dependency for the worst case situation. The first diagram shows the situation for even division ratios between CLKB and CLKT, the second diagram shows this for odd division ratios between CLKB and CLKT (ASYMCLKT bit is not set).

It has to note that when the combination of CLK frequency and load at CLK pin is such that rise or fall times are longer than t_{CYC} / 2 the duty ratio can get worse.

Deviation of t_{CHCL} from t_{CYC} / 2 versus Load (Even CLKB/CLKT division ratios):



Deviation of t_{CHCL} from t_{CYC} / 2 versus Load (Odd CLKB/CLKT division ratios):



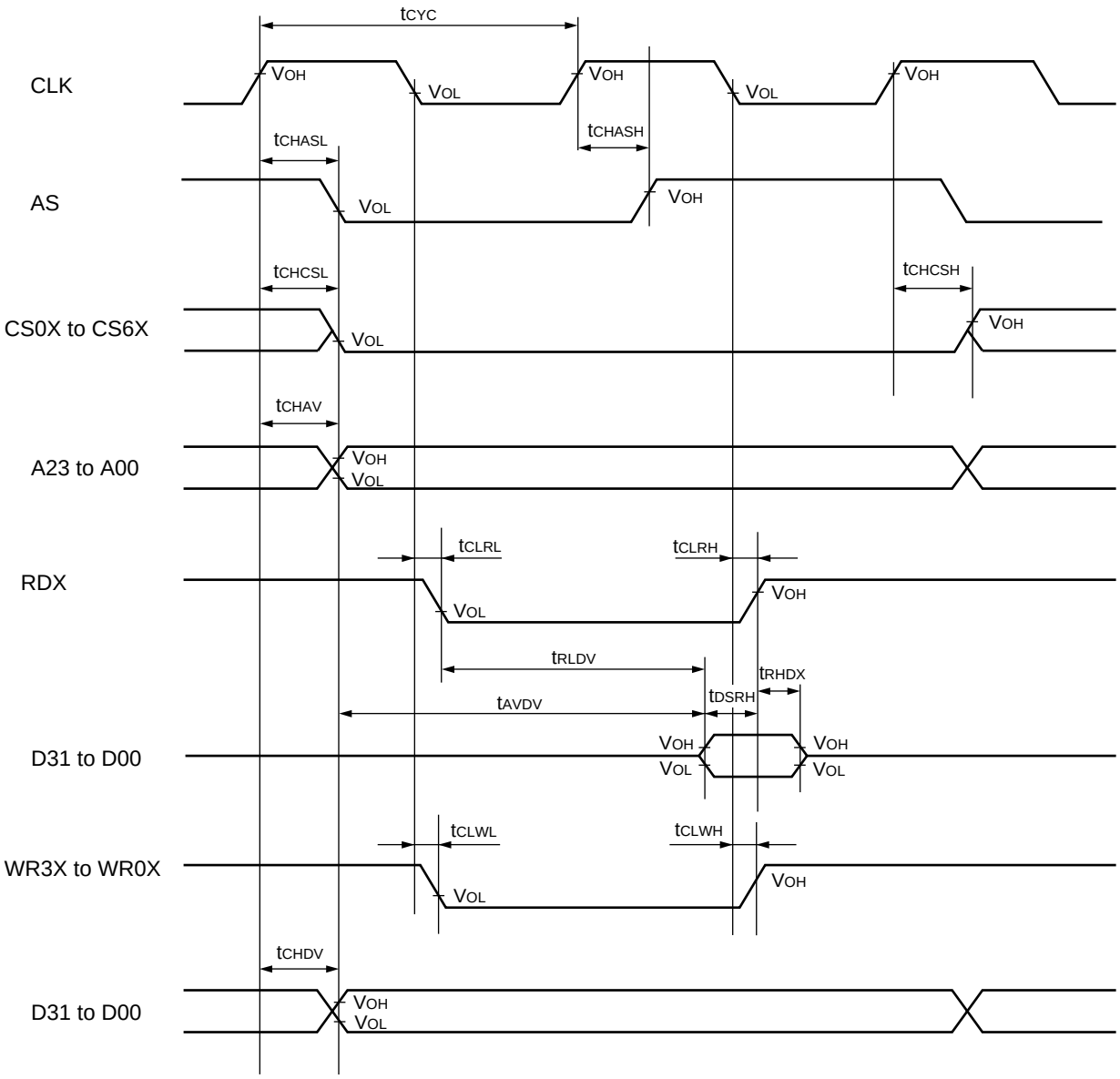
14.11.3 External Bus Interface

(V_{DD} = 4.25 V to 5.25 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
CS6X to CS0X delay time	t_{CHCSL}	CLK, CS6X to CS0X	–	15	ns
CS6X to CS0X delay time	t_{CHCSH}		–	15	ns
Address delay time	t_{CHAV}	CLK, A20 to A0	–	20	ns
Data delay time	t_{CHDV}	CLK, D31 to D0	–	16	ns
RDX delay time	t_{CLRL}	CLK, RDX	–	15	ns
RDX delay time	t_{CLRH}		–	15	ns
WR3X to WR0X delay time	t_{CLWL}	CLK, WR3X to WR0X	–	15	ns
WR3X to WR0X delay time	t_{CLWH}		–	15	ns
Effective address ⇒ Effect data input time	t_{AVDV}	A20 to A0, D31 to D0	–	$3 / 2 \times t_{CYC} - 30$	ns
RDX (↓) → Effect data input time	t_{RLDV}	RDX, D31 to D0	–	$t_{CYC} - 20$ *1 $t_{CYC} - 25$ *2	ns
Data set up → RDX (↑) time	t_{DSRH}		25 *1 30 *2	–	ns
RDX (↑) → Data hold time	t_{RHDX}		0	–	ns
AS delay time	t_{CHASL}	CLK → AS	–	15	ns
AS delay time	t_{CHASH}	CLK → AS	–	15	ns

*1: Values valid for 4.25 V ≤ VDD ≤ 5.25 V

*2: Values valid for 3.00 V ≤ VDD ≤ 4.25 V


tCYC
CLK
VOH
VOL
tCHASH
tCHASL
AS
tCHCSL
tCHCSH
CS0X to CS6X
tCHAV
A23 to A00
tCLRL
tCLRH
RDX
tRLDV
tRHDX
tDSRH
tAVDV
D31 to D00
tCLWL
tCLWH
WR3X to WR0X
tCHDV
D31 to D00

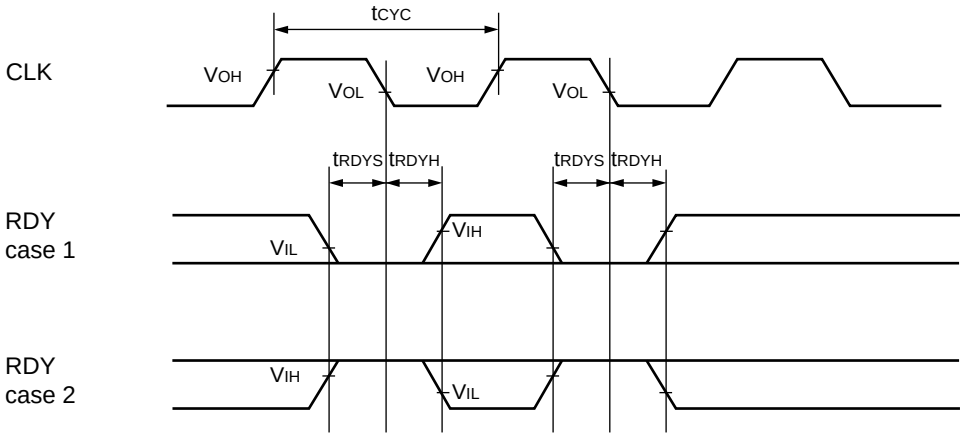
14.11.4 RDY

(V_{DD} = 4.25 V to 5.25 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
RDY setup	t_{RDYS}	CLK, RDY	16 *1 25 *2	–	ns
RDY hold	t_{RDYH}	CLK, RDY	0	–	ns

*1: Values valid for 4.25 V ≤ VDD ≤ 5.25 V

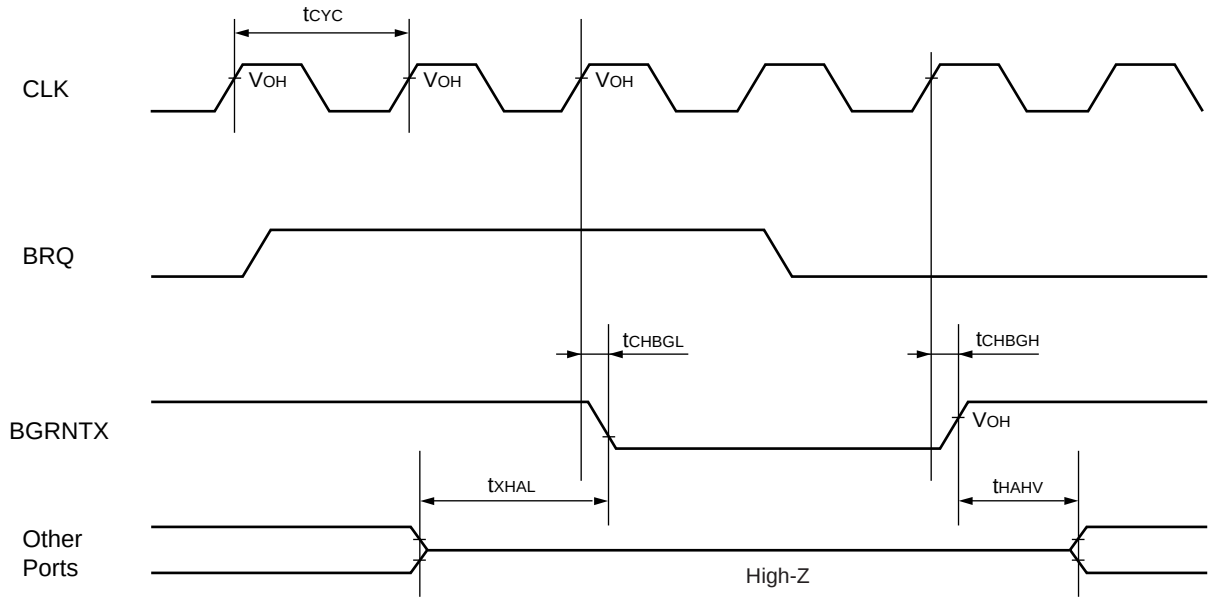
*2: Values valid for 3.00 V ≤ VDD ≤ 4.25 V



14.11.5 BGRNTX

(V_{DD} = 4.25 V to 5.25 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
BGRNTX	t_{CHBGL}	CLK, BGRNTX	–	10	ns
BGRNTX	t_{CHBGH}		–	10	ns
Bus access enabled BGRNTX falling	t_{XHAL}	BGRNTX	tcyc - 15	tcyc + 15	ns
Bus access disabled BGRNTX rising	t_{HAHV}		tcyc - 15	tcyc + 15	ns

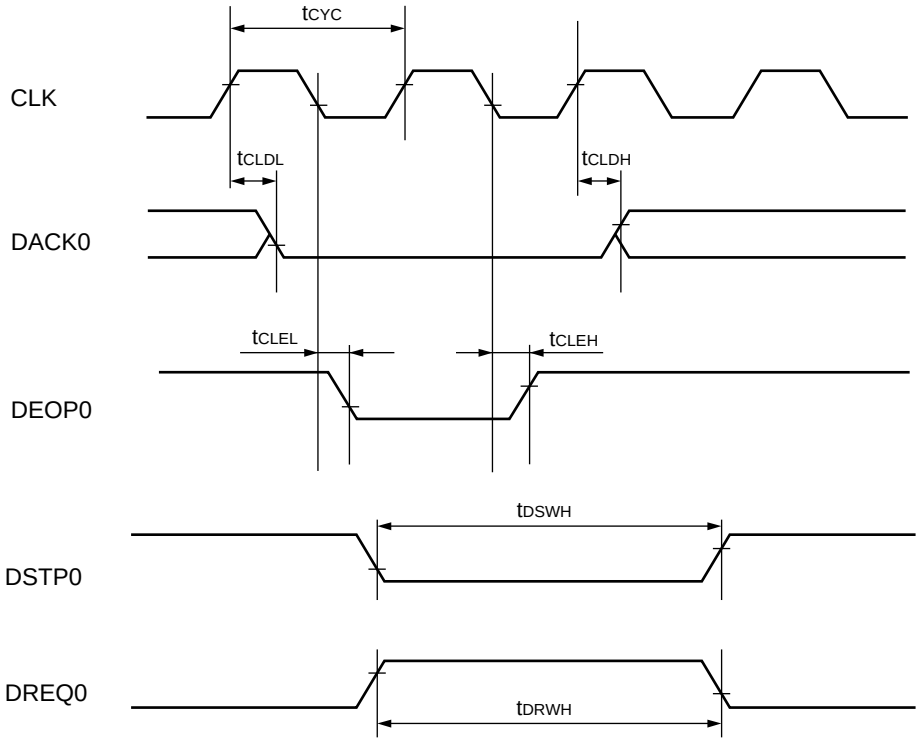


14.11.6 DMA

(V_{DD} = 4.25 V to 5.25 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin Name	Value		Unit
			Min	Max	
DREQ	t_{DRWH}	DREQ0	5t_{CYC}	–	ns
DSTP	t_{DSWH}	DSTP0*	5t_{CYC}	–	ns
DACK	t_{CLDL}	CLK, DACK0	–	20	ns
	t_{CLDH}		–	20	
DEOP	t_{CLEL}	CLK, DEOP0	–	20	ns
	t_{CLEH}		–	20	

*: DSTP and DEOP share a pin. The pin is possible to change DSTP and DEOP functions using a port function register.



15. Package Thermal Resistance and Max Allowed Power Consumption

Package	Thermal Resistance [°C/W]				Maximum Allowed Power Consumption [W] *
	θja (junction to ambient)			θjc (junction to case)	
	0 m/s	1 m/s	3 m/s		
LQM120	30	27	25	5	1.33
HQA160	16	13	11	2.5	2.5
HQB208	16	13	11	2.5	2.5

*: The maximum allowed ambient temperature is +85 °C, the maximum allowed junction temperature is +125 °C. Under these conditions, the maximum allowed power consumption will be

$P_{MAX} = (125\ °C - 85\ °C) \ / \ \theta ja\ (K/W)$

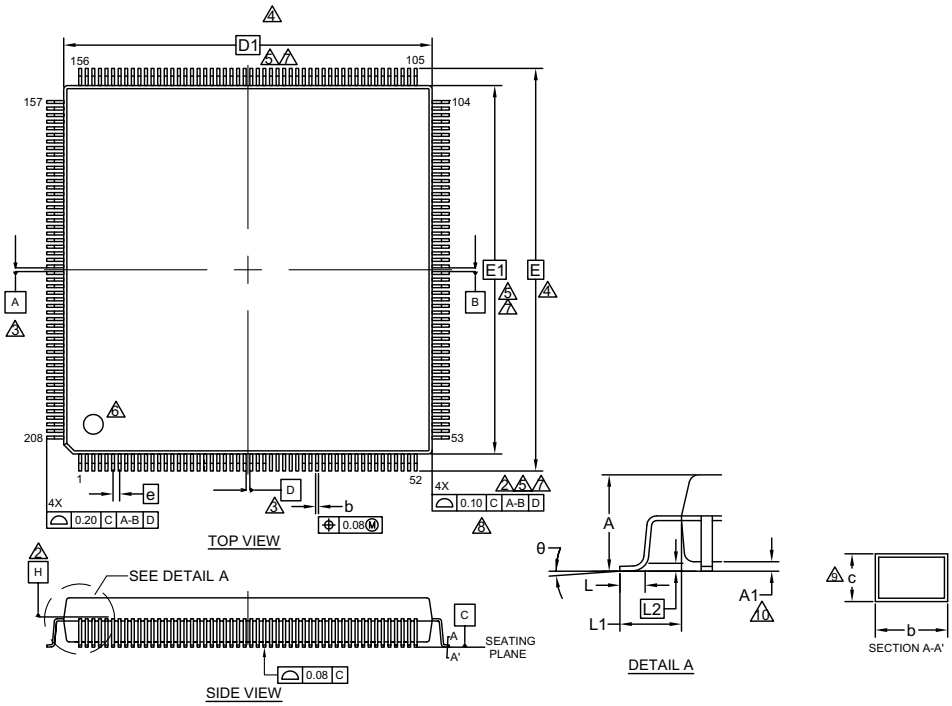
θja is the thermal resistance of this package at 0 m/s when used on a multi-layer board with separate power and ground planes.

16. Ordering Information

Part Number	Package	Remarks
CY91F362GBPVSR-G-UJE2	208-pin plastic QFP (HQB208)	
CY91F376GSPMC3-GS-UJE2	120-pin plastic LQFP (LQM120)	

17. Package Dimensions

Package Type	Package Code
208-pin Plastic QFP	HQB208



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	3.95
A1	0.25	—	0.50
b	0.17	0.22	0.27
c	0.09	—	0.20
D	30.60 BSC		
D1	28.00 BSC		
e	0.50 BSC		
E	30.60 BSC		
E1	28.00 BSC		
θ	0°	—	8°
L	0.45	0.60	0.75
L1	1.30 REF		
L2	0.25 BSC		

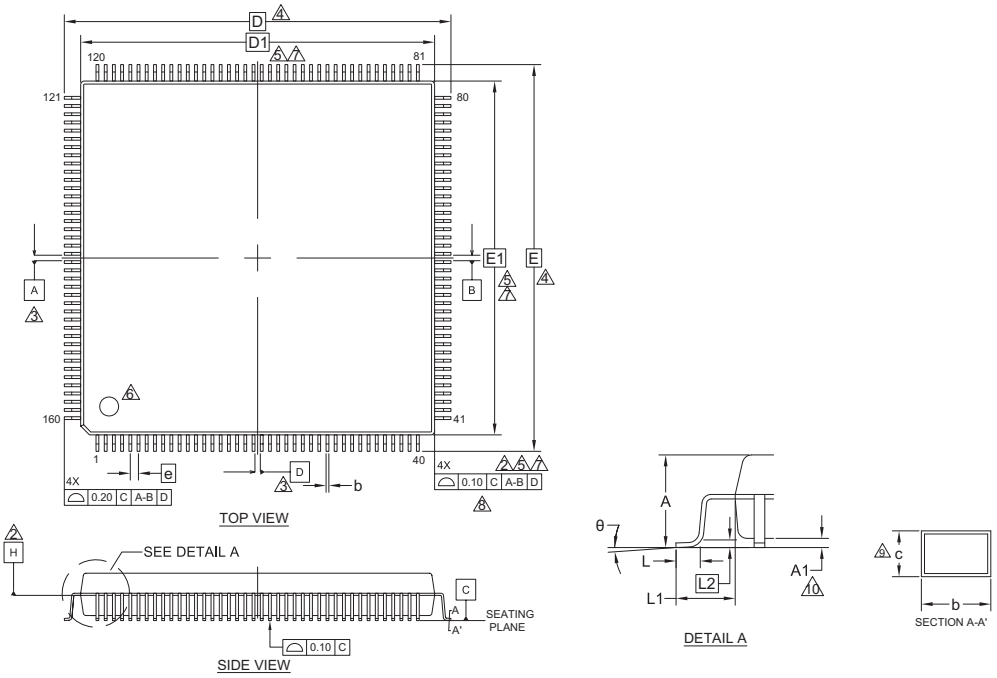
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-18454 **

PACKAGE OUTLINE, 208 LEAD QFP
28.00X28.00X3.95 MM HQB208 REV*.*

Package Type	Package Code
160-pin Plastic QFP	HQA160



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	4.10
A1	0.25	—	0.50
b	0.25	0.32	0.40
c	0.14	—	0.22
D	31.20 BSC		
D1	28.00 BSC		
e	0.65 BSC		
E	31.20 BSC		
E1	28.00 BSC		
θ	0°	—	8°
L	0.73	0.88	1.03
L1	1.60 REF		
L2	0.25 BSC		

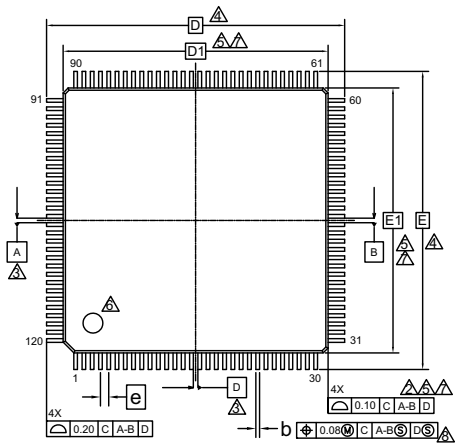
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

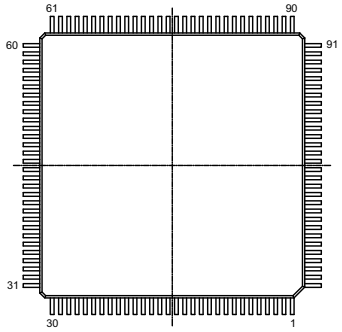
002-19674 **

PACKAGE OUTLINE, 160 LEAD QFP
28.00X28.00X4.10 MM HQA160

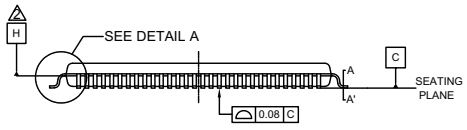
Package Type	Package Code
120-pin plastic LQFP	LQM120



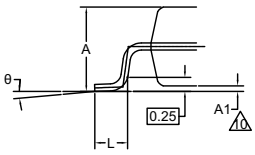
TOP VIEW



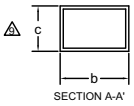
BOTTOM VIEW



SIDE VIEW



DETAIL A



SECTION A-A'

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.115	—	0.195
D		18.00 BSC	
D1		16.00 BSC	
e		0.50 BSC	
E		18.00 BSC	
E1		16.00 BSC	
L	0.45	0.60	0.75
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
11. JEDEC SPECIFICATION NO. REF: N/A.

002-16172 **

PACKAGE OUTLINE, 120 LEAD LQFP
18.0X18.0X1.7 MM LQM120 REV**

18. Major Changes

Spansion Publication Number: DS07-16401-4Ea

Page	Section	Change Results
Rev. *B		
213	16. Ordering Information	Revised Marketing Part Numbers as follows: Before) - MB91F362GBPFVS - MB91F376GPMT After) - CY91F362GBPVSR-G-UJE2 - CY91F376GSPMC3-GS-UJE2 Removed Marketing Part Numbers as follows: Before) - MB91F369GAPQS1 - MB91F365GBPMT - MB91F366GBPMT - MB91F367GBPMT - MB91F368GBPMT - MB91366GAPMT - MB91F364GPMT
217	Major Changes	Added section “18. Major Changes”.
218	Document History	Added Document History
Rev. *C		
197	DC Characteristics	Revised the shading parts as below: 14.3 DC Characteristics Parameter: Before) ESD Protection (Human body model MIL883-B compliant) After) ESD Protection (Human body model AEC-Q100 compliant) Value: Min: Before) 2 kV After) 1 kV

19. Document History Page

Document Title: CY91FV360GA/F362GB/F364G/CY91F365GB/366GA/F366GB/CY91F367GB/F368GB/F369GA/F376G, 32-bit Microcontroller FR50 CY91360G Series Document Number: 002-08044			
Revision	**ECN**	**Submission Date**	**Description of Change**
**	–	06/17/2005	Migrated to Cypress and assigned document number 002-08044. No change to document contents or format.
*A	6059170	02/05/2018	Deleted MB91FV360GACR and PGA-401C-A02 package. Changed following packages; FPT-208P-M04 --> HQB208 FPT-160P-M15 --> HQA160 FPT-120P-M21 --> LQM120 Updated to Cypress template.
*B	6952285	08/20/2020	Revised the following items: Marketing Part Numbers changed from an MB prefix to a CY prefix. 16. Ordering Information 18. Major Changes For details, please see Major Changes section.
*C	7167796	06/23/2021	Revised the following items: 14.3 DC Characteristics For details, please see Major Changes section. Updated to new template.

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