LT3383
Multioutput Power Management Solution with 4 Buck Switching and 3 LDO Linear Regulators

DESCRIPTION

DC2984A is a multi-output power management solution demonstration circuit, featuring the LT®3383. It contains two 2.5A synchronous step-down DC-DC regulators, two 1.5A synchronous step-down DC-DC regulators and three 300mA LDO regulators. All the regulators can be enabled via its corresponding enable pins. The startup sequence of the regulators can be programmed by connecting the outputs of the regulators to the enable pins in desired order.

Design files for this circuit board are available.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		2.7		5.5	V
V_{BUCK1}	BUCK1 Output Voltage	BUCK1 enabled, I(BUCK1) = 0~2.5A		1.20		V
V_{BUCK2}	BUCK2 Output Voltage	BUCK2 enabled, I(BUCK2) = 0~2.5A		1.50		V
V_{BUCK3}	BUCK3 Output Voltage	BUCK3 enabled, I(BUCK3) = 0~1.5A		1.81		V
V_{BUCK4}	BUCK4 Output Voltage	BUCK4 enabled, I(BUCK4) = 0~1.5A		3.31		V
V_{LDO1}	LDO1 Output Voltage	LDO1 enabled, I(LDO1) = 0~300mA		1.20		V
V_{LDO2}	LDO2 Output Voltage	LDO2 enabled, I(LDO2) = 0~300mA		0.80		V
V_{LDO2}	LDO3 Output Voltage	LDO3 enabled, I(LDO3) = 0~300mA		1.80		V

BOARD PHOTO

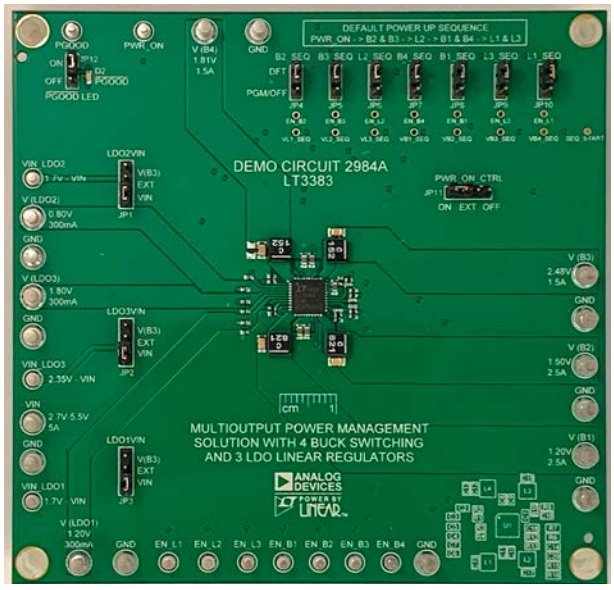


Figure 1. DC2984A Board Photo

QUICK START PROCEDURE

Follow the procedure below to familiarize yourself with the DC2984A.

1. Refer to Figure 2, configure the jumpers on the demo board as follows:

   JP1 = VIN

   JP2 = VIN

   JP3 = VIN

   JP4-JP10 = DFT

   JP11 = ON

   JP12 = ON

2. Set PS1 to 5V, with 5A current limit. Turn on PS1. All the regulators should come up in a default sequence:

   B2 & B3 -> L2 -> B1 & B4 -> L1 & L3

3. The PGOOD LED D2 should stay off, indicating all outputs are in regulation. Check the output voltage of all the regulators, they should read close to the following values:

   V_{VM1} = 1.2V

   V_{VM2} = 1.5V

   V_{VM3} = 2.48V

   V_{VM4} = 1.81V

   V_{VM5}= 1.2V

   V_{VM6}= 0.8V

   V_{VM7} = 1.8V

4. Set each electronic load to its corresponding current level indicated in Figure 2. Turn on each load. The PGOOD LED D2 should stay off, indicating all the outputs are still in regulation under loads. Note that if there are not enough electronic loads for all the regulators, this test can be done sequentially.

5. Optional: The default input of the three LDOs are from VIN. To increase the efficiency, the LDOs can be powered from BUCK3 by configuring JP1-JP3 to V(B3). They can also be powered from external source by configuring these jumpers to EXT and connecting an external supply to the corresponding VIN_LDOX.

6. Optional: The power up sequence can be programmed by configuring JP4-JP10 to PGM/OFF. Referring to Power Up Sequence Programming Section shown in Figure 2, connect the SEQ_START (TP21) to the enable test point of the first regulators to power up. Then connect the subsequent regulators enable test points (TP5-TP11) to the corresponding VX_SEQ (TP14-TP20) according to the desired startup sequence. If the enable test point of a regulator is not connected and the jumper is at PGM/OFF position, this regulator is turned off.

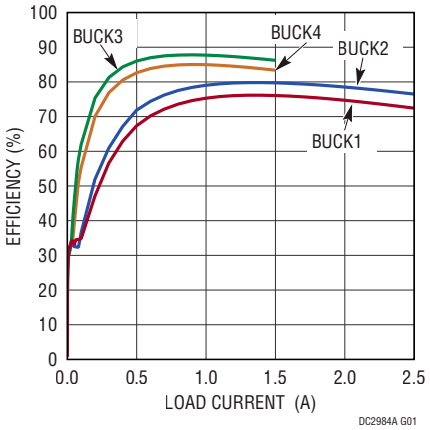
JUMPER DESCRIPTIONS

JUMPER	NAME	FUNCTION	POSITION	DESCRIPTION
JP1-JP3	LDO_XVIN	Input for the LDOs	V(B3)	Input from BUCK3
			EXT	Input from external source connected to VIN_LDO_X turret
			VIN	Input from VIN turret
JP4-JP10	B_X_SEQ or L_X_SEQ	Power up sequence for the regulators	DFT	Default power up sequence
			PGM/OFF	Programmed sequence/Regulator off
JP11	PWR_ON_CTRL	Power On master enable and disable status selection	ON	PWR_ON allows enable pin operation
			EXT	PWR_ON status controlled by external source connected to PWR_ON turret
			OFF	PWR_ON inhibits enable pin operation
JP12	$\overline{\text{PGOOD}}$ LED	Enable/disable Power Good LED indicator (indicating output not in regulation)	ON	Power Good LED indicator enabled
			OFF	Power Good LED indicator disabled

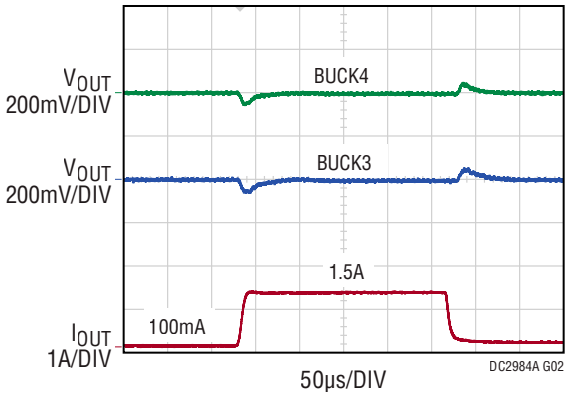
PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

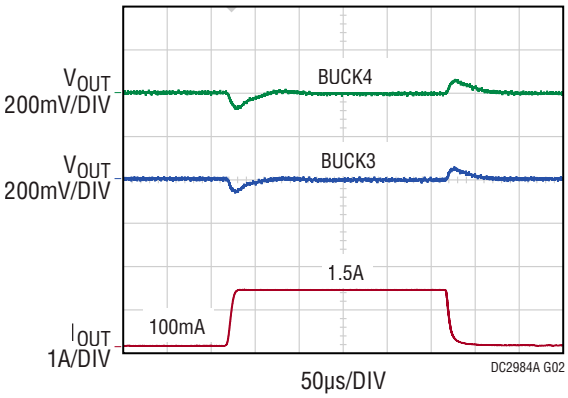
BUCK1-BUCK4 Efficiency



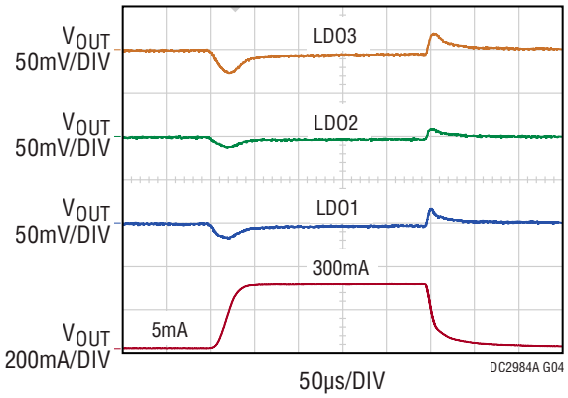
BUCK1-BUCK2 Load Transient Response



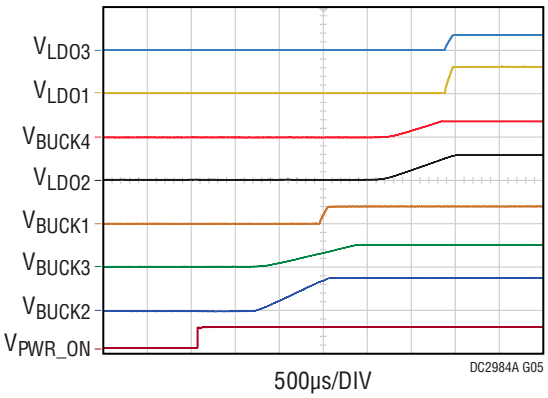
BUCK3-BUCK4 Load Transient Response



LDO1-LDO3 Load Transient Response



Default Regulators Power-Up Sequencing



TEST SETUP

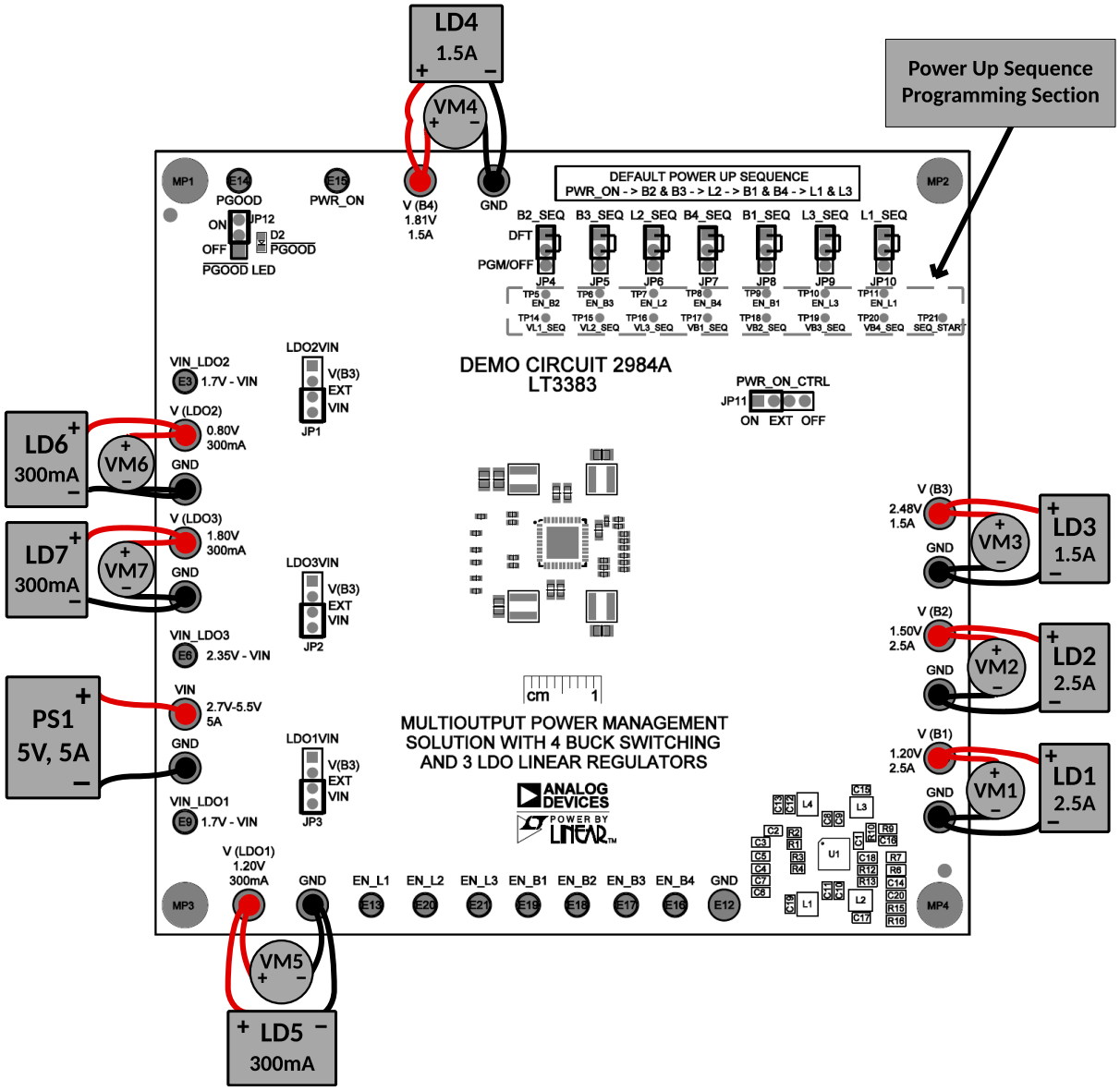


Figure 2. Test Setup for DC2984A Demo Board

OPERATION

Introduction to the DC2984A

The DC2984A a multi-output power management solution featuring the LT3383. It contains four synchronous buck regulators and three LDO regulators. Among the four buck regulators, BUCK1 and BUCK2 deliver up to 2.5A output current, while BUCK3 and BUCK4 deliver up to 1.5A output current. All three LDOs deliver up to 300mA output current. BUCK1-BUCK4 have default output voltages of 1.2V, 1.5V, 2.48V and 1.81V, respectively. LDO1 and LDO2 have default output voltages of 1.2V and 0.8V respectively. These voltages are configured by voltage dividers on the corresponding FB pins and can be changed by the user. LDO3 has a fixed voltage of 1.8V.

Power Up Sequencing

The LT3383 regulators can be powered up in any order by pin-strapping outputs to enable pins. The enable pins have a 0.75V (typical) input voltage threshold. If any enable is driven high, the remaining enable input thresholds switch to an 400mV threshold. There is a built-in 450µs delay from the enable pin threshold crossing to the internal enable of the regulator.

The DC2984A has a default power up sequence. User can also program the power up sequence by selecting JP4-JP10 to PGM/OFF position and connecting the output rails to the enable pins at the Power Up Sequence Programming Section shown in Figure 2. The start of the sequence is the rising edge of the PWR_ON pin. PWR_ON pin can be pulled up to VIN, pulled down to ground, or connected to an external command source by selection JP13, PWR_ON_CTRL jumper.

Figure 3 illustrates the output voltage of the buck regulators when BUCK1-BUCK4 is programmed to start in an ascending order. The demo board connection is shown as follows:

SEQ_START -> EN_B1

VB1_SEQ -> EN_B2

VB2_SEQ -> EN_B3

VB3_SEQ -> EN_B4

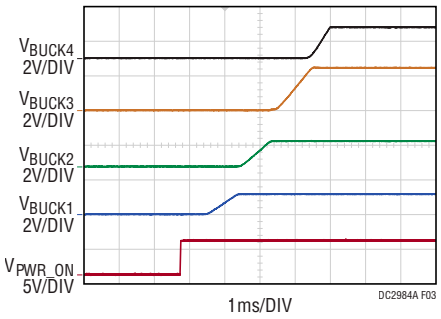


Figure 3. Program BUCK1-BUCK4 Power Up Sequence in Ascending Order

Regulator Enables

When JP4-JP10 is at PGM/OFF position, and no connection is made at the Power Up Sequence Programming Section, all the regulators are disabled. Each regulator can be individually enabled by its corresponding enable turret.

LDO Input Selection

The default input of each LDO is the general input of the demo circuit, VIN. To reduce power loss on the LDOs, the input source of each LDO can be changed to the output of BUCK3 by connection corresponding LDO_XVIN jumper to V(B3). Each LDO can also be powered externally by selecting the corresponding LDO_XVIN jumper to EXT and connecting a separate source to VIN_LDO_X turret. Note that the voltage of this external LDO source must not exceed VIN voltage.

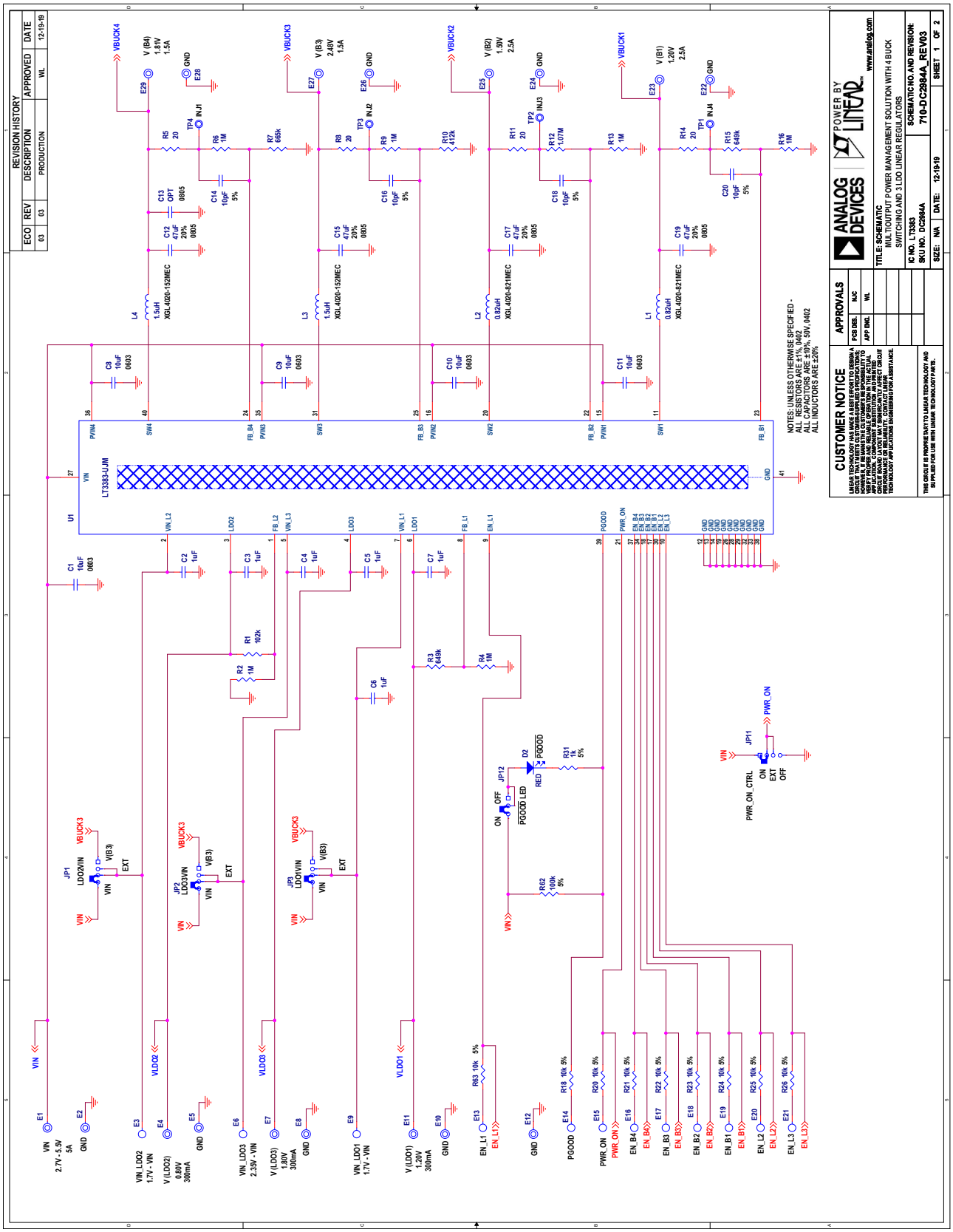
Power Good Indicator

Power Good LED D2 is turned on when PGOOD pin on LT3383 is pulled low. It indicates one or multiple output voltages of the enabled regulators are low. It is also on when no regulator is enabled.

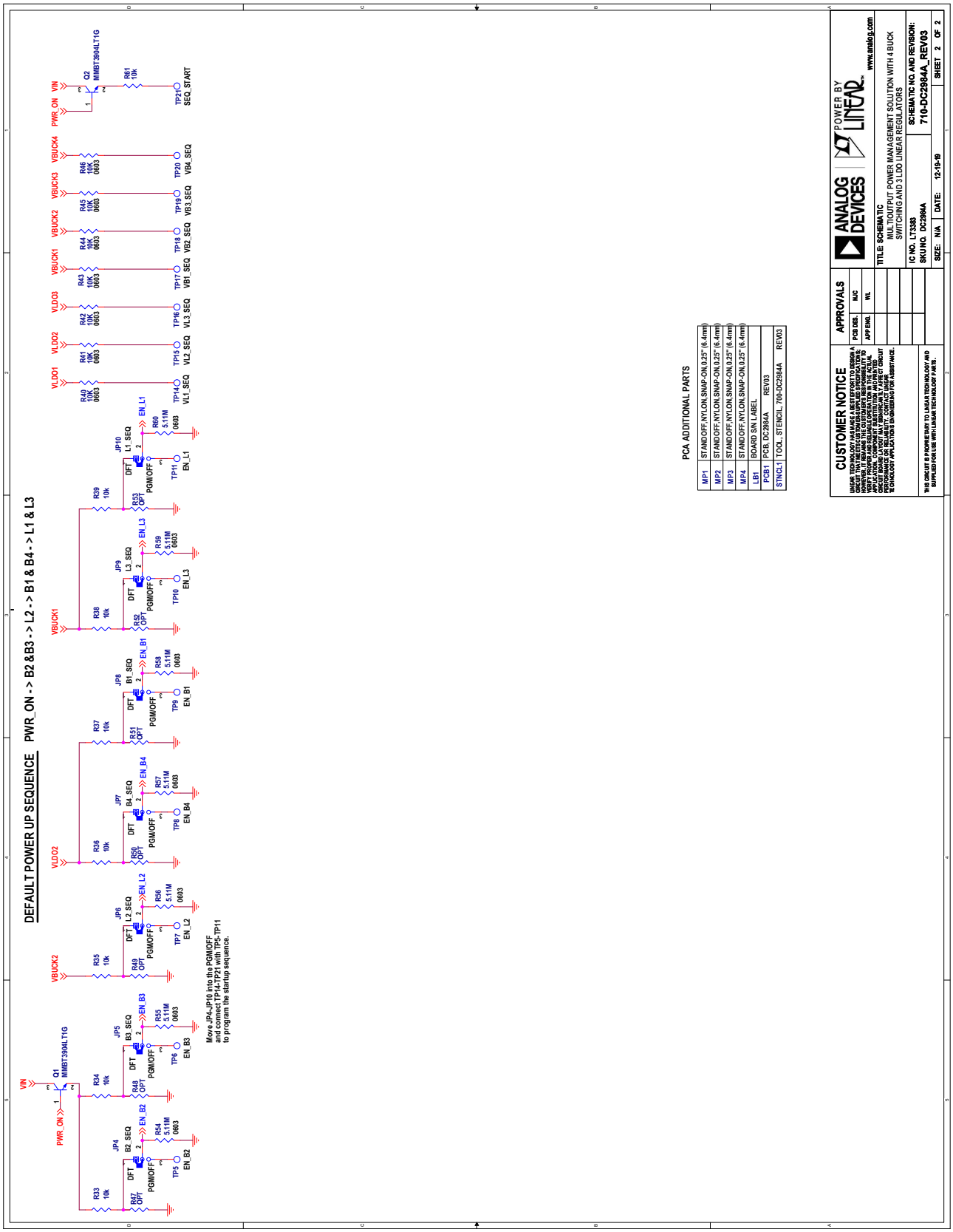
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	5	C1, C8-C11	CAP., 10uF, X5R, 10V, 20%, 0603, AEC-Q200	TAIYO YUDEN, LMK107BBJ106MAHT
2	6	C2-C7	CAP., 1uF, X5R, 25V, 10%, 0402, AEC-Q200	MURATA, GRT155R61E105KE01D
3	4	C12, C15, C17, C19	CAP., 47uF, X5R, 6.3V, 20%, 0805, AEC-Q200	MURATA, GRT21BR60J476ME13L
4	4	C14, C16, C18, C20	CAP., 10pF, C0G, 50V, 5%, 0402, AEC-Q200	MURATA, GCM1555C1H100JA16D
5	2	L1, L2	IND., 0.82UH, POWER, 20%, 14A, DCR 1515, AEC-Q200	COILCRAFT, XGL4020-821MEC
6	2	L3, L4	IND., 1.5UH, PWR, SHIELDED, 20%, 11.1A, AEC-Q200	COILCRAFT, XGL4020-152MEC
7	2	Q1, Q2	XSTR., NPN, 40V, 200MA, SOT23-3	ON SEMICONDUCTOR, MMBT3904LT1G
8	1	R1	RES., 102K OHMS, 1%, 1/16W, 0402, AEC-Q200	STACKPOLE ELECTRONICS INC, RMCF0402FT102K
9	6	R2, R4, R6, R9, R13, R16	RES., 1M OHMS, 1%, 1/16W, 0402, AEC-Q200	STACKPOLE ELECTRONICS INC, RMCF0402FT1M00
10	2	R3, R15	RES., 649K OHMS, 1%, 1/16W, 0402	NIC, NRC04F6493TRF
11	4	R5, R8, R11, R14	RES., 20 OHMS, 1%, 1/16W, 0402, AEC-Q200	NIC, NRC04F20R0TRF
12	1	R7	RES., 665k OHMS, 1%, 1/16W, 0402, AEC-Q200	NIC, NRC04F6653TRF
13	1	R10	RES., 412K OHMS, 1%, 1/16W, 0402	NIC, NRC04F4123TRF
14	1	R12	RES., 1.07M OHMS, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04021M07FKED
15	9	R18, R20-R26, R63	RES., 10K OHMS, 5%, 1/16W, 0402, AEC-Q200	NIC, NRC04J103TRF
16	1	R31	RES., 1K OHM, 5%, 1/16W, 0402, AEC-Q200	NIC, NRC04J102TRF
17	8	R33-R39, R61	RES., 10K OHMS, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040210K0FKED
18	7	R40-R46	RES., 10K OHMS, 1%, 1/10W, 0603, AEC-Q200	PANASONIC, ERJ3EKF1002V
19	7	R54-R60	RES., 5.11M OHMS, 1%, 1/10W, 0603, AEC-Q200	VISHAY, CRCW06035M11FKED
20	1	R62	RES., 100K OHMS, 5%, 1/16W, 0402, AEC-Q200	NIC, NRC04J104TRF
21	1	U1	IC, MULTI-OUTPUT POWER, 40QFN	ANALOG DEVICES, LT3383EUJM#PBF
Additional Demo Board Circuit Components				
1	1	D2	LED, RED, WATER CLEAR, 0603	WURTH ELEKTRONIK, 150060RS75000
Hardware: For Demo Board Only				
1	17	E1, E2, E4, E5, E7, E8, E10-E12, E22-E29	TEST POINT, TURRET, 0.064" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2308-2-00-80-00-00-07-0
2	12	E3, E6, E9, E13-E21	CONN., HDR., MALE, 1x4, 2mm, THT, STR	SULLINS CONNECTOR SOLUTIONS,
3	4	JP1-JP3, JP13	NRPN041PAEN-RC	
4	8	JP4-JP10, JP11	CONN., HDR, MALE, 1x3, 2mm, VERT, STR, THT	WURTH ELEKTRONIK, 62000311121
5	4	MP1-MP4	STANDOFF, NYLON, SNAP-ON, 0.25" (6.4mm)	KEYSTONE, 8831
6	12	XJP1-XJP7, XJP9-XJP13	CONN., SHUNT, FEMALE, 2 POS, 2mm	WURTH ELEKTRONIK, 60800213421

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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