

NIF9N05CL, NIF9N05ACL

Protected Power MOSFET

2.6 A, 52 V, N-Channel, Logic Level, Clamped MOSFET w/ ESD Protection in a SOT-223 Package



ON Semiconductor®

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Benefits

- High Energy Capability for Inductive Loads
- Low Switching Noise Generation

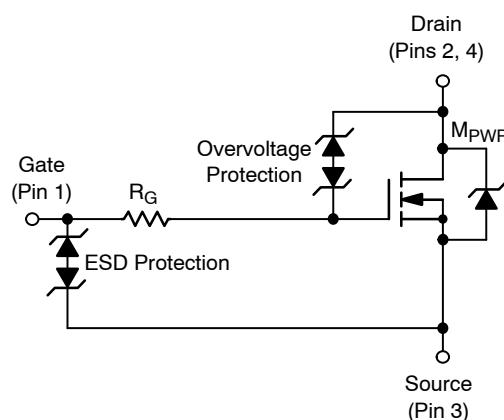
Features

- Diode Clamp Between Gate and Source
- ESD Protection – HBM 5000 V
- Active Over-Voltage Gate to Drain Clamp
- Scalable to Lower or Higher $R_{DS(on)}$
- Internal Series Gate Resistance
- Pb-Free Packages are Available

Applications

- Automotive and Industrial Markets:
Solenoid Drivers, Lamp Drivers, Small Motor Drivers

| V_{DSS} (Clamped) | $R_{DS(ON)}$ TYP | I_D MAX |
|---------------------|------------------|-----------|
| 52 V | 107 mΩ | 2.6 A |

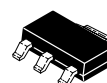


MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-----------------|------------|--------------------|
| Drain-to-Source Voltage Internally Clamped | V_{DSS} | 52–59 | V |
| Gate-to-Source Voltage – Continuous | V_{GS} | ±15 | V |
| Drain Current | I_D | 2.6 | A |
| – Continuous @ $T_A = 25^\circ\text{C}$ | | | |
| – Single Pulse ($t_p = 10 \mu\text{s}$) (Note 1) | I_{DM} | 10 | |
| Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) | P_D | 1.69 | W |
| Operating and Storage Temperature Range | T_J, T_{stg} | –55 to 150 | $^\circ\text{C}$ |
| Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50 \text{ V}$, $I_{D(pk)} = 1.17 \text{ A}$, $V_{GS} = 10 \text{ V}$, $L = 160 \text{ mH}$, $R_G = 25 \Omega$) | E_{AS} | 110 | mJ |
| Thermal Resistance, Junction-to-Ambient (Note 1) | $R_{\theta JA}$ | 74 | $^\circ\text{C/W}$ |
| Junction-to-Ambient (Note 2) | $R_{\theta JA}$ | 169 | |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds | T_L | 260 | $^\circ\text{C}$ |

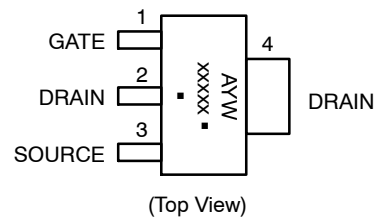
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to a FR4 board using 1" pad size, (Cu area 1.127 in²).
2. When surface mounted to a FR4 board using minimum recommended pad size, (Cu area 0.412 in²).



SOT-223
CASE 318E
STYLE 3

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- xxxxx = F9N05 or 9N05A
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NIF9N05CL, NIF9N05ACL

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | |
|---|---------------|------------|------------------|------------|--------------------------------|
| Drain-to-Source Breakdown Voltage (Note 3) $(V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}, T_J = 25^\circ\text{C})$ $(V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}, T_J = -40^\circ\text{C to } 125^\circ\text{C})$ Temperature Coefficient (Negative) | $V_{(BR)DSS}$ | 52 50.8 | 55 54 -9.3 | 59 59.5 | V V mV/ $^\circ\text{C}$ |
| Zero Gate Voltage Drain Current $(V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V})$ $(V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C})$ | I_{DSS} | | | 10 25 | μA |
| Gate-Body Leakage Current $(V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V})$ $(V_{GS} = \pm 14\text{ V}, V_{DS} = 0\text{ V})$ | I_{GSS} | | ± 22 | ± 10 | μA |

ON CHARACTERISTICS (Note 3)

| | | | | | |
|---|--------------|-----|-------------------|-------------------|---------------------------|
| Gate Threshold Voltage (Note 3) $(V_{DS} = V_{GS}, I_D = 100\ \mu\text{A})$ Threshold Temperature Coefficient (Negative) | $V_{GS(th)}$ | 1.3 | 1.75 -4.1 | 2.5 | V mV/ $^\circ\text{C}$ |
| Static Drain-to-Source On-Resistance (Note 3) $(V_{GS} = 3.5\text{ V}, I_D = 0.6\text{ A})$ $(V_{GS} = 4.0\text{ V}, I_D = 1.5\text{ A})$ $(V_{GS} = 10\text{ V}, I_D = 2.6\text{ A})$ | $R_{DS(on)}$ | | 190 165 107 | 380 200 125 | m Ω |
| Forward Transconductance (Note 3) ($V_{DS} = 15\text{ V}, I_D = 2.6\text{ A}$) | g_{FS} | | 3.8 | | Mhos |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|----------------------|---|-----------|--|-----|-----|---------------|
| Input Capacitance | $V_{DS} = 35\text{ V}, V_{GS} = 0\text{ V},$ $f = 10\text{ kHz}$ | C_{iss} | | 155 | 250 | μF |
| Output Capacitance | | C_{oss} | | 60 | 100 | |
| Transfer Capacitance | | C_{rss} | | 25 | 40 | |
| Input Capacitance | $V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 10\text{ kHz}$ | C_{iss} | | 170 | | μF |
| Output Capacitance | | C_{oss} | | 70 | | |
| Transfer Capacitance | | C_{rss} | | 30 | | |

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.

NIF9N05CL, NIF9N05ACL

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|--|--------------|-----|------|------|------|
| SWITCHING CHARACTERISTICS (Note 4) | | | | | | |
| Turn-On Delay Time | $V_{GS} = 4.5\text{ V}, V_{DD} = 40\text{ V},$ $I_D = 2.6\text{ A}, R_D = 15.4\ \Omega$ | $t_{d(on)}$ | | 275 | 465 | ns |
| Rise Time | | t_r | | 1418 | 2400 | |
| Turn-Off Delay Time | | $t_{d(off)}$ | | 780 | 1320 | |
| Fall Time | | t_f | | 1120 | 1900 | |
| Turn-On Delay Time | $V_{GS} = 4.5\text{ V}, V_{DD} = 40\text{ V},$ $I_D = 1.0\text{ A}, R_D = 40\ \Omega$ | $t_{d(on)}$ | | 242 | | ns |
| Rise Time | | t_r | | 1165 | | |
| Turn-Off Delay Time | | $t_{d(off)}$ | | 906 | | |
| Fall Time | | t_f | | 1273 | | |
| Turn-On Delay Time | $V_{GS} = 10\text{ V}, V_{DD} = 15\text{ V},$ $I_D = 2.6\text{ A}, R_D = 5.8\ \Omega$ | $t_{d(on)}$ | | 107 | | ns |
| Rise Time | | t_r | | 290 | | |
| Turn-Off Delay Time | | $t_{d(off)}$ | | 1540 | | |
| Fall Time | | t_f | | 1000 | | |
| Gate Charge | $V_{GS} = 4.5\text{ V}, V_{DS} = 40\text{ V},$ $I_D = 2.6\text{ A (Note 3)}$ | Q_T | | 4.5 | 7.0 | nC |
| | | Q_1 | | 0.9 | | |
| | | Q_2 | | 2.6 | | |
| Gate Charge | $V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 1.5\text{ A (Note 3)}$ | Q_T | | 3.9 | | nC |
| | | Q_1 | | 1.0 | | |
| | | Q_2 | | 1.7 | | |

SOURCE-DRAIN DIODE CHARACTERISTICS

| | | | | | | |
|--------------------------------|--|----------|--|--------------|-----|---------------|
| Forward On-Voltage | $I_S = 2.6\text{ A}, V_{GS} = 0\text{ V (Note 3)}$ $I_S = 2.6\text{ A}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$ | V_{SD} | | 0.81 0.66 | 1.5 | V |
| Reverse Recovery Time | $I_S = 1.5\text{ A}, V_{GS} = 0\text{ V},$ $di_S/dt = 100\text{ A}/\mu\text{s (Note 3)}$ | t_{rr} | | 730 | | ns |
| | | t_a | | 200 | | |
| | | t_b | | 530 | | |
| Reverse Recovery Stored Charge | | Q_{RR} | | 6.3 | | μC |

ESD CHARACTERISTICS

| | | | | | | |
|-------------------------------------|------------------------|-----|------|--|--|---|
| Electro-Static Discharge Capability | Human Body Model (HBM) | ESD | 5000 | | | V |
| | Machine Model (MM) | | 500 | | | |

3. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

NIF9N05CL, NIF9N05ACL

TYPICAL PERFORMANCE CURVES

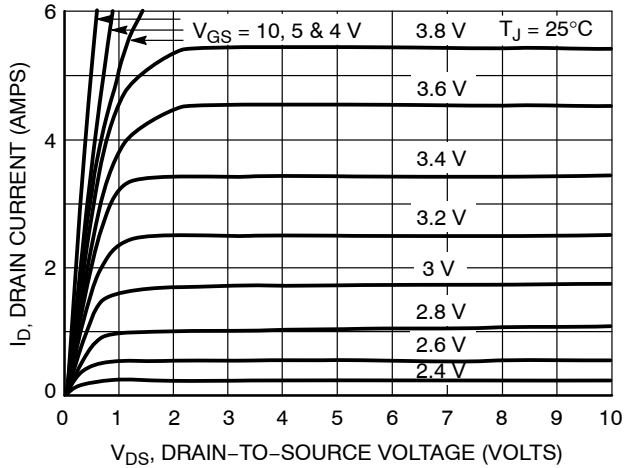


Figure 1. On-Region Characteristics

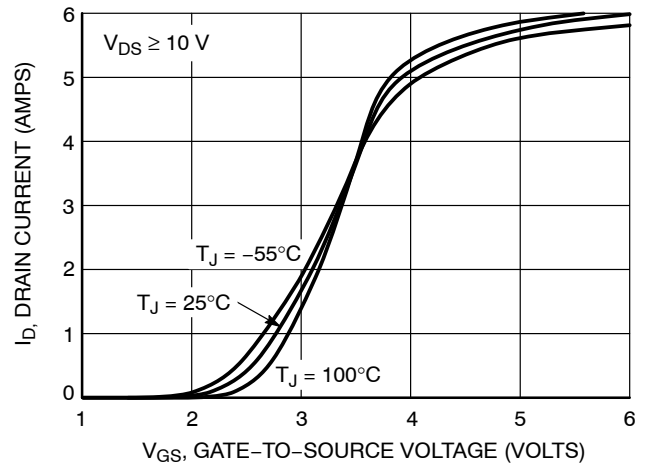


Figure 2. Transfer Characteristics

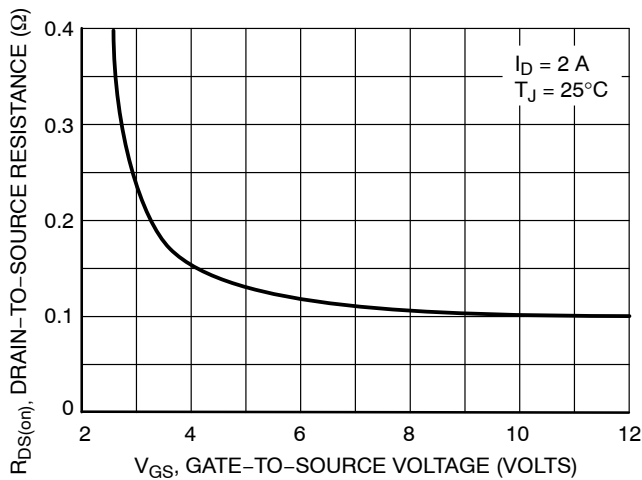


Figure 3. On-Resistance vs. Gate-to-Source Voltage

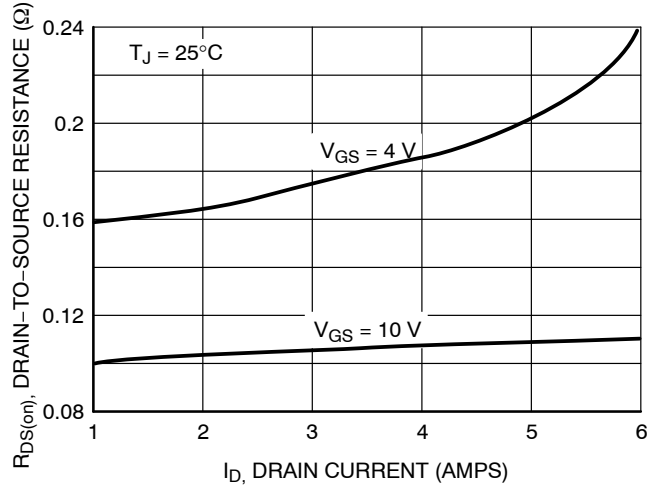


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

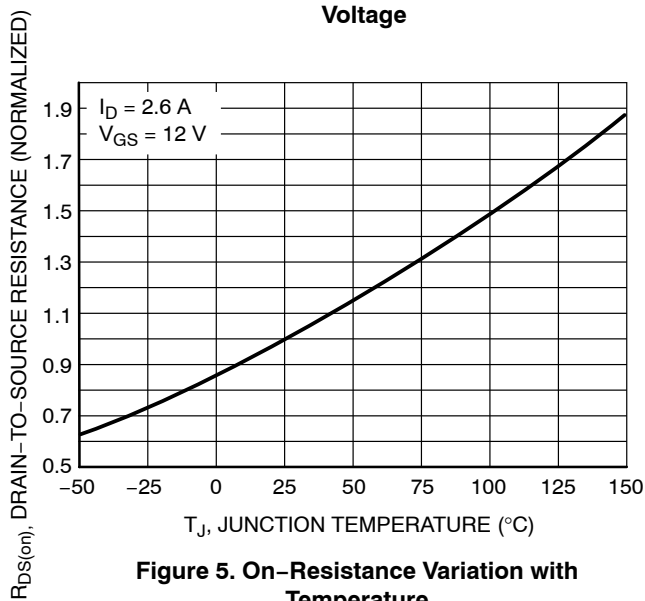


Figure 5. On-Resistance Variation with Temperature

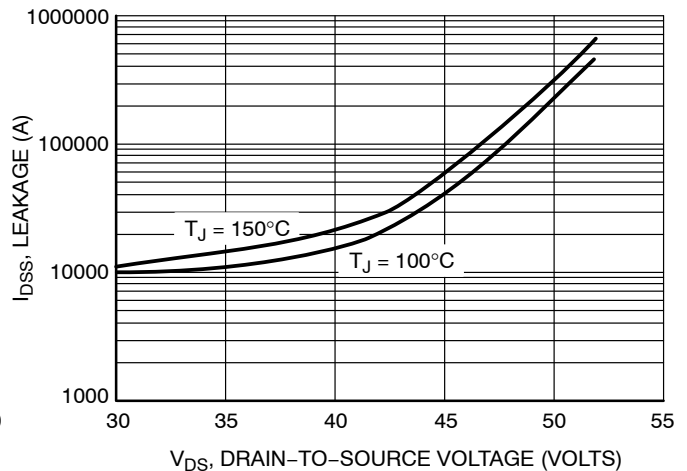


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL PERFORMANCE CURVES

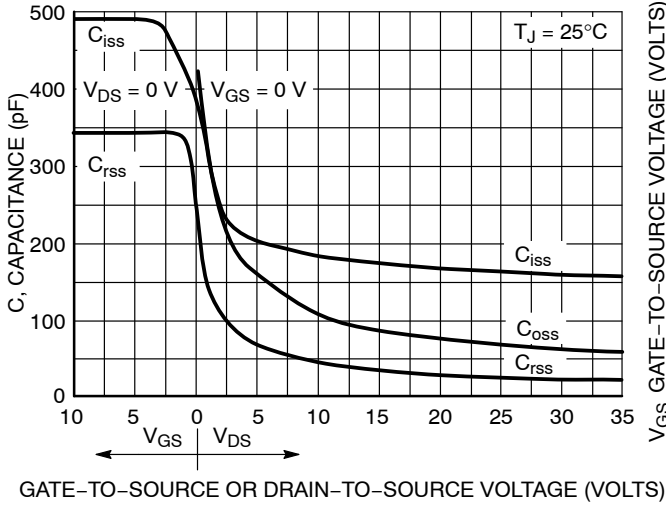


Figure 7. Capacitance Variation

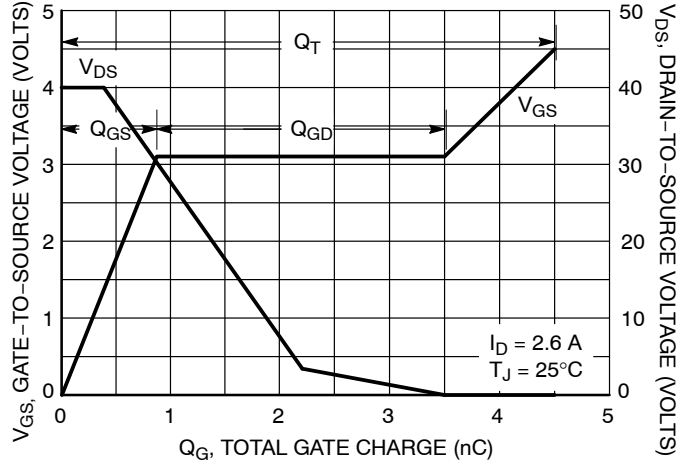


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

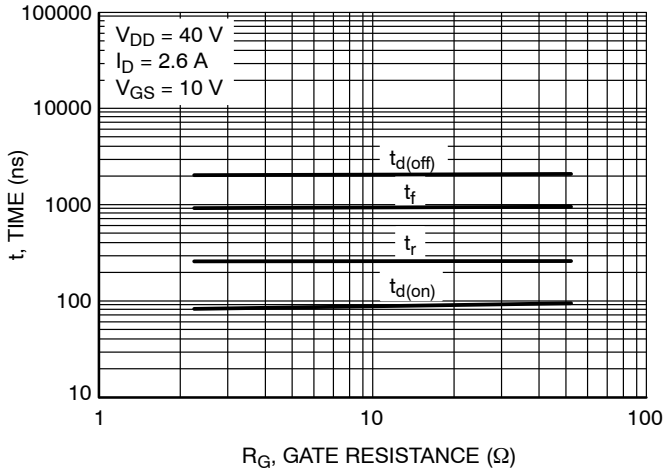


Figure 9. Resistance Switching Time Variation vs. Gate Resistance

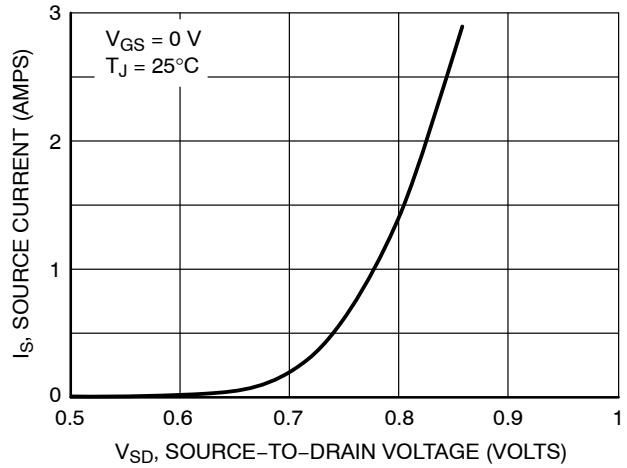


Figure 10. Diode Forward Voltage vs. Current

ORDERING INFORMATION

| Device | Package | Shipping† |
|--------------|-------------------|--------------------|
| NIF9N05CLT1 | SOT-223 | 1000 / Tape & Reel |
| NIF9N05CLT1G | SOT-223 (Pb-Free) | |
| NIF9N05ACL1G | | |
| NIF9N05CLT3 | SOT-223 | 4000 / Tape & Reel |
| NIF9N05CLT3G | SOT-223 (Pb-Free) | |
| NIF9N05ACL3G | | |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

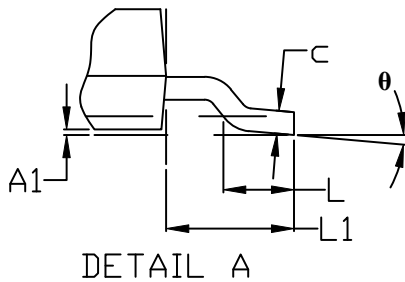
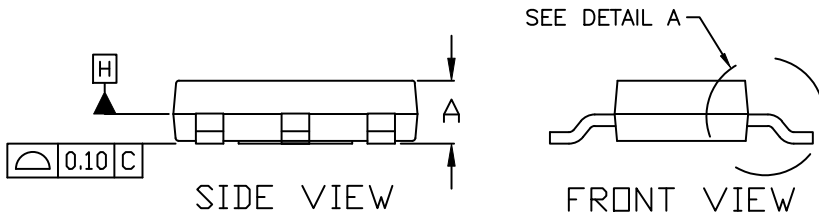
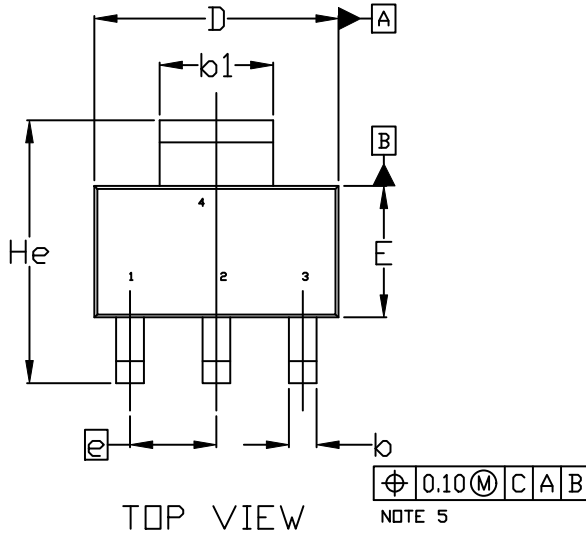
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SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

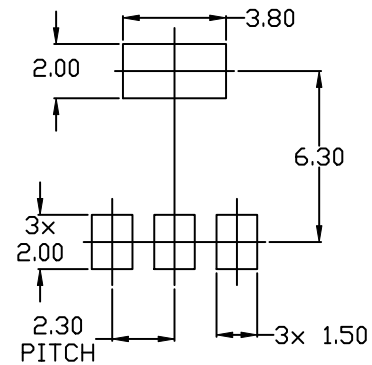
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

| MILLIMETERS | | | |
|-------------|----------|------|------|
| DIM | MIN. | NOM. | MAX. |
| A | 1.50 | 1.63 | 1.75 |
| A1 | 0.02 | 0.06 | 0.10 |
| b | 0.60 | 0.75 | 0.89 |
| b1 | 2.90 | 3.06 | 3.20 |
| c | 0.24 | 0.29 | 0.35 |
| D | 6.30 | 6.50 | 6.70 |
| E | 3.30 | 3.50 | 3.70 |
| e | 2.30 BSC | | |
| L | 0.20 | --- | --- |
| L1 | 1.50 | 1.75 | 2.00 |
| He | 6.70 | 7.00 | 7.30 |
| θ | 0° | --- | 10° |



| | | |
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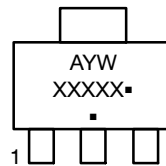
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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

- | | | | | |
|--|---|---|---|---|
| STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR | STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE | STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN | STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN | STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE |
| STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT | STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE | STYLE 8: CANCELLED | STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND | STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE |
| STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2 | STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT | STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR | | |

**GENERIC
 MARKING DIAGRAM***



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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