LM2738 550-kHz/1.6-MHz 1.5-A Step-Down DC-DC Switching Regulator

1 Features

- Space-Saving WSON and MSOP-PowerPAD™ Packages
- 3-V to 20-V Input Voltage Range
- 0.8-V to 18-V Output Voltage Range
- 1.5-A Output Current
- 550-kHz (LM2738Y) and 1.6-MHz (LM2738X) Switching Frequencies
- 250-mΩ NMOS Switch
- 400-nA Shutdown Current
- 0.8-V, 2% Internal Voltage Reference
- Internal Soft-Start
- Current-Mode, PWM Operation
- Thermal Shutdown

2 Applications

- Local Point of Load Regulation
- Core Power in HDDs
- Set-Top Boxes
- Battery Powered Devices
- USB Powered Devices
- DSL Modems

3 Description

The LM2738 regulator is a monolithic, high-frequency, PWM step-down DC-DC converter in an 8-pin WSON or 8-pin MSOP-PowerPAD package. It provides all the active functions for local DC-DC conversion with fast transient response and accurate regulation in the smallest possible PCB area.

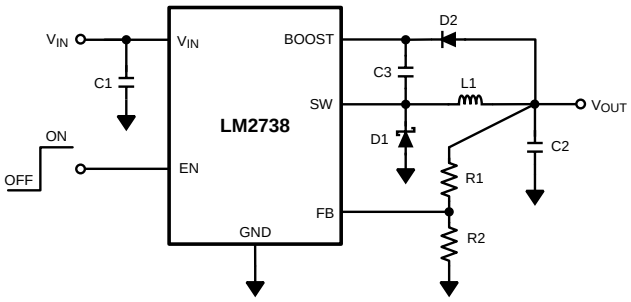
With a minimum of external components, the LM2738 is easy to use. The ability to drive 1.5-A loads with an internal 250-mΩ NMOS switch using state-of-the-art 0.5-µm BiCMOS technology results in the best power density available. Switching frequency is internally set to 550 kHz (LM2738Y) or 1.6 MHz (LM2738X), allowing the use of extremely small surface-mount inductors and chip capacitors. Even though the operating frequencies are very high, efficiencies up to 90% are easy to achieve. External enable is included, featuring an ultralow standby current of 400 nA. The LM2738 utilizes current-mode control and internal compensation to provide high-performance regulation over a wide range of operating conditions. Additional features include internal soft-start circuitry to reduce in-rush current, cycle-by-cycle current limit, thermal shutdown, and output over-voltage protection.

Device Information(1)

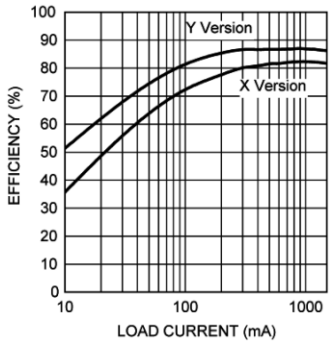
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2738	WSON (8)	3.00 mm × 3.00 mm
	MSOP-PowerPAD (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



Efficiency vs Load Current
V_{IN} = 12 V, V_{OUT} = 3.3 V



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2013) to Revision C **Page**

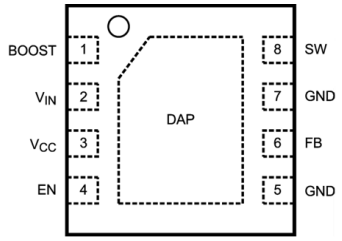
- Added *Device Information* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision A (April 2013) to Revision B **Page**

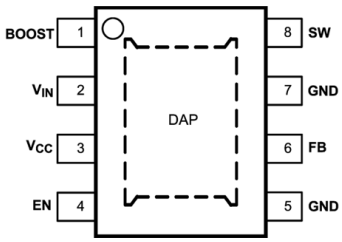
- Changed layout of National Data Sheet to TI format 29

5 Pin Configuration and Functions

NGQ Package
8-Pin WSON With Exposed Thermal Pad
Top View



DGN Package
8-Pin MSOP-PowerPAD
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	BOOST	I	Boost voltage that drives the internal NMOS control switch. A bootstrap capacitor is connected between the BOOST and SW pins.
2	V_{IN}	PWR	Supply voltage for output power stage. Connect a bypass capacitor to this pin. Must tie pins 2 and 3 together at package.
3	V_{CC}	I	Input supply voltage of the device. Connect a bypass capacitor to this pin. Must tie pins 2 and 3 together at the package.
4	EN	I	Enable control input. Logic high enables operation. Do not allow this pin to float or be greater than V_{IN} + 0.3 V.
5, 7	GND	PWR	Signal and power ground pins. Place the bottom resistor of the feedback network as close as possible to these pins.
6	FB	I	Feedback pin. Connect FB to the external resistor divider to set output voltage.
8	SW	O	Output switch. Connects to the inductor, catch diode, and bootstrap capacitor.
DAP	GND	—	Signal and power ground. Must be connected to GND on the PCB.

(1) I = Input, O = Output, and PWR = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
V_{IN}, V_{CC}		–0.5	24	V
SW voltage		–0.5	24	V
Boost voltage		–0.5	30	V
Boost to SW voltage		–0.5	6	V
FB voltage		–0.5	3	V
EN voltage		–0.5	V_{IN} + 0.3	V
Junction temperature			150	°C
Soldering information	Infrared and convection reflow (15 s)		220	°C
	Wave soldering lead temperature (10 s)		260	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military or Aerospace specified devices are required, contact the Texas Instruments Sales Office or Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human body model, 1.5 kΩ in series with 100 pF.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN}, V_{CC}	3	20	V
SW voltage	–0.5	20	V
Boost voltage	–0.5	25.5	V
Boost to SW voltage	2.5	5.5	V
Junction temperature	−40	125	°C
Thermal shutdown		165	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM2738		UNIT
		NGQ (WSON)	DGN (MSOP PowerPAD)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	45.9	50.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.6	54.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.2	31.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.2	31.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.8	4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and device Package Thermal Metrics* application report, SPRA953.
(2) Typical thermal shutdown occurs if the junction temperature exceeds 165°C. The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$ and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} – T_A) / R_{\theta JA}$. All numbers apply for packages soldered directly onto a 3 inches × 3 inches PC board with 2 oz. copper on 4 layers in still air in accordance to JEDEC standards. Thermal resistance varies greatly with layout, copper thickness, number of layers in PCB, power distribution, number of thermal vias, board size, ambient temperature, and air flow.

6.5 Electrical Characteristics

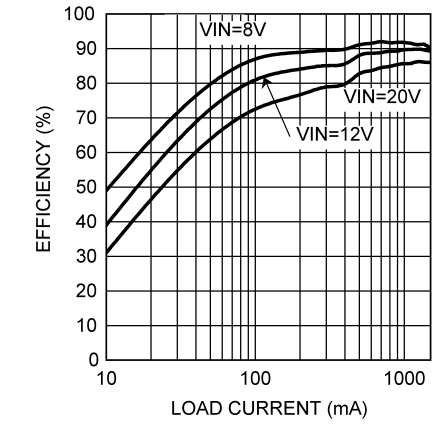
All typical limits apply over T_J = 25°C, and all maximum and minimum limits apply over the full operating temperature range (T_J = –40°C to +125°C). V_{IN} = 12 V, $V_{BOOST} – V_{SW}$ = 5 V unless otherwise specified. Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.

PARAMETER		TEST CONDITIONS	MIN[1]	TYP[2]	MAX[1]	UNIT
V_{FB}	Feedback voltage		0.784	0.800	0.816	V
$\Delta V_{FB}/\Delta V_{IN}$	Feedback voltage line regulation	V_{IN} = 3 V to 20 V		0.02		%/V
I_{FB}	Feedback input bias current	Sink or source		0.1	100	nA
UVLO	Undervoltage lockout	V_{IN} Rising		2.7	2.9	V
	Undervoltage lockout	V_{IN} Falling	2	2.3		
	UVLO hysteresis			0.4		
F_{SW}	Switching frequency	LM2738X	1.28	1.6	1.92	MHz
		LM2738Y	0.364	0.55	0.676	
D_{MAX}	Maximum duty cycle	LM2738X , Load = 150 mA		92%		
		LM2738Y, Load = 150 mA		95%		
D_{MIN}	Minimum duty cycle	LM2738X		7.5%		
		LM2738Y		2%		
$R_{DS(ON)}$	Switch ON resistance	$V_{BOOST} – V_{SW}$ = 3 V, Load = 400 mA		250	500	mΩ
I_{CL}	Switch current limit	$V_{BOOST} – V_{SW}$ = 3 V, V_{IN} = 3 V	2	2.9		A
I_Q	Quiescent current	Switching		1.9	3	mA
		Non-Switching		1.9		mA
	Quiescent current (shutdown)	V_{EN} = 0 V		400		nA
I_{BOOST}	Boost pin current	LM2738X (27% Duty Cycle)		4.5		mA
		LM2738Y (27% Duty Cycle)		2.5		
V_{EN_TH}	Shutdown threshold voltage	V_{EN} Falling			0.4	V
	Enable threshold voltage	V_{EN} Rising	1.4			
I_{EN}	Enable pin current	Sink / Source		10		nA
I_{SW}	Switch leakage	V_{IN} = 20 V		100		nA

(1) Ensured to average outgoing quality level (AOQL).
(2) Typicals represent the most likely parametric norm.

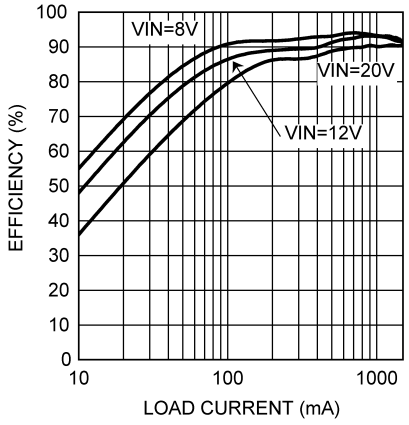
6.6 Typical Characteristics

All curves taken at V_{IN} = 12 V, $V_{BOOST} – V_{SW}$ = 5 V, and T_A = 25°C, unless specified otherwise.



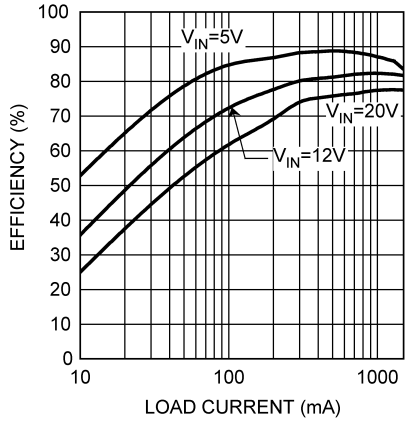
V_{OUT} = 5 V

Figure 1. Efficiency vs Load Current – X Version



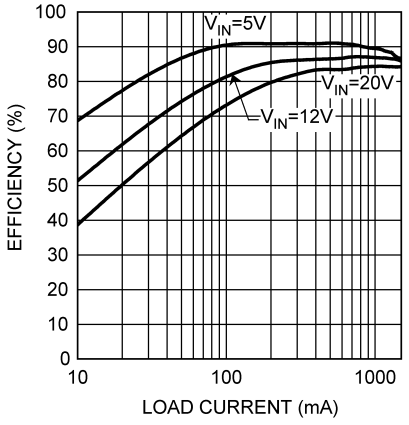
V_{OUT} = 5 V

Figure 2. Efficiency vs Load Current – Y Version



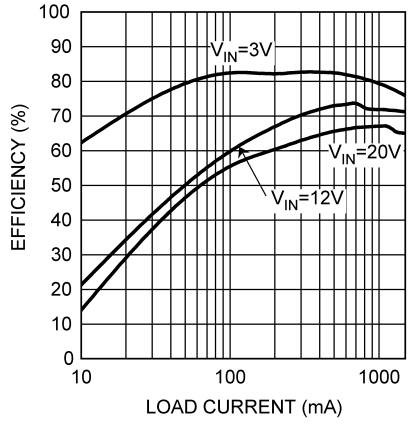
V_{OUT} = 3.3 V

Figure 3. Efficiency vs Load Current – X Version



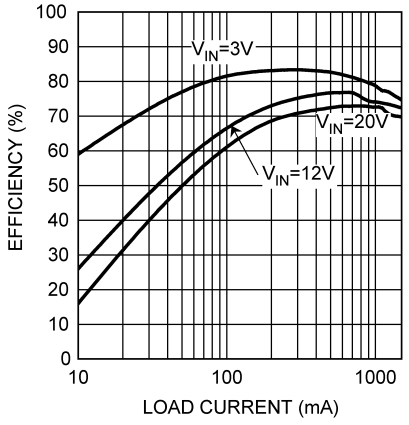
V_{OUT} = 3.3 V

Figure 4. Efficiency vs Load Current – Y Version



V_{OUT} = 1.5 V

Figure 5. Efficiency vs Load Current – X Version



V_{OUT} = 1.5 V

Figure 6. Efficiency vs Load Current – Y Version

Typical Characteristics (continued)

All curves taken at V_{IN} = 12 V, $V_{BOOST} - V_{SW}$ = 5 V, and T_A = 25°C, unless specified otherwise.

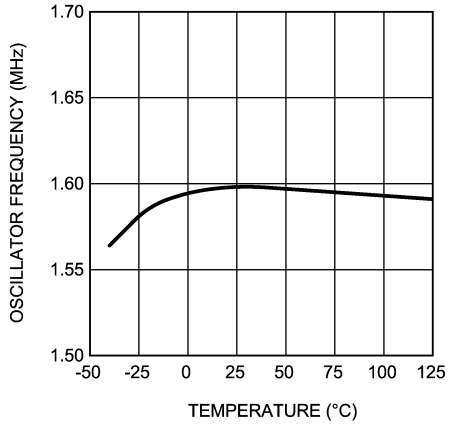


Figure 7. Oscillator Frequency vs Temperature – X Version

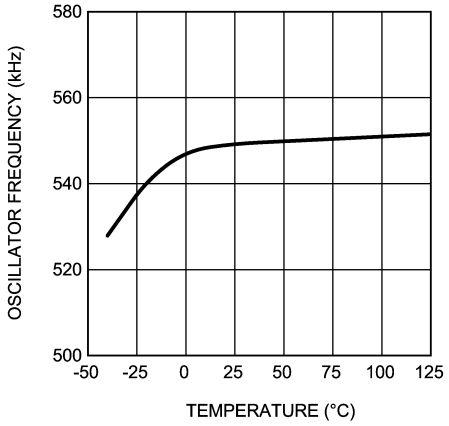
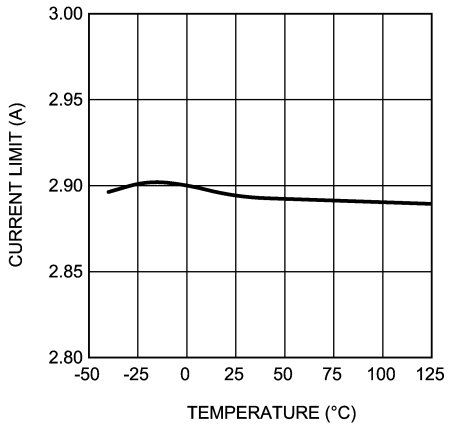


Figure 8. Oscillator Frequency vs Temperature – Y Version



V_{IN} = 5 V

Figure 9. Current Limit vs Temperature

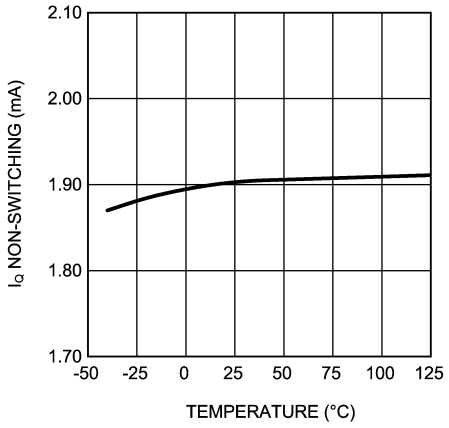


Figure 10. I_Q Non-Switching vs Temperature

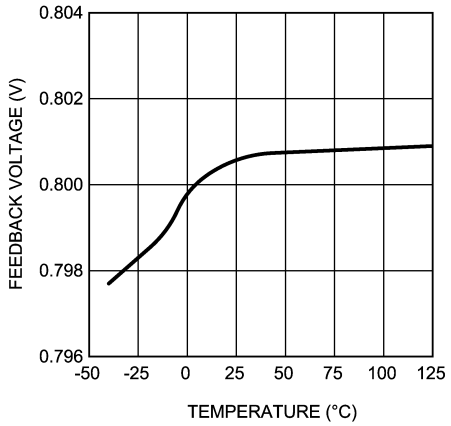


Figure 11. V_{FB} vs Temperature

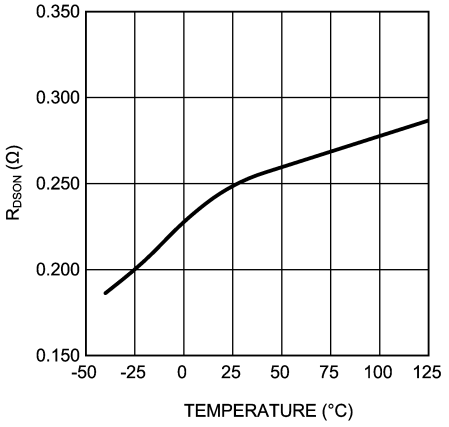
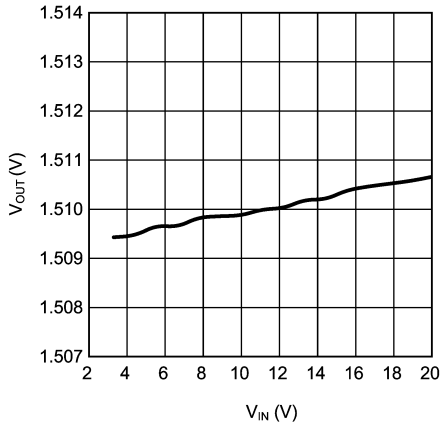


Figure 12. R_{DSON} vs Temperature

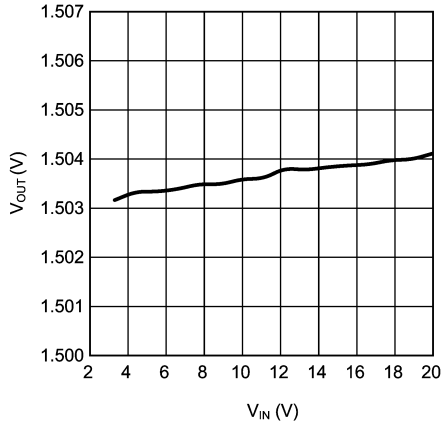
Typical Characteristics (continued)

All curves taken at V_{IN} = 12 V, $V_{BOOST} - V_{SW}$ = 5 V, and T_A = 25°C, unless specified otherwise.



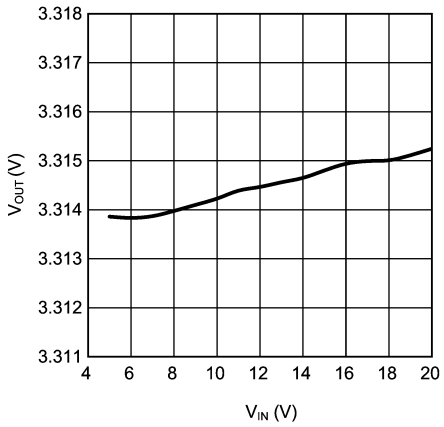
V_{OUT} = 1.5 V I_{OUT} = 750 mA

Figure 13. Line Regulation – X Version



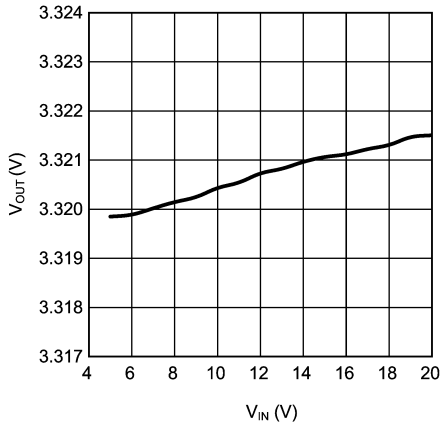
V_{OUT} = 1.5 V I_{OUT} = 750 mA

Figure 14. Line Regulation – Y Version



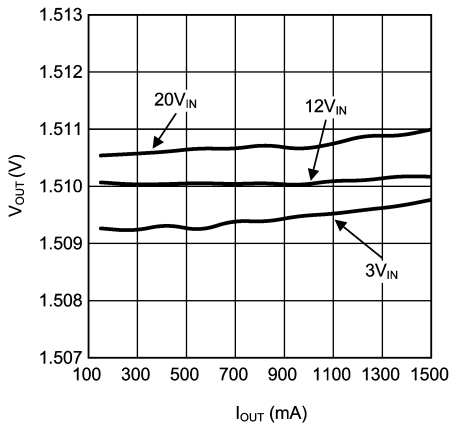
V_{OUT} = 3.3 V I_{OUT} = 750 mA

Figure 15. Line Regulation – X Version



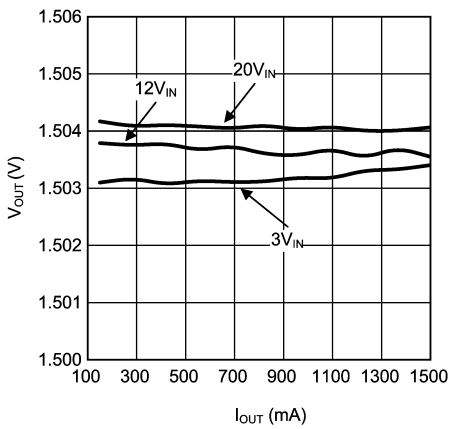
V_{OUT} = 3.3 V I_{OUT} = 750 mA

Figure 16. Line Regulation – Y Version



V_{OUT} = 1.5 V

Figure 17. Load Regulation – X Version

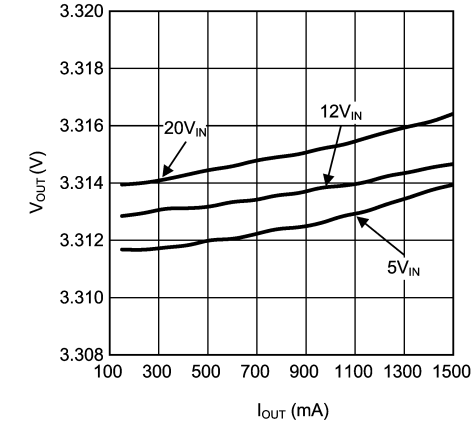


V_{OUT} = 1.5 V

Figure 18. Load Regulation – Y Version

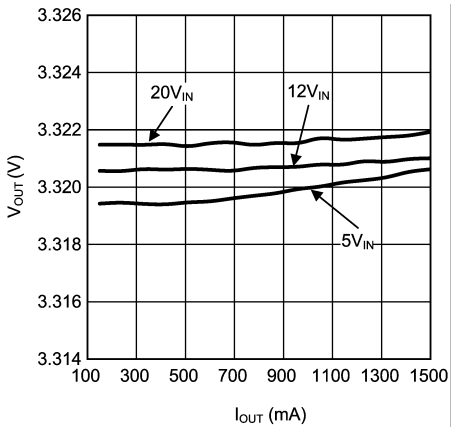
Typical Characteristics (continued)

All curves taken at V_{IN} = 12 V, $V_{BOOST} - V_{SW}$ = 5 V, and T_A = 25°C, unless specified otherwise.



V_{OUT} = 3.3 V

Figure 19. Load Regulation – X Version



V_{OUT} = 3.3 V

Figure 20. Load Regulation – Y Version

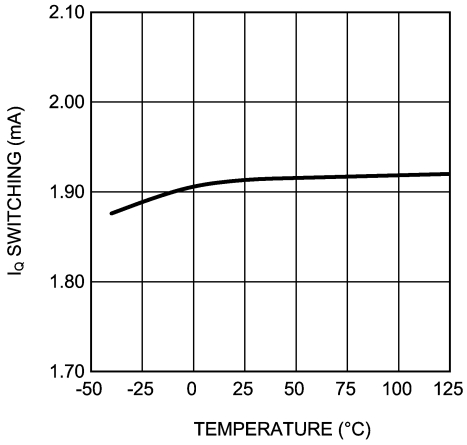
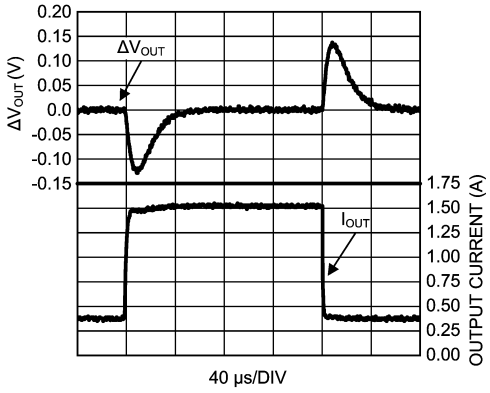
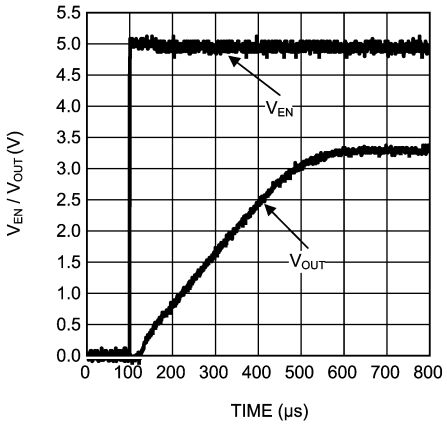


Figure 21. I_Q Switching vs Temperature



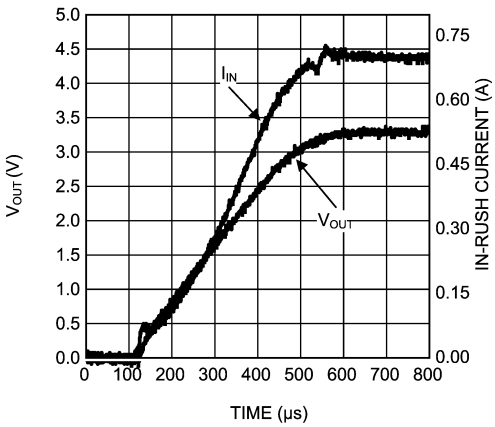
V_{OUT} = 3.3 V V_{IN} = 12 V

Figure 22. Load Transient – X Version



V_{OUT} = 3.3 V V_{IN} = 12 V I_{OUT} = 1.5 A

Figure 23. Startup – X Version (Resistive Load)



V_{OUT} = 3.3 V V_{IN} = 12 V I_{OUT} = 1.5 A

Figure 24. In-Rush Current – X Version (Resistive Load)

7 Detailed Description

7.1 Overview

The LM2738 is a constant frequency PWM buck regulator device that delivers a 1.5-A load current. The regulator has a preset switching frequency of either 550 kHz (LM2738Y) or 1.6 MHz (LM2738X). These high frequencies allow the LM2738 to operate with small surface-mount capacitors and inductors, resulting in DC-DC converters that require a minimum amount of board space. The LM2738 is internally compensated, so it is simple to use and requires few external components. The LM2738 uses current-mode control to regulate the output voltage.

The LM2738 supplies a regulated output voltage by switching the internal NMOS control switch at constant frequency and variable duty cycle. A switching cycle begins at the falling edge of the reset pulse generated by the internal oscillator. When this pulse goes low, the output control logic turns on the internal NMOS control switch. During this on time, the SW pin voltage (V_{SW}) swings up to approximately V_{IN}, and the inductor current (I_L) increases with a linear slope. I_L is measured by the current-sense amplifier, which generates an output proportional to the switch current. The sense signal is summed with the regulator's corrective ramp and compared to the error amplifier's output, which is proportional to the difference between the feedback voltage and V_{REF}. When the PWM comparator output goes high, the output switch turns off until the next switching cycle begins. During the switch off-time, inductor current discharges through Schottky diode D1, which forces the SW pin to swing below ground by the forward voltage (V_D) of the catch diode. The regulator loop adjusts the duty cycle (D) to maintain a constant output voltage. See *Functional Block Diagram* and Figure 25.

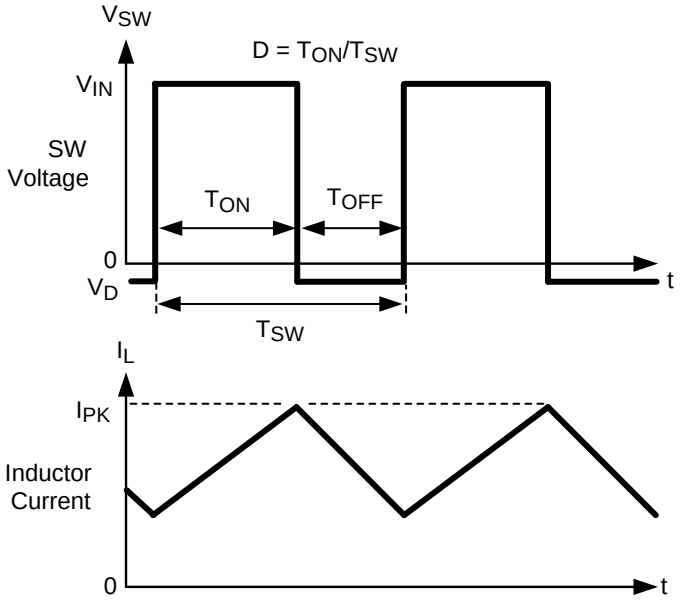
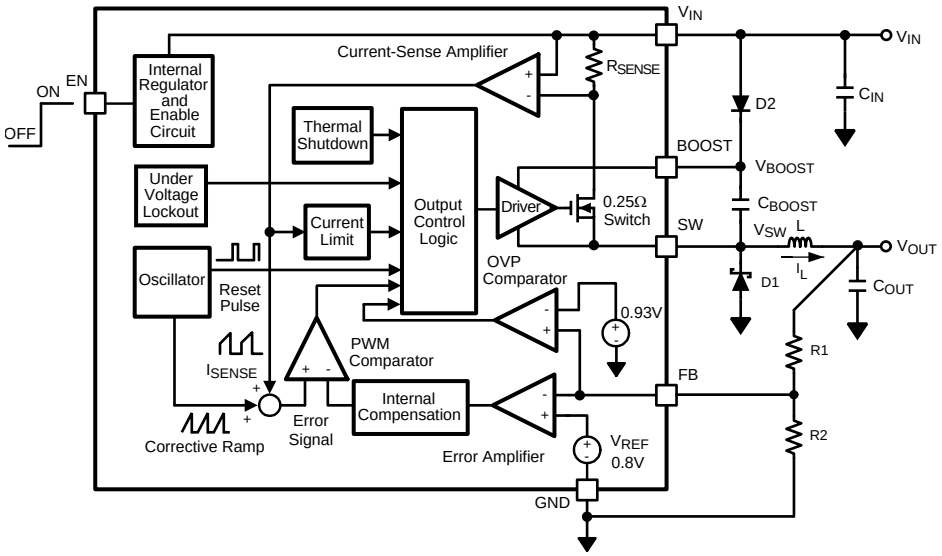


Figure 25. LM2738 Waveforms of SW Pin Voltage and Inductor Current

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Boost Function

Capacitor C_{BOOST} and diode D2 in Figure 26 are used to generate a voltage V_{BOOST}. $V_{BOOST} – V_{SW}$ is the gate-drive voltage to the internal NMOS control switch. To properly drive the internal NMOS switch during its on time, V_{BOOST} must be at least 2.5 V greater than V_{SW}. TI recommends that V_{BOOST} be greater than 2.5 V above V_{SW} for best efficiency. $V_{BOOST} – V_{SW}$ must not exceed the maximum operating limit of 5.5 V. For best performance, see Equation 1.

$$5.5\ V > V_{BOOST} – V_{SW} > 2.5\ V \quad (1)$$

When the LM2738 starts up, internal circuitry from the BOOST pin supplies a maximum of 20 mA to C_{BOOST}. This current charges C_{BOOST} to a voltage sufficient to turn the switch on. The BOOST pin continues to source current to C_{BOOST} until the voltage at the feedback pin is greater than 0.76 V.

There are various methods to derive V_{BOOST}:

1. From the input voltage ($3\ V < V_{IN} < 5.5\ V$)
2. From the output voltage ($2.5\ V < V_{OUT} < 5.5\ V$)
3. From an external distributed voltage rail ($2.5\ V < V_{EXT} < 5.5\ V$)
4. From a shunt or series Zener diode

As seen on the *Functional Block Diagram*, capacitor C_{BOOST} and diode D2 supply the gate-drive voltage for the NMOS switch. Capacitor C_{BOOST} is charged via diode D2 by V_{IN}. During a normal switching cycle, when the internal NMOS control switch is off (T_{OFF}) (refer to Figure 25), V_{BOOST} equals V_{IN} minus the forward voltage of D2 (V_{FD2}), during which the current in the inductor (L) forward biases the Schottky diode D1 (V_{FD1}). Therefore the voltage stored across C_{BOOST} is Equation 2:

$$V_{BOOST} – V_{SW} = V_{IN} – V_{FD2} + V_{FD1} \quad (2)$$

When the NMOS switch turns on (T_{ON}), the switch pin rises to Equation 3:

$$V_{SW} = V_{IN} – (R_{DSON} \times I_L), \quad (3)$$

forcing V_{BOOST} to rise, thus reverse biasing D2. The voltage at V_{BOOST} is then Equation 4:

$$V_{BOOST} = 2\ V_{IN} – (R_{DSON} \times I_L) – V_{FD2} + V_{FD1} \quad (4)$$

which is approximately $2\ V_{IN} – 0.4$ V for many applications. Thus the gate-drive voltage of the NMOS switch is approximately $V_{IN} – 0.2$ V.

Feature Description (continued)

An alternate method for charging C_{BOOST} is to connect D2 to the output as shown in Figure 26. The output voltage must be between 2.5 V and 5.5 V so that proper gate voltage is applied to the internal switch. In this circuit, C_{BOOST} provides a gate-drive voltage that is slightly less than V_{OUT}.

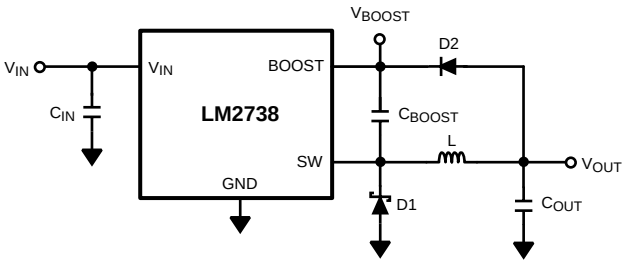


Figure 26. V_{OUT} Charges C_{BOOST}

In applications where both V_{IN} and V_{OUT} are greater than 5.5 V, or less than 3 V, C_{BOOST} cannot be charged directly from these voltages. If V_{IN} and V_{OUT} are greater than 5.5 V, C_{BOOST} can be charged from V_{IN} or V_{OUT} minus a Zener voltage by placing a Zener diode D3 in series with D2, as shown in Figure 27. When using a series Zener diode from the input, ensure that the regulation of the input supply does not create a voltage that falls outside the recommended V_{BOOST} voltage.

$(V_{INMAX} - V_{D3}) < 5.5$ V

$(V_{INMIN} - V_{D3}) > 2.5$ V

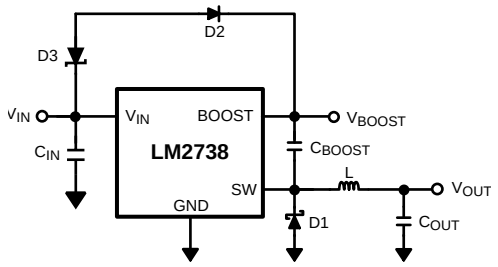


Figure 27. Zener Reduces Boost Voltage from V_{IN}

An alternative method is to place the Zener diode D3 in a shunt configuration as shown in Figure 28. A small 350-mW to 500-mW 5.1-V Zener in a SOT-23 or SOD package can be used for this purpose. A small ceramic capacitor such as a 6.3-V, 0.1-µF capacitor (C4) must be placed in parallel with the Zener diode. When the internal NMOS switch turns on, a pulse of current is drawn to charge the internal NMOS gate capacitance. The 0.1-µF parallel shunt capacitor ensures that the V_{BOOST} voltage is maintained during this time.

Feature Description (continued)

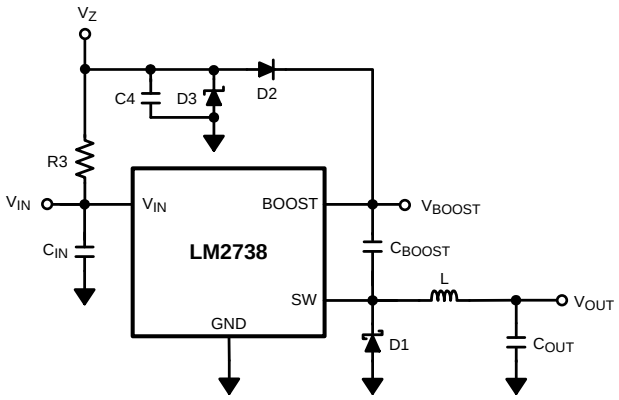


Figure 28. Boost Voltage Supplied from the Shunt Zener on V_{IN}

Resistor R3 must be selected to provide enough RMS current to the Zener diode (D3) and to the BOOST pin. A recommended choice for the Zener current (I_{ZENER}) is 1 mA. The current I_{BOOST} into the BOOST pin supplies the gate current of the NMOS control switch and varies typically according to the formula in Equation 5 for the X version:

$$I_{BOOST} = 0.56 \times (D + 0.54) \times (V_{ZENER} - V_{D2})\ mA \quad (5)$$

I_{BOOST} can be calculated for the Y version using Equation 6:

$$I_{BOOST} = 0.22 \times (D + 0.54) \times (V_{ZENER} - V_{D2})\ \mu A$$

where

- D is the duty cycle
- V_{ZENER} and V_{D2} are in volts
- I_{BOOST} is in milliamps
- V_{ZENER} is the voltage applied to the anode of the boost diode (D2)
- V_{D2} is the average forward voltage across D2 (6)

The formula for I_{BOOST} in Equation 6 gives typical current. For the worst case I_{BOOST}, increase the current by 40%. In that case, the worst case boost current is Equation 7:

$$I_{BOOST\text{-}MAX} = 1.4 \times I_{BOOST} \quad (7)$$

R3 is then given by Equation 8:

$$R3 = (V_{IN} - V_{ZENER}) / (1.4 \times I_{BOOST} + I_{ZENER}) \quad (8)$$

For example, using the X-version let V_{IN} = 10 V, V_{ZENER} = 5 V, V_{D2} = 0.7 V, I_{ZENER} = 1 mA, and duty cycle D = 50%. Then Equation 9 and Equation 10:

$$I_{BOOST} = 0.56 \times (0.5 + 0.54) \times (5 - 0.7)\ mA = 2.5\ mA \quad (9)$$

$$R3 = (10\ V - 5\ V) / (1.4 \times 2.5\ mA + 1\ mA) = 1.11\ k\Omega \quad (10)$$

7.3.2 Soft-Start

This function forces V_{OUT} to increase at a controlled rate during start-up. During soft-start, the error amplifier's reference voltage ramps from 0 V to its nominal value of 0.8 V in approximately 600 µs. This forces the regulator output to ramp up in a more linear and controlled fashion, which helps reduce in-rush current.

7.3.3 Output Overvoltage Protection

The overvoltage comparator compares the FB pin voltage to a voltage that is 16% higher than the internal reference V_{REF}. Once the FB pin voltage goes 16% above the internal reference, the internal NMOS control switch is turned off, which allows the output voltage to decrease toward regulation.

Feature Description (continued)

7.3.4 Undervoltage Lockout

Undervoltage lockout (UVLO) prevents the LM2738 from operating until the input voltage exceeds 2.7 V (typical).

The UVLO threshold has approximately 400 mV of hysteresis, so the part operates until V_{IN} drops below 2.3 V (typical). Hysteresis prevents the part from turning off during power up if the V_{IN} ramp-up is non-monotonic.

7.3.5 Current Limit

The LM2738 uses cycle-by-cycle current limiting to protect the output switch. During each switching cycle, a current limit comparator detects if the output switch current exceeds 2.9 A (typical), and turns off the switch until the next switching cycle begins.

7.3.6 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the output switch when the device junction temperature exceeds 165°C. After thermal shutdown occurs, the output switch doesn't turn on until the junction temperature drops to approximately 150°C.

7.4 Device Functional Modes

7.4.1 Enable Pin and Shutdown Mode

The LM2738 has a shutdown mode that is controlled by the enable pin (EN). When a logic low voltage is applied to EN, the part is in shutdown mode, and its quiescent current drops to typically 400 nA. The voltage at this pin must never exceed V_{IN} + 0.3 V.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2738 operates over a wide range of conditions, which is limited by the ON time of the device. Figure 29 shows the recommended operating area for the X version at the full load (1.5 A) and at 25°C ambient temperature. The Y version of the LM2738 operates at a lower frequency, and therefore operates over the entire range of operating voltages.

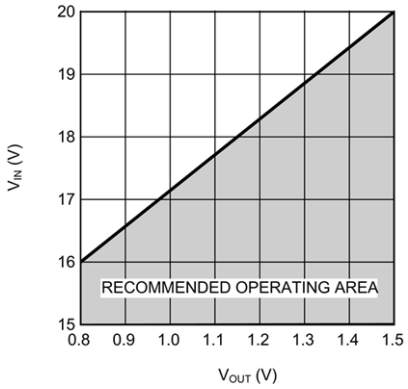


Figure 29. LM2738X – 1.6 MHz (25°C, Load = 1.5 A)

8.2 Typical Applications

8.2.1 LM2738X Circuit Example 1

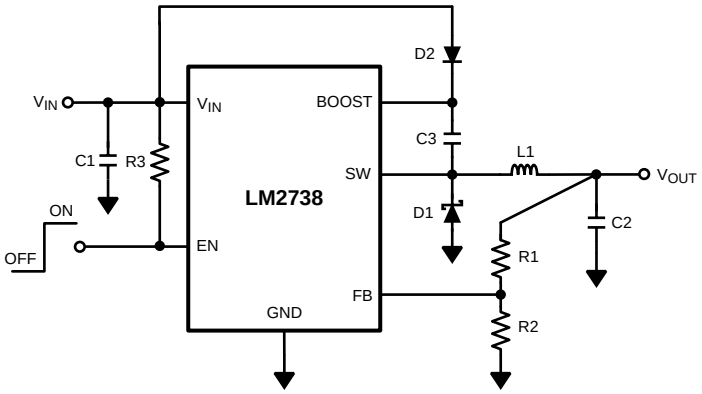


Figure 30. LM2738X (1.6 MHz)
V_{BOOST} Derived from V_{IN}
5 V to 1.5 V/1.5 A

8.2.1.1 Design Requirements

The device must be able to operate at any voltage within the *Recommended Operating Conditions*. The load current must be defined to properly size the inductor, input, and output capacitors. The inductor must be able to support the full expected load current as well as the peak current generated from load transients and start-up.

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

Table 1. Bill of Materials for Figure 30

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1.5-A Buck Regulator	LM2738X	Texas Instruments
C1, Input Cap	10 µF, 6.3 V, X5R	C3216X5ROJ106M	TDK
C2, Output Cap	22 µF, 6.3 V, X5R	C3216X5ROJ226M	TDK
C3, Boost Cap	0.1 uF, 16 V, X7R	C1005X7R1C104K	TDK
D1, Catch Diode	0.34 V_F Schottky 1.5 A, 30 V	CRS08	Toshiba
D2, Boost Diode	1 V_F at 100-mA Diode	BAT54WS	Diodes, Inc.
L1	2.2 µH, 1.9 A,	MSS5131-222ML	Coilcraft
R1	8.87 kΩ, 1%	CRCW06038871F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.1.2.1 Inductor Selection

The duty cycle (D) can be approximated quickly using the ratio of output voltage (V_O) to input voltage (V_{IN}), using Equation 11:

$$D = \frac{V_O}{V_{IN}} \tag{11}$$

The catch diode (D1) forward voltage drop and the voltage drop across the internal NMOS switch must be included to calculate a more accurate duty cycle. Calculate D by using Equation 12:

$$D = \frac{V_O + V_D}{V_{IN} + V_D - V_{SW}} \tag{12}$$

V_{SW} can be approximated by Equation 13:

$$V_{SW} = I_{OUT} \times R_{DSON} \tag{13}$$

The diode forward drop (V_D) can range from 0.3 V to 0.7 V depending on the quality of the diode. The lower the V_D, the higher the operating efficiency of the converter. The inductor value determines the output ripple current. Lower inductor values decrease the size of the inductor, but increase the output ripple current. An increase in the inductor value decreases the output ripple current.

One must ensure that the minimum current limit (2 A) is not exceeded, so the peak current in the inductor must be calculated. The peak current (I_{LPK}) in the inductor is calculated by Equation 14 and Equation 15:

$$I_{LPK} = I_{OUT} + \Delta i_L \tag{14}$$

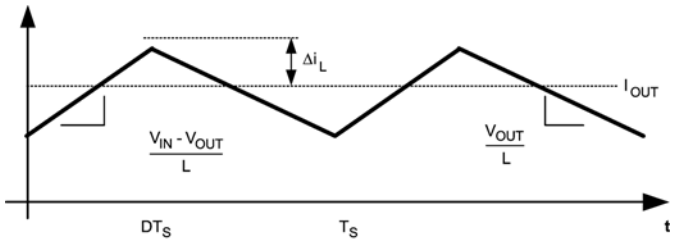


Figure 31. Inductor Current

$$\frac{V_{IN} - V_{OUT}}{L} = \frac{2\Delta i_L}{DT_S} \tag{15}$$

In general in Equation 16,

$$\Delta i_L = 0.1 \times (I_{OUT}) \rightarrow 0.2 \times (I_{OUT}) \tag{16}$$

Typical Applications (continued)

If Δi_L = 33.3% of 1.5 A, the peak current in the inductor is 2 A. The minimum specified current limit over all operating conditions is 2 A. One can either reduce Δi_L, or make the engineering judgment that zero margin is safe enough. The typical current limit is 2.9 A.

The LM2738 operates at frequencies allowing the use of ceramic output capacitors without compromising transient response. Ceramic capacitors allow higher inductor ripple without significantly increasing output ripple. See the *Output Capacitor* section for more details on calculating output voltage ripple. Now that the ripple current is determined, the inductance is calculated by Equation 17:

$$P_{COND} = (I_{OUT}^2 \times D)\left(1 + \frac{1}{3} \times \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) R_{DSON}$$

where

- $T_S = \frac{1}{f_S}$ (17)

When selecting an inductor, make sure that it is capable of supporting the peak output current without saturating. Inductor saturation results in a sudden reduction in inductance and prevents the regulator from operating correctly. Because of the speed of the internal current limit, the peak current of the inductor need only be specified for the required maximum output current. For example, if the designed maximum output current is 1 A and the peak current is 1.25 A, the inductor must be specified with a saturation current limit of > 1.25 A. There is no must specify the saturation or peak current of the inductor at the 2.9-A typical switch current limit. Because of the operating frequency of the LM2738, ferrite based inductors are preferred to minimize core losses. This presents little restriction because of the variety of ferrite-based inductors available. Lastly, inductors with lower series resistance (R_{DCR}) provide better operating efficiency. For recommended inductors see *LM2738X Circuit Example 1*.

8.2.1.2.2 Input Capacitor

An input capacitor is necessary to ensure that V_{IN} does not drop excessively during switching transients. The primary specifications of the input capacitor are capacitance, voltage, RMS current rating, and equivalent series inductance (ESL). The recommended input capacitance is 10 µF. The input voltage rating is specifically stated by the capacitor manufacturer. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating input voltage and the operating temperature. The input capacitor maximum RMS input current rating ($I_{RMS\text{-}IN}$) must be greater than Equation 18:

$$I_{RMS\_IN} \sqrt{D\left[I_{OUT}^2 (1-D) + \frac{2\Delta i_L}{3}\right]} \quad (18)$$

Neglecting inductor ripple simplifies Equation 18 to Equation 19:

$$I_{RMS\_IN} = I_{OUT} \times \sqrt{D(1-D)} \quad (19)$$

Equation 19 shows that maximum RMS capacitor current occurs when D = 0.5. Always calculate the RMS at the point where the duty cycle D is closest to 0.5. The ESL of an input capacitor is usually determined by the effective cross-sectional area of the current path. A large leaded capacitor has high ESL and a 0805 ceramic-chip capacitor has very low ESL. At the operating frequencies of the LM2738, leaded capacitors may have an ESL so large that the resulting impedance (2πfL) is higher than that required to provide stable operation. As a result, surface-mount capacitors are strongly recommended.

Sanyo POSCAP, Tantalum or Niobium, Panasonic SP, and multilayer ceramic capacitors (MLCC) are all good choices for both input and output capacitors and have very low ESL. For MLCCs, TI recommends using X7R or X5R type capacitors due to their tolerance and temperature characteristics. Consult the capacitor manufacturer's data sheets to see how rated capacitance varies over operating conditions.

8.2.1.2.3 Output Capacitor

The output capacitor is selected based upon the desired output ripple and transient response. The initial current of a load transient is provided mainly by the output capacitor. The output ripple of the converter is Equation 20:

Typical Applications (continued)

$$\Delta V_{OUT} = \Delta I_L \left(R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}} \right) \quad (20)$$

When using MLCCs, the equivalent series resistance (ESR) is typically so low that the capacitive ripple may dominate. When this occurs, the output ripple is approximately sinusoidal and 90° phase shifted from the switching action. Given the availability and quality of MLCCs and the expected output voltage of designs using the LM2738, there is really no must review any other capacitor technologies. Another benefit of ceramic capacitors is the ability to bypass high-frequency noise. A certain amount of switching edge noise couples through parasitic capacitances in the inductor to the output. A ceramic capacitor bypasses this noise while a tantalum capacitor does not. Since the output capacitor is one of the two external components that control the stability of the regulator control loop, most applications require a minimum of 22 µF of output capacitance. Capacitance, in general, is often increased when operating at lower duty cycles. Refer to the *Circuit Examples* for suggested output capacitances of common applications. Like the input capacitor, recommended multilayer ceramic capacitors are X7R or X5R types.

8.2.1.2.4 Catch Diode

The catch diode (D1) conducts during the switch off time. A Schottky diode is recommended for its fast switching times and low forward voltage drop. The catch diode must be chosen so that its current rating is greater than Equation 21:

$$I_{D1} = I_{OUT} \times (1\text{-}D) \quad (21)$$

The reverse breakdown rating of the diode must be at least the maximum input voltage plus appropriate margin. To improve efficiency, choose a Schottky diode with a low forward-voltage drop.

8.2.1.2.5 Output Voltage

The output voltage is set using Equation 22 and Equation 23 where R2 is connected between the FB pin and GND, and R1 is connected between V_O and the FB pin. A good value for R2 is 10 kΩ. When designing a unity gain converter (V_O = 0.8 V), R1 must be between 0 Ω and 100 Ω, and R2 must not be loaded.

$$R1 = \left(\frac{V_O}{V_{REF}} - 1 \right) \times R2 \quad (22)$$

$$V_{REF} = 0.80\ V \quad (23)$$

8.2.1.2.6 Calculating Efficiency and Junction Temperature

The complete LM2738 DC-DC converter efficiency can be calculated by Equation 24 or Equation 25:

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (24)$$

or,

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_{LOSS}} \quad (25)$$

Calculations for determining the most significant power losses are shown in Equation 26. Other losses totaling less than 2% are not discussed.

Power loss (P_{LOSS}) is the sum of two basic types of losses in the converter: switching and conduction. Conduction losses usually dominate at higher output loads, whereas switching losses remain relatively fixed and dominate at lower output loads. The first step in determining the losses is to calculate the duty cycle (D):

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{SW}} \quad (26)$$

V_{SW} is the voltage drop across the internal NFET when it is on, and is equal to Equation 27:

$$V_{SW} = I_{OUT} \times R_{DSON} \quad (27)$$

Typical Applications (continued)

V_D is the forward voltage drop across the Schottky catch diode. It can be obtained from the diode manufacturer's data sheet *Electrical Characteristics* section. If the voltage drop across the inductor (V_{DCR}) is accounted for, the equation becomes Equation 28:

$$D = \frac{V_{OUT} + V_D + V_{DCR}}{V_{IN} + V_D + V_{DCR} - V_{SW}} \quad (28)$$

The conduction losses in the free-wheeling Schottky diode are calculated by Equation 29:

$$P_{DIODE} = V_D \times I_{OUT} \times (1\text{-}D) \quad (29)$$

Often this is the single most significant power loss in the circuit. Care must be taken to choose a Schottky diode that has a low forward-voltage drop.

Another significant external power loss is the conduction loss in the output inductor. The equation can be simplified to Equation 30:

$$P_{IND} = I_{OUT}^2 \times R_{DCR} \quad (30)$$

The LM2738 conduction loss is mainly associated with the internal NFET switch in Equation 31:

$$P_{COND} = (I_{OUT}^2 \times D)\left(1 + \frac{1}{3} \times \left(\frac{\Delta i_L}{I_{OUT}}\right)^2\right) R_{DSON} \quad (31)$$

If the inductor ripple current is fairly small, the conduction losses can be simplified to Equation 32:

$$P_{COND} = I_{OUT}^2 \times R_{DSON} \times D \quad (32)$$

Switching losses are also associated with the internal NFET switch. They occur during the switch on and off transition periods, where voltages and currents overlap resulting in power loss. The simplest means to determine this loss is to empirically measure the rise and fall times (10% to 90%) of the switch at the switch node.

Switching Power Loss is calculated as follows in Equation 33, Equation 34, and Equation 35:

$$P_{SWR} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{RISE}) \quad (33)$$

$$P_{SWF} = 1/2(V_{IN} \times I_{OUT} \times F_{SW} \times T_{FALL}) \quad (34)$$

$$P_{SW} = P_{SWR} + P_{SWF} \quad (35)$$

Another loss is the power required for operation of the internal circuitry in Equation 36:

$$P_Q = I_Q \times V_{IN} \quad (36)$$

I_Q is the quiescent operating current, and is typically around 1.9 mA for the 0.55-MHz frequency option.

Table 2 lists the power losses for a typical application, and in Equation 37, Equation 38, and Equation 39.

Table 2. Typical Configuration and Power Loss Calculation

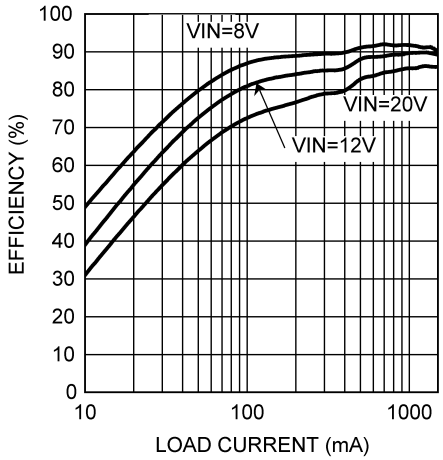
PARAMETER	VALUE	POWER PARAMETER	CALCULATED POWER
V_{IN}	12 V	—	—
V_{OUT}	3.3 V	P_{OUT}	4.125 W
I_{OUT}	1.25 A	—	—
V_D	0.34 V	P_{DIODE}	317 mW
F_{SW}	550 kHz	—	—
I_Q	1.9 mA	P_Q	22.8 mW
T_{RISE}	8 nS	P_{SWR}	33 mW
T_{FALL}	8 nS	P_{SWF}	33 mW
$R_{DS(ON)}$	275 mΩ	P_{COND}	118 mW
IND_{DCR}	70 mΩ	P_{IND}	110 mW
D	0.275	P_{LOSS}	634 mW
η	86.7%	$P_{INTERNAL}$	207 mW

$$\Sigma P_{COND} + P_{SW} + P_{DIODE} + P_{IND} + P_Q = P_{LOSS} \quad (37)$$

$$\Sigma P_{COND} + P_{SWF} + P_{SWR} + P_Q = P_{INTERNAL} \quad (38)$$

$$P_{INTERNAL} = 207 \text{ mW} \quad (39)$$

8.2.1.3 Application Curve



V_{OUT} = 5 V

Figure 32. Efficiency vs Load Current – X Version

8.2.2 LM2738X Circuit Example 2

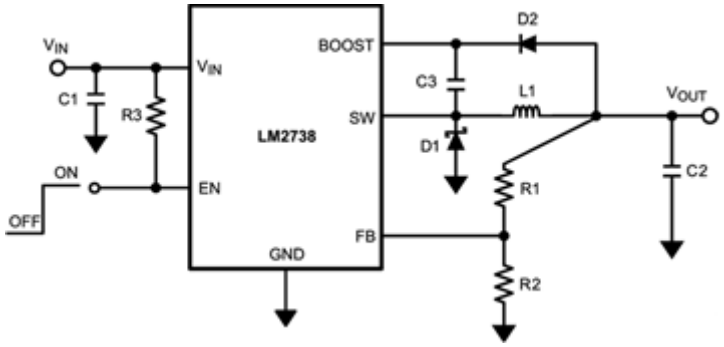


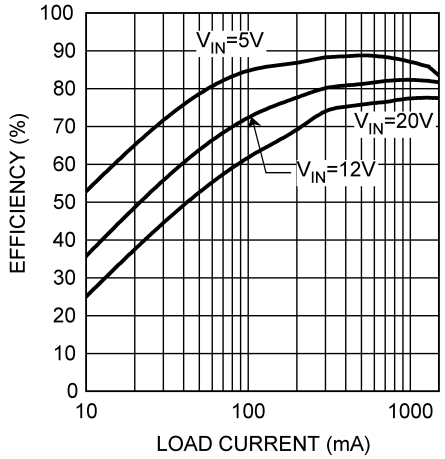
Figure 33. LM2738X (1.6 MHz)
V_{BOOST} Derived from V_{OUT}
12 V to 3.3 V / 1.5 A

8.2.2.1 Detailed Design Procedure

Table 3. Bill of Materials for Figure 33

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1.5-A Buck Regulator	LM2738X	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	33 µF, 6.3 V, X5R	C3216X5ROJ336M	TDK
C3, Boost Cap	0.1 µF, 16 V, X7R	C1005X7R1C104K	TDK
D1, Catch Diode	0.34 V_F Schottky 1.5 A, 30 V	CRS08	Toshiba
D2, Boost Diode	1 V_F at 100-mA Diode	BAT54WS	Diodes, Inc.
L1	5 µH, 2.9 A	MSS7341- 502NL	Coilcraft
R1	31.6 kΩ, 1%	CRCW06033162F	Vishay
R2	10 kΩ, 1%	CRCW06031002F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.2.2 Application Curve



V_{OUT} = 3.3 V

Figure 34. Efficiency vs Load Current – X Version

8.2.3 LM2738X Circuit Example 3

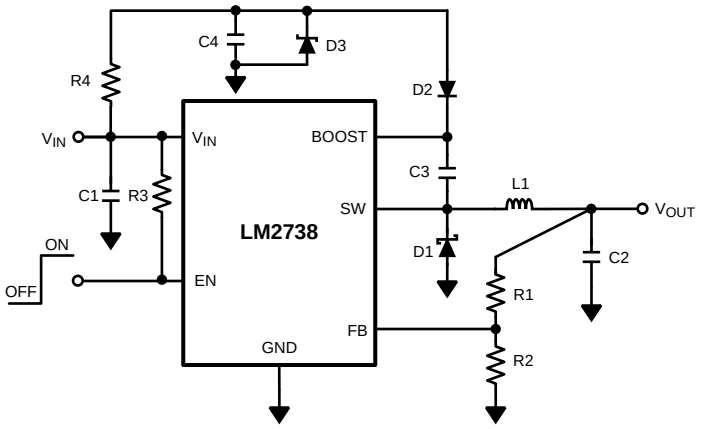


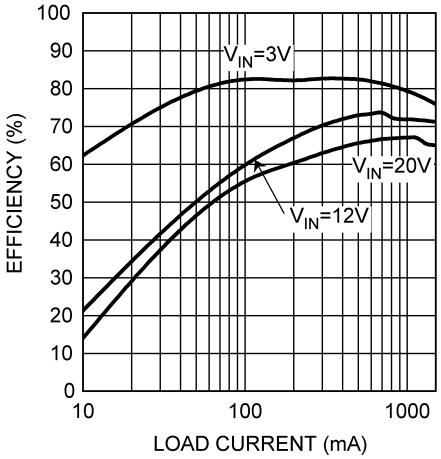
Figure 35. LM2738X (1.6 MHz)
V_{BOOST} Derived from V_{SHUNT}
18 V to 1.5 V / 1.5 A

8.2.3.1 Detailed Design Procedure

Table 4. Bill of Materials for Figure 35

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1.5-A Buck Regulator	LM2738X	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	47 µF, 6.3 V, X5R	C3216X5ROJ476M	TDK
C3, Boost Cap	0.1 µF, 16 V, X7R	C1005X7R1C104K	TDK
C4, Shunt Cap	0.1 µF, 6.3 V, X5R	C1005X5R0J104K	TDK
D1, Catch Diode	0.34 V_F Schottky 1.5 A, 30 V	CRS08	Toshiba
D2, Boost Diode	1 V_F at 100-mA Diode	BAT54WS	Diodes, Inc.
D3, Zener Diode	5.1-V 250-Mw SOT-23	BZX84C5V1	Vishay
L1	2.7 µH, 1.76 A	VLCF5020T-2R7N1R7	TDK
R1	8.87 kΩ, 1%	CRCW06038871F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay
R4	4.12 kΩ, 1%	CRCW06034121F	Vishay

8.2.3.2 Application Curve



V_{OUT} = 1.5 V

Figure 36. Efficiency vs Load Current – X Version

8.2.4 LM2738X Circuit Example 4

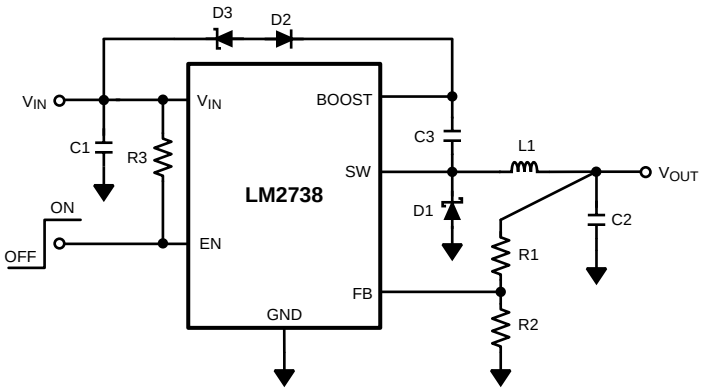


Figure 37. LM2738X (1.6 MHz)
V_{BOOST} Derived from Series Zener Diode (V_{IN})
15 V to 1.5 V / 1.5 A

8.2.4.1 Detailed Design Procedure

Table 5. Bill of Materials for Figure 37

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1.5-A Buck Regulator	LM2738X	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	47 µF, 6.3 V, X5R	C3216X5ROJ476M	TDK
C3, Boost Cap	0.1 µF, 16 V, X7R	C1005X7R1C104K	TDK
D1, Catch Diode	0.34 V_F Schottky 1.5 A, 30 V	CRS08	Toshiba
D2, Boost Diode	1 V_F at 100-mA Diode	BAT54WS	Diodes, Inc.
D3, Zener Diode	11-V 350-Mw SOT-23	BZX84C11T	Diodes, Inc.
L1	3.3 µH, 3.5 A	MSS7341-332NL	Coilcraft
R1	8.87 kΩ, 1%	CRCW06038871F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.5 LM2738X Circuit Example 5

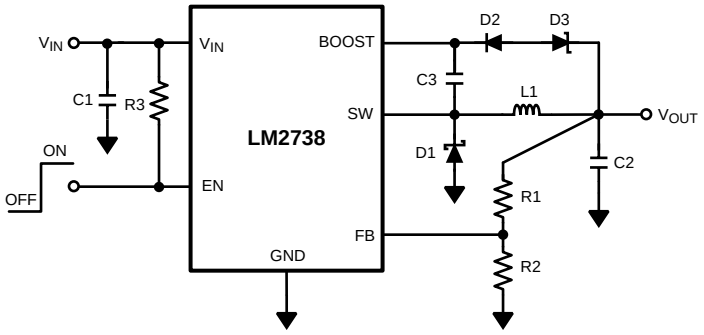


Figure 38. LM2738X (1.6 MHz)
V_{BOOST} Derived from Series Zener Diode (V_{OUT})
15 V to 9 V / 1.5 A

8.2.5.1 Detailed Design Procedure

Table 6. Bill of Materials for Figure 38

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1.5-A Buck Regulator	LM2738X	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22 µF, 16 V, X5R	C3216X5R1C226M	TDK
C3, Boost Cap	0.1 µF, 16 V, X7R	C1005X7R1C104K	TDK
D1, Catch Diode	0.34 V_F Schottky 1.5 A, 30 V	CRS08	Toshiba
D2, Boost Diode	1 V_F at 100-mA Diode	BAT54WS	Diodes, Inc.
D3, Zener Diode	4.3-V 350-mw SOT-23	BZX84C4V3	Diodes, Inc.
L1	6.2 µH, 2.5 A	MSS7341-622NL	Coilcraft
R1	102 kΩ, 1%	CRCW06031023F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.6 LM2738Y Circuit Example 6

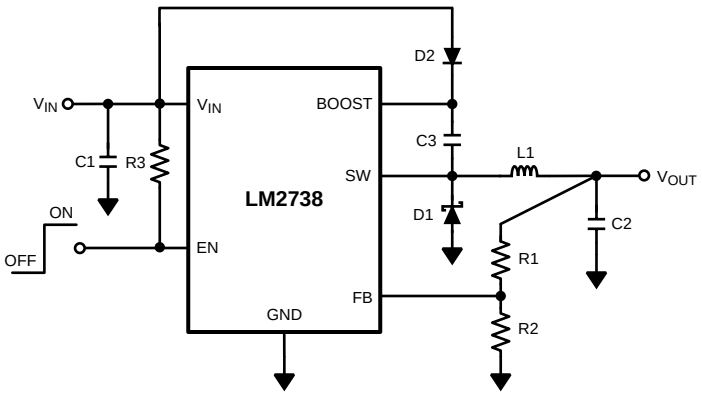


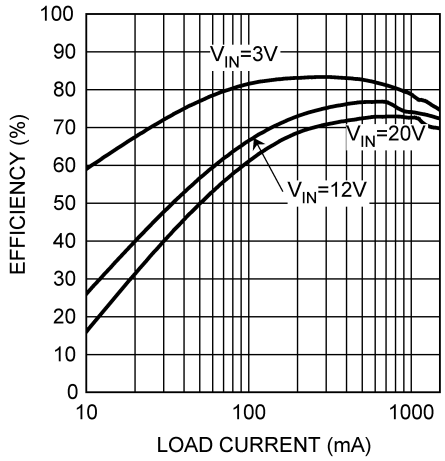
Figure 39. LM2738Y (550 kHz)
V_{BOOST} Derived from V_{IN}
5 V to 1.5 V / 1.5 A

8.2.6.1 Detailed Design Procedure

Table 7. Bill of Materials for Figure 39

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1.5-A Buck Regulator	LM2738Y	Texas Instruments
C1, Input Cap	10 µF, 6.3 V, X5R	C3216X5ROJ106M	TDK
C2, Output Cap	47 µF, 6.3 V, X5R	C3216X5ROJ476M	TDK
C3, Boost Cap	0.1 µF, 16 V, X7R	C1005X7R1C104K	TDK
D1, Catch Diode	0.34 V_F Schottky 1.5 A, 30 V	CRS08	Toshiba
D2, Boost Diode	1 V_F at 100-mA Diode	BAT54WS	Diodes, Inc.
L1	6.2 µH, 2.5 A,	MSS7341-622NL	Coilcraft
R1	8.87 kΩ, 1%	CRCW06038871F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.6.2 Application Curve



V_{OUT} = 1.5 V

Figure 40. Efficiency vs Load Current – Y Version

8.2.7 LM2738Y Circuit Example 7

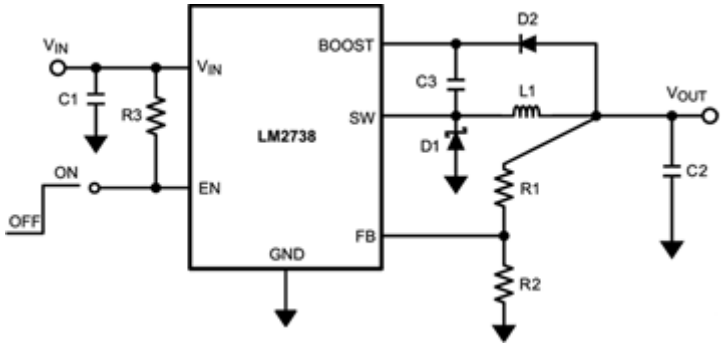


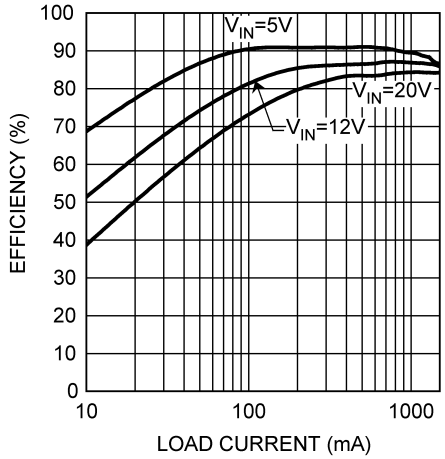
Figure 41. LM2738Y (550 kHz)
V_{BOOST} Derived from V_{OUT}
12 V to 3.3 V / 1.5 A

8.2.7.1 Detailed Design Procedure

Table 8. Bill of Materials for Figure 41

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1.5-A Buck Regulator	LM2738Y	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	47 µF, 6.3 V, X5R	C3216X5ROJ476M	TDK
C3, Boost Cap	0.1 µF, 16 V, X7R	C1005X7R1C104K	TDK
D1, Catch Diode	0.34 V_F Schottky 1.5 A, 30 V	CRS08	Toshiba
D2, Boost Diode	1 V_F at 100-mA Diode	BAT54WS	Vishay
L1	12 µH, 1.7 A,	MSS7341-123NL	Coilcraft
R1	31.6 kΩ, 1%	CRCW06033162F	Vishay
R2	10 kΩ, 1%	CRCW06031002F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.7.2 Application Curve



V_{OUT} = 3.3 V

Figure 42. Efficiency vs Load Current – Y Version

8.2.8 LM2738Y Circuit Example 8

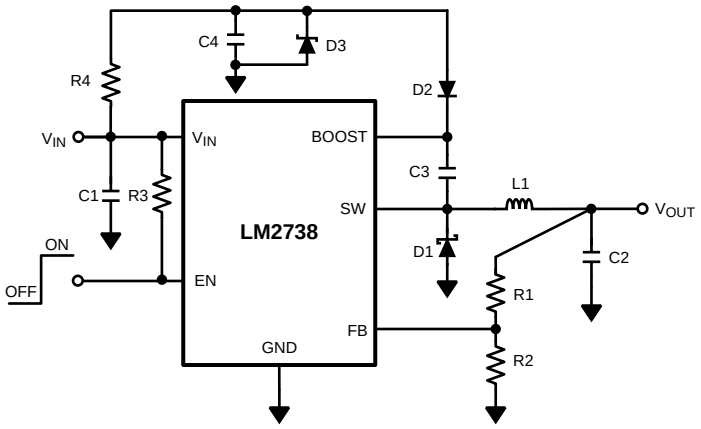


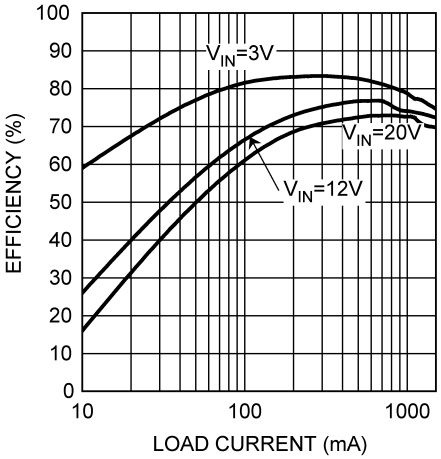
Figure 43. LM2738Y (550 kHz)
V_{BOOST} Derived from V_{SHUNT}
18 V to 1.5 V / 1.5 A

8.2.8.1 Detailed Design Procedure

Table 9. Bill of Materials for Figure 43

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1.5-A Buck Regulator	LM2738Y	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	(47 µF, 6.3 V, X5R) × 2 = 94 µF	C3216X5ROJ476M	TDK
C3, Boost Cap	0.1 µF, 16 V, X7R	C1005X7R1C104K	TDK
C4, Shunt Cap	0.1 µF, 6.3 V, X5R	C1005X5R0J104K	TDK
D1, Catch Diode	0.34 V_F Schottky 1.5 A, 30 V	CRS08	Toshiba
D2, Boost Diode	1 V_F at 100-mA Diode	BAT54WS	Diodes, Inc.
D3, Zener Diode	5.1-V 250-Mw SOT-23	BZX84C5V1	Vishay
L1	8.7 µH, 2.2 A	MSS7341-872NL	Coilcraft
R1	8.87 kΩ, 1%	CRCW06038871F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay
R4	4.12 kΩ, 1%	CRCW06034121F	Vishay

8.2.8.2 Application Curve



V_{OUT} = 1.5 V

Figure 44. Efficiency vs Load Current – Y Version

8.2.9 LM2738Y Circuit Example 9

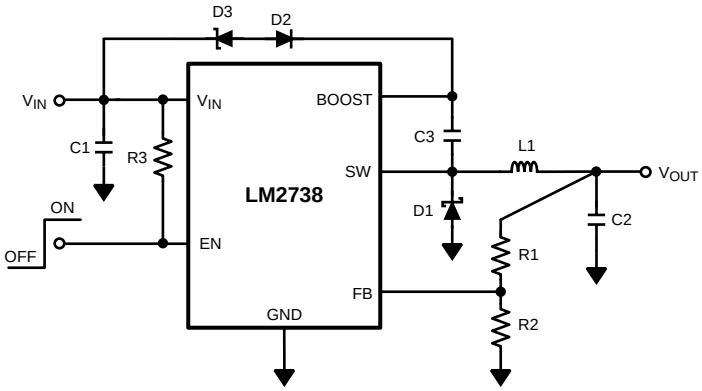


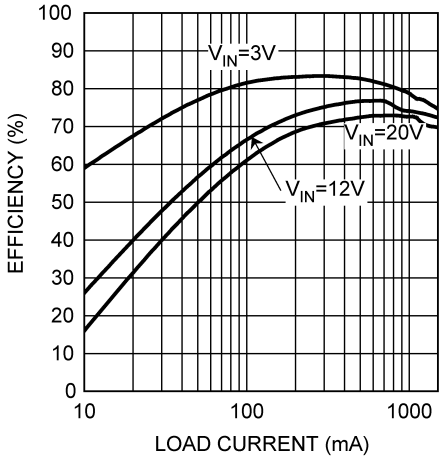
Figure 45. LM2738Y (550 kHz)
V_{BOOST} Derived from Series Zener Diode (V_{IN})
15 V to 1.5 V / 1.5 A

8.2.9.1 Detailed Design Procedure

Table 10. Bill of Materials for Figure 45

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1.5-A Buck Regulator	LM2738Y	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	(47 µF, 6.3 V, X5R) × 2 = 94 µF	C3216X5ROJ476M	TDK
C3, Boost Cap	0.1 µF, 16 V, X7R	C1005X7R1C104K	TDK
D1, Catch Diode	0.34 V_F Schottky 1.5 A, 30 V	CRS08	Toshiba
D2, Boost Diode	1 V_F at 100-mA Diode	BAT54WS	Diodes, Inc.
D3, Zener Diode	11-V 350-Mw SOT-23	BZX84C11T	Diodes, Inc.
L1	8.7 µH, 2.2 A	MSS7341-872NL	Coilcraft
R1	8.87 kΩ, 1%	CRCW06038871F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

8.2.9.2 Application Curve



V_{OUT} = 1.5 V

Figure 46. Efficiency vs Load Current – Y Version

8.2.10 LM2738Y Circuit Example 10

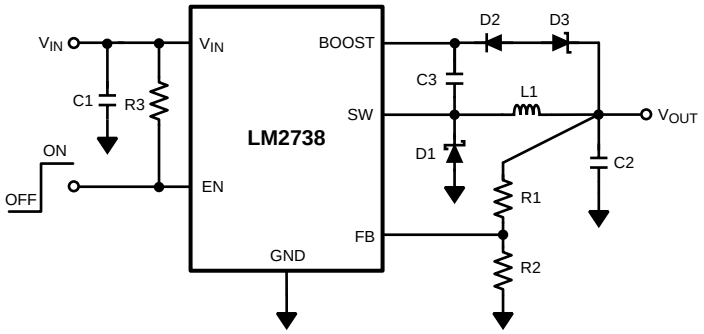


Figure 47. LM2738Y (550 kHz)
V_{BOOST} Derived from Series Zener Diode (V_{OUT})
15 V to 9 V / 1.5 A

8.2.10.1 Detailed Design Procedure

Table 11. Bill of Materials for Figure 47

PART ID	PART VALUE	PART NUMBER	MANUFACTURER
U1	1.5-A Buck Regulator	LM2738Y	Texas Instruments
C1, Input Cap	10 µF, 25 V, X7R	C3225X7R1E106M	TDK
C2, Output Cap	22 µF, 16 V, X5R	C3216X5R1C226M	TDK
C3, Boost Cap	0.1 µF, 16 V, X7R	C1005X7R1C104K	TDK
D1, Catch Diode	0.34 V_F Schottky 1.5 A, 30 V	CRS08	Toshiba
D2, Boost Diode	1 V_F at 100-mA Diode	BAT54WS	Diodes, Inc.
D3, Zener Diode	4.3-V 350-mw SOT-23	BZX84C4V3	Diodes, Inc.
L1	15 µH, 2.1 A	SLF7055T150M2R1-3PF	TDK
R1	102 kΩ, 1%	CRCW06031023F	Vishay
R2	10.2 kΩ, 1%	CRCW06031022F	Vishay
R3	100 kΩ, 1%	CRCW06031003F	Vishay

9 Power Supply Recommendations

The input voltage is rated as 3 V to 20 V. Care must be taken in certain circuit configurations, such as when V_{BOOST} is derived from V_{IN}, where the requirement that $V_{BOOST} - V_{SW}$ is less than 5.5 V must be observed. Also for best efficiency, V_{BOOST} must be at least 2.5 V above V_{SW}. The voltage on the enable (EN) pin must not exceed V_{IN} by more than 0.3 V.

10 Layout

10.1 Layout Guidelines

When planning layout there are a few things to consider when trying to achieve a clean, regulated output. The most important consideration is the close coupling of the GND connections of the input capacitor and the catch diode D1. These ground ends must be close to one another and be connected to the GND plane with at least two through-holes. Place these components as close as possible to the device. Next in importance is the location of the GND connection of the output capacitor, which must be near the GND connections of C_{IN} and D1. There must be a continuous ground plane on the bottom layer of a two-layer board except under the switching node island. The FB pin is a high-impedance node, and take care to make the FB trace short to avoid noise pickup and inaccurate regulation. The feedback resistors must be placed as close to the device as possible, with the GND of R1 placed as close to the GND of the device as possible. The V_{OUT} trace to R2 must be routed away from the inductor and any other traces that are switching. High AC currents flow through the V_{IN}, SW, and V_{OUT} traces, so they must be as short and wide as possible. However, making the traces wide increases radiated noise, so the designer must make this trade-off. Radiated noise can be decreased by choosing a shielded inductor. The remaining components must also be placed as close to the device as possible. See *AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines* (SNVA054) for further considerations, and the LM2738 demo board as an example of a four-layer layout.

10.1.1 WSON Package

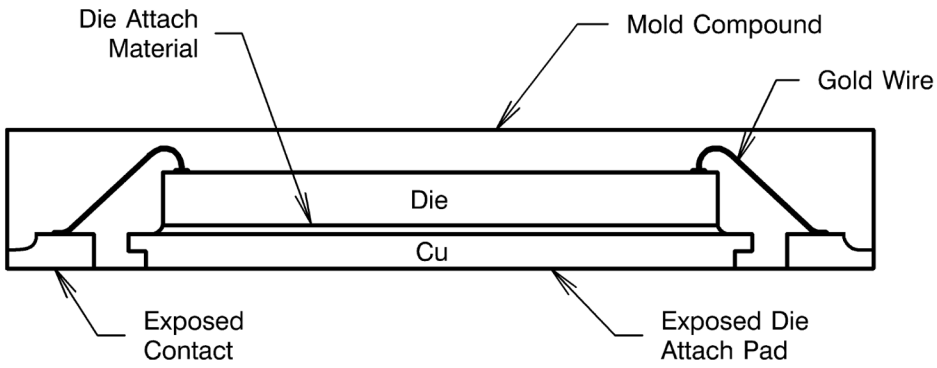


Figure 48. Internal WSON Connection

For certain high power applications, the PCB land may be modified to a dog-bone shape (see Figure 49). By increasing the size of ground plane, and adding thermal vias, the $R_{\theta JA}$ for the application can be reduced.

10.2 Layout Example

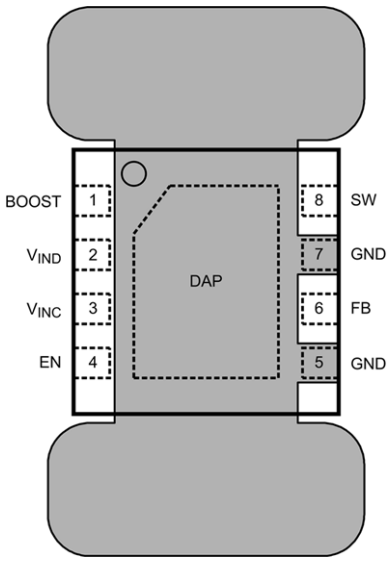


Figure 49. 8-Lead WSON PCB Dog Bone Layout

10.3 Thermal Considerations

Heat in the LM2738 due to internal power dissipation is removed through conduction and/or convection.

Conduction: Heat transfer occurs through cross sectional areas of material. Depending on the material, the transfer of heat can be considered to have poor to good thermal conductivity properties (insulator vs. conductor).

Heat Transfer goes as:

Silicon → package → lead frame → PCB

Convection: Heat transfer is by means of airflow. This could be from a fan or natural convection. Natural convection occurs when air currents rise from the hot device to cooler air.

Thermal impedance is defined as Equation 40:

$$R\theta = \frac{\Delta T}{Power} \tag{40}$$

Thermal impedance from the silicon junction to the ambient air is defined as Equation 41:

$$R\theta_{JA} = \frac{T_J - T_A}{Power} \tag{41}$$

The PCB size, weight of copper used to route traces and ground plane, and number of layers within the PCB can greatly effect $R_{\theta JA}$. The type and number of thermal vias can also make a large difference in the thermal impedance. Thermal vias are necessary in most applications. They conduct heat from the surface of the PCB to the ground plane. Four to six thermal vias must be placed under the exposed pad to the ground plane if the WSON package is used.

Thermal impedance also depends on the thermal properties due to the application's operating conditions (V_{IN}, V_O, I_O and so forth), and the surrounding circuitry.

10.3.1 Silicon Junction Temperature Determination Methods

To accurately measure the silicon temperature for a given application, two methods can be used.

10.3.1.1 Method 1

The first method requires the user to know the thermal impedance of the silicon junction to top case temperature.

Thermal Considerations (continued)

To clarify:

$R_{\theta JC}$ is the thermal impedance from all six sides of a device package to silicon junction.

In this data sheet $R_{\Phi JC}$ is used, allowing the user to measure top case temperature with a small thermocouple attached to the top case.

$R_{\Phi JC}$ is approximately 30°C/W for the 8-pin WSON package with the exposed pad. With the internal dissipation from the efficiency calculation given previously, and the case temperature, $R_{\Phi JC}$ can be empirically measured on the bench as Equation 42.

$$R\Phi_{JC} = \frac{T_J - T_C}{\text{Power}} \quad (42)$$

Therefore in Equation 43:

$$T_j = (R_{\Phi JC} \times P_{LOSS}) + T_C \quad (43)$$

From the previous example, shows Equation 44 and Equation 45:

$$T_j = (R_{\Phi JC} \times P_{INTERNAL}) + T_C \quad (44)$$

$$T_j = 30°C/W \times 0.207\ W + T_C \quad (45)$$

10.3.1.2 Method 2

The second method can give a very accurate silicon junction temperature.

The first step is to determine $R_{\theta JA}$ of the application. The LM2738 has overtemperature protection circuitry. When the silicon temperature reaches 165°C, the device stops switching. The protection circuitry has a hysteresis of about 15°C. Once the silicon temperature has decreased to approximately 150°C, the device starts to switch again. Knowing this, the $R_{\theta JA}$ for any application can be characterized during the early stages of the design one may calculate the $R_{\theta JA}$ by placing the PCB circuit into a thermal chamber. Raise the ambient temperature in the given working application until the circuit enters thermal shutdown. If the SW pin is monitored, it is obvious when the internal NFET stops switching, indicating a junction temperature of 165°C. Knowing the internal power dissipation from the above equations, the junction temperature and the ambient temperature $R_{\theta JA}$ can be determined with Equation 46.

$$R\theta_{JA} = \frac{165° - T_A}{P_{INTERNAL}} \quad (46)$$

Once $R_{\theta JA}$ is determined, the maximum ambient temperature allowed for a desired junction temperature can be calculated.

An example of calculating $R_{\theta JA}$ for an application using the Texas Instruments LM2738 WSON demonstration board is shown in Equation 48.

The four-layer PCB is constructed using FR4 with ½ oz copper traces. The copper ground plane is on the bottom layer. The ground plane is accessed by two vias. The board measures 3 cm × 3 cm. It was placed in an oven with no forced airflow. The ambient temperature was raised to 144°C, and at that temperature, the device went into thermal shutdown.

From the previous example, Equation 47 and Equation 48 shows:

$$P_{INTERNAL} = 207\ mW \quad (47)$$

$$R\theta_{JA} = \frac{165°C - 144°C}{207\ mW} = 102°C/W \quad (48)$$

If the junction temperature is kept below 125°C, then the ambient temperature cannot go above 109°C, seen in Equation 49 and Equation 50.

$$T_j - (R_{\theta JA} \times P_{LOSS}) = T_A \quad (49)$$

$$125°C - (102°C/W \times 207\ mW) = 104°C \quad (50)$$

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

AN-1229 SIMPLE SWITCHER® PCB Layout Guidelines (SNVA054)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2738XMY/NOPB	ACTIVE	HVSSOP	DGN	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	STDB	Samples
LM2738XSD/NOPB	ACTIVE	WSON	NGQ	8	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L237B	Samples
LM2738YMY/NOPB	ACTIVE	HVSSOP	DGN	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	SJBB	Samples
LM2738YSD/NOPB	ACTIVE	WSON	NGQ	8	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	L174B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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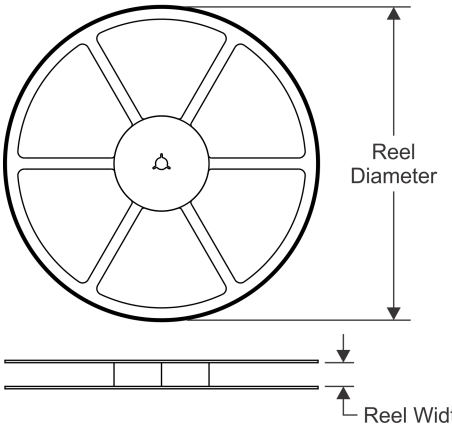
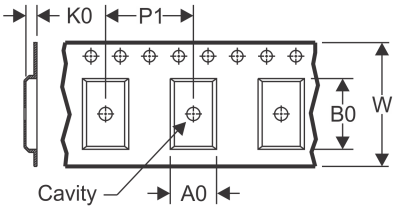
TAPE AND REEL INFORMATION

REEL DIMENSIONS

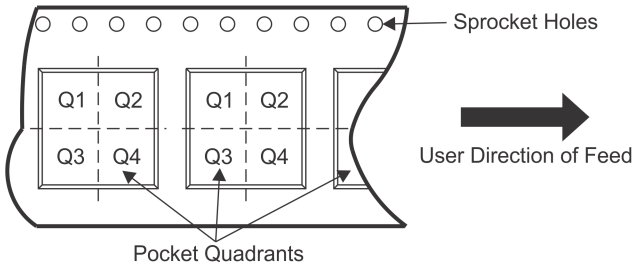


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

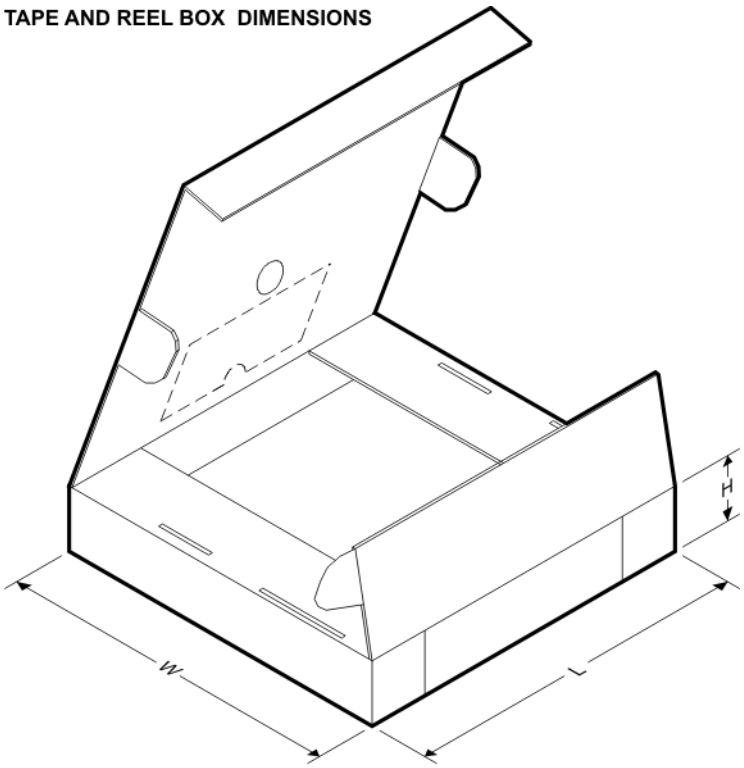
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2738XMY/NOPB	HVSSOP	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2738XSD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LM2738YMY/NOPB	HVSSOP	DGN	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2738YSD/NOPB	WSON	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

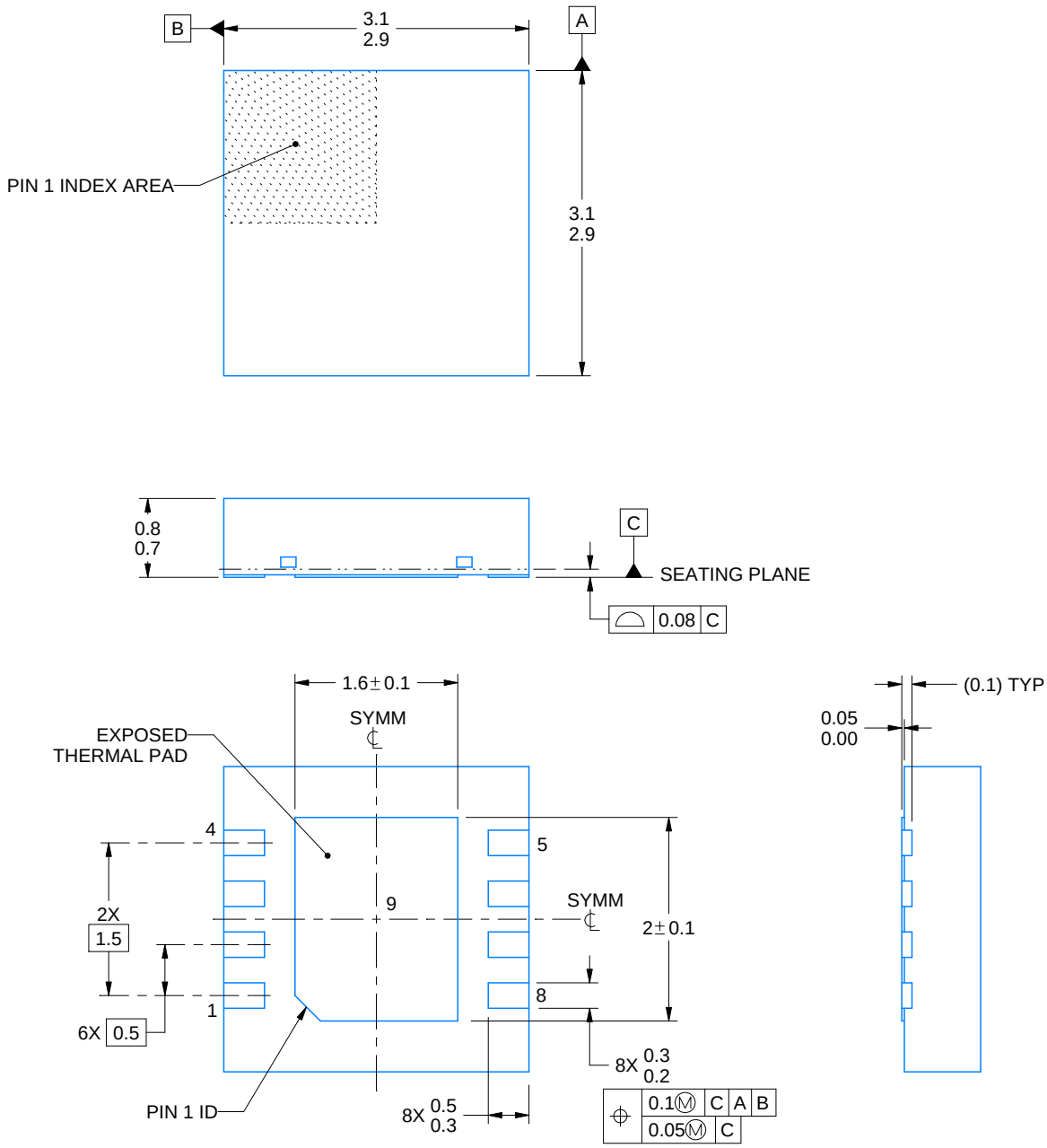
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2738XMY/NOPB	HVSSOP	DGN	8	1000	210.0	185.0	35.0
LM2738XSD/NOPB	WSON	NGQ	8	1000	208.0	191.0	35.0
LM2738YMY/NOPB	HVSSOP	DGN	8	1000	210.0	185.0	35.0
LM2738YSD/NOPB	WSON	NGQ	8	1000	208.0	191.0	35.0

PACKAGE OUTLINE

NGQ0008A

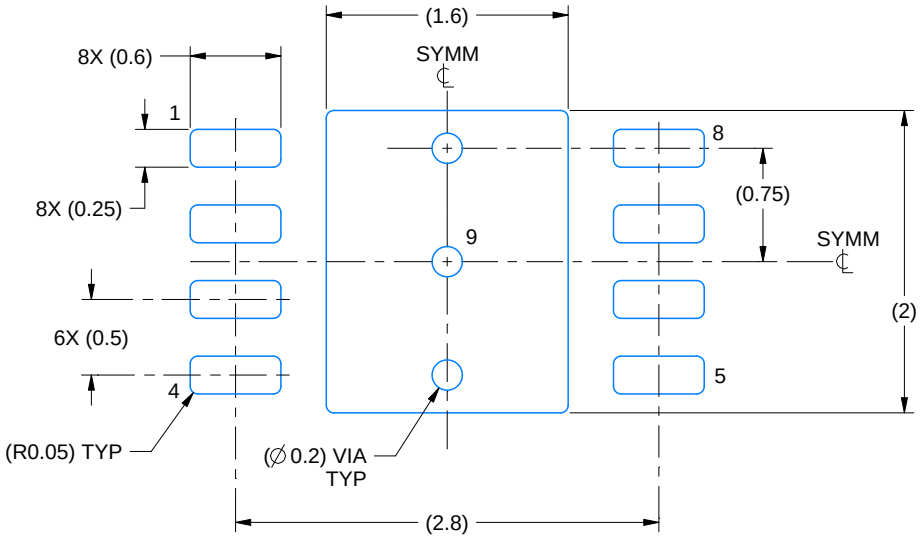
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

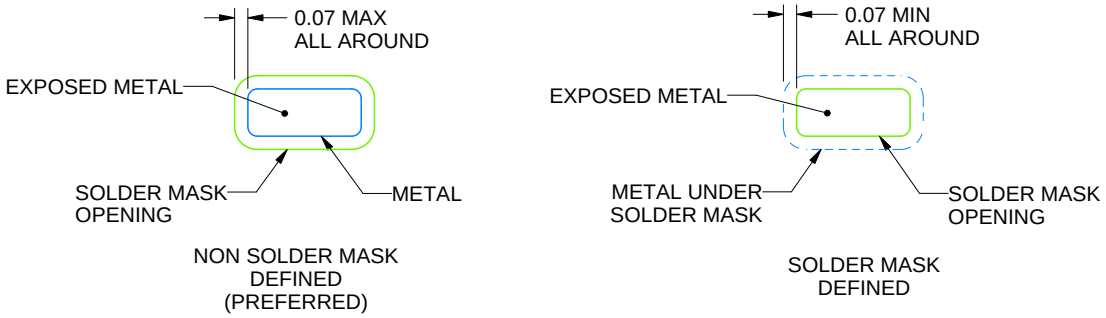


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

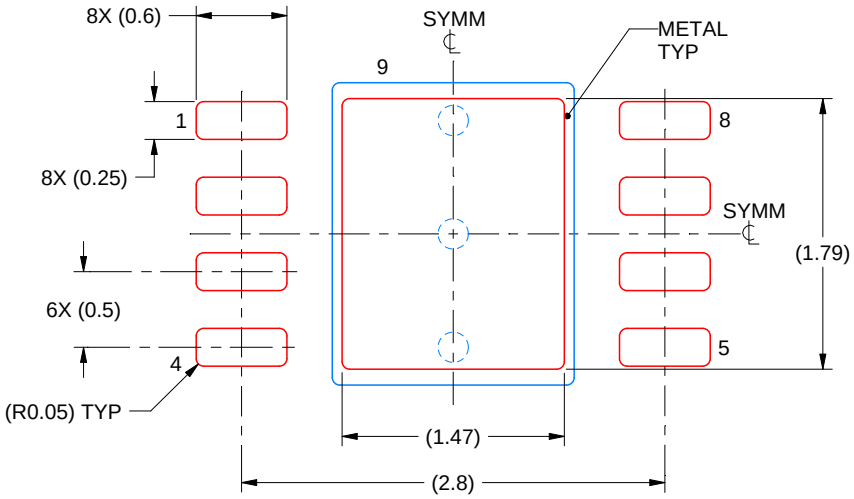


SOLDER MASK DETAILS

4214922/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

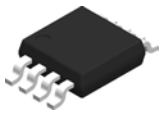
4214922/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

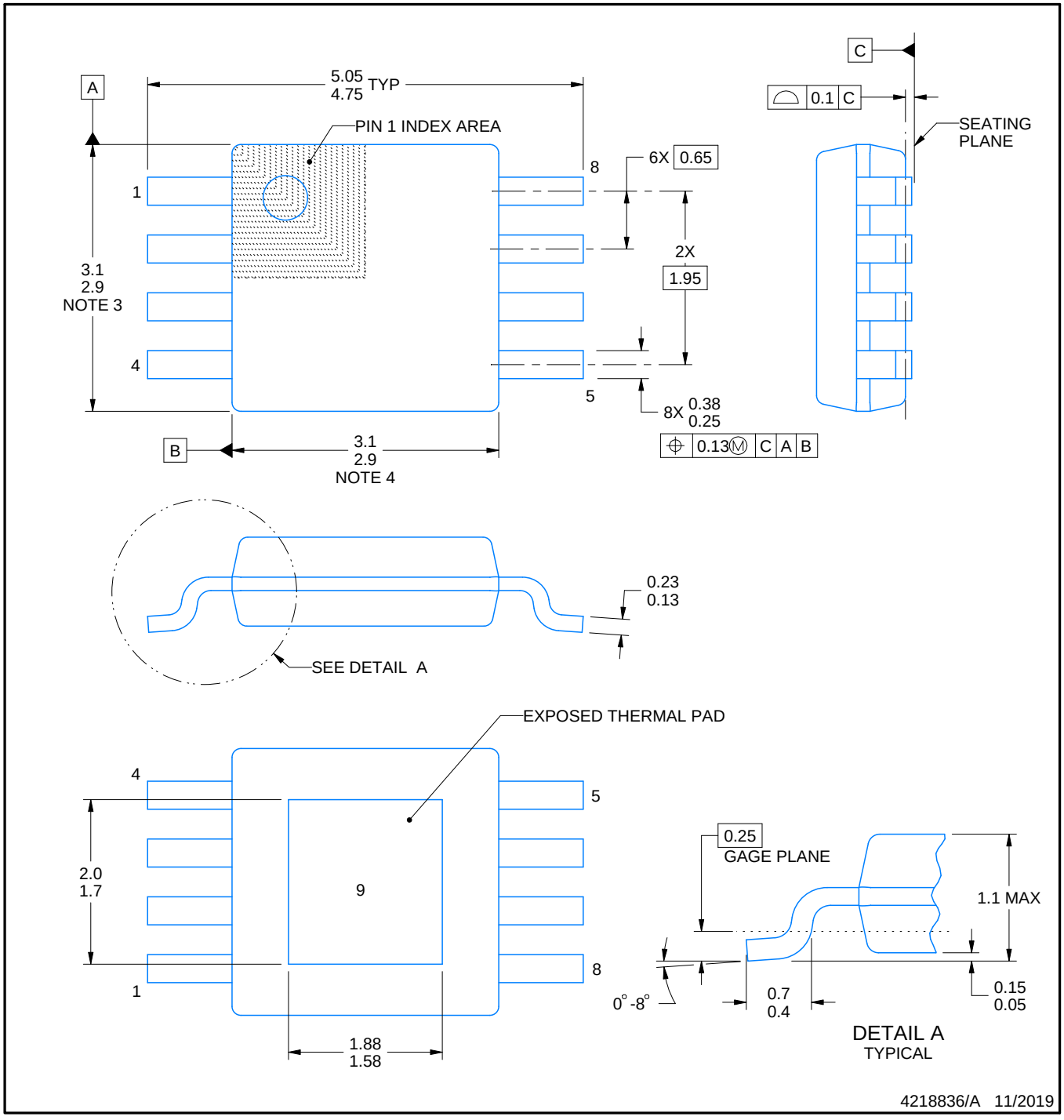
PACKAGE OUTLINE

DGN0008A



PowerPAD™ VSSOP - 1.1 mm max height

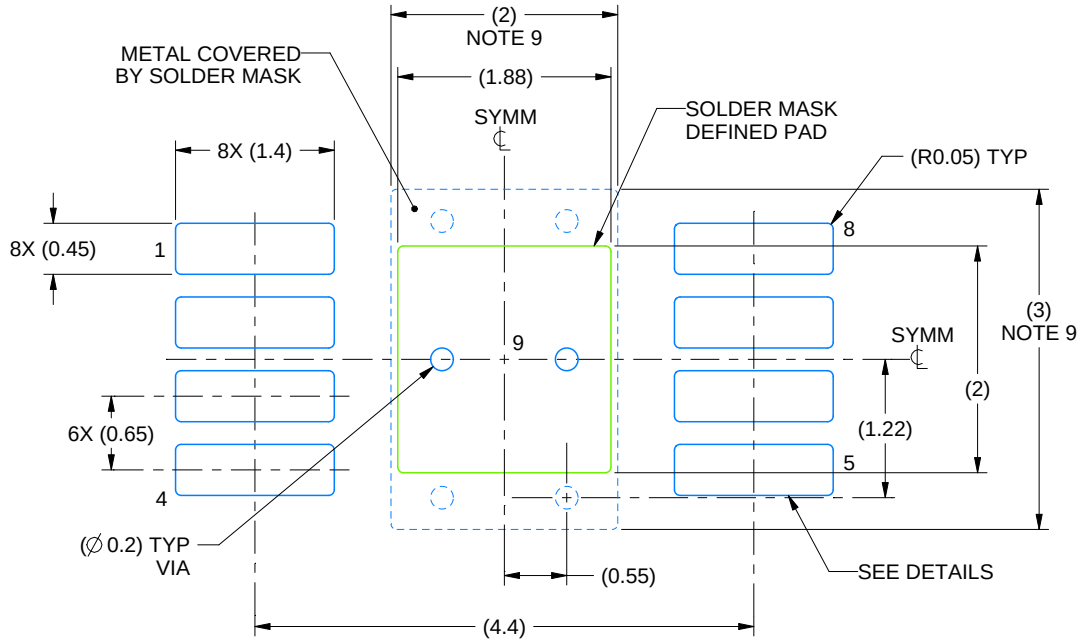
SMALL OUTLINE PACKAGE



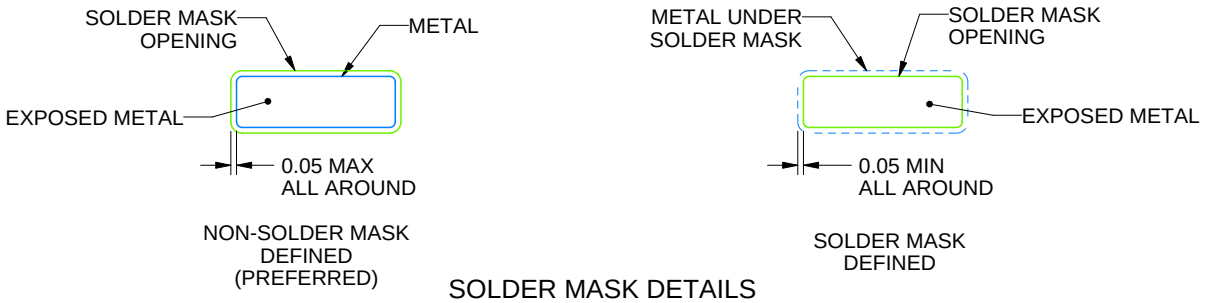
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4218836/A 11/2019

NOTES: (continued)

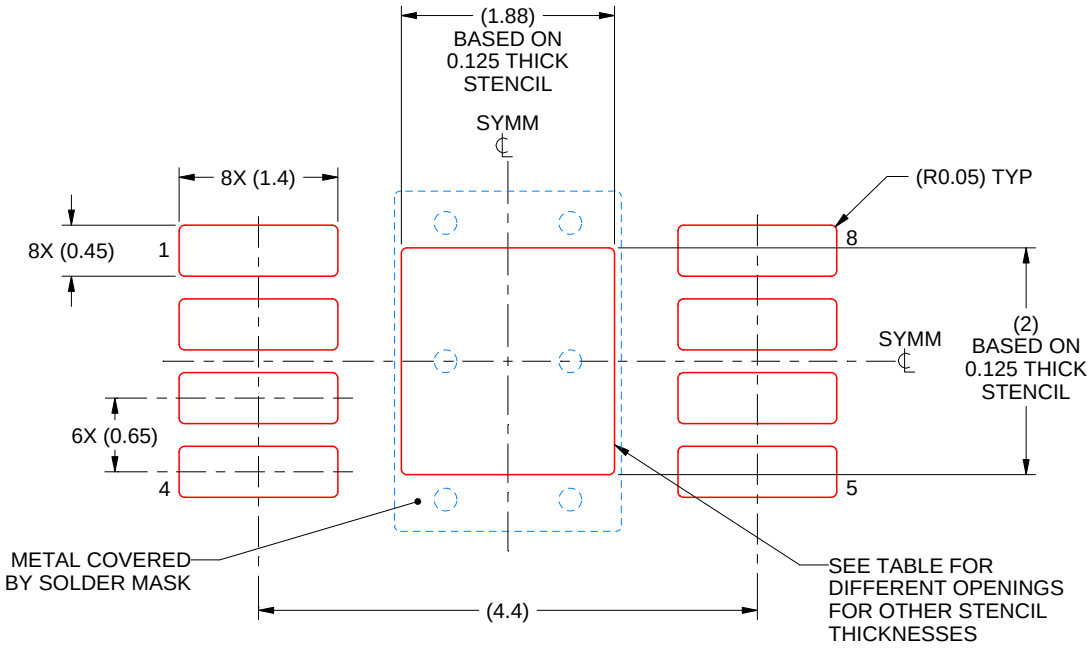
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008A

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.24
0.125	1.88 X 2.00 (SHOWN)
0.15	1.72 X 1.83
0.175	1.59 X 1.69

4218836/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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