



IRF740

N-channel 400V - 0.46Ω - 10A TO-220
PowerMESH™ II Power MOSFET

General features

Type	V _{DSS} (@T _{jmax})	R _{DS(on)}	I _D
IRF740	400V	<0.55Ω	10A

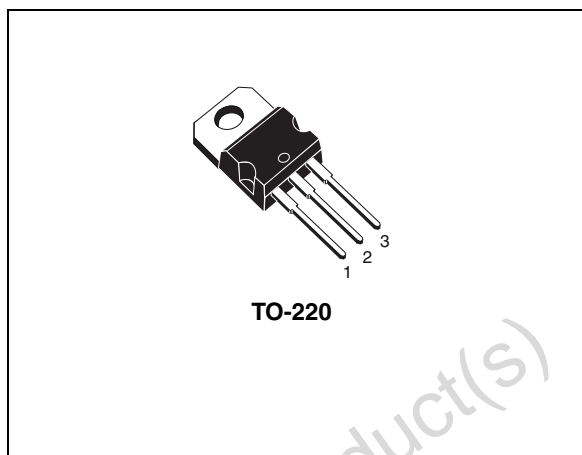
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge
- Very low intrinsic capacitances

Description

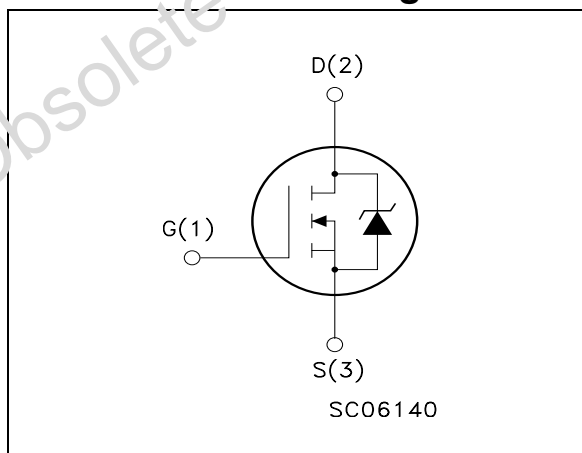
The PowerMESH™II is the evolution of the first generation of MESH OVERLAY™. The layout refinements introduced greatly improve the Ron*area figure of merit while keeping the device at the leading edge for what concerns switching speed, gate charge and ruggedness.

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
IRF740	IRF740@	TO-220	Tube

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Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	400	V
V_{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	400	V
V_{GS}	Gate- source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	10	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	6.3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	40	A
P_{tot}	Total dissipation at $T_C = 25^\circ\text{C}$	125	W
	Derating Factor	1.0	W/ $^\circ\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.0	V/ns
T_{stg}	Storage temperature	-65 to 150	$^\circ\text{C}$
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 0\text{A}$, $di/dt \leq 300\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Table 2. Thermal data

$R_{thj-case}$	Thermal resistance junction-case max	1	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$
T_j	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j \text{ Max}$)	10	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$, $I_d=I_{AR}$, $V_{dd}=50\text{V}$)	520	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}C$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250 \mu A, V_{GS} = 0$	400			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating},$ $V_{DS} = \text{Max rating} @ 125^{\circ}C$			1 50	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20V$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10V, I_D = 5.3A$		0.46	0.55	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max},$ $I_D = 6A$		7		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25V, f = 1 \text{ MHz},$ $V_{GS} = 0$		1400 220 27		pF pF pF
$t_{d(on)}$ t_r	Turn-on delay time Rise Time	$V_{DD} = 200V, I_D = 5A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ (see Figure 12)		17 10		ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 320V, I_D = 10.7A$ $V_{GS} = 10V$		35 11 12	43	nC nC nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current				10	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				40	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD}=10A, V_{GS}=0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD}=10A,$ $di/dt = 100A/\mu s,$ $V_{DD}=100V, T_J=150^\circ C$ (see Figure 12)		370		ns
Q_{rr}	Reverse recovery charge			3.2		μC
I_{RRM}	Reverse recovery current			17		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Obsolete Product(s) - Obsolete Product(s)

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

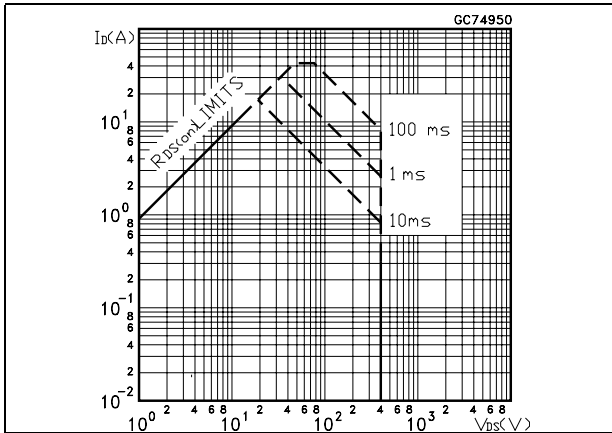


Figure 2. Thermal impedance

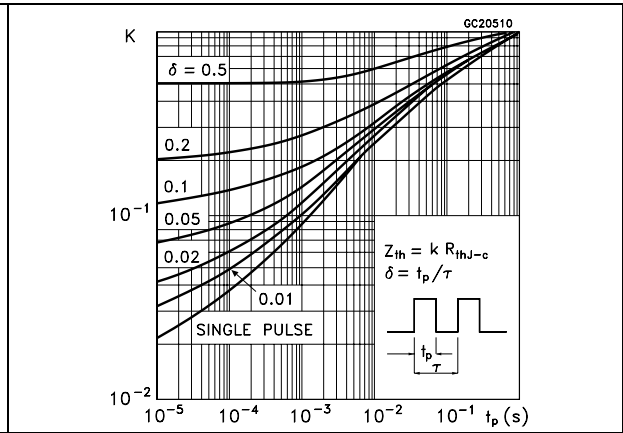


Figure 3. Output characteristics

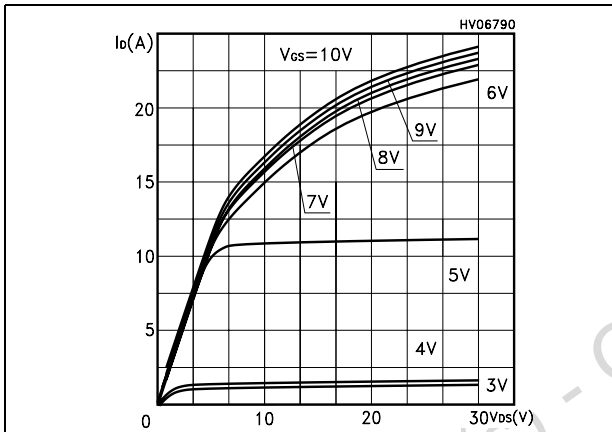


Figure 4. Transfer characteristics

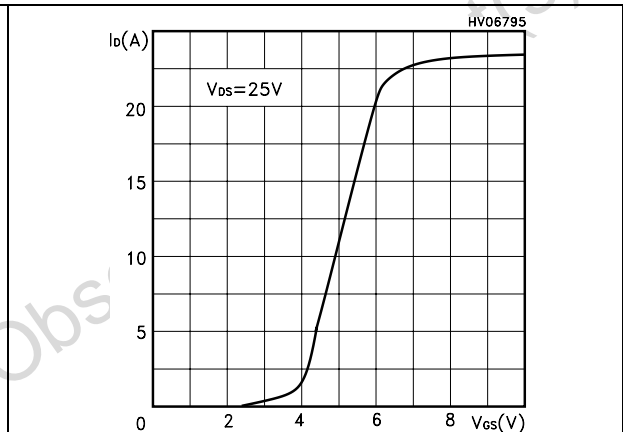


Figure 5. Transconductance

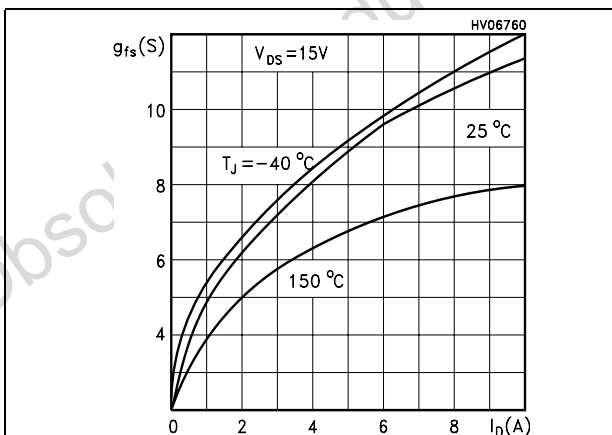


Figure 6. Static drain-source on resistance

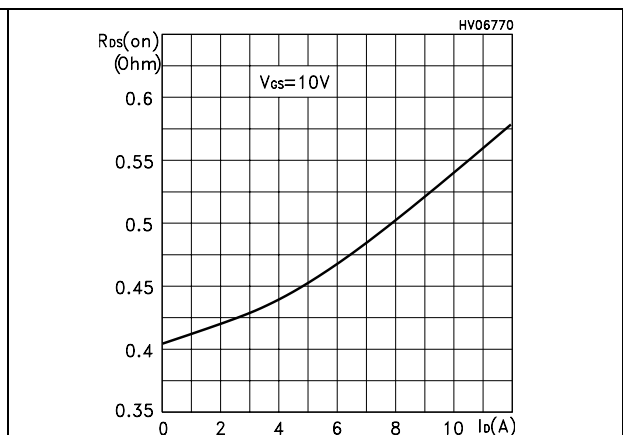


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

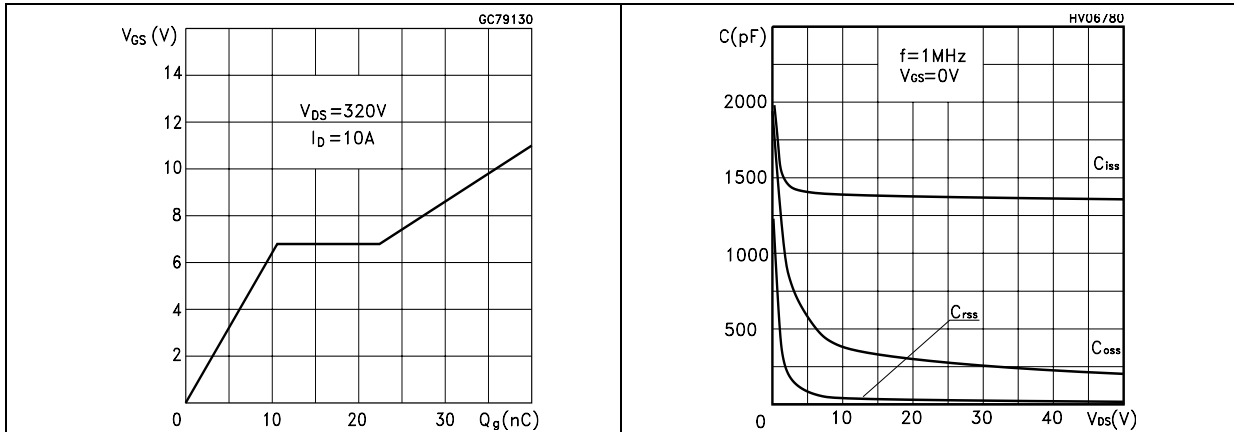


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

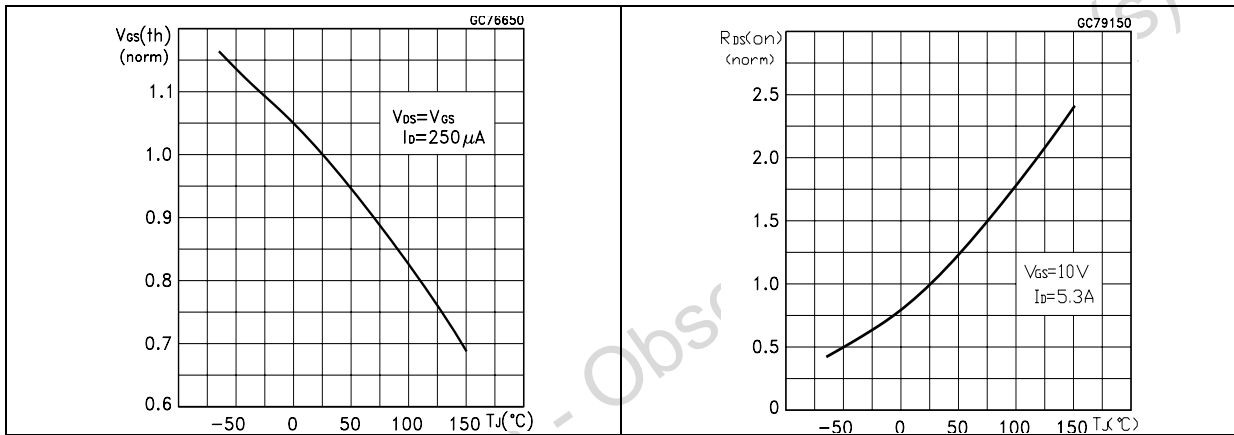
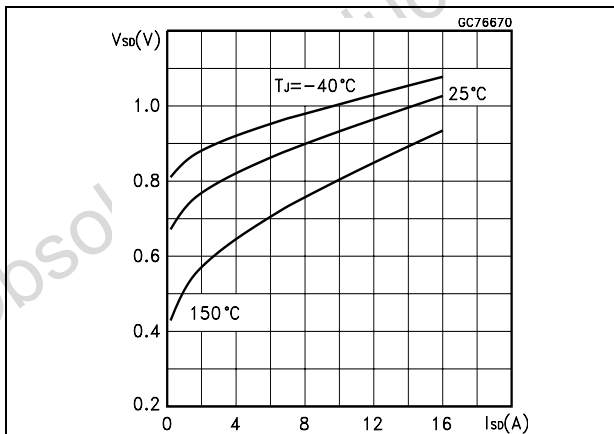


Figure 11. Source-drain diode forward characteristics



3 Test circuit

Figure 12. Switching times test circuit for resistive load

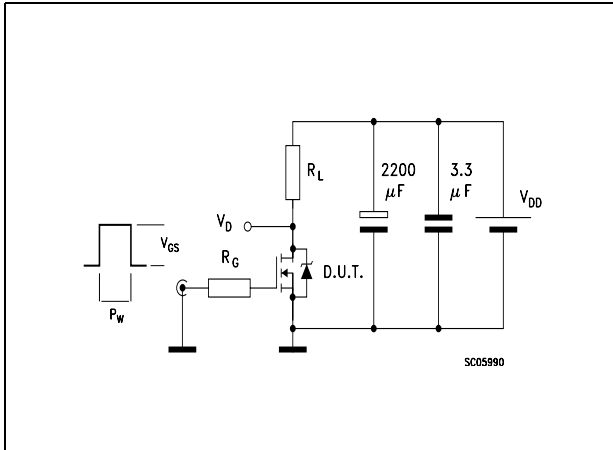


Figure 13. Gate charge test circuit

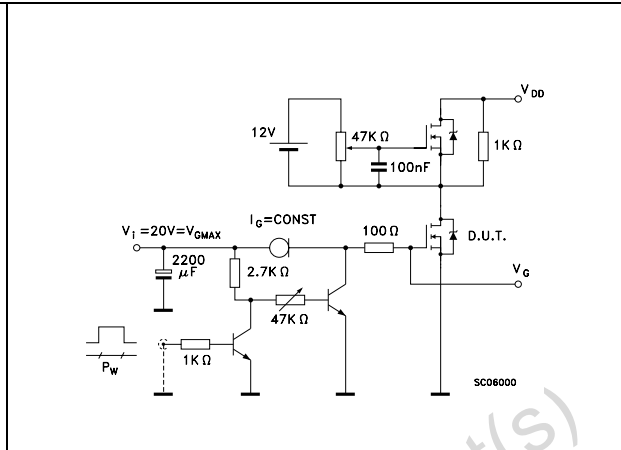


Figure 14. Test circuit for inductive load switching and diode recovery times

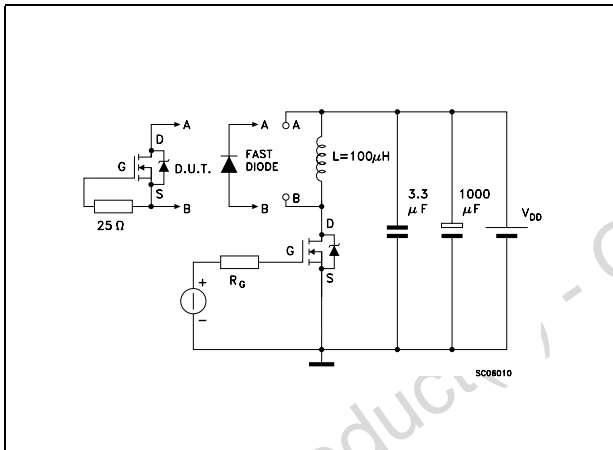


Figure 15. Unclamped Inductive load test circuit

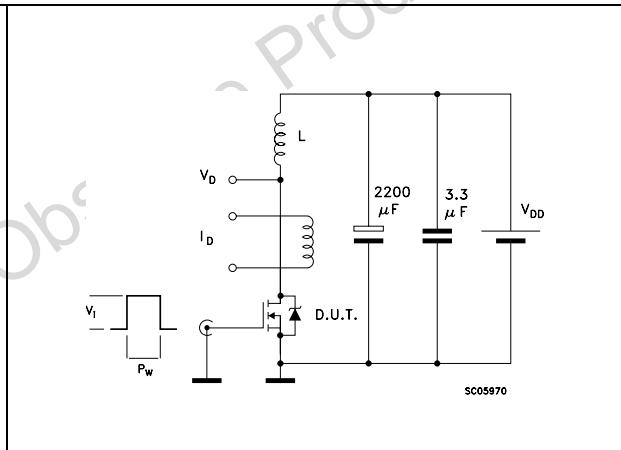


Figure 16. Unclamped inductive waveform

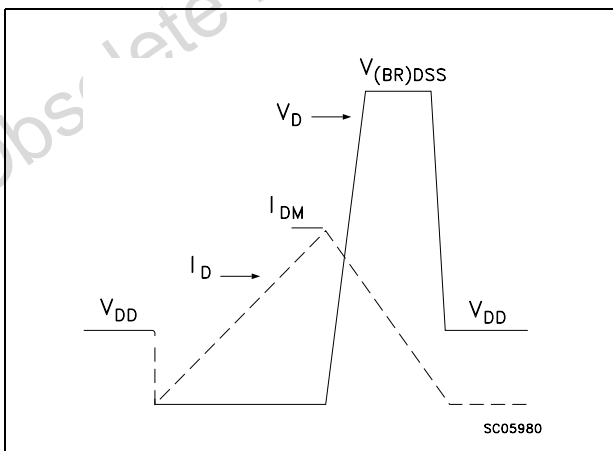
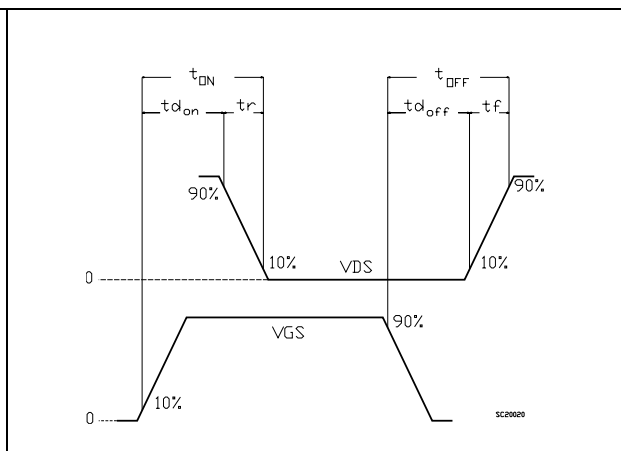


Figure 17. Switching time waveform



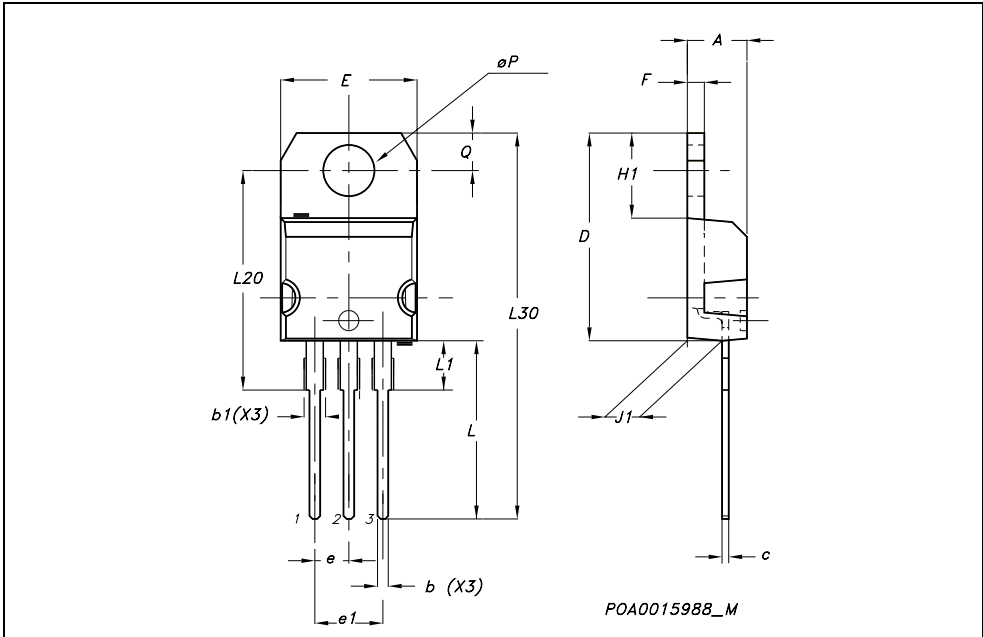
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



Obsole

5 Revision history

Table 7. Revision history

Date	Revision	Changes
09-Sep-2004	3	Complete version,new datasheet according to PCN DSG/CT/2C14. special marking: IRF740 @
03-Aug-2006	4	New template, no content change

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