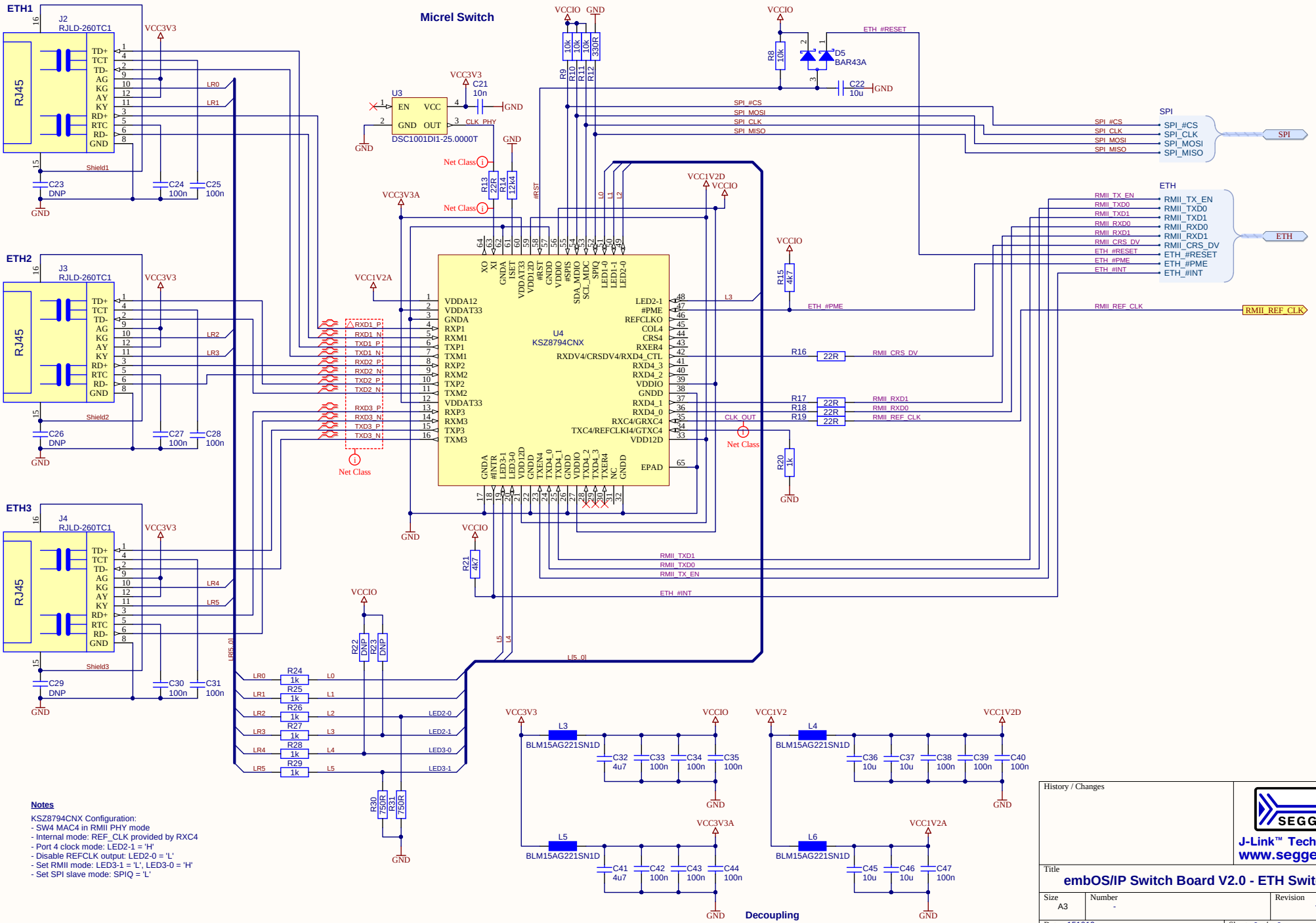
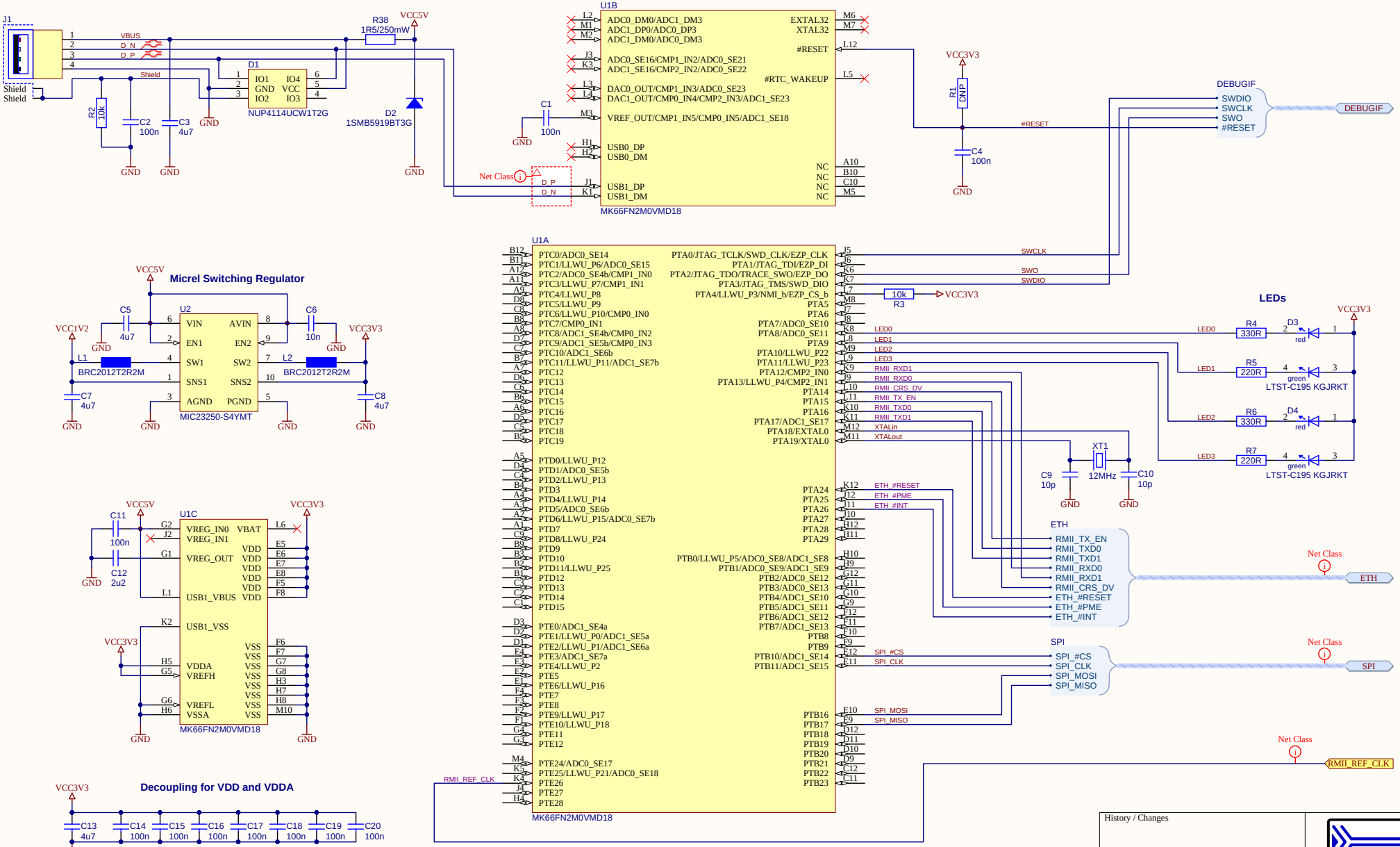

ETH1
J2
RJLD-260TC1
RJ45
ETH2
J3
RJLD-260TC1
RJ45
ETH3
J4
RJLD-260TC1
RJ45
Micrel Switch
U4
KSZ8794CNX
U3
DSC1001DI1-25.0000T
VCC3V3
VCC3V3A
VCC1V2D
VCC1V2A
VCCIO
GND
SPI_#CS
SPI_MOSI
SPI_CLK
SPI_MISO
SPI
ETH
RMII_TX_EN
RMII_TXD0
RMII_TXD1
RMII_RXD0
RMII_RXD1
RMII_CRS_DV
ETH_#RESET
ETH_#PME
ETH_#INT
RMII_REF_CLK
CLK_OUT
Net Class
Notes
KSZ8794CNX Configuration:
- SW4 MAC4 in RMII PHY mode
- Internal mode: REF_CLK provided by RXC4
- Port 4 clock mode: LED2-1 = 'H'
- Disable REFCLK output: LED2-0 = 'L'
- Set RMII mode: LED3-1 = 'L', LED3-0 = 'H'
- Set SPI slave mode: SPIQ = 'L'
Decoupling
SEGGER
J-Link™ Technology
www.segger.com
History / Changes
Title
embOS/IP Switch Board V2.0 - ETH Switch
Size
A3
Number
-
Revision
-
Date: 151019
Sheet 2 / 3
File: Sheet03_ETHSwitch.SchDoc
Drawn: VK

History / Changes

V2.0 First public version

Freescale Kinetis K66 MCU



Notes

Configuration and status reading of the switch MACs and PHYs is done via SPI - and not the MDC/MDIO management interface of the controller

Unless otherwise specified:

==========

- Ceramic capacitors are of type X5R/X7R or C0G/NP0 with a voltage rating of at least 6.3V (100n at least 16V)

- Resistors are 1% tolerance types

History / Changes

SEGGER

J-Link™ Technology

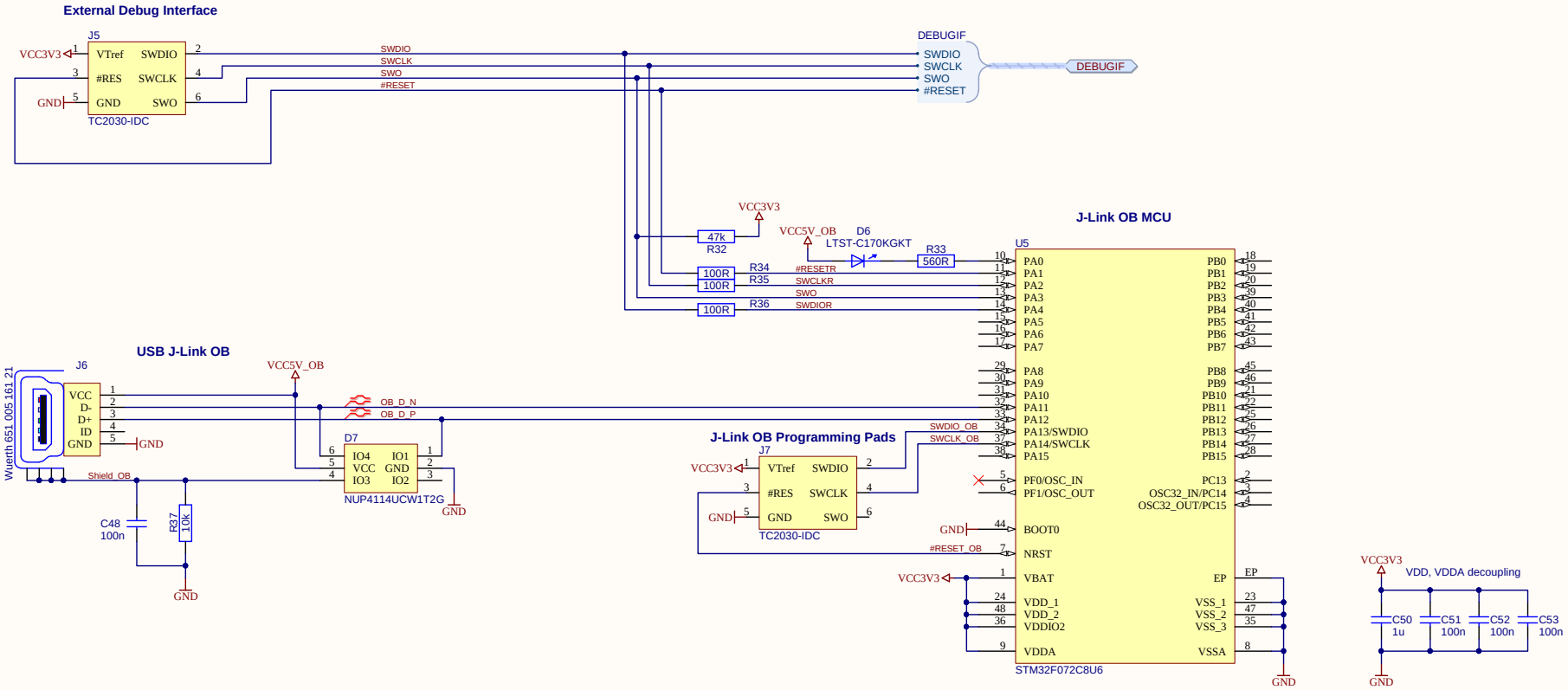
www.segger.com

Title: **embOS/IP Switch Board V2.0 - MCU, USB, Power**

Size	Number	Revision
A3	-	-

Date: 151019 | Sheet 1 / 3

File: Sheet02_MCU_USB_PWR.SchDoc | Drawn: VK



History / Changes

SEGGER
J-Link™ Technology
www.segger.com

Title
embOS/IP Switch Board V2.0 - J-Link OB

Size	Number	Revision
A3	-	-

Date: 151019	Sheet 3 / 3
File: Sheet04_OB.SchDoc	Drawn: VK