PE29100

Document Category: Product Specification

UltraCMOS® High-speed FET Driver, 33 MHz

Features

- High- and Low-side FET drivers
- Dead-time control
- Fast propagation delay, 8 ns
- Tri-state enable mode
- Sub-nanosecond rise and fall time
- 2A/4A peak source/sink current
- Package – Flip chip

Applications

- DC–DC conversions
- AC–DC conversions
- Wireless power
- Class D amplifiers

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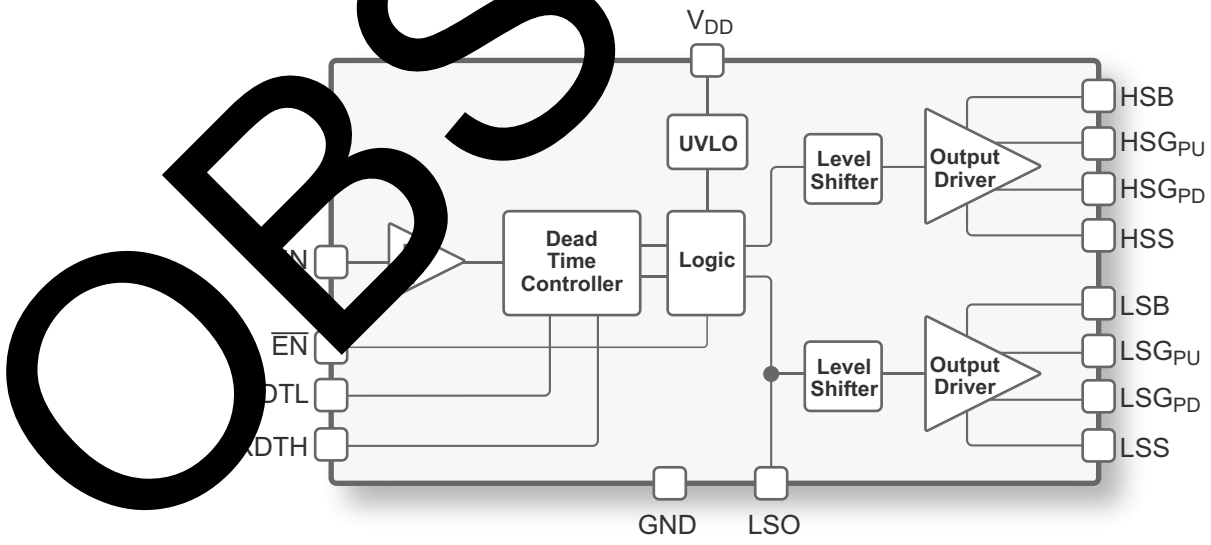
Product Description

The PE29100 integrated high-speed driver is designed to control the gate of external power devices, such as enhancement mode gallium nitride (eGaN®) FETs. The outputs of the PE29100 are capable of providing switching transition speeds in the sub-nanosecond range for hard switching applications up to 33 MHz. High switching speeds result in smaller peripheral components and enable new applications like the Rezence A4WP wireless power transfer. The PE29100 is available in flip chip package.

The PE29100 is manufactured on Peregrine's UltraCMOS process, a patented advanced form of silicon-on-insulator (SOI) technology, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1 • *PE29100 Functional Diagram*



Absolute Maximum Ratings

Exceeding absolute maximum ratings listed in **Table 1** may cause permanent damage. Operation should be restricted to the limits in **Table 2**. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

ESD Precautions

When handling this UltraCMOS device, observe the same precautions as with any other ESD sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in **Table 1**.

Latch-up Immunity

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Table 1 • *Absolute Maximum Ratings for PE29100*

Parameter/Condition	Min	Max	Unit
Low-side bias (LSB) to low-side source (LSS)	–0.3	6	V
High-side bias (HSB) to high-side source (HSS)	–0.3	6	V
Input signal	–0.3	6	V
HSS to LSS	–1	100	V
ESD voltage HBM(*), all pins		25	V

Note: * Human body model (MIL-STD 883 Method 30

Recommended Operating Conditions

Table 2 lists the recommended operating conditions for the PE29100. Devices should not be operated outside the recommended operating conditions listed below.

Table 2 • *Recommended Operating Conditions for PE29100*

Parameter	Min	Typ	Max	Unit
Supply for driver front-end, V_{DD}	4.0	5.0		V
Supply for high-side driver, HSB	3.7	5	5.5	
Supply for low-side driver, LSB	3.7	5.0	5.5	V
Logic HIGH for control input	1.6		5.5	V
Logic LOW for control input	0		5	V
HSS range			80	V
Minimum input pulse width	10			ns
Operating temperature	–40		+105	°C
Junction temperature	–40		+125	°C

Electrical Specifications

Table 3 provides the key electrical specifications @ +25 °C, V_{DD} = , load = 2.2Ω resistor in series with 100 pF capacitor, HSB and LSB bootstrap diode included, unless otherwise specified.

Table 3 • *DC Characteristics*

Parameter	Conditions	Min	Typ	Max	Unit
DC Characteristics					
V_{DD} quiescent current	V_{DD} = 5V		3	4.0	mA
HSB quiescent current	V_{DD} = 5V		2.5	3.4	mA
LSB quiescent current	V_{DD} = 5V		2.5	3.4	mA
Under Voltage Lockout					
Under voltage release (rising)		3.1	3.6	4.3	V
Under voltage hysteresis			200		mV
Gate Drivers					
HSG_{PU}/LSG_{PU} pull-up resistance			1.2		Ω
HSG_{PD}/LSG_{PD} pull-down resistance			0.5		Ω
HSG_{PU}/LSG_{PU} leakage current	HSB–HSG_{PU} = 5.5V/LSB–LSG_{PU} = 5.5V		10		µA
HSG_{PD}/LSG_{PD} leakage current	HSG_{PD}–HSS = 5.5V/LSG_{PD}–HSS = 5.5V		10		µA
Dead-time Control					

Table 3 • *DC Characteristics (Cont.)*

Parameter	Condition	Min	Typ	Max	Unit
Dead-time control voltages	30k to 80 kΩ resistor to GND		1.2		V
Dead-time from HSG going low to LSG going high	RDHL = 30 kΩ		0.8		ns
	RDHL = 80 kΩ		3.4		ns
Dead-time from LSG going low to HSG going high	RDLH = 30 kΩ		0.8		ns
	RDLH = 80 kΩ				ns
Switching Characteristics					
LSG turn-off propagation delay	At min dead time		8.4		ns
HSG rise time	10%–90%		1.0		ns
	10%–90% with 1000 pF load		2.5		
LSG rise time	10%–90%		1.0	1.2	ns
	10%–90% with 1000 pF load				
HSG fall time	10%–90%		0.9	1.0	ns
	10%–90% with 1000 pF load		2.5		
LSG fall time	10%–90%		0.9	1.0	ns
	10%–90% with 1000 pF load		1.8		
Max switching frequency @ 50% duty cycle	RDHL = RDLH = 80 kΩ		33		MHz

Control Logic

Table 4 provides the control logic truth table for the PE29100.

Table 4 • *Truth Table for PE29100*

$\overline{EN}$	IN	LSG_{PU}–HSS	HSG_{PD}–HSS	LSG_{PU}–LSS	LSG_{PD}–LSS
L	L	Hi–Z	L	H	Hi–Z
L	H	H	Hi–Z	Hi–Z	L
H	L	Hi–Z	L	Hi–Z	L
H	H	Hi–Z	L	Hi–Z	L

Typical Performance Data

Figure 2–Figure 4 show the typical performance data @ +25 °C, V_{DD} = 5V, load = 2.2Ω resistor in series with 100 pF capacitor, HSB and LSB bootstrap diode included, unless otherwise specified.

Figure 2 • *Quiescent Current vs Temperature*

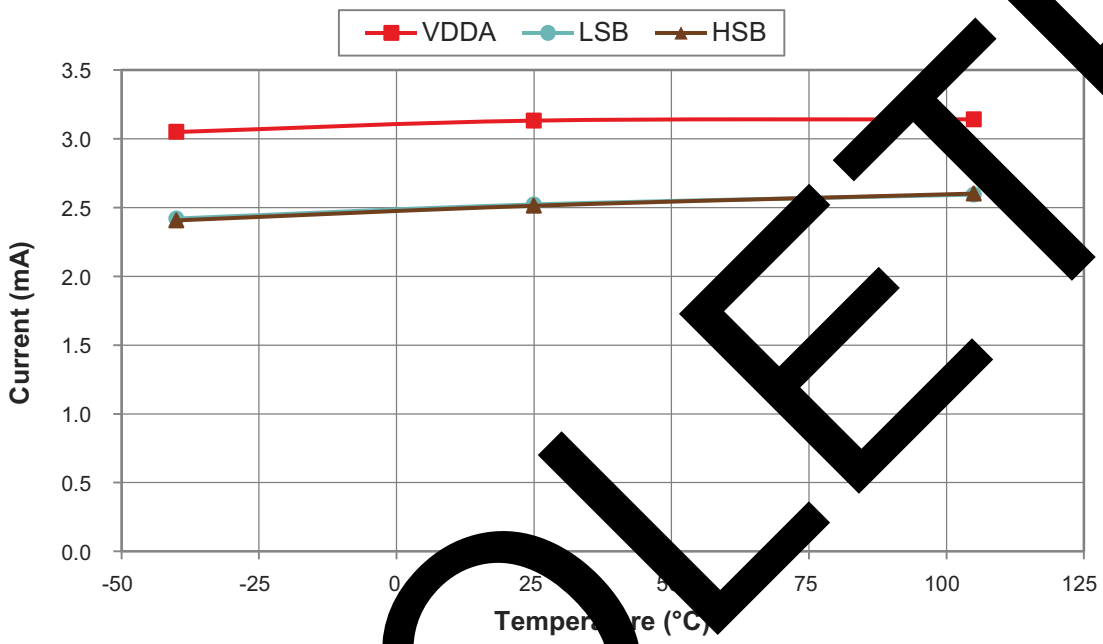


Figure 3 • *UVLO Threshold vs Temperature*

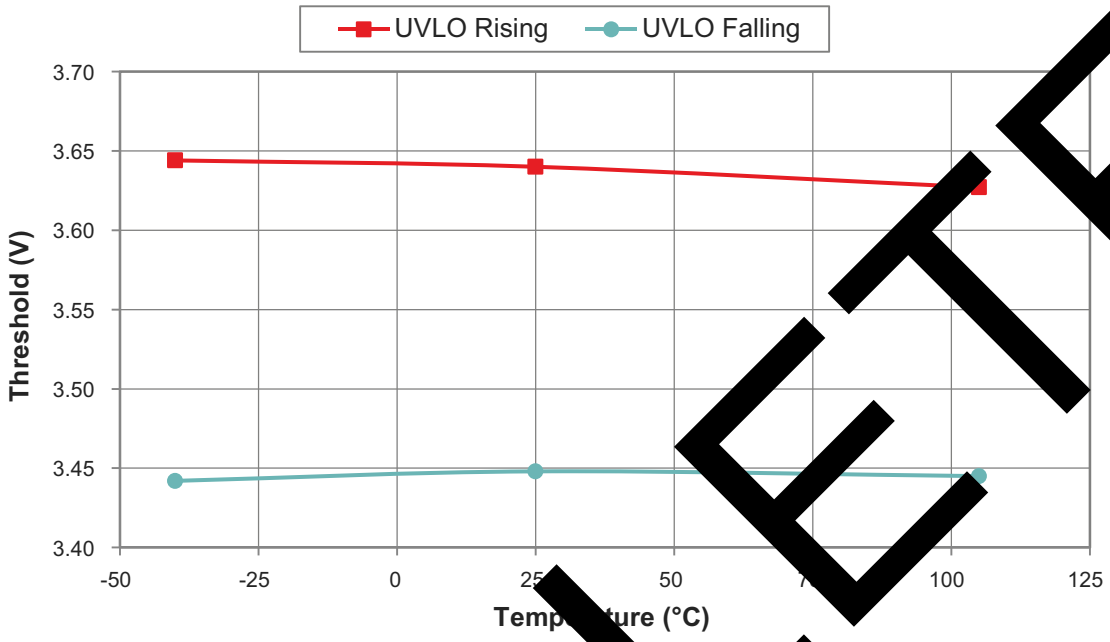
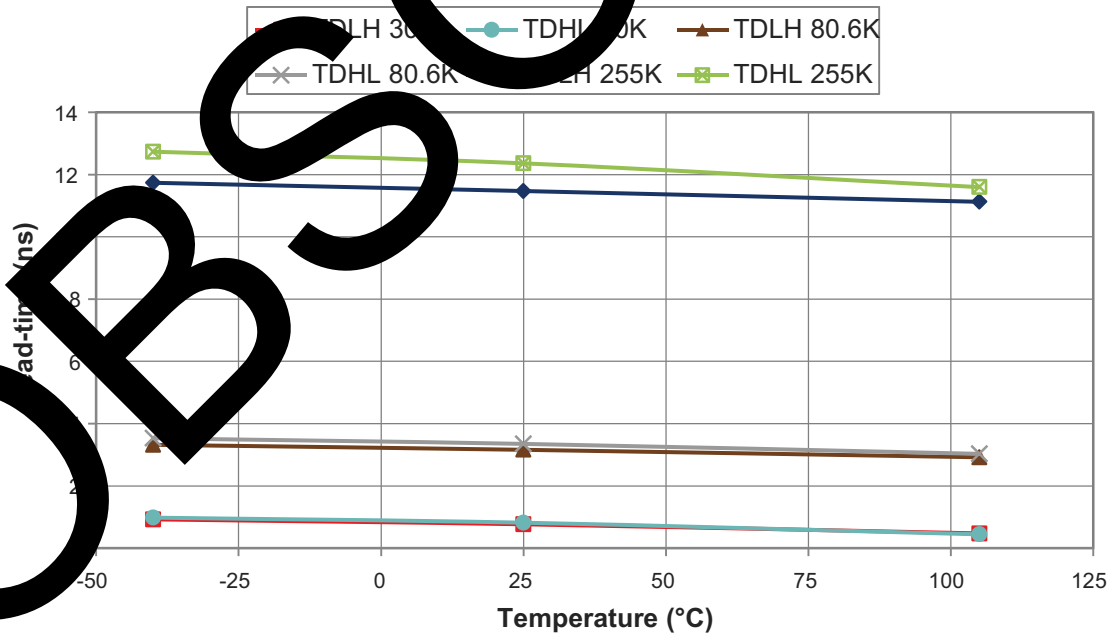


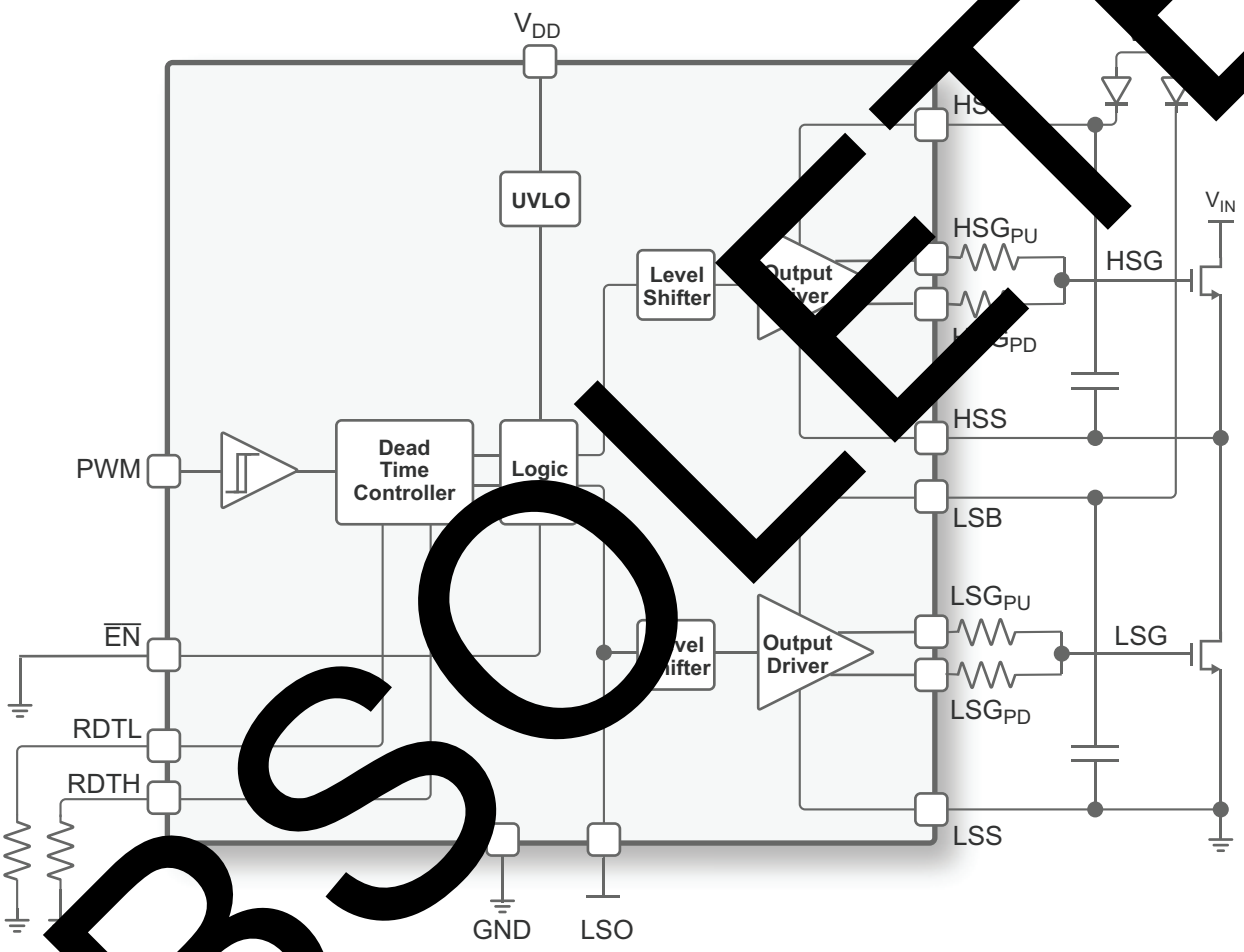
Figure 4 • *Dead-time vs Temperature*



Test Diagram

Figure 5 shows the test circuit used for obtaining measurements. The two bootstrap diodes shown in the schematic are used for symmetry purposes in characterization. In practice, only the HSB diode is required. Removing the LSB diode will result in higher low-side supply voltage since the diode drop is eliminated. As a result, the dead-time resistor can be adjusted to compensate for any changes in propagation delay.

Figure 5 • *Test Circuit for PE29100*



Theory of Operation

General

The PE29100 is intended to drive both the high-side (HS) and the low-side (LS) gates of external power FETs, such as eGaN FETs, for power management applications. The PE29100 favors applications requiring higher switching speeds due to the reduced parasitic properties of the high resistivity insulating substrate inherent with Peregrine's UltraCMOS process.

The driver uses a single-ended pulse width modulation (PWM) input that feeds a dead-time control, capable of generating a small and accurate dead-time. The dead-time circuit prevents shoot-through current in the output stage. The propagation delay of the dead-time controller must be small to meet the fast switching requirements when driving eGaN FETs. The differential outputs of the dead-time controller are then level-shifted from a low-voltage domain to a high-voltage domain required by the output drivers.

Each of the output drivers includes two separate pull-up and pull-down outputs allowing independent control of the turn-on and turn-off gate loop resistance. The low impedance output of the drivers improves external power FETs switching speed and efficiency, and minimizes the effects of the voltage rise time (dv/dt) transients.

Under-voltage Lockout

An internal under-voltage lockout (UVLO) feature prevents the PE29100 from powering up before input voltage rises above the UVLO threshold of 3.6V (typ), and 200mV (typ) of hysteresis is built in to prevent false triggering of the UVLO circuit. The UVLO must be cleared and the $\overline{EN}$ pin must be released before the part will be enabled.

Dead-time Adjustment

The PE29100 features a dead-time adjustment that allows the user to control the timing of the LS and HS gates to eliminate any large shoot-through current which could dramatically reduce the efficiency of the circuit and potentially damage the eGaN FETs. Two external resistors control the timing of outputs in the dead-time controller block. The timing waveforms are illustrated in **Figure 6**.

The dead-time resistors only affect the LS output; the HS output will always equal the duty-cycle of the input. The HS FET gate node will track the duty cycle of the PWM input with a shift in the response, as both rising and falling edges are shifted in the same direction. The LS FET gate node duty cycle can be controlled with the dead-time resistors. Each resistor will move the rising and falling edges in opposite directions. RDLH will change the dead-time from low-side gate (LSG) falling to high-side gate (HSG) rising and RDHL will change the dead-time from HSG falling to LSG rising. **Figure 7** shows the resulting dead-time versus the external resistor values with both HS and LS bias diode/capacitors installed as indicated in **Figure 2**. The LS bias diode and capacitor is included for symmetry only and is not required for the part to function. Removing the LS bias diode will increase the LSG voltage by approximately 0.3V, resulting in a wider separation of the t_{DHL} and t_{DLH} curves in **Figure 7**.

Figure 6 and **Figure 7** provide the dead-time description for the PE29100.

Figure 6 • *Dead-time Description*

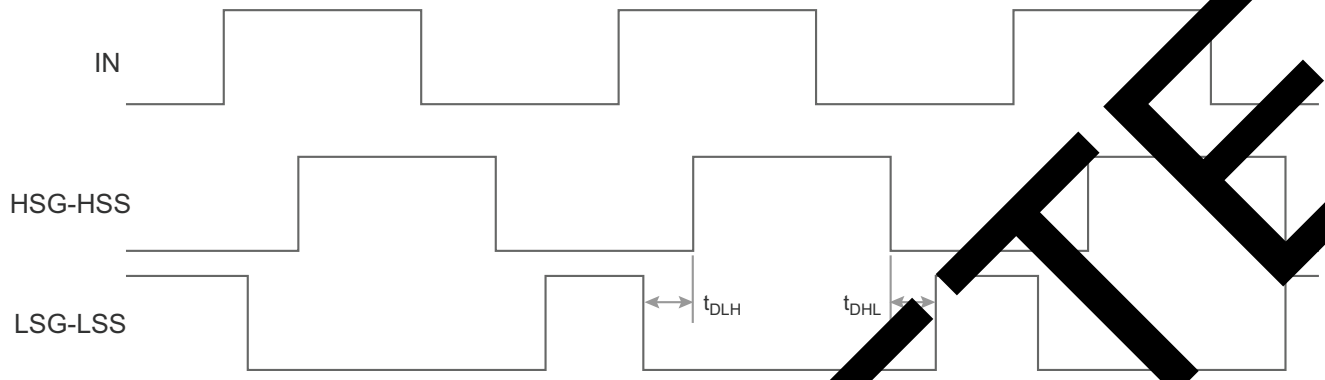
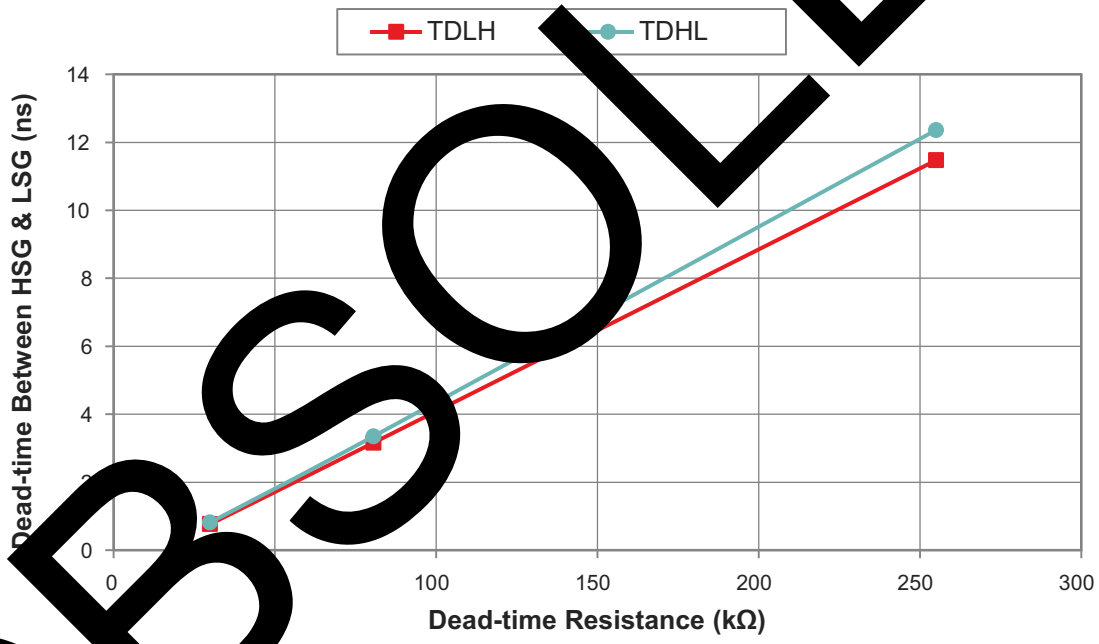


Figure 7 • *Dead-time vs Dead-time Resistor*



Application Circuit

Figure 8 shows a typical application diagram of the PE29100 and its external components in a half-bridge configuration(*). The PE29100 is designed to provide a LS gate driver, referenced to ground, and a floating HS gate driver referenced to the switch node (HSS). A common technique to generate the floating HS gate drive uses a bootstrap diode in conjunction with a decoupling capacitor. However, if the LS device conducts currents through its body diode during the dead-time period, an overvoltage condition across the bootstrap capacitor can result.

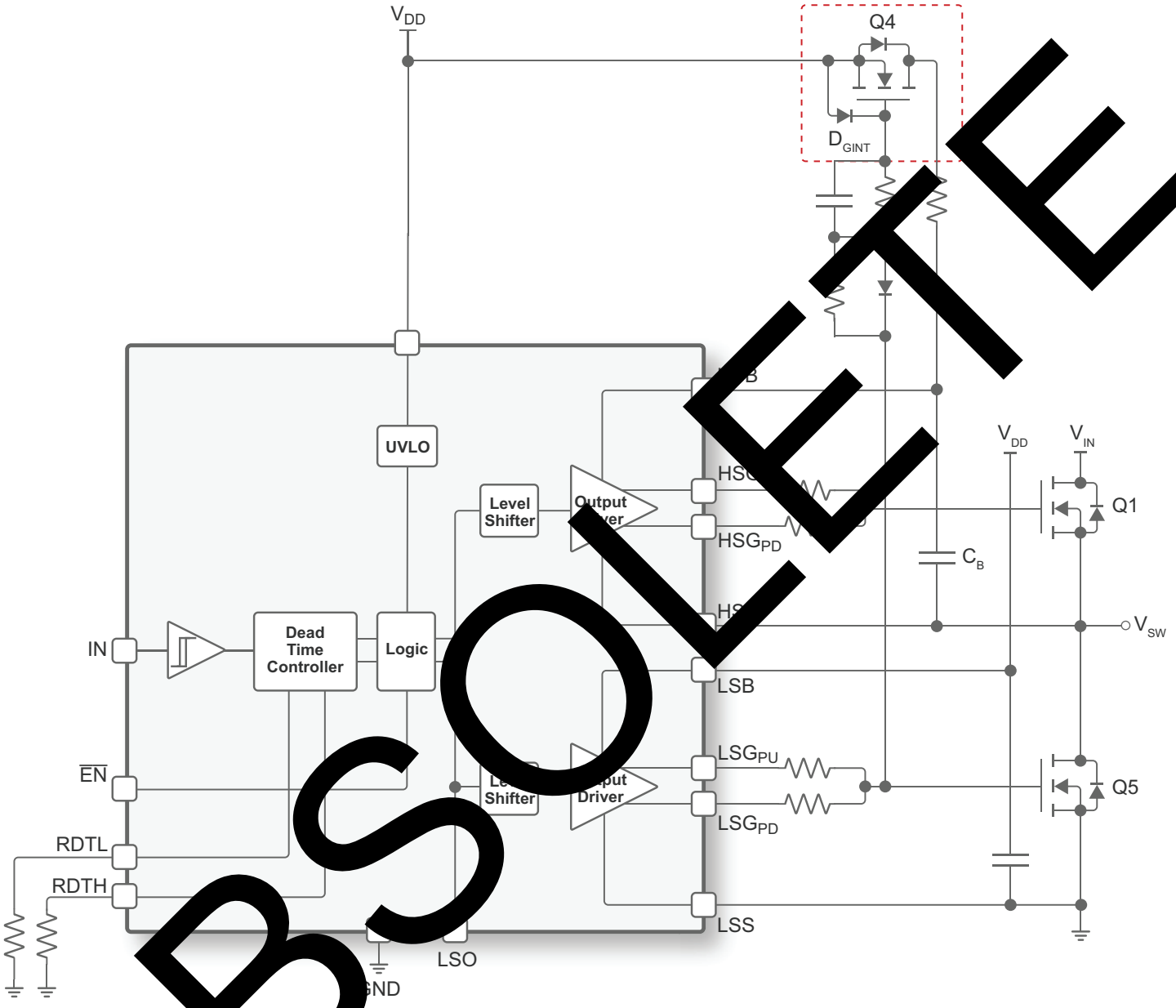
A more elegant approach replaces the HS bootstrap diode with an eGaN FET (Q4). The EPC2038 is used as a synchronous bootstrap FET to prevent overvoltage of the HS device. The EPC2038 includes an internal diode and prevents the bootstrap capacitor from overcharging during the dead-time period. This is accomplished by synchronously switching Q4 using the LSG signal so that Q4 turns on and charges the bootstrap capacitor when LSG is high, but turns off as soon as LSG turns low so that no inadvertent bootstrap overcharging occurs during the dead-time periods.

The external gate resistors are required to de-Q the inductance in the gate loop and dampen any ringing on the FET gates and the SW node.

Dead-time resistors RDHL and RDLH can be adjusted to compensate for any changes in propagation delay.

Note: * For applications greater than 30V in a half-bridge configuration, the PE29100 can be sensitive to high dv/dt conditions on HSS.

Figure 8 • *Applications Diagram for PE29100*



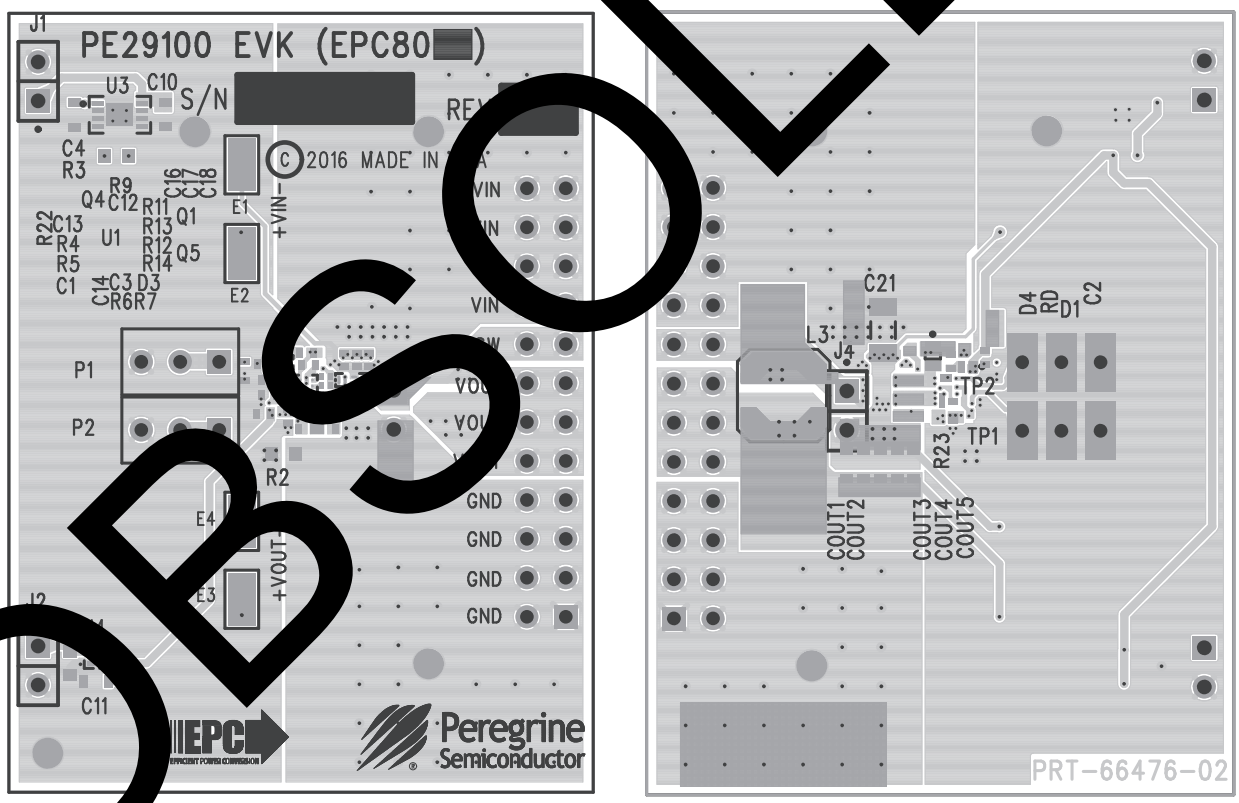
Evaluation Board

The PE29100 evaluation board (EVB) was designed to ease customer evaluation of the PE29100 gate driver. The EVB is assembled with a PE29100 driver and two EPC8009 eGaN FETs in a half-bridge configuration. VDD is applied at J1 to bias the driver. VIN is applied to the multipin connector, J3, to supply power to the GaN FETs. A PWM signal with an adjustable duty cycle is applied to J2 as the input. VIN can be monitored at test points E1 and E2, while the DC output can be monitored at test points E3 and E4. The switched output node can be observed on an oscilloscope at J3.

Because the PE29100 is capable of generating fast switching speeds, the printed circuit board (PCB) layout is a critical component of the design. The layout should occupy a small area with the power FETs and external bypass capacitors placed as close as possible to the driver to reduce any resonance associated with the gate loops, common source and power loop inductances. Since the maximum allowable gate-to-source voltage for eGaN FETs is 6V, resonance in the gate loops can generate ringing that can degrade the performance and potentially damage the power devices due to high voltage spikes. Additionally, it is important to keep ground paths short.

The PCB is fabricated on FR4 material, with a total thickness of 0.062 inches. A minimum copper thickness of 1 ounce or more is recommended on the PCB outer layers to limit resistive losses and improve thermal spreading.

Figure 9 • *Evaluation Kit Layout for PE29100*



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Pin Configuration

This section provides pin information for the PE29100. **Figure 10** shows the pin map of this device for the available package. **Table 5** provides a description for each pin.

Figure 10 • *Pin Configuration (Bumps Up)*

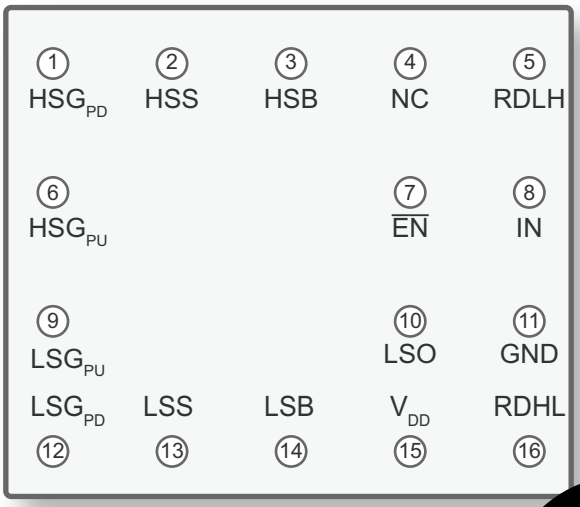


Table 5 • *Pin Descriptions for PE29100*

Pin No.	Pin Name	Description
1	HSG_{PD}	High-side gate dri pull-down
2	HSS	High-side so
3	HSB	High-si ias
4	NC	No nect (tie to boa round)
5	RDLH	ead- control resistor LSG falling to G rising delay (external resistor to G)
6	SG_{PU}	High-side gate d pull-up
7	$\overline{EN}$	nable active low, tri-state outputs when high
8		Cont put
9	LSG	-side gate drive pull-up
10	LS	Look ahead for LSG_{PU}. LSO pre-cedes LSG_{PU} and LSG_{PD} by 4 ns.
11	GND	Ground
12	LSG_{PD}	Low-side gate drive pull-down
13	LSS	Low-side source
14	LSB	Low-side bias
15	V_{DD}	+5V supply voltage
16	RDHL	Dead-time control resistor sets HSG falling to LSG rising delay (external resistor to ground)

Die Mechanical Specifications

This section provides the die mechanical specifications for the PE29100.

Table 6 • *Die Mechanical Specifications for PE29100*

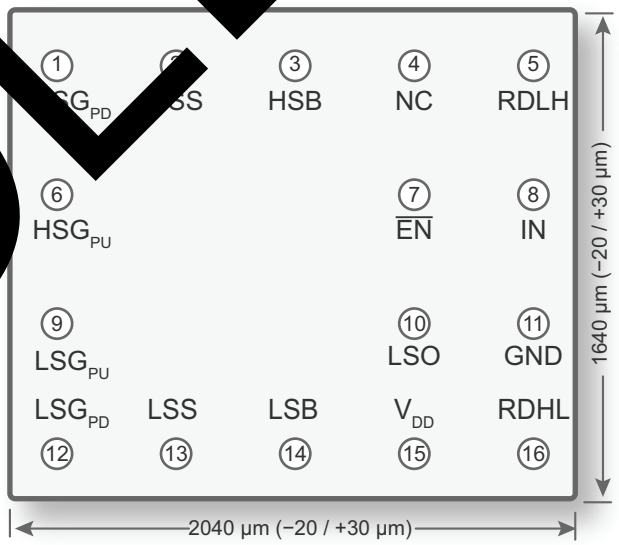
Parameter	Min	Typ	Max	Unit	Test Condition
Die size, singulated (x,y)		2040 × 1640		µm	Including sawstreet, max tolerance –20/+30
Wafer thickness	180	200	200	µm	
Wafer size				µm	
Bump pitch		400		µm	
Bump height		85		µm	
Bump diameter		110		µm	max tolerance = ±17

Table 7 • *Pin Coordinates for PE29100*(*)

Pin #	Pin Name	Pin Center (µm)	
		X	Y
1	HSG_{PD}	–800	600
2	HSS	–400	600
3	HSB	0	600
4	NC		
5	RDLH	800	600
6	HSG_{PU}	–800	0
7	$\overline{EN}$	400	0
8	IN	800	200
9	LSG_{PU}	0	–200
10		0	–200
11	GND	800	–200
12	LSG_{PD}	–800	–600
13	LSS	–400	–600
14	LSB	0	–600
15	V_{DD}	400	–600
16	RDHL	800	–600

Note: * All pin locations originate from the die center and refer to the center of the pin.

Figure 11 • *Pinout for PE29100*(1)(2)



Notes:
1) Drawings are not drawn to scale.
2) Singulated die size shown, bump side up.

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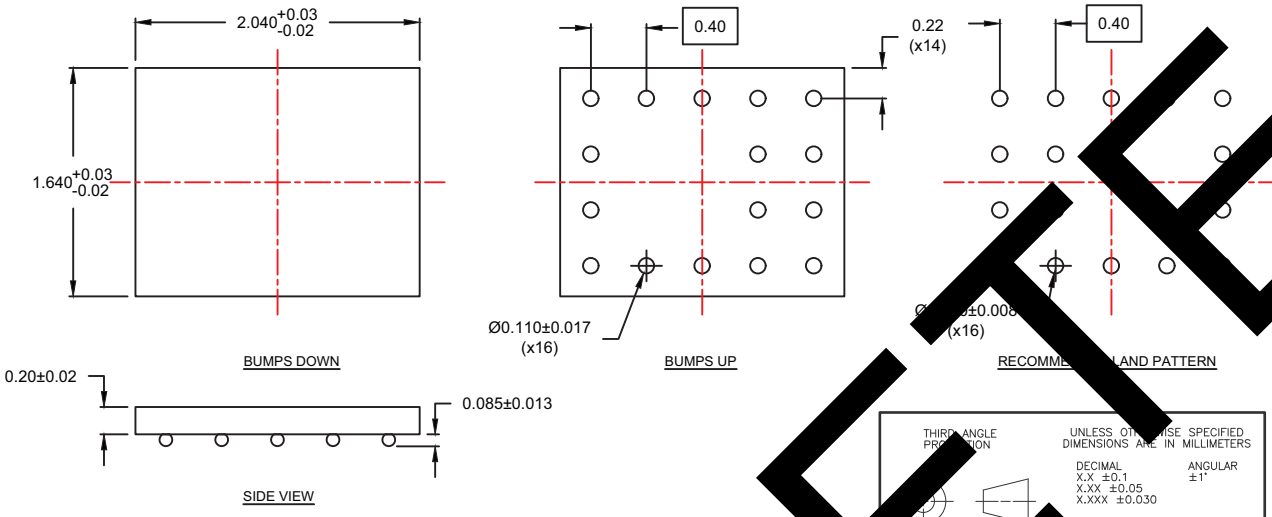
Figure 12 • *Recommended Land Pattern for PE29100*



Ordering Information

Table 8 lists the available ordering code for the PE29100.

Table 8 • *Order Code for PE29100*

Order Codes	Description	Packaging	Shipping Method
PE29100A-X	PE29100 flip chip	Die on tape and reel	5000 units/T&R
PE29100A-Z	PE29100 flip chip	Die on tape and reel	3000 units/T&R

Document Categories

Advance Information

The product is in a formative or design stage. The datasheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The datasheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

The datasheet contains final data. In the event Peregrine decides to change the specifications, Peregrine will notify customers of the intended changes by issuing a CNF (Customer Notification Form).

Sales Contact

For additional information, contact Sales at sales@psemi.com.

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