DS21458 Quad and DS26528 Octal Transceiver Software Comparison

This application note describes the differences between the DS21458 quad and DS26528 octal transceivers. It contains a complete breakdown of all feature differences and compares the two devices on a register-by-register basis.

1. Introduction

This document describes the differences between the DS21458 quad and the DS2652 octal transceivers. The DS21458 and DS26528 both contain a line interface unit (LIU) and a T1/E1 framer. The DS21458 is available up to four ports, and the DS26528 is an 8-port device.

2. Indirect Registers

The DS21458 uses indirect registers for the following "per-channel" functions. The DS26528 uses direct registers for these functions. The DS26528 only uses indirect registers for loading repetitive patterns, up to 512 bytes, in the BERT.

DS21458 Indirect Register Function	**DS26528 Direct Register**	**Comments**
Per-Channel Transmit Idle Code	TIDR1 to TIDR24	
Per-Channel Receive Idle Code	RIDR1 to RIDR24	
Bert Transmit Channel Select	TBCS1to TBCS4	
Transmit Fractional Channel Select	TGCCS1 to TGCCS4	
Payload Error Insert Channel Select		Not supported
Transmit Hardware Signaling Channel Select	SSIE1 to SSIE4	
Bert Receive Channel Select	RBCS1 to RBCS4	
Receive Fractional Channel Select	RGCCS1 to RGCCS4	
Receive Signaling Reinsertion Channel Select	RSI1 to RSI4	
Receive Signaling All-Ones Insertion Channel Select	T1RSAOI1 to T1RSAOI3	T1 mode

3. Terminology

Some terminology in the DS26528 data sheet is different from previous T1/E1 data sheets from Dallas Semiconductor. As an example, previous data sheets used the acronym RLOS to refer to Receive Loss of Sync. In the DS26528 data sheet, RLOS more correctly refers to Receive Loss of Signal. The table below shows the differences.

Condition	**DS26528 Data Sheet**	**Previous Data Sheets**
Loss of in-bound signal	RLOS (**R**eceive **L**oss **o**f **S**ignal)	RCL (**R**eceive **C**arrier **L**oss)
Loss of synchronization	RLOF (**R**eceive **L**oss **o**f **F**raming)	RLOS (**R**eceive **L**oss **o**f **S**ynchronization)
In-bound all ones	AIS (**A**larm **I**ndication **S**ignal) T1 and E1 modes	AIS for E1 mode; Blue Alarm for T1 mode
Remote Alarm	RAI (**R**emote **A**larm **I**ndication) T1 and E1 modes	RAI for E1 mode; Yellow Alarm for T1 mode

4. Register Mapping

Most of the functions are independently programmed for each of the eight ports in the DS26528. Therefore, there are eight separate, but identical registers for each port. See the register address ranges in **Table 1**. The only functions shared by all eight ports are the Global and BERT functions. The Global function registers are GTCR1, GFCR, GTCR2, GTCCR, GLSRR, GFSRR, GFISR, GBISR, GLISR, GFIMR, GBIMR, GLIMR, and IDR register.

The full address for each port is found by the following:
Base Address + (0x200 * n), where n = 0 to 7 for ports 1 through 8.

Table 1. Register Address Ranges (in Hex)

	GLOBAL REGISTERS	RECEIVE FRAMER	TRANSMIT FRAMER	LIU	BERT
	00F0 – 00FF	—	—	—	—
CH1	—	0000 – 00EF	0100 – 01EF	1000 – 101F	1100 – 110F
CH 2	—	0200 – 02EF	0300 – 03EF	1020 – 103F	1110 – 111F
CH 3	—	0400 – 04EF	0500 – 05EF	1040 – 105F	1120 – 112F
CH 4	—	0600 – 06EF	0700 – 07EF	1060 – 107F	1130 – 113F
CH 5	—	0800 – 08EF	0900 – 09EF	1080 – 109F	1140 – 114F
CH 6	—	0A00 – 0AEF	0B00 – 0BEF	10A0 – 10BF	1150 – 115F
CH 7	—	0C00 – 0CEF	0D00 – 0DEF	10C0 – 10DF	1160 – 116F
CH 8	—	0E00 – 0EEF	0F00 – 0FEF	10E0 – 10FF	1170 – 117F

All addresses are shown in hexadecimal; only the base address is shown for each register in this application note.

4.1 Direct Register Mapping

The following registers in the DS21458 can be mapped directly to registers in the DS26528.

DS21458 Address	DS21458 Symbol	DS26528 Address	DS26528 Symbol	DS21458 Register Description
08	SSIE1	118	SSIE1	Software Signaling Insertion Enable 1
09	SSIE2	119	SSIE2	Software Signaling Insertion Enable 2
0A	SSIE3	11A	SSIE3	Software Signaling Insertion Enable 3
0B	SSIE4	11B	SSIE4	Software Signaling Insertion Enable 4
0C	T1RDMR1	03C	T1RDMWE1	T1 Receive Digital Milliwatt Enable Register 1
0D	T1RDMR2	03D	T1RDMWE2	T1 Receive Digital Milliwatt Enable Register 2
0E	T1RDMR3	03E	T1RDMWE3	T1 Receive Digital Milliwatt Enable Register 3
0F	IDR	0F8	IDR	Device Identification Register
38	RSINFO1	098	RSS1	Receive Signaling Change of State Information 1
39	RSINFO2	099	RSS2	Receive Signaling Change of State Information 2
3A	RSINFO3	09A	RSS3	Receive Signaling Change of State Information 3
3B	RSINFO4	09B	RSS4	Receive Signaling Change of State Information 4
3C	RSCSE1	0A8	RSCSE1	Receive Signaling Change of State Interrupt Enable 1
3D	RSCSE2	0A9	RSCSE2	Receive Signaling Change of State Interrupt Enable 2
3E	RSCSE3	0AA	RSCSE3	Receive Signaling Change of State Interrupt Enable 3
3F	RSCSE4	0AB	RSCSE4	Receive Signaling Change of State Interrupt Enable 4
42	LCVCR1	050	LCVCR1	Line Code Violation Count Register 1
43	LCVCR2	051	LCVCR2	Line Code Violation Count Register 2
44	PCVCR1	052	PCVCR1	Path Code Violation Count Register 1
45	PCVCR2	053	PCVCR2	Path Code Violation Count Register 2
46	FOSCR1	054	FOSCR1	Frames Out-of-Sync Count Register 1
47	FOSCR2	055	FOSCR2	Frames Out-of-Sync Count Register 2
48	EBCR1	056	E1EBCR1	E-Bit Count Register 1
49	EBCR2	057	E1EBCR2	E-Bit Count Register 2
4B	PCLR1	1D0	PCL1	Per-Channel Loopback Enable Register 1
4C	PCLR2	1D1	PCL2	Per-Channel Loopback Enable Register 2
4D	PCLR3	1D2	PCL3	Per-Channel Loopback Enable Register 3
4E	PCLR4	1D3	PCL4	Per-Channel Loopback Enable Register 4
50	TS1	140	TS1	Transmit Signaling Register 1
51	TS2	141	TS2	Transmit Signaling Register 2
52	TS3	142	TS3	Transmit Signaling Register 3
53	TS4	143	TS4	Transmit Signaling Register 4
54	TS5	144	TS5	Transmit Signaling Register 5

55	TS6	145	TS6	Transmit Signaling Register 6
56	TS7	146	TS7	Transmit Signaling Register 7
57	TS8	147	TS8	Transmit Signaling Register 8
58	TS9	148	TS9	Transmit Signaling Register 9
59	TS10	149	TS10	Transmit Signaling Register 10
5A	TS11	14A	TS11	Transmit Signaling Register 11
5B	TS12	14B	TS12	Transmit Signaling Register 12
5C	TS13	14C	TS13	Transmit Signaling Register 13
5D	TS14	14D	TS14	Transmit Signaling Register 14
5E	TS15	14E	TS15	Transmit Signaling Register 15
5F	TS16	14F	TS16	Transmit Signaling Register 16
60	RS1	040	RS1	Receive Signaling Register 1
61	RS2	041	RS2	Receive Signaling Register 2
62	RS3	042	RS3	Receive Signaling Register 3
63	RS4	043	RS4	Receive Signaling Register 4
64	RS5	044	RS5	Receive Signaling Register 5
65	RS6	045	RS6	Receive Signaling Register 6
66	RS7	046	RS7	Receive Signaling Register 7
67	RS8	047	RS8	Receive Signaling Register 8
68	RS9	048	RS9	Receive Signaling Register 9
69	RS10	049	RS10	Receive Signaling Register 10
6A	RS11	04A	RS11	Receive Signaling Register 11
6B	RS12	04B	RS12	Receive Signaling Register 12
6C	RS13	04C	RS13	Receive Signaling Register 13
6D	RS14	04D	RS14	Receive Signaling Register 14
6E	RS15	04E	RS15	Receive Signaling Register 15
6F	RS16	04F	RS16	Receive Signaling Register 16
74	TDS0SEL	189	TDS0SEL	Transmit Channel Monitor Select
75	TDS0M	1BB	TDS0M	Transmit DS0 Monitor Register
76	RDS0SEL	012	RDS0SEL	Receive Channel Monitor Select
77	RDS0M	060	RDS0M	Receive DS0 Monitor Register
80	TCICE1	150	TCICE1	Transmit Idle Code Enable Register 1
81	TCICE2	151	TCICE2	Transmit Idle Code Enable Register 2
82	TCICE3	152	TCICE3	Transmit Idle Code Enable Register 3
83	TCICE4	153	TCICE4	Transmit Idle Code Enable Register 4
84	RCICE1	0D0	RCICE1	Receive Idle Code Enable Register 1
85	RCICE2	0D1	RCICE2	Receive Idle Code Enable Register 2
86	RCICE3	0D2	RCICE3	Receive Idle Code Enable Register 3
87	RCICE4	0D3	RCICE4	Receive Idle Code Enable Register 4
88	RCBR1	0C4	RCBR1	Receive Channel Blocking Register 1
89	RCBR2	0C5	RCBR2	Receive Channel Blocking Register 2
8A	RCBR3	0C6	RCBR3	Receive Channel Blocking Register 3
8B	RCBR4	0C7	RCBR4	Receive Channel Blocking Register 4
8C	TCBR1	1C4	TCBR1	Transmit Channel Blocking Register 1
8D	TCBR2	1C5	TCBR2	Transmit Channel Blocking Register 2
8E	TCBR3	1C6	TCBR3	Transmit Channel Blocking Register 3

8F	TCBR4	1C7	TCBR4	Transmit Channel Blocking Register 4
B7	TCD1	1AC	T1TCD1	Transmit Code Definition Register 1
B8	TCD2	1AD	T1TCD2	Transmit Code Definition Register 2
B9	RUPCD1	0AC	T1RUPCD1	Receive Up Code Definition Register 1 (T1 Mode Only)
BA	RUPCD2	0AD	T1RUPCD2	Receive Up Code Definition Register 2 (T1 Mode Only)
BB	RDNCD1	0AE	T1RDNCD1	Receive Down Code Definition Register 1 (T1 Mode Only)
BC	RDNCD2	0AF	T1RDNCD2	Receive Down Code Definition Register 2 (T1 Mode Only)
BE	RSCD1	09C	T1RSPCD1	Receive Spare Code Definition Register 1 (T1 Mode Only)
BF	RSCD2	09D	T1RSPCD2	Receive Spare Code Definition Register 2 (T1 Mode Only)
C0	RFDL	062	T1RFDL E1RRTS7	Receive FDL Register (T1 Mode) E1 Receive Real-Time Status 7 (E1 Mode)
C1	TFDL	162	T1TFDL	Transmit FDL Register (T1 Mode Only)
C6	RAF	064	T1RSLC1 E1RAF	Receive SLC96 Data Link 1 (T1 Mode) Receive Align Frame Register (E1 Mode)
C7	RNAF	065	T1RSLC2 E1RNAF	Receive SLC96 Data Link 2 (T1 Mode) Receive Non-align Frame Register (E1 Mode)
C8	RSiAF	066	T1RSLC3 E1RSiAF	Receive SLC96 Data Link 3 (T1 Mode) Receive Si Align Frame (E1 Mode)
C9	RSiNAF	067	E1RSiNAF	Receive Si Non-align Frame (E1 Mode Only)
CA	RRA	068	E1RNAF	Receive Remote Alarm Bits (E1 Mode Only)
CB	RSa4	069	E1RSa4	Receive Sa4 Bits (E1 Mode Only)
CC	RSa5	06A	E1RSa5	Receive Sa5 Bits (E1 Mode Only)
CD	RSa6	06B	E1RSa6	Receive Sa6 Bits (E1 Mode Only)
CE	RSa7	06C	E1RSa7	Receive Sa7 Bits (E1 Mode Only)
CF	RSa8	06D	E1RSa8	Receive Sa8 Bits (E1 Mode Only)
D0	TAF	164	T1TSLC1 E1TAF	Transmit SLC96 Data Link 1 (T1 Mode) E1 Transmit Align Frame (E1 Mode)
D1	TNAF	165	T1TSLC2 E1TNAF	Transmit SLC96 Data Link 2 (T1 Mode) E1 Transmit Non-align Frame (E1 Mode)
D2	TSiAF	166	T1TSLC3 E1TSiAF	Transmit SLC96 Data Link 3 (T1 Mode) E1 Transmit Si Align Frame (E1 Mode)
D3	TSiNAF	167	E1TSiNAF	E1 Transmit Si Non-align Frame (E1 Mode Only)
D4	TRA	168	E1TRA	E1 Transmit Remote Alarm (E1 Mode Only)
D5	TSa4	169	E1TSa4	E1 Transmit Sa4 Bits (E1 Mode Only)
D6	TSa5	16A	E1TSa5	E1 Transmit Sa5 Bits (E1 Mode Only)
D7	TSa6	16B	E1TSa6	E1 Transmit Sa6 Bits (E1 Mode Only)
D8	TSa7	16C	E1TSa7	E1 Transmit Sa7 Bits (E1 Mode Only)
D9	TSa8	16D	E1TSa8	E1 Transmit Sa8 Bits (E1 Mode Only)
DA	TSACR	114	E1TSACR	E1 Transmit Sa Bit Control Register

4.2 Bit Level Mapping

The following registers in the DS21458 do not have direct mappings to registers in the DS26528. The following table shows how to map the individual bits of the DS21458 registers into the individual bit in the DS26528 registers.

***Note:** NS = not supported

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
00	MSTRREG	Master Mode Register	0 = RMMR.1 and TMMR.1 1 = RMMR.0 and TMMR.0 2 = 3 = 4 = 5 = 6 = 7 =	
01	IOCR1	I/O Configuration Register 1	0 = TCR3.7 1 = TIOCR.2 2 = TIOCR.0 3 = TIOCR.1 4 = RIOCR.2 5 = RIOCR.0 6 = RIOCR.1 7 = RIOCR.3	
02	IOCR2	I/O Configuration Register 2	0 = RIOCR.4 1 = TIOCR.4 2 = RIOCR.5 3 = TIOCR.5 4 = TIOCR.6 5 = RIOCR.6 6 = TIOCR.7 7 = RIOCR.7	

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
03	T1RCR1	T1 Receive Control Register 1	0 = RCR1.0 1 = RCR1.1 2 = RCR1.7 3 = RCR1.3 4 = T1RCR2.2 5 = T1RCR2.3 6 = RCR1.4 7 =	
04	T1RCR2	T1 Receive Control Register 2	0 = T1RCR2.0 1 = RCR1.2 2 = **NS* 3 = **NS**** 4 = T1RCR2.4 5 = RCR1.6 6 = RCR1.5 7 =	*ZBTSI not supported in the DS26528. **Information available in HDLC section.
05	T1TCR1	T1 Transmit Control Register 1	0 = TCR1.0* 1 = TCR1.1* 2 = TCR2.7* 3 = TCR1.3* 4 = TCR1.4* 5 = TCR1.5* 6 = TCR1.6* 7 = TCR1.7*	*T1 Mode
06	T1TCR2	T1 Transmit Control Register 2	0 = TCR2.0* 1 = **NS**** 2 = TCR2.2* 3 = TCR2.3* 4 = TCR2.4* 5 = **NS***** 6 = TCR2.6* 7 = TCR1.2*	*T1 Mode **ZBTSI not supported in the DS26528. ***Information available in HDLC section.

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
07	T1CCR1	T1 Common Control Register 1	0 = TCR3.0 1 = TCR2.1* 2 = TCR3.2 3 = TCR4.2* 4 = TCR4.3* 5 = 6 = 7 =	*T1 Mode
10	INFO1	Information Register 1	0 = RLS2.0* 1 = RLS2.1* 2 = RLS2.2* 3 = RLS2.3* 4 = RLS2.4* 5 = RLS2.5* 6 = TLS1.3 7 = RLS2.7*	*T1 Mode
11	INFO2	Information Register 2	0 = **NS** 1 = **NS** 2 = **NS** 3 = **NS** 4 = **NS*** 5 = **NS** 6 = **NS*** 7 = **NS****	*Information available in LIU section. **Information available in BERT section.
12	INFO3	Information Register 3	0 = RLS2.5* 1 = RLS2.4* 2 = RLS2.6* 3 = 4 = 5 = 6 = 7 =	*E1 Mode Only
13		UNUSED		
14	IIR1	Interrupt Information Register 1		Consult RIIR and TIIR DS26528 registers.

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
15	IIR2	Interrupt Information Register 2		Consult RIIR and TIIR DS26528 registers
16	SR1	Status Register 1	0 = **NS*** 1 = **NS*** 2 = **NS** 3 = **NS*** 4 = **NS*** 5 = RLS4.3 6 = RLS4.1 7 = **NS**	*Information available in LIU section.
17	IMR1	Interrupt Mask Register 1	0 = **NS*** 1 = **NS*** 2 = **NS** 3 = **NS*** 4 = **NS*** 5 = RIM4.3 6 = RIM4.1 7 = NS	*Information available in LIU section.
18	SR2	Status Register 2	0 = RLS1.0* 1 = RLS1.1** 2 = RLS1.2 3 = RLS1.3 4 = RLS1.4 5 = RLS1.5 6 = RLS1.6 7 = RLS1.7	*The DS21458 data sheet uses the acronym RLOS (Receive Loss of Synchronization) to refer to RLOF (Receive Loss of Frame). **The DS21458 data sheet uses the acronym RCL (Receive Carrier Loss) to refer to RLOS (Receive Loss of Signal).
19	IMR2	Interrupt Mask Register 2	0 = RIM1.0 1 = RIM1.1 2 = RIM1.2 3 = RIM1.3 4 = RIM1.4 5 = RIM1.5 6 = RIM1.6 7 = RIM1.7	

<table>
<tr><th>DS21458
Address</th><th>DS21458
Symbol</th><th>DS21458
Register Description</th><th>DS26528 Bit Location
21458 Bit = 26528 Reg. Bit</th><th colspan="2">Comments</th></tr>
<tr><td rowspan="2">1A</td><td rowspan="2">SR3</td><td rowspan="2">Status Register 3</td><td rowspan="2">0 = RLS1.3*
1 = RLS3.0*
2 = RLS3.1*
3 = RLS3.3*
4 = TLS1.0
5 = RLS3.0**
6 = RLS3.1**
7 = RLS3.2**</td><td colspan="2">*E1 Mode Only

**The DS26528 uses separate interrupt and clear bits, while the DS21458 uses a double-polled interrupt bit.

DS26528 interrupt and clear bits</td></tr>
<tr><td>DS26528 Interrupt

RLS3.0 E1 Mode
RLS3.1 E1 Mode
RLS3.3 E1 Mode
TLS1.0
RLS3.0 T1 Mode
RLS3.1 T1 Mode
RLS3.2 T1 Mode</td><td>DS26528 Clear

RLS3.4 E1 Mode
RLS3.5 E1 Mode
RLS3.7 E1 Mode
TLS1.1
RLS3.4 T1 Mode
RLS3.5 T1 Mode
RLS3.6 T1 Mode</td></tr>
<tr><td>1B</td><td>IMR3</td><td>Interrupt Mask Register 3</td><td>0 = RIM1.0
1 = RIM3.1*
2 = RIM3.2*
3 = RIM3.3*
4 = TIM1.0
5 = RIM3.0**
6 = RIM3.1**
7 = RIM3.2**</td><td colspan="2">*E1 Mode

**T1 Mode</td></tr>
<tr><td>1C</td><td>SR4</td><td>Status Register 4</td><td>0 = RLS2.0*
1 = RLS2.1*
2 = RLS4.0
3 = TLS1.3
4 = TLS1.2
5 = RLS2.2*
6 = RLS2.3*
7 = RLS7.4**</td><td colspan="2">*E1 Mode

**T1 Mode</td></tr>
</table>

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
1D	IMR4	Interrupt Mask Register 4	0 = RIM2.0* 1 = RIM2.1* 2 = RIM4.0 3 = TIM1.3 4 = TIM1.2 5 = RIM2.2* 6 = RIM2.3* 7 = RIM7.4**	*E1 Mode **T1 Mode
1E	SR5	Status Register 5	0 = RLS4.5 1 = RLS4.6 2 = RLS4.7 3 = TLS1.5 4 = TLS1.6 5 = TLS1.7 6 = 7 =	
1F	IMR5	Interrupt Mask Register 5	0 = RLS4.5 1 = RLS4.6 2 = RLS4.7 3 = TLS1.5 4 = TLS1.6 5 = TLS1.7 6 = 7 =	
20	SR6	Status Register 6		Information available in HDLC section.
21	IMR6	Interrupt Mask Register 6		Information available in HDLC section.
22	SR7	Status Register 7		Information available in HDLC section.
23	IMR7	Interrupt Mask Register 7		Information available in HDLC section.

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
24	SR8	Status Register 8	0 = RLS7.0* 1 = **NS** 2 = TLS2.4 3 = RLS7.2* 4 = **NS** 5 = RLS7.1* 6 = 7 =	*T1 Mode
25	IMR8	Interrupt Mask Register 8	0 = RIM7.0* 1 = **NS** 2 = TIM2.4 3 = RIM7.2* 4 = **NS** 5 = RIM7.1* 6 = 7 =	*T1 Mode
26	SR9	Status Register 9		Information available in BERT section.
27	IMR9	Interrupt Mask Register 9		Information available in BERT section.
28	PCPR	Per-Channel Pointer Register		Information is in Indirect Register section.
29	PCDR1	Per-Channel Data Register 1		Information is in Indirect Register section.
2A	PCDR2	Per-Channel Data Register 2		Information is in Indirect Register section.
2B	PCDR3	Per-Channel Data Register 3		Information is in Indirect Register section.
2C	PCDR4	Per-Channel Data Register 4		Information is in Indirect Register section.
2D	INFO4	Information Register 4		Information available in HDLC section.
2E	INFO5	Information Register 5		Information available in HDLC section.
2F	INFO6	Information Register 6		Information available in HDLC section.
30	INFO7	Information Register 7	0 = E1RRTS7.2* 1 = E1RRTS7.1* 2 = E1RRTS7.0* 3 = E1RRTS7.3* 4 = E1RRTS7.4* 5 = E1RRTS7.5* 6 = E1RRTS7.6* 7 = E1RRTS7.7*	*E1 Mode

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
31	H1RC	HDLC #1 Receive Control		Information available in HDLC section.
32	H2RC	HDLC #2 Receive Control		Unsupported function in the DS26528.
33	E1RCR1	E1 Receive Control Register 1	0 = RCR1.0* 1 = RCR1.1* 2 = RCR1.2* 3 = RCR1.3* 4 = RCR1.4* 5 = RCR1.6* 6 = RCR1.5* 7 = RCR3.5	*E1 Mode
34	E1RCR2	E1 Receive Control Register 2	0 = E1RCR2.0 1 = 2 = 3 = E1RCR2.3* 4 = E1RCR2.4* 5 = E1RCR2.5* 6 = E1RCR2.6* 7 = E1RCR2.7*	*E1 Mode
35	E1TCR1	E1 Transmit Control Register 1	0 = TCR1.0* 1 = TCR1.5* 2 = TCR1.2* 3 = TCR1.3* 4 = TCR1.4* 5 = TCR1.1* 6 = TCR1.6* 7 = TCR1.7*	*E1 Mode
36	E1TCR2	E1 Transmit Control Register 2	0 = TCR2.5* 1 = TCR2.6* 2 = TCR2.7* 3 = TCR2.4* 4 = TCR2.3* 5 = TCR2.2* 6 = TCR2.1* 7 = TCR2.0*	*E1 Mode

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
37	BOCC	BOC Control Register	0 = THC2.6 1 = RBOCC.1 2 = RBOCC.2 3 = RBOCC.7 4 = **NS*** 5 = 6 = 7 =	*The DS26528 has a dedicated, receive BOC message register.
40	SIGCR	Signaling Control Register	0 = RSIGC.4* 1 = 2 = 3 = RSIGC.2 4 = RSIGC.1 5 = 6 = 7 = **NS****	*The DS26528 forces signaling to all ones on a per-channel basis using the T1RSAOI1-T1RSAOI3 registers. **The DS26528 selects signaling reinsertion on a per-channel basis using the RSI1-RSI4 registers.
41	ERCNT	Error Count Configuration Register	0 = ERCNT.0 1 = ERCNT.1* 2 = ERCNT.2* 3 = ERCNT.0 4 = ERCNT.3 5 = ERCNT.4 6 = ERCNT.5 7 =	*T1 Mode Only
4A	LBCR	Loopback Control Register	0 = RCR3.0 1 = RCR3.1 2 = LMCR.3 3 = LMCR.5 4 = 5 = 6 = 7 =	

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
4F	ESCR	Elastic Store Control Register	0 = RESCR.0 1 = RESCR.1 2 = RESCR.2 3 = RESCR.3 4 = TESCR.0 5 = TESCR.1 6 = TESCR.2 7 = TESCR.3	
70	CCR1	Common Control Register 1	0 = GTCR1.5 1 = TCR3.4 2 = TCR3.5 3 = 4 = TCR3.6 5 = RSIGC.0 6 = TCR3.0 7 =	
71	CCR2	Common Control Register 2	0 = **NS*** 1 = GFCR.4** 2 = GFCR.5** 3 = 4 = 5 = 6 = 7 =	*Backplane clock is always enabled. **The setting is opposite from the setting in DS21458. See the DS26528 data sheet for details.
72	CCR3	Common Control Register 3	0 = RESCR.6 1 = RESCR.7 2 = TESCR.6 3 = TESCR.7 4 = 5 = 6 = 7 =	

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
73	CCR4	Common Control Register 4	0 = 1 = 2 = 3 = 4 = **NS** 5 = **NS** 6 = **NS** 7 = **NS**	
78	LIC1	Line Interface Control 1		Information available in LIU section.
79	LIC2	Line Interface Control 2		Information available in LIU section.
7A	LIC3	Line Interface Control 3		Information available in LIU section.
7B	LIC4	Line Interface Control 4		Information available in LIU section.
7C		UNUSED		
7D	TLBC	Transmit Line Build-Out Control		Consult the LTITSR register in DS26528.
7E	IAAR	Idle Array Address Register		The DS26528 does not use Direct Registers.
7F	PCICR	Per-Channel Idle Code Value Register		The DS26528 does not use Direct Registers.
90 - 9F	HDLC1	HDLC #1 Functions Registers		Information available in HDLC section.
A0 - AF	HDLC2	HDLC #2 Functions Registers		Unsupported function in the DS26528.
B0	ESIBCR1	Extend System Information Bus Control Register 1		Unsupported function in the DS26528.
B1	ESIBCR2	Extend System Information Bus Control Register 2		Unsupported function in the DS26528.
B2	ESIB1	Extend System Information Bus Register 1		Unsupported function in the DS26528.
B3	ESIB2	Extend System Information Bus Register 2		Unsupported function in the DS26528.
B4	ESIB3	Extend System Information Bus Register 3		Unsupported function in the DS26528.
B5	ESIB4	Extend System Information Bus Register 4		Unsupported function in the DS26528.

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
B6	IBCC	In-Band Code Control Register	0 = T1RIBCC.0 1 = T1RIBCC.1 2 = T1RIBCC.2 3 = T1RIBCC.3 4 = T1RIBCC.4 5 = T1RIBCC.5 6 = TCR4.0* 7 = TCR4.1*	*T1 Mode Only
BD	RSCC	In-Band Receive Spare Control Register	0 = T1RSCC.0 1 = T1RSCC.1 2 = T1RSCC.2 3 = 4 = 5 = 6 = 7 =	
C2	RFDLM1	Receive FDL Match Register 1		Unsupported function in the DS26528.
C3	RFDLM2	Receive FDL Match Register 2		Unsupported function in the DS26528.
C4		Unused		Unused
C5	IBOC	Interleave Bus Operation Control Register		The DS26528 Interleave Bus Operation function has separate receive and transmit control registers. DS26528 Address: 084 — Function: Receive IBO control DS26528 Address: 188 — Function: Transmit IBO control
DB - E1	BERT	BERT Functions Registers		Information available in BERT section.
E2		Unused		Unused
E3 - EF	BERT	BERT Functions Registers		Information available in BERT section.
F0 - FF	TEST	Test Register		Unsupported function in the DS26528.

5. LIU Register Bit Map

DS21458 Address	DS21458 Symbol	DS21458 Register Description	DS26528 Bit Location 21458 Bit = 26528 Reg. Bit	Comments
11	INFO2	Information Register 2	0 = 1 = 2 = 3 = 4 = LRSR.2 5 = 6 = RLS7.0 7 =	
16	SR1	Status Register 1	0 = TLS1.0 1 = LLSR.2 2 = 3 = LLSR.0 4 = LLSR.3 and LLSR.7 5 = 6 = 7 =	
17	IMR1	Interrupt Mask Register 1	0 = TIM1.0 1 = LSIMR.2 2 = 3 = LSIMR.0 4 = LSIMR.3 5 = 6 = 7 =	

4A	LBCR	Loopback Control Register	0 = 1 = 2 = LMCR.3 3 = LMCR.5 4 = 5 = 6 = 7 =	
79	LIC2	Line Interface Control 2	0 = 1 = 2 = 3 = 4 = TCR1.1 ** 5 = TCR3.1 6 = * 7 = LTRCR.1	*The DS26528 has a global register (GLSRR) to reset each LIU. See the DS26528 data sheet for details. **E1 Mode
7A	LIC3	Line Interface Control 3	0 = LRISMR.7 1 = 2 = 3 = 4 = 5 = 6 = 7 =	
7B	LIC4	Line Interface Control 4	0 = 1 = 2 = 3 = 4 = * 5 = * 6 = 7 =	*Consult GTCCR.0-1 register in the DS26528 data sheet.

6. HDLC Controller

The DS26528 has a single HDLC controller that may be mapped to any timeslot or to the FDL (T1 mode), or to any combinations of Sa bits (E1 mode). The table below lists the differences between the DS21458's and the DS26528's HDLC function.

	DS21458	**DS26528**
Number of Controllers	2	1
FIFO Size	128 Bytes	64 Bytes
Channel Assignment	Any combination of channels, Facilities Data Link bit stream, Any combinations of Sa bits	Any single DS0, Facilities Data Link bit stream, Any combination of Sa bits
SS7 Support	Yes	No

DS21458 Address	**DS21458 Symbol**	**DS21458 Register Description**	**DS26528 Bit Location 21458 Bit = 26528 Reg. Bit**	**Comments**
31	H1RC	HDLC #1 Receive Control	0 = **NS*** 1 = 2 = 3 = 4 = 5 = 6 = RHC.5 7 = RHC.6	*The DS26528 does not have support for Signaling System 7 (SS7).
32	H2RC	HDLC #2 Receive Control		Unsupported function in the DS26528.
90	H1TC	HDLC #1 Transmit Control	0 = THC1.0 1 = THC1.1 2 = THC1.2 3 = THC1.3 4 = THC1.4 5 = THC1.5 6 = THC1.6 7 = THC1.7	

91	H1FC	HDLC #1 FIFO Control	0 = RHFC.0 1 = RHFC.1 2 = **NS*** 3 =THFC.0 4 =THFC.1 5 = **NS*** 6 = 7 =	*The HDLC FIFO is only 64 bytes deep on the DS26528.
92	H1RCS1	HDLC #1 Receive Channel Select 1		The DS26528 uses the RHC register to select the channel to receive HDLC data. The DS26528 can only receive HDLC data in a single DSO channel.
93	H1RCS2	HDLC #1 Receive Channel Select 2		
94	H1RCS3	HDLC #1 Receive Channel Select 3		
95	H1RCS4	HDLC #1 Receive Channel Select 4		
96	H1RTSBS	HDLC #1 Receive Time Slot Bits/Sa Bits Select		
97	H1TCS1	HDLC #1 Transmit Channel Select1		The DS26528 uses the THC2 register to select the channel to transmit HDLC data. The DS26528 can only transmit HDLC data in a single DSO channel.
98	H1TCS2	HDLC #1 Transmit Channel Select2		
99	H1TCS3	HDLC #1 Transmit Channel Select3		
9A	H1TCS4	HDLC #1 Transmit Channel Select4		
9B	H1TTSBS	HDLC #1 Transmit Time Slot Bits/Sa Bits Select		
9C	H1RPBA	HDLC #1 Receive Packet Bytes Available	0B5 RHPBA	
9D	H1TF	HDLC #1 Transmit FIFO	1B4 THF	
9E	H1RF	HDLC #1 Receive FIFO	0B6 RHF	
9F	H1TFBA	HDLC #1 Transmit FIFO Buffer Available	1B3 TFBA	

A0	H2TC	HDLC #2 Transmit Control		Unsupported function in the DS26528.
A1	H2FC	HDLC #2 FIFO Control		Unsupported function in the DS26528.
A2	H2RCS1	HDLC #2 Receive Channel Select 1		Unsupported function in the DS26528.
A3	H2RCS2	HDLC #2 Receive Channel Select 2		Unsupported function in the DS26528.
A4	H2RCS3	HDLC #2 Receive Channel Select 3		Unsupported function in the DS26528.
A5	H2RCS4	HDLC #2 Receive Channel Select 4		Unsupported function in the DS26528.
A6	H2RTSBS	HDLC #2 Receive Time Slot Bits/Sa Bits Select		Unsupported function in the DS26528.
A7	H2TCS1	HDLC #2 Transmit Channel Select1		Unsupported function in the DS26528.
A8	H2TCS2	HDLC #2 Transmit Channel Select2		Unsupported function in the DS26528.
A9	H2TCS3	HDLC #2 Transmit Channel Select3		Unsupported function in the DS26528.
AA	H2TCS4	HDLC #2 Transmit Channel Select4		Unsupported function in the DS26528.
AB	H2TTSBS	HDLC #2 Transmit Time Slot Bits/Sa Bits Select		Unsupported function in the DS26528.
AC	H2RPBA	HDLC #2 Receive Packet Bytes Available		Unsupported function in the DS26528.
AD	H2TF	HDLC #2 Transmit FIFO		Unsupported function in the DS26528.
AE	H2RF	HDLC #2 Receive FIFO		Unsupported function in the DS26528.
AF	H2TFBA	HDLC #2 Transmit FIFO Buffer Available		Unsupported function in the DS26528

7. BERT Functions

The DS26528 BERT functions are more full-featured than on the DS21458, so a direct register mapping is not possible. The DS26528 pseudorandom patterns are fully programmable over 32 bits compared to the fixed set of pseudorandom patterns found in the DS21458. Also, large repetitive patterns up to 512 bytes may be loaded with an indirect register. The BERT register set for the DS21458 follows, but the DS26528 data sheet should be consulted for all BERT functions.

DS21458 Address	DS21458 Symbol	DS21458 Register Description	Comments
DB	BAWC	BERT Alternating Word Count Rate	Consult DS26528 data sheet.
DC	BRP1	BERT Repetitive Pattern Set Register 1	Consult DS26528 data sheet.
DD	BRP2	BERT Repetitive Pattern Set Register 2	Consult DS26528 data sheet.
DE	BRP3	BERT Repetitive Pattern Set Register 3	Consult DS26528 data sheet.
DF	BRP4	BERT Repetitive Pattern Set Register 4	Consult DS26528 data sheet.
E0	BC1	BERT Control Register 1	Consult DS26528 data sheet.
E1	BC2	BERT Control Register 2	Consult DS26528 data sheet.
E2		Unused	Unused
E3	BBC1	BERT Bit Count Register 1	Consult DS26528 data sheet.
E4	BBC2	BERT Bit Count Register 2	Consult DS26528 data sheet.
E5	BBC3	BERT Bit Count Register 3	Consult DS26528 data sheet.
E6	BBC4	BERT Bit Count Register 4	Consult DS26528 data sheet.
E7	BEC1	BERT Error Count Register 1	Consult DS26528 data sheet.
E8	BEC2	BERT Error Count Register 2	Consult DS26528 data sheet.
E9	BEC3	BERT Error Count Register 3	Consult DS26528 data sheet.
EA	BIC	BERT Interface Control Register	Unsupported function in the DS26528.
EB	ERC	Error Rate Control Register	Unsupported function in the DS26528.
EC	NOE1	Number-of-Errors 1	Unsupported function in the DS26528.
ED	NOE2	Number-of-Errors 2	Unsupported function in the DS26528.
EE	NOEL1	Number-of-Errors Left 1	Unsupported function in the DS26528.
EF	NOEL2	Number-of-Errors Left 2	Unsupported function in the DS26528.

8. Features Exclusive to the DS26528

There are many new features in the DS26528. A summary of the new functions follows.

8.1 Transmit Side Synchronizer

The DS26528 has a basic synchronizer on the transmit side. This function allows the transmitter to align to the data stream present at TSER when there is no externally supplied, frame sync signal available.

Register Name: TSYNCC
Register Description: Transmit Synchronizer Control Register
Register Address: 18EH + (200h x n), where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
--	--	--	CRC4	TSEN	TSEN	SYNCE	RESYNC
0	0	0	0	0	0	0	0

Bit 0 - Resynchronize (RESYNC)
When toggled from low to high, a resynchronization of the transmit side framer is initiated. It must be cleared and set again for a subsequent resync.

Bit 1 - Sync Enable (SYNCE)
0 = Automatic resync enabled
1 = Automatic resync disabled

Bit 2 - Transmit Synchronizer Enable (TSEN)
0 = Transmit-side synchronizer disabled
1 = Transmit-side synchronizer enabled

Register Name: TLS3
Register Description: Transmit Latched Status Register 3 (Synchronizer)
Register Address: 192H + (200h x n), where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
--	--	--	--	--	--	LOF	LOFD
0	0	0	0	0	0	0	0

Bit 0 - Loss of Frame Synchronization Detect (LOFD)
This is a latched bit which is set when the transmit synchronizer is searching for the sync pattern in the incoming data stream.

Bit 1 - Loss of Frame (LOF)
A real-time status bit which indicates that the transmit side synchronizer is searching for the synchronization pattern in the incoming data stream.

8.2 Other Functions Exclusive to the DS26528

Register Name: GTCR1
Register Description: Global Transceiver Control Register 1
Register Address: 0F0H
Read/Write Function: R/W

7	6	5	4	3	2	1	0
--	--	RLOFLTS	GIBO	--	BWE	GCLE	GIPI
0	0	0	0	0	0	0	0

Bit 0 - Global Interrupt Pin Inhibit (GIPI)
0 = Normal Operation. Interrupt pin (INT) will toggle low on an unmasked interrupt condition
1 = Interrupt Inhibit. Interrupt pin (INT) is forced high (inactive) when this bit is set.

Bit 1 - Global Counter Latch Enable (GCLE)
A low-to-high transition on this bit will, when enabled, latch the framer performance monitor counters. Each framer can be independently enabled to accept this input. This bit must be cleared and set again to perform another counter latch.

Bit 2 - Bulk Write Enable (BWE)
When this bit is set, a port write to one of the octal ports will be mapped into all eight ports. This applies to the framer, BERT, and LIU register sets. It must be cleared before performing a read operation. This bit is useful for device initialization.
0 = Normal operation
1 = Bulk write is enabled

Bit 4 - Ganged IBO Enable (GIBO)
This bit is used to select either the internal mux for IBO operation or an external “wire-OR” operation. Normally this bit should be set = 0 and the internal mux used.
0 = Use internal IBO mux.
1 = Externally .wire-OR. TSERs and RSERs for IBO operation.

Bit 5 – Receive Loss of Frame/Loss of Transmit Clock Indication Select (RLOFLTS)
0 = RLOF/LOTCx pins indicate framer receive loss of frame.
1 = RLOF/LOTCx pins indicate framer loss of transmit clock.

Register Name: GFCR
Register Description: Global Framer Control Register
Register Address: 0F1H
Read/Write Function: R/W

7	6	5	4	3	2	1	0
IBOMS0	IBOMS0	BPCLK1	BPCLK0	RFLOSSFS	RFMSS	TCBCS	RCBCS
0	0	0	0	0	0	0	0

Bit 0 - Receive Channel Block/Clock Select (RCBCS)

This bit controls the function of all eight RCHBLK/CLK pins.
0 = RCHBLK/CLK pins output RCHBLK (1-8) (Receive Channel Block)
1 = RCHBLK/CLK pins output RCHCLK (1-8) (Receive Channel Clock)

Bit 1- Transmit Channel Block/Clock Select (TCBCS)

This bit controls the function of all eight TCHBLK/CLK pins.
0 = TCHBLK/CLK pins output TCHBLK (1-8) (Transmit Channel Block)
1 = TCHBLK/CLK pins output TCHCLK (1-8) (Transmit Channel Clock)

Bit 2 - Receive Frame/Multiframe Sync Select (RFMSS)

This bit controls the function of all eight RM/RFSYNC pins.
0 = RM/RFSYNC pins output RFSYNC (1-8) (Receive Frame Sync)
1 = RM/RFSYNC pins output RMSYNC (1-8) (Receive Multi-Frame Sync)

Bit 3 - Receive Loss of Signal/Signaling Freeze Select (RLOSSFS)

This bit controls the function of all eight AL/RSIGF/FLOS pins. The Receive LOS is further selected between Framer LOS and LIU LOS by GTCR2 Bit 2.
0 = AL/RSIGF/FLOS pins output RLOS (1-8) (Receive Loss)
1 = AL/RSIGF/FLOS pins output RSIGF (1-8) (Receive Signaling Freeze)

GFCR.7,6 - Interleave Bus Operation Mode Select 1, 0 (IBOMS[1:0])

These bits determine the configuration of the IBO (interleaved bus) multiplexer. These bits should be used in conjunction with the Rx and Tx IBO control registers within each of the framer units.

IBOMS1	IBOMS0	IBO Mode
0	0	IBO Mux Disabled
0	1	4.096MHz (2 per)
1	0	8.192MHz (4 per)
1	1	16.384MHz (8 per)

Register Name: GTCR2
Register Description: Global Framer Control Register 2
Register Address: 0F2H
Read/Write Function: R/W

7	6	5	4	3	2	1	0
--	--	--	--	--	LOSS	TSSYNCIOSEL	--
0	0	0	0	0	0	0	0

Bit 1 - Transmit System Synchronization I/0 Select (TSSYNCIOSEL)
If this bit is set to a 1, the TSSYNCIO is an 8kHz output synchronous to the BPCLK. This "frame pulse" can be used in conjunction with the backplane clock to provide IBO signals for a system backplane. If this bit is reset, TSSYNCIO is an input. An 8kHz frame pulse is required for Transmit Synchronization and IBO operation.

Bit 2 - LOS Selection
If this bit is set, the AL/RSIGF/FLOS pins can be driven with LIU Loss and if reset by Framer LOS. The selection of whether to drive AL/RSIGF/FLOS pins with LOS (analog or digital) or Signaling Freeze is controlled by GFCR bit 2. This selection affects all ports.

Register Name: GTCCR
Register Description: Global Transceiver Clock Control Register
Register Address: 0F3H
Read/Write Function: R/W

7	6	5	4	3	2	1	0
BPREFSEL3	BPREFSEL2	BPREFSEL1	BPREFSEL0	BFREQSEL	FREQSEL	MPS1	MPS0
0	0	0	0	0	0	0	0

Bit 1, 0 - Master Period Select 1, 0 (MPS[1:0])
In conjunction with the FREQSEL bit, these bits select the external MCLK frequency of the signal input at the MCLK pin of the DS26528. Consult the DS26528 data sheet for details.

Bit 2 - Frequency Selection (FREQSEL)
In conjunction with the MPS[1:0] bits, selects the external MCLK frequency of the signal input at the MCLK pin of the DS26528.
0 = The external master clock is 2.048MHz or multiple thereof.
1 = The external master clock is 1.544MHz or multiple thereof.

Bit 3 – Backplane Frequency Select
In conjunction with BPRFSEL[3:0], identifies the reference-clock frequency used by the DS26528 backplane clock-generation circuit. Note that the setting of this bit should match the T1/E1 selection for the LIU whose recovered clock is being used to generate the backplane clock.
0 = Backplane reference clock is 2.048MHz.
1 = Backplane reference clock is 1.544MHz.

Bit 7 to 4 - Backplane Clock Reference Selects (BPREFSEL[3:0])

These bits select which reference clock source will be used for BPCLK generation. The BPCLK can be generated from any of the LIU recovered clocks, an external reference, or derivatives of MCLK input. Consult DS26528 data sheet for details.

Register Name: GLSRR
Register Description: Global LIU Software Reset Register
Register Address: 0F5H
Read/Write Function: R/W

7	6	5	4	3	2	1	0
LSRST8	LSRST7	LSRST6	LSRST5	LSRST4	LSRST3	LSRST2	LSRST1
0	0	0	0	0	0	0	0

Bit 0 - Channel 1 LIU Software Reset (LSRST1)

LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.
0 = Normal Operation
1 = Reset LIU

Bit 1 - Channel 2 LIU Software Reset (LSRST2)

LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.
0 = Normal Operation
1 = Reset LIU.

Bit 2 - Channel 3 LIU Software Reset (LSRST3)

LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.
0 = Normal Operation
1 = Reset LIU

Bit 3 - Channel 4 LIU Software Reset (LSRST4)

LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.
0 = Normal Operation
1 = Reset LIU

Bit 4 - Channel 5 LIU Software Reset (LSRST5)

LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.
0 = Normal Operation
1 = Reset LIU

Bit 5 - Channel 6 LIU Software Reset (LSRST6)

LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.
0 = Normal Operation
1 = Reset LIU

Bit 6 - Channel 7 LIU Software Reset (LSRST7)

LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal Operation

1 = Reset LIU

Bit 7 - Channel 8 LIU Software Reset (LSRST8)

LIU logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal Operation

1 = Reset LIU

Register Name: GFSRR
Register Description: Global Framer and BERT Software Reset Register
Register Address: 0F6H
Read/Write Function: R/W

7	6	5	4	3	2	1	0
FSRST8	FSRST7	FSRST6	FSRST5	FSRST4	FSRST3	FSRST2	FSRST1
0	0	0	0	0	0	0	0

Bit 0 – Channel 1 Framer and BERT Software Reset (FSRST1)

Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal Operation

1 = Reset Framer and BERT

Bit 1 – Channel 2 Framer and BERT Software Reset (FSRST2)

Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal Operation

1 = Reset Framer and BERT

Bit 2 – Channel 3 Framer and BERT Software Reset (FSRST3)

Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal Operation

1 = Reset Framer and BERT

Bit 3 –Channel 4 Framer and BERT Software Reset (FSRST4)

Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal Operation

1 = Reset Framer and BERT

Bit 4 – Channel 5 Framer and BERT Software Reset (FSRST5)

Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal Operation

1 = Reset Framer and BERT

Bit 5 – Channel 6 Framer and BERT Software Reset (FSRST6)

Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal Operation

1 = Reset Framer and BERT

Bit 6 –Channel 7 Framer and BERT Software Reset (FSRST7)

Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal Operation

1 = Reset Framer and BERT

Bit 7 – Channel 8 Framer and BERT Software Reset (FSRST8)

Framer logic and registers are reset with a 0-to-1 transition in this bit. The reset is released when a zero is written to this bit.

0 = Normal Operation

1 = Reset Framer and BERT

Register Name: GBISR
Register Description: Global Burt Interrupt Status Register
Register Address: 0FAH
Read/Write Function: R

7	6	5	4	3	2	1	0
BIS8	BIS7	BIS6	BIS5	BIS4	BIS3	BIS2	BIS1
0	0	0	0	0	0	0	0

Bit 0 - BERT Interrupt Status 1

0 = BERT 1 has not issued an interrupt.

1 = BERT 1 has issued an interrupt.

Bit 1 - BERT Interrupt Status 2

0 = BERT 2 has not issued an interrupt.

1 = BERT 2 has issued an interrupt.

Bit 2 - BERT Interrupt Status 3

0 = BERT 3 has not issued an interrupt.

1 = BERT 3 has issued an interrupt.

Bit 3 - BERT Interrupt Status 4

0 = BERT 4 has not issued an interrupt.

1 = BERT 4 has issued an interrupt.

Bit 4 - BERT Interrupt Status 5

0 = BERT 5 has not issued an interrupt.

1 = BERT 5 has issued an interrupt.

Bit 5 - BERT Interrupt Status 6

0 = BERT 6 has not issued an interrupt.

1 = BERT 6 has issued an interrupt.

Bit 6 - BERT Interrupt Status 7

0 = BERT 7 has not issued an interrupt.
1 = BERT 7 has issued an interrupt.

Bit 7 - BERT Interrupt Status 8

0 = BERT 8 has not issued an interrupt.
1 = BERT 8 has issued an interrupt.

Register Name: **GLISR**
Register Description: **Global LIU Interrupt Status Register**
Register Address: **0FBH**
Read/Write Function: **R**

7	6	5	4	3	2	1	0
LIS8	LIS7	LIS6	LIS5	LIS4	LIS3	LIS2	LIS1
0	0	0	0	0	0	0	0

Bit 0 - LIU Interrupt Status 1

0 = LIU 1 has not issued an interrupt.
1 = LIU 1 has issued an interrupt.

Bit 1 - LIU Interrupt Status 2

0 = LIU 2 has not issued an interrupt.
1 = LIU 2 has issued an interrupt.

Bit 2 - LIU Interrupt Status 3

0 = LIU 3 has not issued an interrupt.
1 = LIU 3 has issued an interrupt.

Bit 3 - LIU Interrupt Status 4

0 = LIU 4 has not issued an interrupt.
1 = LIU 4 has issued an interrupt.

Bit 4 - LIU Interrupt Status 5

0 = LIU 5 has not issued an interrupt.
1 = LIU 5 has issued an interrupt.

Bit 5 - LIU Interrupt Status 6

0 = LIU 6 has not issued an interrupt.
1 = LIU 6 has issued an interrupt.

Bit 6 - LIU Interrupt Status 7

0 = LIU 7 has not issued an interrupt.
1 = LIU 7 has issued an interrupt.

Bit 7 - LIU Interrupt Status 8

0 = LIU 8 has not issued an interrupt.
1 = LIU 8 has issued an interrupt.

Register Name: GFIMR
Register Description: Global Framer Interrupt Mask Register
Register Address: 0FCH
Read/Write Function: R/W

7	6	5	4	3	2	1	0
FIM8	FIM 7	FIM 6	FIM 5	FIM 4	FIM 3	FIM 2	FIM 1
0	0	0	0	0	0	0	0

Bit 0 - Framer 1 Interrupt Mask (FIM1)
0 = Interrupt masked
1 = Interrupt enabled

Bit 1 - Framer 2 Interrupt Mask (FIM2)
0 = Interrupt masked
1 = Interrupt enabled

Bit 2 - Framer 3 Interrupt Mask (FIM3)
0 = Interrupt masked
1 = Interrupt enabled

Bit 3 - Framer 4 Interrupt Mask (FIM4)
0 = Interrupt masked
1 = Interrupt enabled

Bit 4 - Framer 5 Interrupt Mask (FIM5)
0 = Interrupt masked
1 = Interrupt enabled

Bit 5 - Framer 6 Interrupt Mask (FIM6)
0 = Interrupt masked
1 = Interrupt enabled

Bit 6 - Framer 7 Interrupt Mask (FIM7)
0 = Interrupt masked
1 = Interrupt enabled

Bit 7 - Framer 8 Interrupt Mask (FIM8)
0 = Interrupt masked
1 = Interrupt enabled

Register Name: GBIMR
Register Description: Global Burt Interrupt Mask Register
Register Address: 0FDH
Read/Write Function: R/W

7	6	5	4	3	2	1	0
BIM8	BIM 7	BIM 6	BIM 5	BIM 4	BIM 3	BIM 2	BIM 1
0	0	0	0	0	0	0	0

Bit 0 - BERT Interrupt Mask 1
0 = Interrupt masked
1 = Interrupt enabled

Bit 1 - BERT Interrupt Mask 2
0 = Interrupt masked
1 = Interrupt enabled

Bit 2 - BERT Interrupt Mask 3
0 = Interrupt masked
1 = Interrupt enabled

Bit 3 - BERT Interrupt Mask 4
0 = Interrupt masked
1 = Interrupt enabled

Bit 4 - BERT Interrupt Mask 5
0 = Interrupt masked
1 = Interrupt enabled

Bit 5 - BERT Interrupt Mask 6
0 = Interrupt masked
1 = Interrupt enabled

Bit 6 - BERT Interrupt Mask 7
0 = Interrupt masked
1 = Interrupt enabled

Bit 7 - BERT Interrupt Mask 8
0 = Interrupt masked
1 = Interrupt enabled

Register Name: GLIMR
Register Description: Global LIU Interrupt Mask Register
Register Address: 0FEH
Read/Write Function: R/W

7	6	5	4	3	2	1	0
LIM8	LIM 7	LIM 6	LIM 5	LIM 4	LIM 3	LIM 2	LIM 1
0	0	0	0	0	0	0	0

Bit 0 – LIU Interrupt Mask 1
0 = Interrupt masked
1 = Interrupt enabled

Bit 1 – LIU Interrupt Mask 2
0 = Interrupt masked
1 = Interrupt enabled

Bit 2 – LIU Interrupt Mask 3
0 = Interrupt masked
1 = Interrupt enabled

Bit 3 – LIU Interrupt Mask 4
0 = Interrupt masked
1 = Interrupt enabled

Bit 4 – LIU Interrupt Mask 5
0 = Interrupt masked
1 = Interrupt enabled

Bit 5 – LIU Interrupt Mask 6
0 = Interrupt masked
1 = Interrupt enabled

Bit 6 – LIU Interrupt Mask 7
0 = Interrupt masked
1 = Interrupt enabled

Bit 7 – LIU Interrupt Mask 8
0 = Interrupt masked
1 = Interrupt enabled

Register Name: T1RCR2
Register Description: Receive Control Register 2
Register Address: 014H + (200h x n), where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
--	--	--	RSLC96	OOF2	OOF1	RAIIE	RD4RM
0	0	0	0	0	0	0	0

Bit 1 - Receive RAI Integration Enable (RAIIE)

The ESF RAI indication can be interrupted for a period not to exceed 100ms per interruption (T1.403). In ESF mode, setting RAIIE will cause the RAI status from the DS26528 to be integrated for 200ms.

0 = RAI detects when 16 consecutive patterns of 00FF appear in the FDL.
RAI clears when 14 or less patterns of 00FF hex out of 16 possible appear in the FDL

1 = RAI detects when the condition has been present for greater than 200ms.
RAI clears when the condition has been absent for greater than 200ms.

Register Name: RCR3
Register Description: Receive Control Register 3
Register Address: 083H + (200h x n): where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
IDF	--	RSERC	--	--	--	PLB	FLB
0	0	0	0	0	0	0	0

Bit 7 - Input Data Format (IDF)

0 = Bipolar data is expected at RPOS and RNEG (either AMI or B8ZS).

1 = NRZ data is expected at RPOS. The BPV counter will be disabled and RNEG will be ignored by the DS26528.

Register Name: RRTS1
Register Description: Receive Real Time Status Register 1
Register Address: 0B0H + (200h x n): where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
--	--	--	--	RRAI	RAIS	RLOS	RLOF
0	0	0	0	0	0	0	0

Bit 0 - Receive Loss of Frame Condition (RLOF)

Set when the DS26528 is not synchronized to the received data stream.

Bit 1 - Receive Loss of Signal Condition (RLOS)

Set when 255 (or 2048 if RCR2.0 = 1) consecutive zeros have been detected at RPOS and RNEG.

Bit 2 - Receive Alarm Indication Signal Condition (RAIS)

Set when an unframed all ones code is received at RPOS and RNEG.

Bit 3 - Receive Remote Alarm Indication Condition (RRAI)

Set when a remote alarm is received at RPOS and RNEG.

Register Name: RRTS3 -T1 Mode
Register Description: Receive Real Time Status Register 3
Register Address: 0B2H + (200h x n), where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
--	--	--	--	LORC	LSP	LDN	LUP
0	0	0	0	0	0	0	0

Bit 0 - (T1 MODE) Loop Up Code Detected Condition (LUP)
Set when the loop up code, as defined in the RUPCD1/2 register, is being received.

(E1 MODE) Receive Distant MF Alarm Condition (RDMA)
Set when bit-6 of timeslot 16 in frame 0 has been set for two consecutive multiframes. This alarm is not disabled in the CCS signaling mode.

Bit 1 - (T1 MODE) Loop Down Code Detected Condition (LDN)
Set when the loop down code, as defined in the RDNCD1/2 register, is being received.

(E1 MODE) V5.2 Link Detected Condition (V52LNK)
Set on detection of a V5.2 link identification signal (G.965).

Bit 2 - Spare Code Detected Condition (LSP)
Set when the spare code, as defined in the RSCD1/2 registers, is being received.

Bit 3 - Loss of Receive Clock Condition (LORC)
Set when the RCLK pin has not transitioned for one channel time.

Register Name: RLS4
Register Description: Receive Latched Status Register 4
Register Address: 093H + (200h x n): where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
RESF	RESEM	RSLIP	--	RSCOS	1SEC	TIMER	RMF
0	0	0	0	0	0	0	0

RLS4.2 - One Second Timer (1SEC)
Set every 1 second based on RCLK.

Register Name: RLS7 – T1 Mode
Register Description: Receive Latched Status Register 7
Register Address: 096H + (200h x n): where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
--	--	RRAI-CI	RAIS-CI	RSLC96	RFDLF	BC	BD
0	0	0	0	0	0	0	0

Bit 3 - Receive SLC-96 Alignment Event (RSLC96)

Set when a valid SLC-96 alignment pattern is detected in the Fs bit stream, and the RSLCx registers have data available for retrieval. (Section 11.12)

Bit 5 - Receive RAI-CI Detect (RRAI-CI)

Set when an RAI-CI pattern has been detected by the receiver (Section 11.5.1). This bit is active in ESF framing mode only, and will set only if an RAI condition is being detected (RRTS1.3). When the host reads (and clears) this bit, it will set again each time the RAI-CI pattern is detected (approximately every 1.1 seconds).

Register Name: ERCNT
Register Description: Error Counter Configuration Register
Register Address: 086H + (200h x n): where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
1SECS	MCUS	MECU	ECUS	EAMS	FSBE	MOSCRF	LCVCRF
0	0	0	0	0	0	0	0

Bit 6 - Manual Counter Update Select (MCUS)

When manual update mode is enabled with EAMS, this bit can be used to allow the GLCE bit in GCR1 to latch all counters. Useful for synchronously latching counters of multiple framers.
0 = MECU is used to manually latch counters.
1 = GLCE is used to manually latch counters.

Bit 7 - One Second Select (1SECS)

When timed update is enabled by EAMS, setting this bit for a specific framer will allow that framer's counters to latch on the 1 second reference from framer #1. Note that this bit should always be clear for framer #1.
0 = Use internally generated 1 second timer.
1 = Use 1 second timer from framer #1.

Register Name: RESCR
Register Description: Receive Elastic Store Control Register
Register Address: 085H + (200h x n): where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
RDATFMT	RGCLKEN	-	RSZS	RESALGN	RESR	RESMDM	RESE
0	0	0	0	0	0	0	0

Bit 4 - Receive Slip Zone Select (RSZS)

This bit determines the minimum distance allowed between the elastic-store read and write pointers before forcing a controlled slip. This bit is only applies during T1 to E1, or E1 to T1 conversion applications.

0 = force a slip at 9 bytes or less of separation (used for clustered blank channels).

1 = force a slip at 2 bytes or less of separation (used for distributed blank channels).

Register Name: T1RBOCC
Register Description: Receive BOC Control Register
Register Address: 015H + (200h x n), where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
RBR	--	RBD1	RBD0	--	RBF1	RBF0	-
0	0	0	0	0	0	0	0

Bit 5, 4 - Receive BOC Disintegration bits (RBD[1:0])

The BOC Disintegration filter sets the number of message bits that must be received without a valid BOC in order to set the BC bit indicating that a valid BOC is no longer being received.

RBD1	RBD0	Consecutive Message Bits for BOC Clear Identification
0	0	16
0	1	32
1	0	48
1	1	64

Register Name: TCR3
Register Description: Transmit Control Register 3
Register Address: 183H + (200h x n), where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
ODF	ODM	TCSS1	TCSS0	MFRS	TFM	IBPV	TLOOP
0	0	0	0	0	0	0	0

Bit 1 - Insert BPV (IBPV)

A 0 to 1 transition on this bit will cause a single bipolar violation (BPV) to be inserted into the transmit data stream. Once this bit has been toggled from a 0 to a 1, the device waits for the next occurrence of three consecutive ones to insert the BPV. This bit must be cleared and set again for a subsequent error to be inserted.

Register Name: TIOCR
Register Description: Transmit I/O Configuration Register
Register Address: 184H + (200h x n): where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
TCLKINV	TSYNCINV	TSSYNCINV	TSCLKM	TSSM	TSIO	TSDW	TSM
0	0	0	0	0	0	0	0

Bit 3 - TSSYNC Mode Select (TSSM)

Selects frame or multiframe mode for the TSSYNC pin.
0 = frame mode
1 = multiframe mode

Register Name: TLS1
Register Description: Transmit Latched Status Register
Register Address: 190 + (200h x n), where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
TESF	TESEM	TSLIP	TSLC96	TPDV	TMF	LOTCC	LOTC
0	0	0	0	0	0	0	0

Bit 4 – (T1 Mode Only) Transmit SLC96 Multiframe Event (TSLC96)

When enabled by TCR2.6, this bit will set once per SLC96 multiframe (72 frames) to alert the host that new data may be written to the TSLC1-TSLC3 registers.

Register Name: TESCR
Register Description: Transmit Elastic Store Control Register
Register Address: 185H + (200h x n), where n = 0 to 7, for ports 1 to 8

7	6	5	4	3	2	1	0
TDATFMT	TGCLKEN	--	TSZS	TESALGN	TESR	TESMDM	TESE
0	0	0	0	0	0	0	0

Bit 4 - Transmit Slip Zone Select (TSZS)

This bit determines the minimum distance allowed between the elastic-store read and write pointers before forcing a controlled slip. This bit only affects the elastic stores when used in T1 to E1, or E1 to T1 conversion applications.
0 = force a slip at 9 bytes or less of separation (used for clustered blank channels).
1 = force a slip at 2 bytes or less of separation (used for distributed blank channels.

9. Conclusion

This application note shows the differences between the DS26528 and the DS21458 transceivers. It includes the terminology, the register mapping, and the features exclusive to the DS26528.

If you have further questions about our T1/E1 products, please contact the Telecommunication Applications support team.