User's Guide
SBAU331–May 2019

BP-ADS7128 BoosterPack™ Plug-In Module

The ADS7128 BoosterPack™ plug-in module (BP-ADS7128) allows users to evaluate the functionality of Texas Instruments' ADS7128 low power, eight-channel programmable successive approximation register (SAR) analog-to-digital converter(ADC). This user's guide describes both the hardware platform showcasing the ADS7128 device and the graphical user interface (GUI) software used to configure the various modes of operation of this device.

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1 Introduction

The ADS7128 BoosterPack™ is a fully-assembled evaluation platform designed to highlight the ADS7128 features and various modes of operations that make this device suitable for ultra-low-power, small-size sensor monitor applications.

The accompanying MSP432E401Y LaunchPad™ development kit (MSP-EXP432E401Y) is used as a USB-to-PC GUI communication bridge. This kit also serves as an example implementation of a master microcontroller (MCU) to communicate with the ADS7128 through an I^2C interface.

NOTE: The BP-ADS7128 requires an external master controller to evaluate the ADS7128.

The MSP-EXP432E401Y is controlled by commands received from the ADS7128 GUI, and returns data to the GUI for display and analysis. If the MSP-EXP432E401Y is not used, the BoosterPack™ plug-in module format of the BP-ADS7128 board allows for an alternative external host to communicate with the ADS7128.

The BP-ADS7128 incorporates all required circuitry and components with the following features:

- ADS7128 low-power, ultra-small, eight-channel sensor monitor with I^2C interface and alert output
- External power-supply connection available to provide 3.3 V to power the ADS7128 DVDD supply instead of the universal serial bus (USB) power from the MSP432E401Y LaunchPad™
- Optional adjustable linear regulator, TI's TPS78001, to generate stable output voltage to power the ADS7128 AVDD and DVDD pins when using the 5-V USB power from the MSP432E401Y LaunchPad™
- I^2C interface for communication and configuration of modes available on the ADS7128

Figure 1 shows the ADS7128EVM architecture, identifying the key components and blocks previously listed.

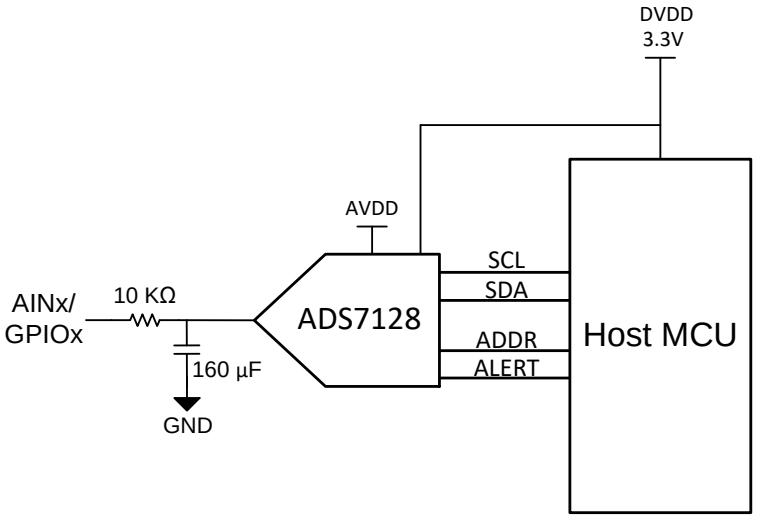

Figure 1. ADS7128EVM Block Diagram

2 BP-ADS7128EVM Overview

This section describes various onboard components that are used to interface the analog input, general-purpose inputs/outputs (GPIOs), digital interface, and provide power supply to the BP-ADS7128. Figure 2 shows a BP-ADS7128 overview.

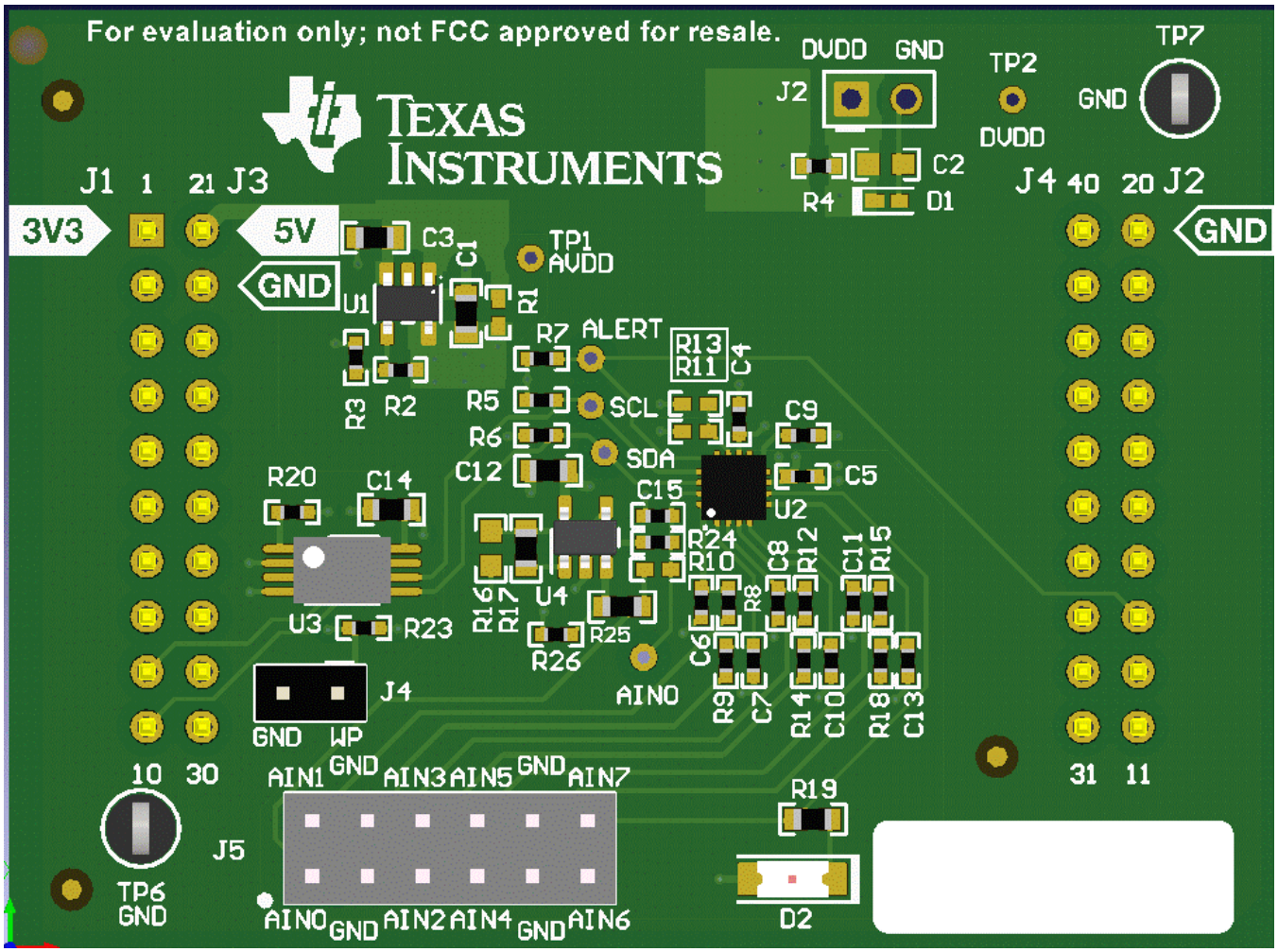

Figure 2. BP-ADS7128 Top Level Overview

2.1 Connector for Channels

The BP-ADS7128 is designed for easy interface to an external, analog single-ended source, or to GPIOs through a 100-mil header. Connector J5 provides a connection to the device channels. Table 1 lists the channel connections. The ADS7128 channel AIN0 has a buffered operational amplifier, TLV9061, to drive the analog input. Channels AIN1 through AIN6 have a resistor and capacitor filter circuit to condition the analog input. GPIO7 does not have a resistor and capacitor filter used for the single-ended analog input; instead, GPIO7 has a resistor and light-emitting diode (LED) to visibly demonstrate and monitor the channel state.

Table 1. Channel Connections

J5 Connector Pin	Description
J5:1	Single-ended analog input with buffer or GPIO for channel 0 of the ADC
J5:2	Single-ended analog input or GPIO for channel 1 of the ADC
J5:5	Single-ended analog input or GPIO for channel 2 of the ADC
J5:6	Single-ended analog input or GPIO for channel 3 of the ADC
J5:7	Single-ended analog input or GPIO for channel 4 of the ADC
J5:8	Single-ended analog input or GPIO for channel 5 of the ADC
J5:11	Single-ended analog input or GPIO for channel 6 of the ADC
J5:12	Single-ended analog input or LED GPIO for channel 7 of the ADC
J5:3 and J5:4; J5:9 and J5:10	BoosterPack™ ground

2.2 Digital Interface

As noted in Section 1, the BP-ADS7128 interfaces with the MSP-EXP432E401Y LaunchPad™, which in turn communicates with the computer over the USB. The two devices on the booster pack that the MSP432E401Y communicates over I^2C are the ADS7128 ADC and the electrically erasable programmable read-only memory (EEPROM). The EEPROM comes preprogrammed with the information required to configure and initialize the BP-ADS7128 platform. Once the hardware is initialized, the EEPROM is no longer used.

2.3 ADS7128 LaunchPad™ Interface

The BP-ADS7128 supports the I^2C digital interface and functional modes as detailed in the ADS7128 device datasheet. The MSP432E401Y LaunchPad™ is capable of operating at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC.

2.4 Power Supplies

The device supports a wide range of operation on its analog supply. The AVDD can operate from 2.35 V to 5.5 V. The DVDD operates from 1.65 V to 5.5 V, independent of the AVDD supply. The 3.3-V voltage regulator available on the MSP-EXP432E401Y is used to supply 3.3 V to DVDD and to AVDD through a low-dropout (LDO) regulator, the TPS78001, on the BP-ADS7128. There is an onboard option to use an external power supply for DVDD.

3 BP-ADS7128 EVM Initial Setup

3.1 Installing ADS7128 GUI Online and TI Cloud Agent Application Installation

The following steps describe the ADS7128 GUI software installation:

1. On the BP-ADS7128 BoosterPack™ plug-in module site, click on the link under *Software* to connect to the installer. Connecting to the installer may require you to login to your user account privileges to use the online version and to install the available applications.
2. Click on the BP-ADS7128 GUI icon. As shown in Figure 3, first-time users may be prompted to download and install the browser extension for Firefox™ or Chrome™ and the TI Cloud Agent Application.

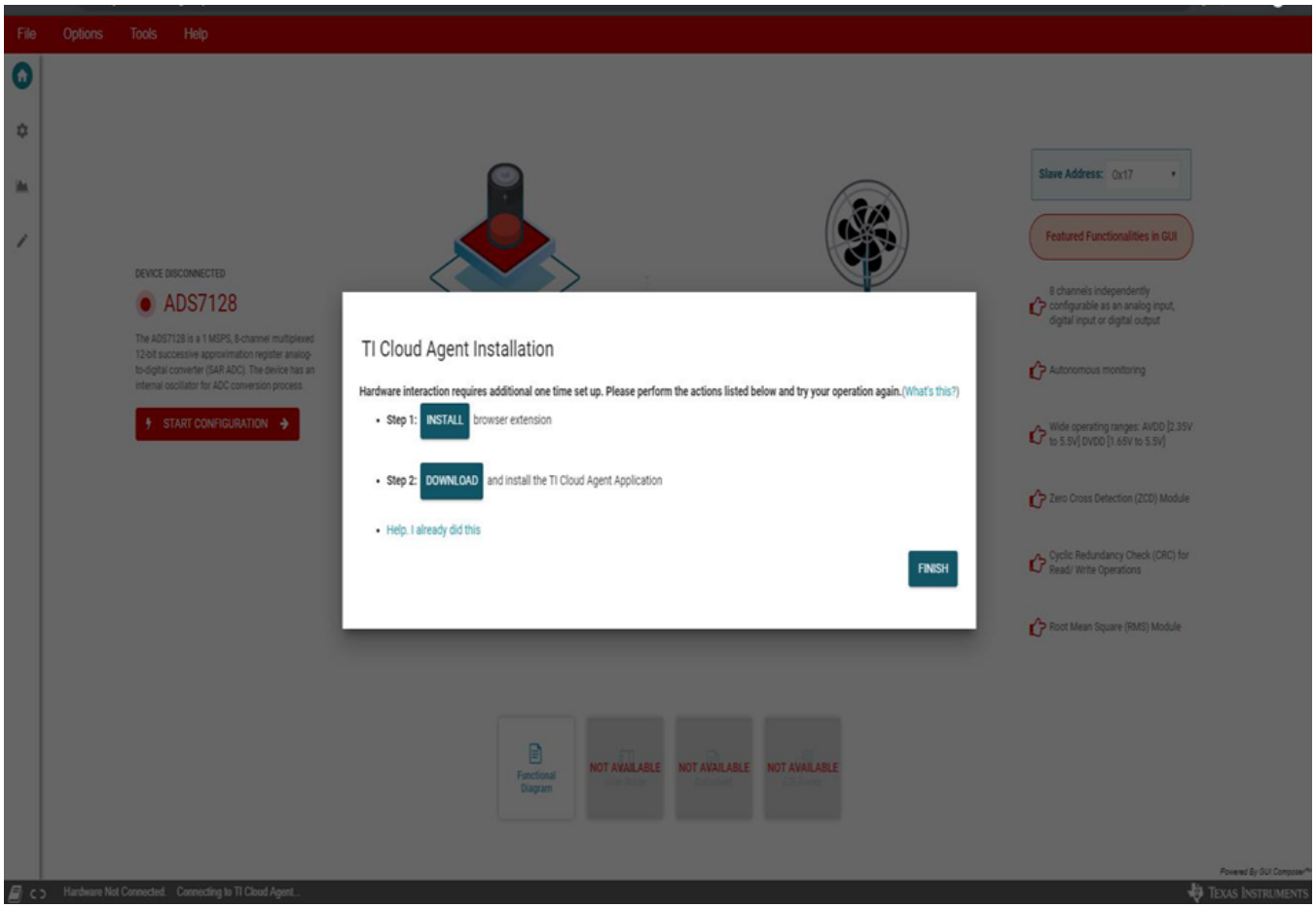

Figure 3. Browser Extension and TI Cloud Agent Installation

3.2 UNIFLASH Programmer for MSP-EXP432E401Y Software Programming

The MSP432E401Y LaunchPad™ ships with a default firmware program flashed on its memory. When a LaunchPad™ is connected to the PC for the first time, its firmware must be updated for communications with the BP-ADS7128. The following steps describe how to program this firmware on the flash memory:

1. On the MSP432E401Y LaunchPad™, remove jumper JP6 from its default position and place this jumper on the JP1 jumper, as shown in Figure 4, at location 5V-OTG.

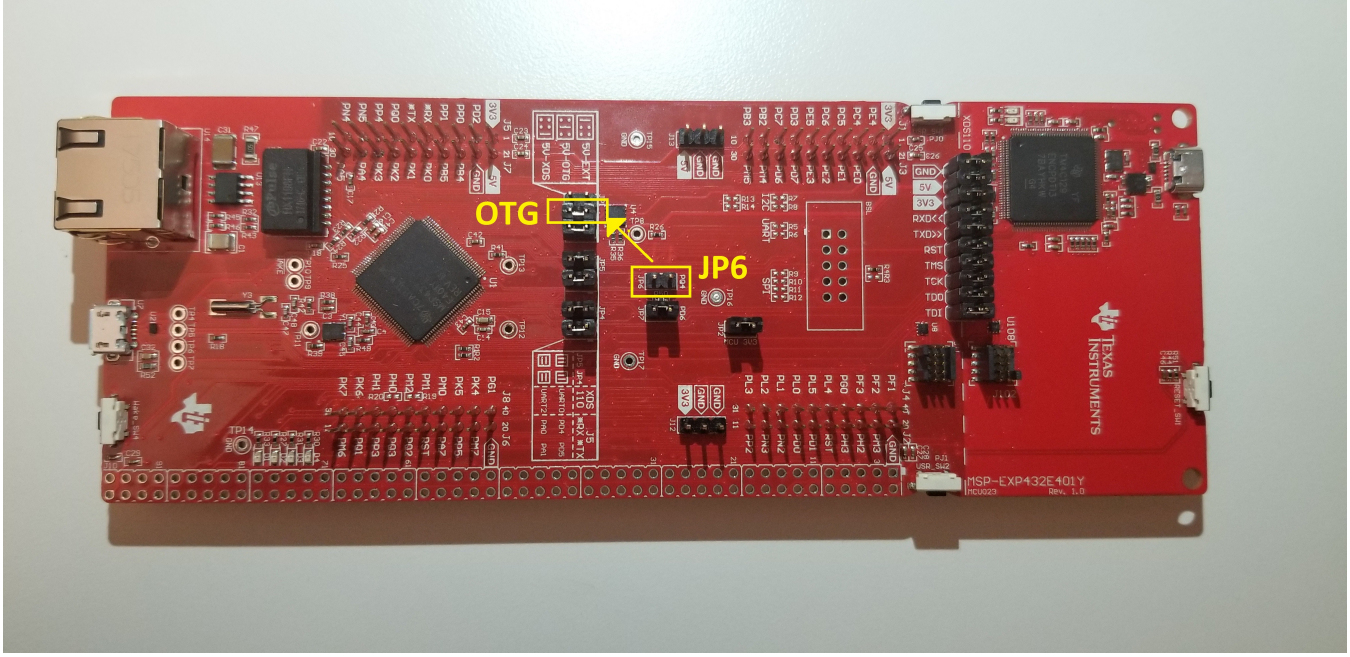

Figure 4. MSP432E401Y LaunchPad™ 5V-OTG Jumper

2. Connect the MSP432E401Y LaunchPad™ debug port connector, as shown in Figure 5, to an available USB port on the PC.

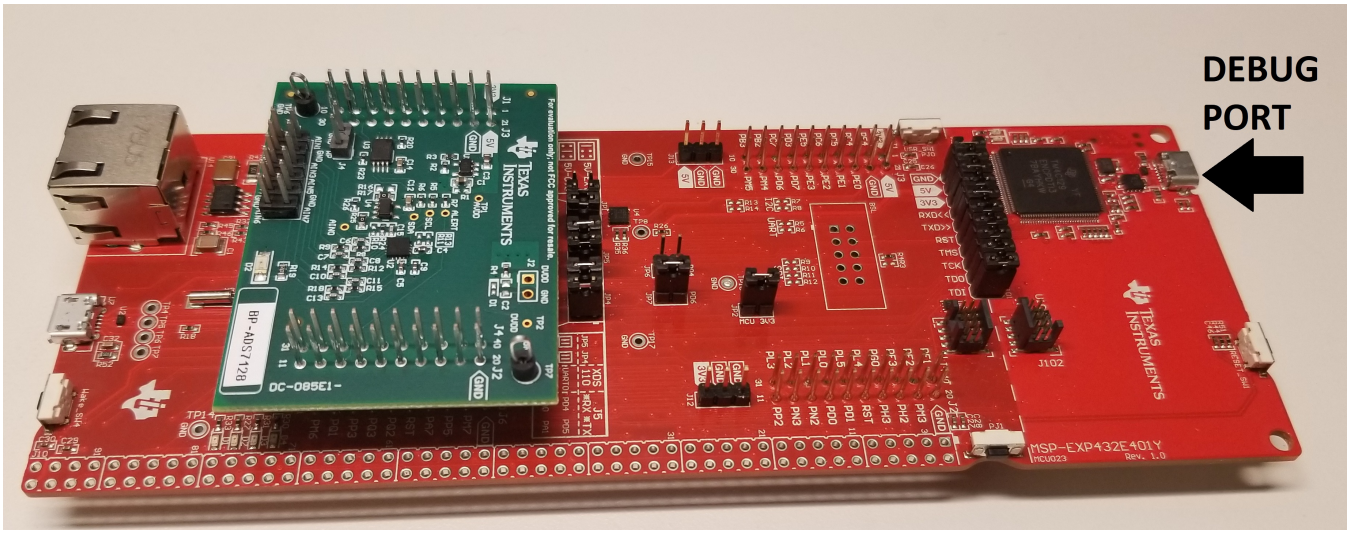

Figure 5. LaunchPad™ Debug Port

3. As shown in Figure 6, after the BP-ADS7128 GUI has been set up, select *Program Device* from the *File* menu option. This selection automatically recognizes the MSP432E401Y LaunchPad™ and FLASH program, see Figure 7, to communicate with the BP-ADS7128.

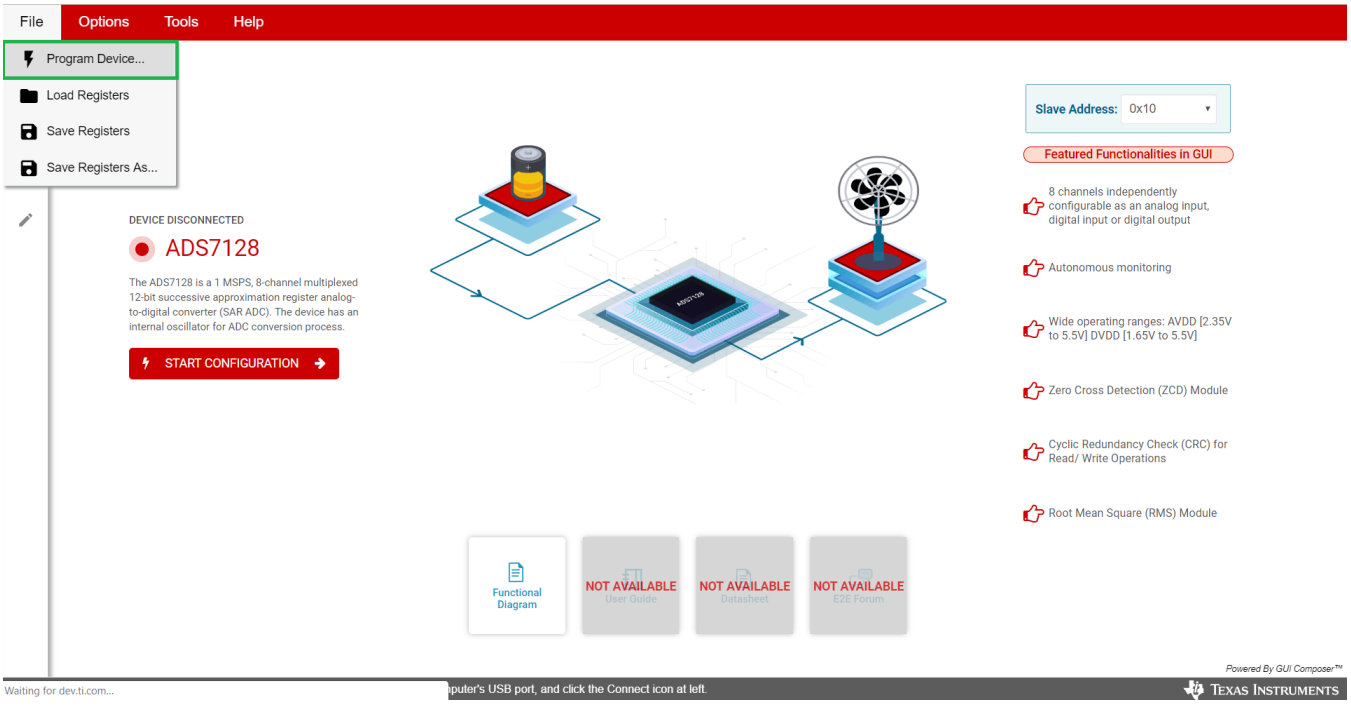

Figure 6. UNIFLASH Programming Set-Up

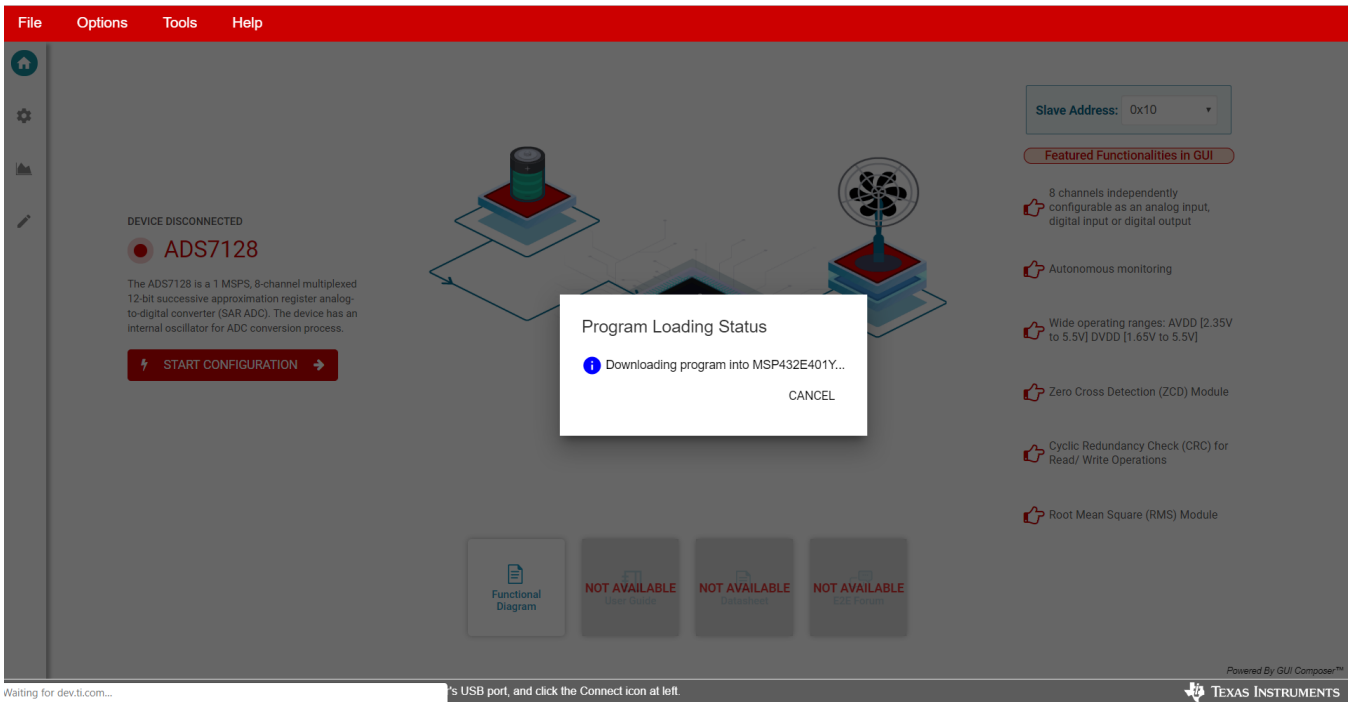

Figure 7. FLASH Programming LaunchPad™

4. After programming and verification is successful, as shown in Figure 8, disconnect the USB from the MSP-EXP432E401Y debug port.

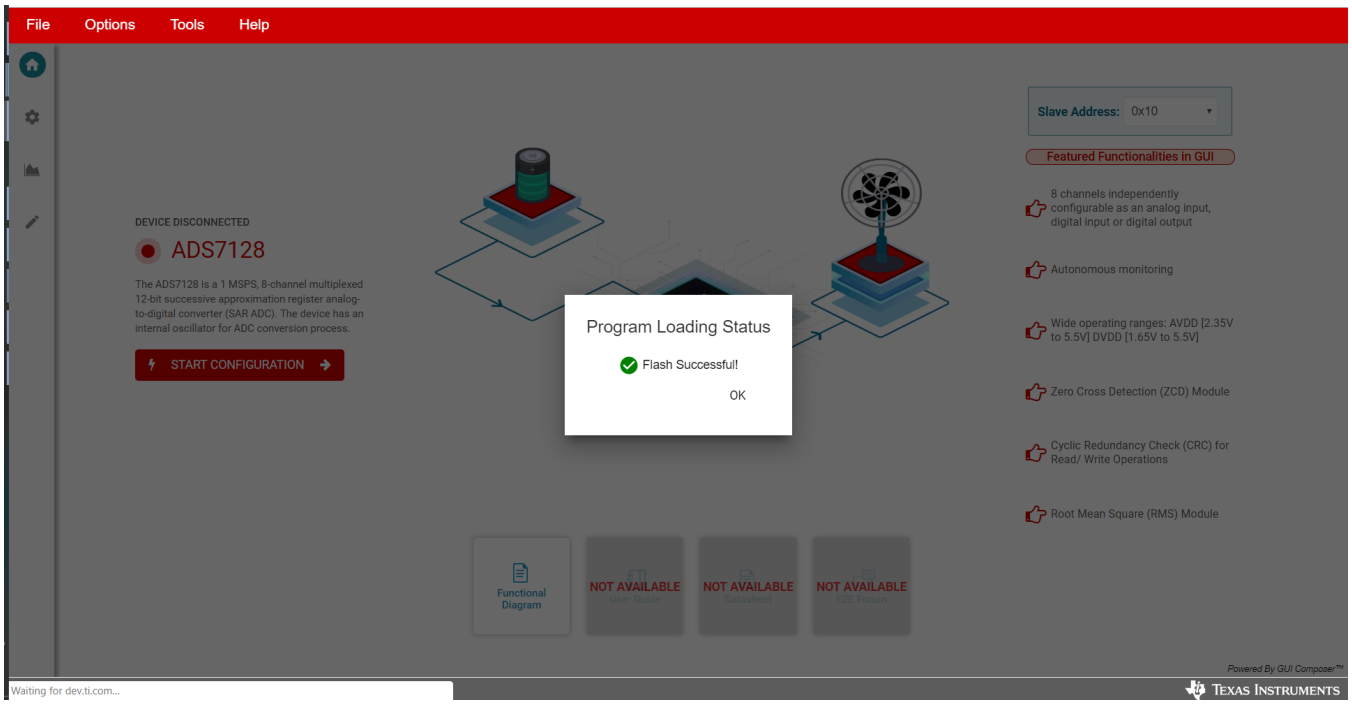

Figure 8. Successful FLASH Program

3.2.1 BoosterPack™ Plug-In Hardware Setup Instructions

Following are the instructions to set up the BP-ADS7128 for evaluation:

1. Stack the BP-ADS7128 on the MSP432E401Y LaunchPad™ MSP-EXP432E401Y. Make sure the 20-pin connector (J1, J3) on the BP-ADS7128 is mapped to connector (J5, J7) and that connector (J4, J2) on the BP-ADS7128 is mapped to connector (J8, J6) on the MSP-EXP432E401Y. The silk screen on the BP-ADS7128 must match with the MSP-EXP432E401Y.
2. Connect the MSP-EXP432E401Y micro USB data port to an available USB port on the PC. Figure 9 shows the assembled BP-ADS7128 and MSP-EXP432E401Y configuration.

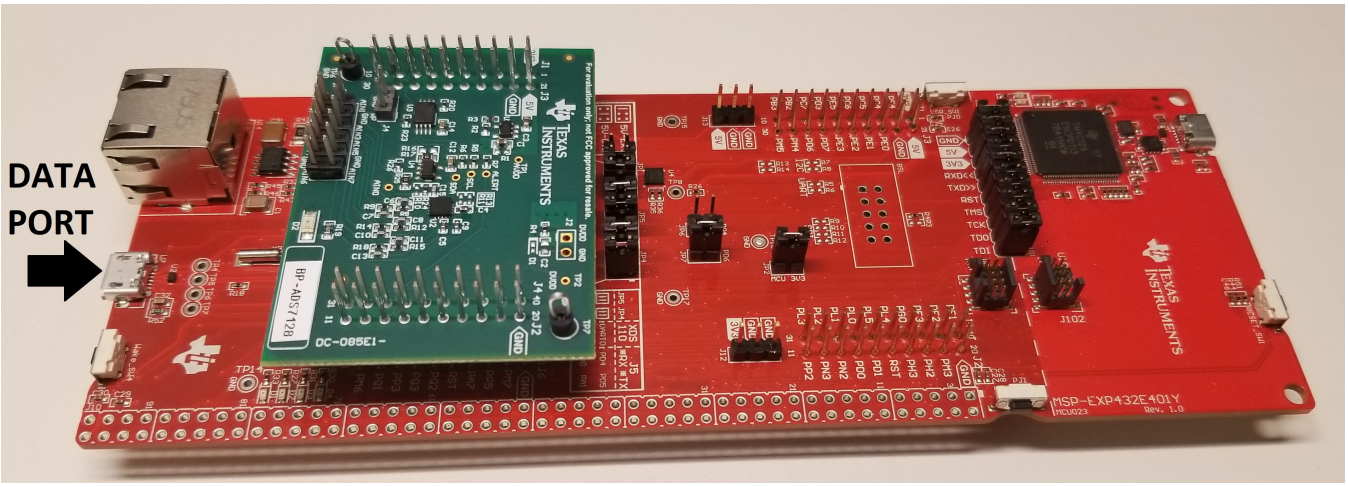

Figure 9. BP-ADS7128 Stacked on the MSP432E401Y LaunchPad™

3.3 ADS7128 GUI Description

3.3.1 Description

Figure 10 shows the landing page of the ADS7128 GUI. This page provides a high-level overview of the ADS7128 device. The left corner shows the tabs to navigate through the GUI: home, function configurations, data capture, and register map. When the BP-ADS7128 is stacked on the MSP432E401Y and connected to the PC via the micro USB cable, the GUI detects the BoosterPack™ module by reading the onboard EEPROM. When detected and connected, the GUI indicates this status as *connected*. At the bottom left corner of the GUI, there is an option to connect and disconnect the hardware from the GUI.

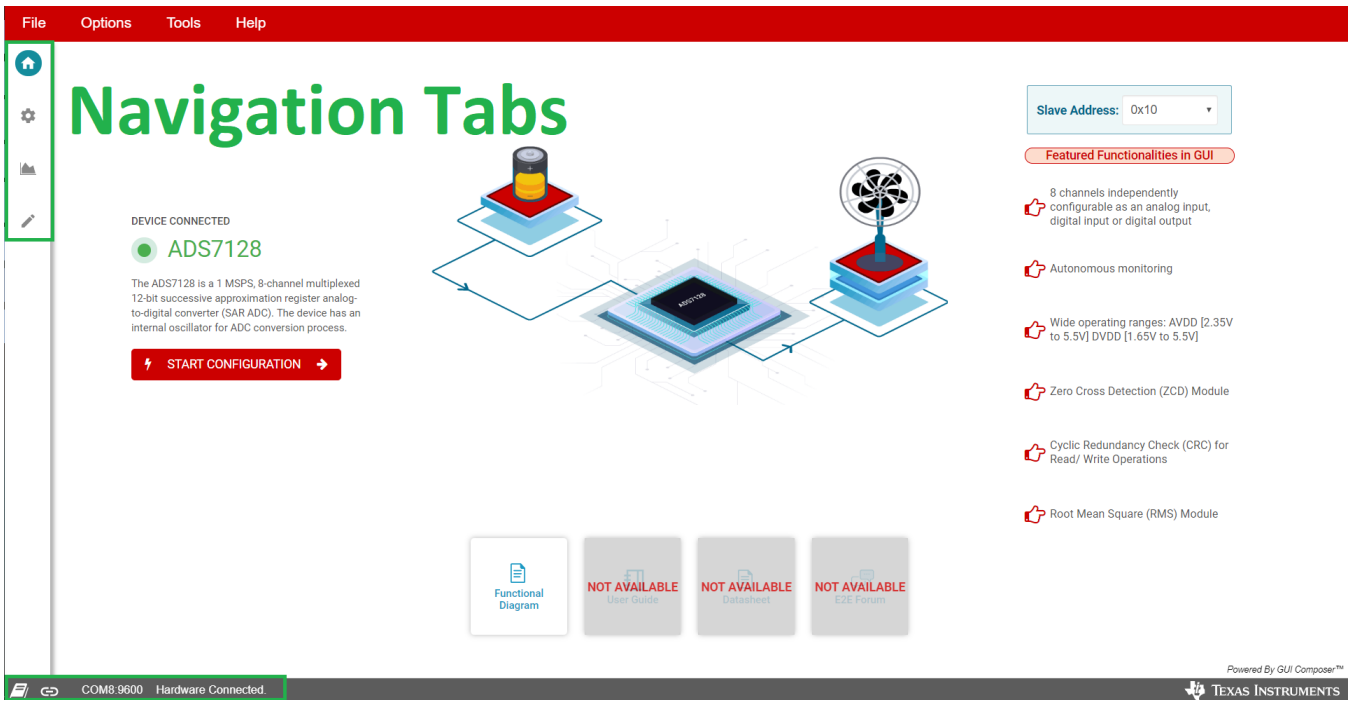

Figure 10. ADS7128 GUI Landing Page

3.3.2 Functional Configuration Tab

As shown in Figure 11, the ADS7128 device configuration tab has two sections. The left-most section lists the multiple functions the user can configure. These options enable the user to navigate through the various functions of the ADS7128. The right-most section displays the configuration options for each function.

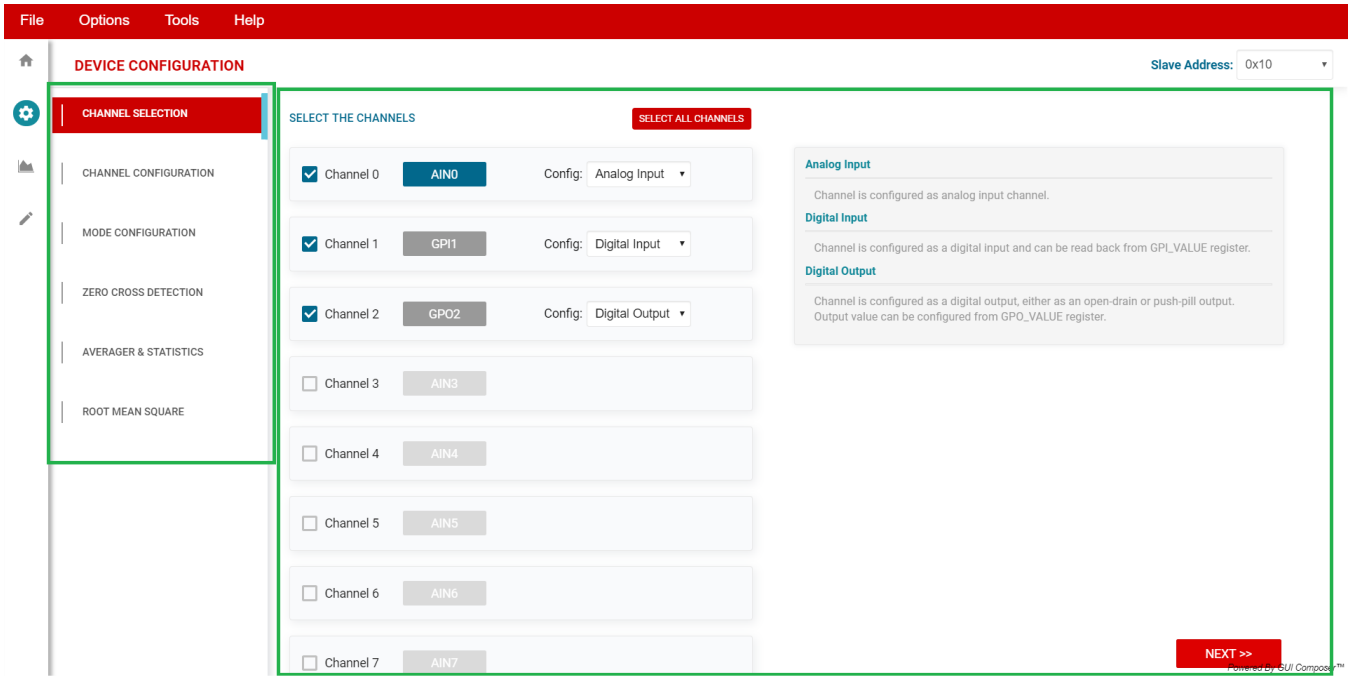

Figure 11. ADS7128 Device Configuration Tab

3.3.2.1 Channel Selection

This page selects channels and functionality. Each channel can be enabled or disabled, and configured as an analog input (default), digital input, or digital output. On the top right corner is an option to enable all ADC channels as analog input channels. TI recommends enabling this option to then disable the preferred ADC channels and configure the selected channels based on user preference.

3.3.2.2 Channel Configuration

This page sets channel-specific configurations, and consist of two tabs:

- Input channels tab: All selected input channels, analog or digital, can be configured
- Output channels tab: The selected digital output channels can be configured

For example, the first three channels were previously selected in the *Channel Selection* page as an analog input, digital input, and digital output, respectively. The *Channel Configuration* page then automatically updates to reflect the selected channel options.

3.3.2.2.1 Input Channels

Continuing with the example, both analog and digital inputs are displayed, as shown in Figure 12, in the *Input Channels* tab. Analog channels are listed on top, digital channels are listed below. The available configuration options are displayed for each type of input.

Any analog input channel can be selected to trigger the ALERT pin when the set high or low threshold code entered is crossed. Hysteresis can also be configured.

Any digital input channel can be selected to trigger the ALERT pin when the selected state change occurs.

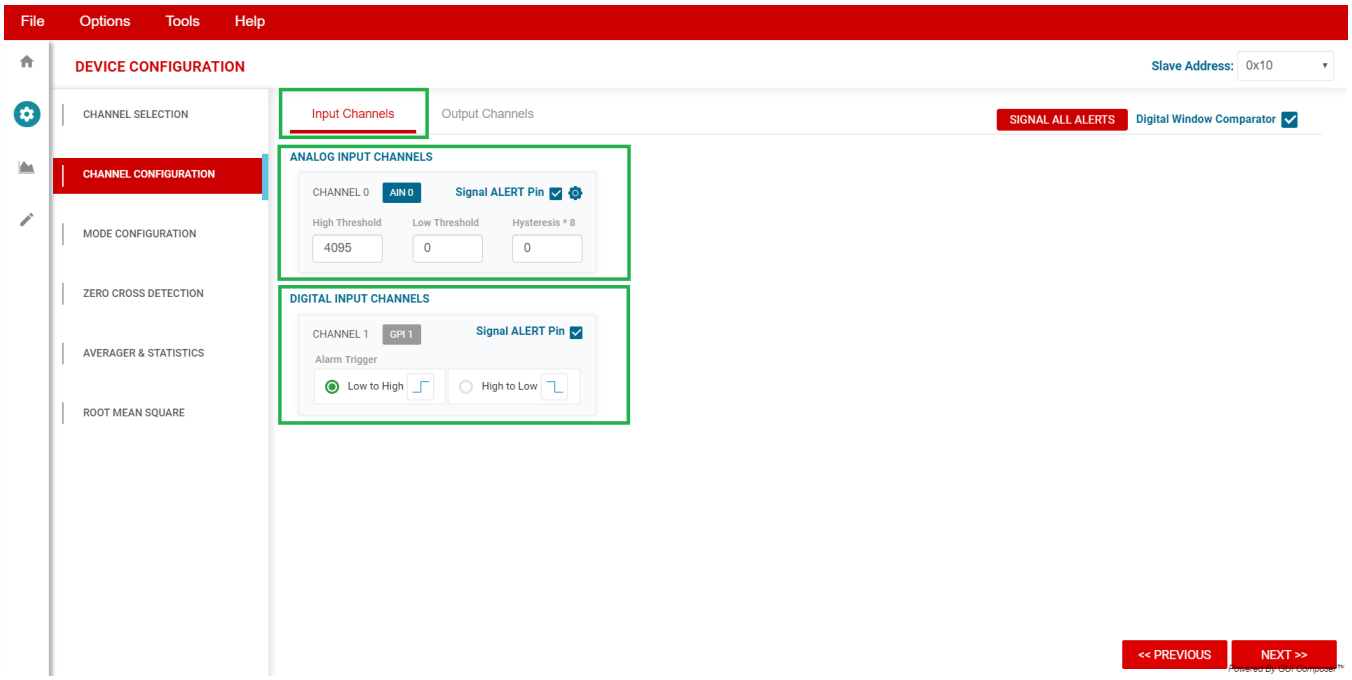

Figure 12. Channel Configuration Page, Input Channel Tab

3.3.2.2.2 Output Channels

The output channels tab also auto-updates to display the selected digital output channels in the *Channel Selection* page. In this example, only channel 2 was selected as a digital output. In this tab, the digital output channels can be selected as open-drain (default) or changed to push-pull. Figure 13 shows the zero-cross detection (ZCD) and trigger logic. This tab visually represents the logic within the device, and allows the user to enable ZCD, and select the input channels as a trigger.

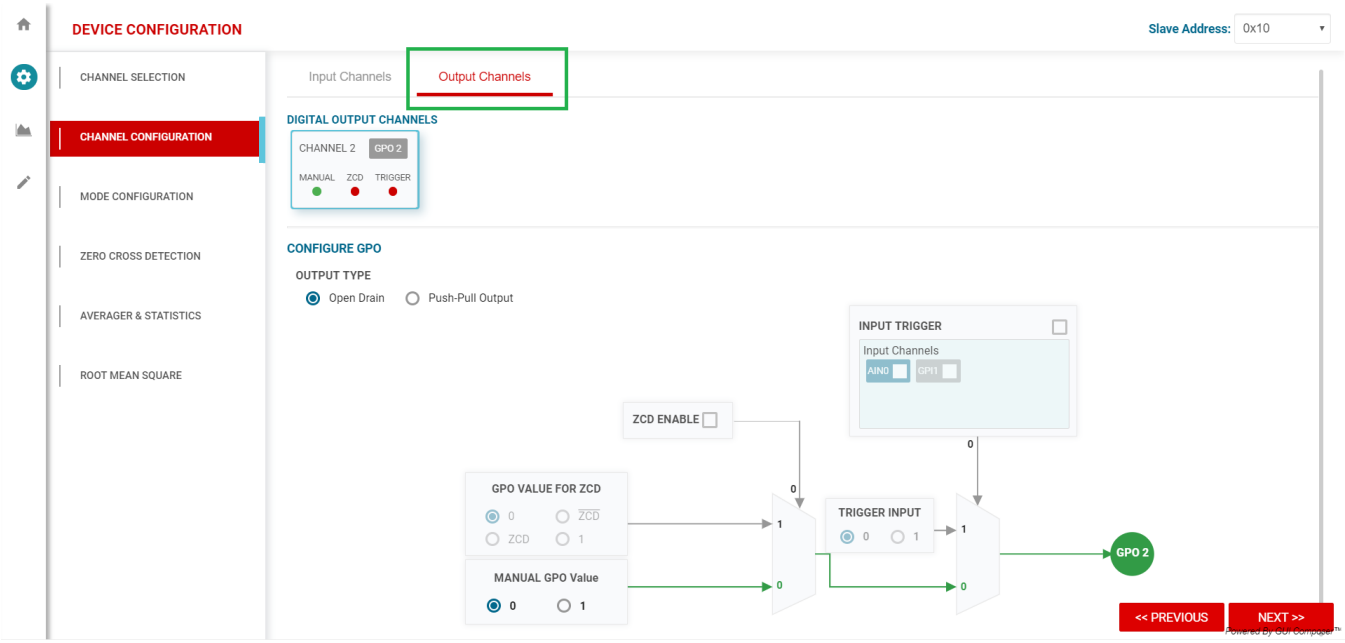

Figure 13. Channel Configuration Page, Output Channels Tab

3.3.2.2.3 Sampling Mode Configuration

The ADS7128 can operate in three sampling modes. The mode configuration tab (Figure 14) allows the user to select the device mode of operation.

The ADS7128 device has the following sampling modes:

- **Manual Mode:** Allows the external host processor to directly request and control when the data are sampled. The host provides I^2C frames to control conversions and the captured data are returned over the I^2C bus after each conversion.
- **Auto-Sequence Mode:** The host can configure the device to scan through the enabled analog input channels. The host must provide continuous clocks (SCL) to the device to scan through the channels and to read the data from the device. The mux automatically switches through the predetermined channel sequence, and the data conversion results are sent through the data bus.
- **Autonomous Mode:** After receiving the first start of conversion pulse from the host, the ADS7128 device then generates the subsequent start of conversion signals autonomously. The device features an internal oscillator to generate the start of ADC conversion pulses without the host controlling the conversions. Output data are not returned over the digital bus; only a signal on the ALERT pin is generated when an input signal crosses the programmable high or low threshold values.

The device powers up in manual mode and can be configured into any of the functional modes by writing the configuration registers for the desired mode.

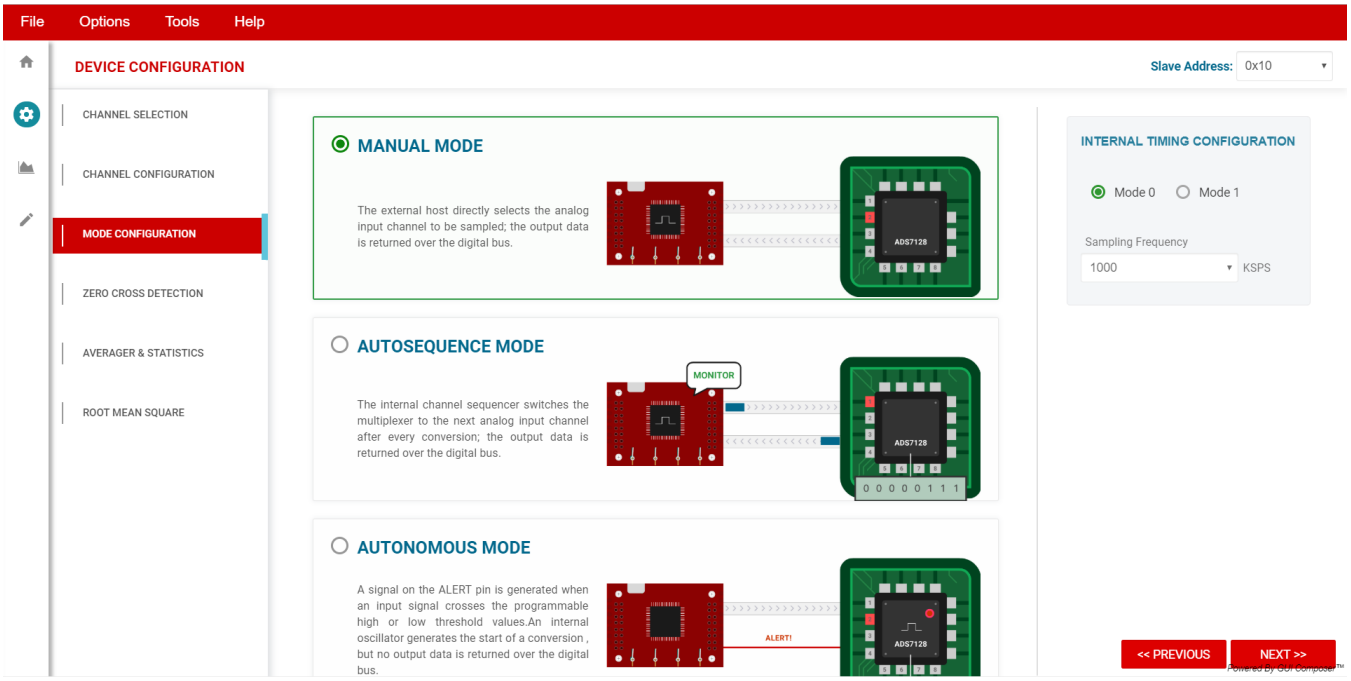

Figure 14. Sampling Mode Configuration

3.3.2.2.4 *Zero-Cross Detection (ZCD)*

The zero-cross detection tab, as shown in Figure 15, provides a timing diagram demonstrating the ZCD functionality and the blanking time transients of the input signal. only one input channel can be selected to monitor. The programmable blanking time can be disabled or enabled.

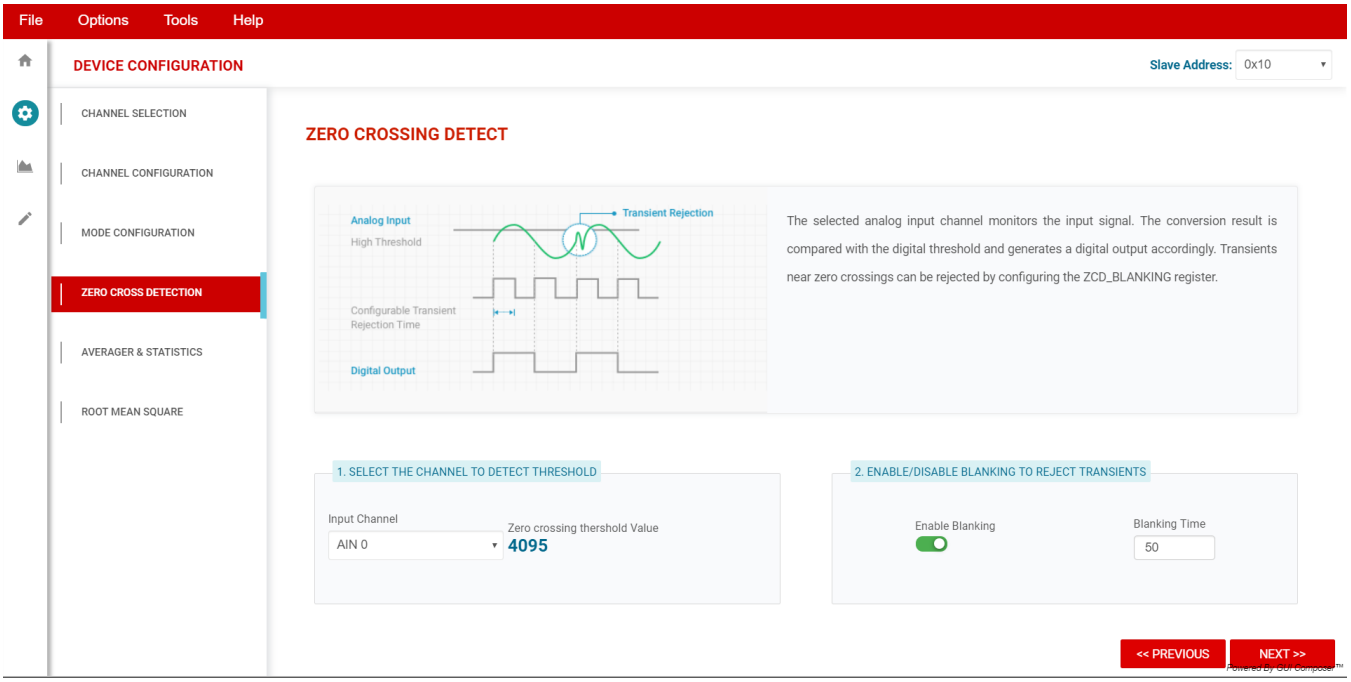

Figure 15. Zero-Cross Detection Page

3.3.2.2.5 Average and Statistics Configuration

Within the averager and statistics page, as shown in Figure 16, the oversampling ratio can be selected that applies to all analog input channels enabled. The statistic function can also be enabled or disable within this page.

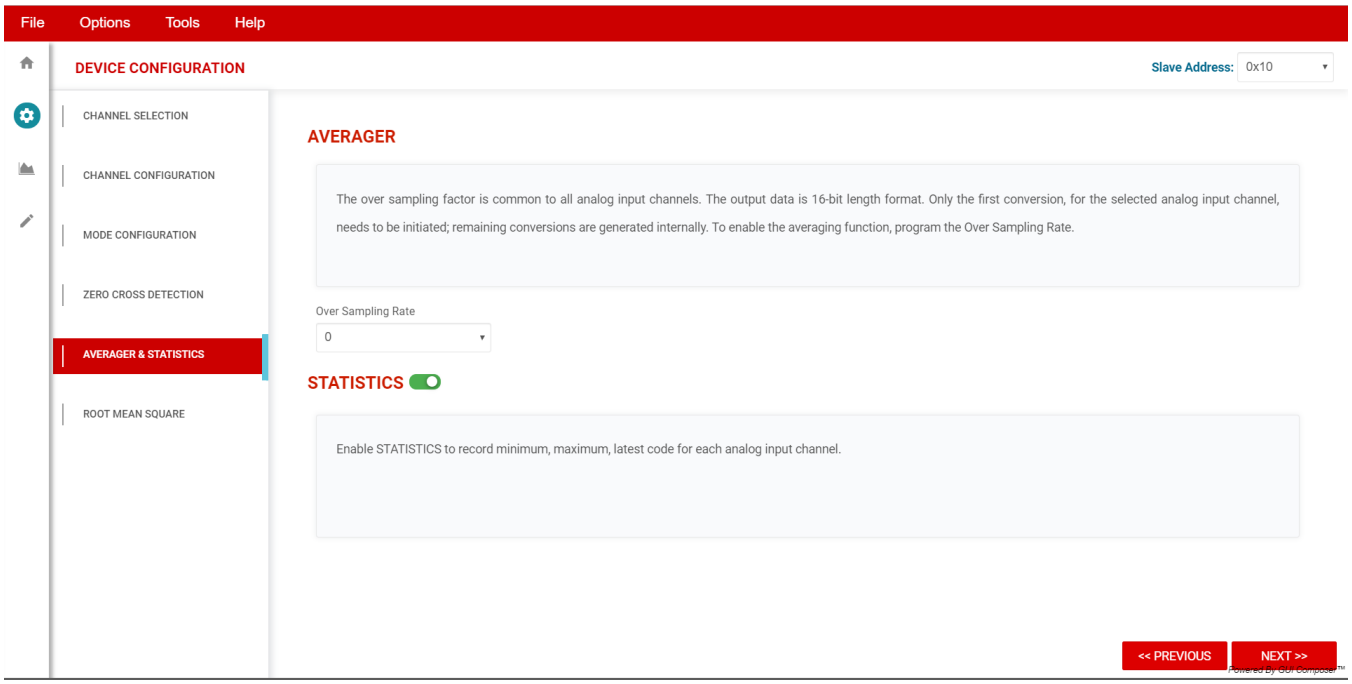

Figure 16. Averager and Statistics Page

3.3.2.2.6 Root Mean Square

The root mean square (RMS) page, as shown in Figure 17, displays the equation that the device uses to calculate the root mean square, if enabled. Based on the number of samples selected, the RMS is calculated using the final formula shown.

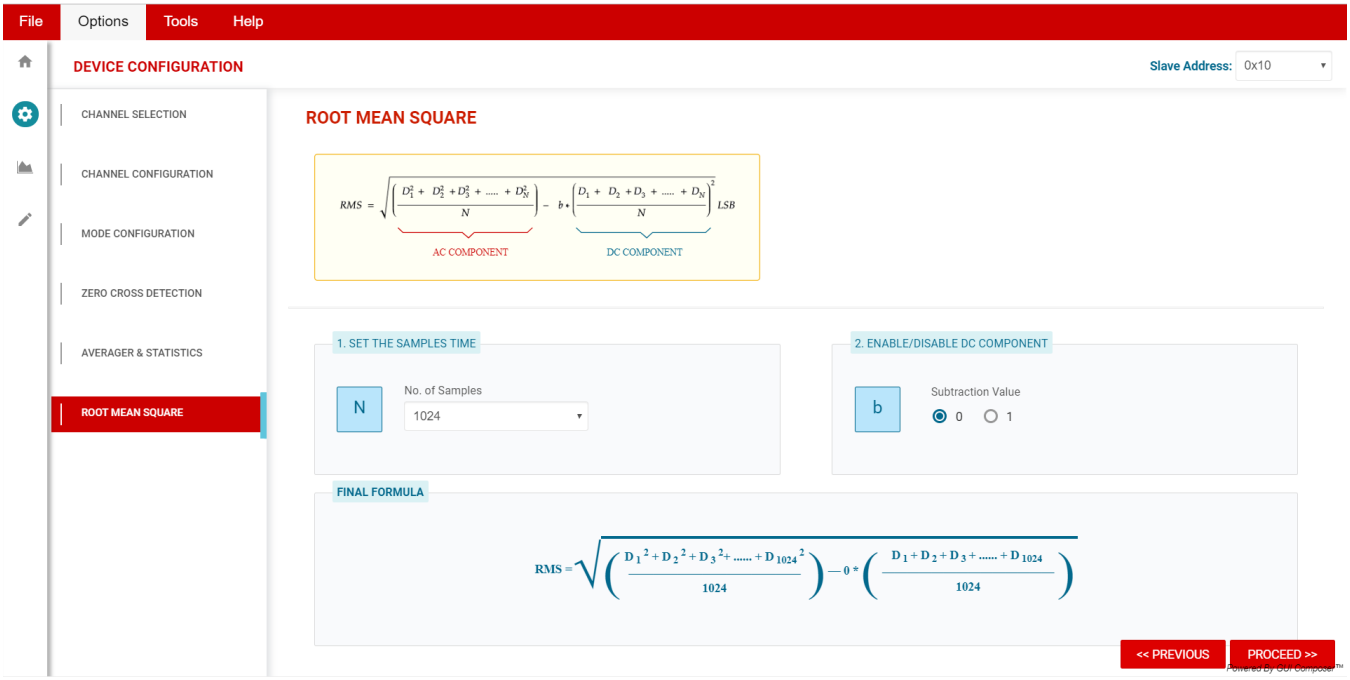

Figure 17. ADS7128 RMS Page

3.3.3 Data Capture Tab

The data capture tab displays the conversion results of the sampled data of the enabled channels. As shown in Figure 18, clicking the red **Capture** button commences a sample data set. This tab features two pages:

- **Analog Inputs:** The sample and conversion results for each enabled analog input is displayed in this page
- **Digital I/O:** The enabled digital channels, input or output, are displayed in this page

See Section 3.3.5 for more information on capturing data.

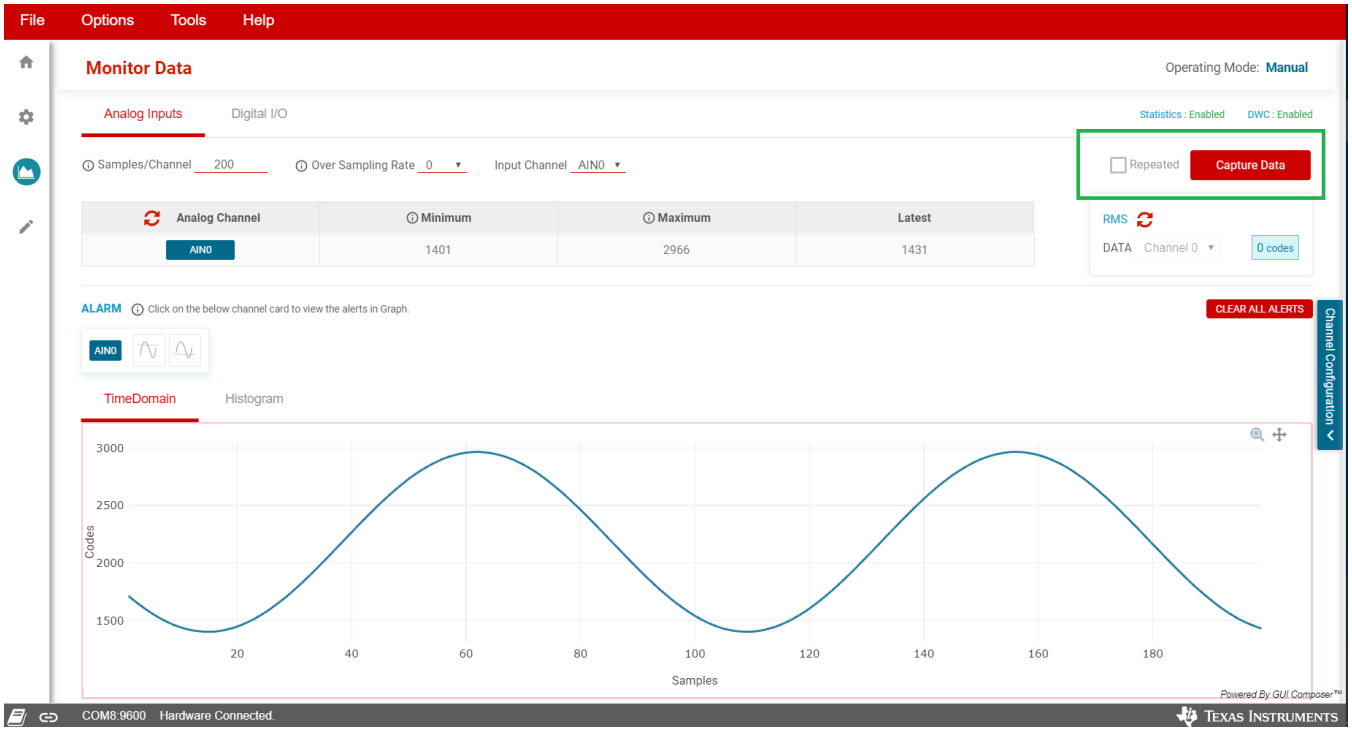

Figure 18. ADS7128 Data Capture Tab

3.3.4 Register Map

Figure 19 shows the register map for the ADS7128. On the top right corner are options to read registers individually, read all the registers at the same time, or write an individual register. Users can choose to have the register values modified in the GUI to be written on the device instantaneously by selecting the *Immediate* option or later using the *Deferred* option. In the field view, the registers are broken down into the configurable bits they are made up of. When making changes, the bit being changed is highlighted in yellow.

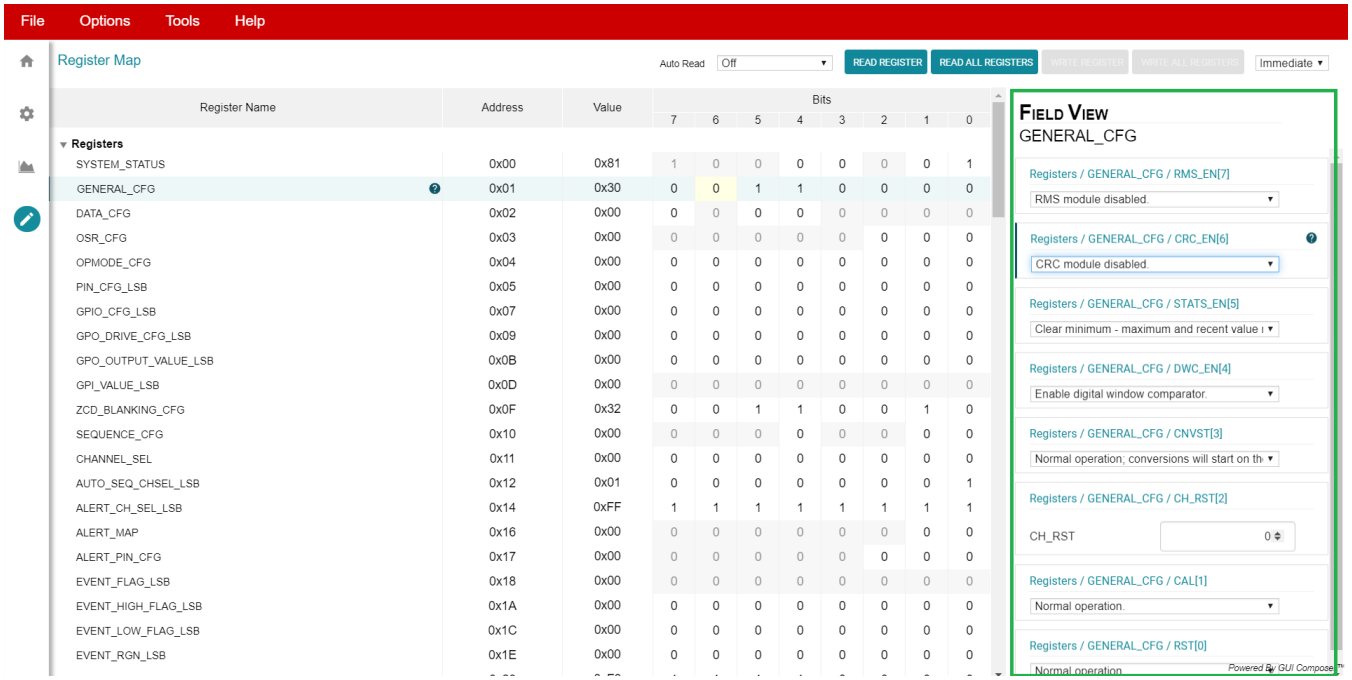

Figure 19. ADS7128 Register Map Page

3.3.5 Data Capture Features

This section describes the features available in the data capture tab of the GUI. This page auto updates to reflect the inputs in Section 3.3.2.2 based on the channel-specific configuration. The data capture tab displays both analog enable channels, under the analog inputs page, and the digital input and output enabled channels in the digital I/O page.

3.3.5.1 Analog Inputs Page

The analog input page provides an interface to the conversion results for analog input channels. Data are captured, as shown in Figure 20, by clicking on the **Capture Data** button. The analog inputs page also displays:

- Number of samples per the enabled analog input channels
- A drop-down option for increasing the oversampling rate
- A drop-down option for selecting input channel display
- Displays the minimum and maximum sample code
- When enabled, the RMS data of the channel selected in the drop-down option
- Alarm trigger and clear alarm option

The data capture page provides tabs to display the conversion results of the analog inputs and, within the analog input display tab, the conversion results can be displayed in either the time domain graph or the histogram graph.

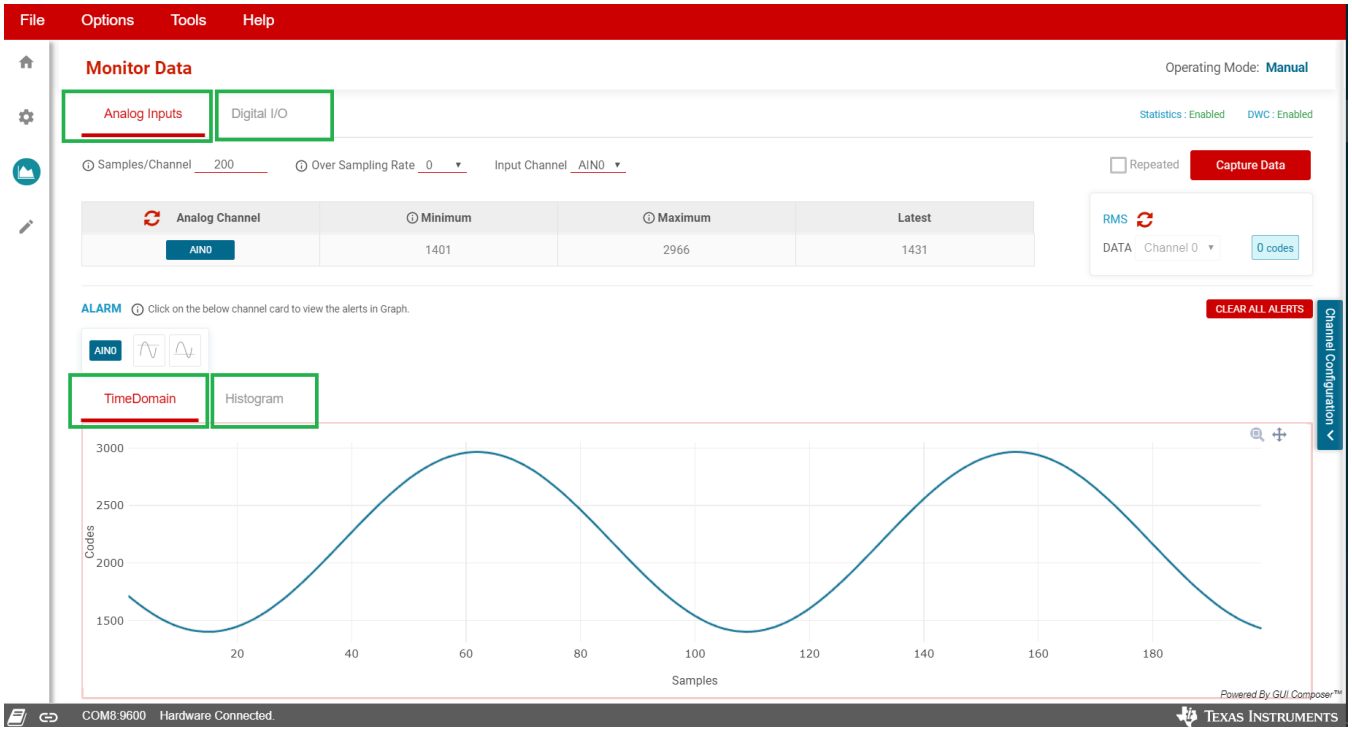

Figure 20. Data Capture Conversion Results

3.3.5.1.1 Time Domain Display

The time domain graph displays the conversion results of an analog input channel of a sampled data set. When in manual mode, the graph can only display one analog input conversion results at a time; in auto-sequence mode, all sampled channels are displayed. As shown in Figure 21, select the channel through the drop-down menu shown.

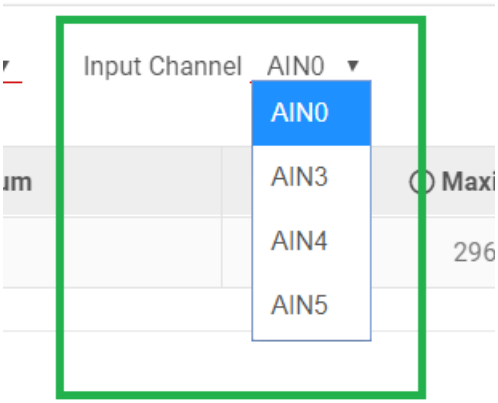

Figure 21. Time Domain Channel Selection

Within the time domain graph, the high and low thresholds (configured in Section 3.3.2.2) are automatically displayed inFigure 22 as solid red to visually demonstrate the levels that the analog signal triggers an alarm. Hysteresis (if configured), is also displayed within this graph as dashed red lines.

Figure 22. Time Domain Display With Threshold and Hysteresis

3.3.5.1.2 Histogram Graph Display

The conversion results can also be shown as a histogram through the histogram tab (shown in Figure 23) within the analog input data capture. The high and low threshold levels and the configured hysteresis are also displayed in the histogram graph.

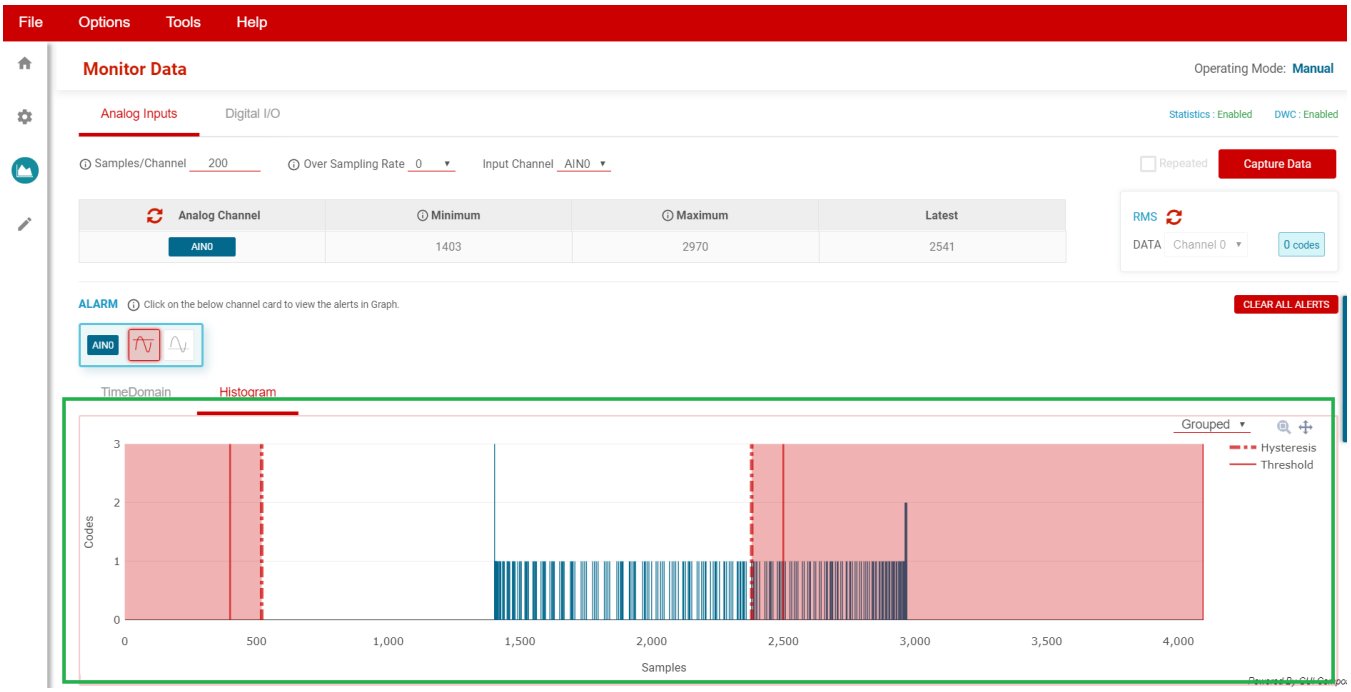

Figure 23. Histogram Graph Display With Threshold and Hysteresis

3.3.5.1.3 Alarm

As shown in Figure 24, if an analog input signal crosses the configured thresholds, then an alarm is triggered, as demonstrated in the analog inputs page within the data capture tab. This page provides an *ALARM* section where the corresponding image to the threshold crossed, high or low, turns red when triggered. The alarm can be cleared by clicking on the red icon.

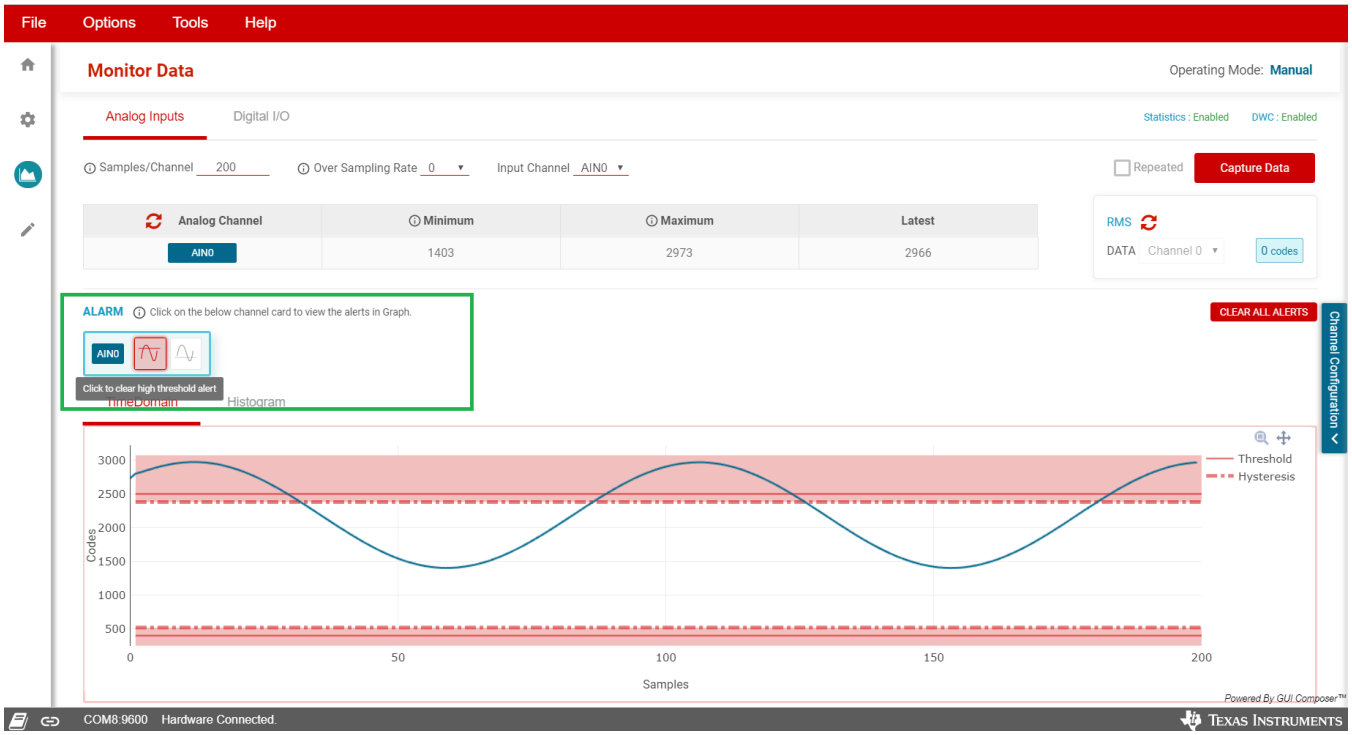

Figure 24. Alarm Triggered

3.3.5.2 Digital I/O Page

The digital I/O page displays the enabled digital input channels as configured in Section 3.3.2.1. In the example shown in Figure 25, two channels were configured as digital input channels. Each channel indicates the present logic state, followed by an icon demonstrating the triggering edge for a state change, rising edge of falling edge. The icon turns red when triggered.

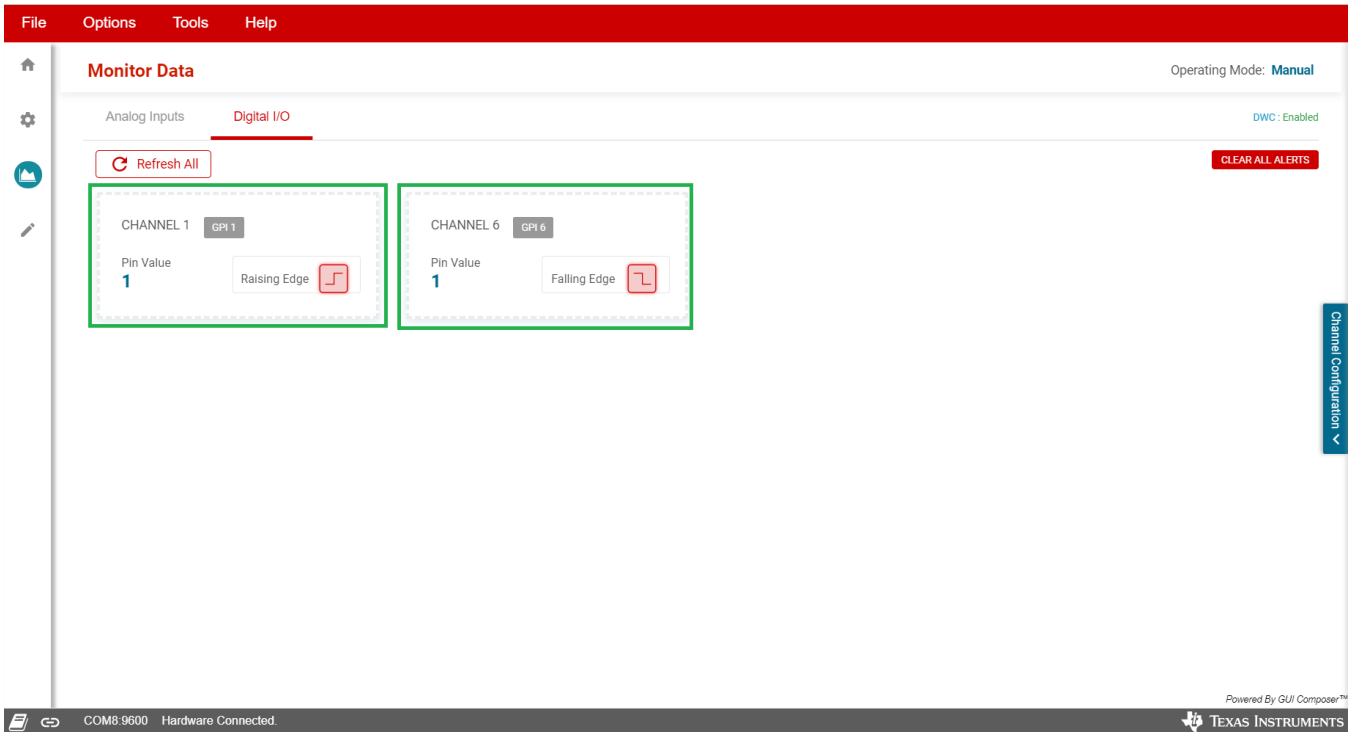

Figure 25. Digital I/O Page Display

4 Input Signal-Conditioning Block on the BP-ADS7128

For applications where the input signal requires additional conditioning before being interfaced to the ADC, the BP-ADS7128 has an onboard signal-conditioning path on channel 0 between the input signal and the ADS7128. By default, this signal-conditioning block is populated on the evaluation board as a noninverting buffer. The board has a provision to bypass the operational amplifier (U4) based on the signal conditioning requirement. In order to bypass this block, remove the R25 0-Ω resistor and populate R10. See Section 5.3 for more details.

5 Bill of Materials, Printed Circuit Board Layout, and Schematics

This section contains the BP-ADS7128 bill of materials (BOM), printed circuit board (PCB) layout, and schematics.

5.1 Bill of Materials

Table 2 lists the bill of materials (BOM) for the ADS7128EVM.

Table 2. Bill of Materials

Designator	Quantity	Description	Manufacturer Part Number	Manufacturer
C1, C3	2	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	C0603C105K3RACTU	Kemet
C4, C5, C9	3	CAP, CERM, 1 uF, 6.3 V, +/- 20%, X7R, 0402	GRM155R70J105MA12D	MuRata
C6, C7, C8, C10, C11, C13, C15	7	CAP, CERM, 160 pF, 50 V, +/- 5%, C0G/NP0, 0402	GRM1555C1H161JA01D	MuRata
C12, C14	2	CAP, CERM, 0.1 µF, 25 V,+/- 10%, X5R, 0603	CL10A104KA8NNNC	Samsung Electro-Mechanics
D2	1	LED, Red, SMD	LTST-C150CKT	Lite-On
J1, J3	2	Receptacle, 2.54mm, 10x2, Tin, TH	SSQ-110-03-T-D	Samtec
J4	1	Header, 100mil, 2x1, Tin, TH	PEC02SAAN	Sullins Connector Solutions
J5	1	Header, 100mil, 6x2, Tin, TH	PEC06DAAN	Sullins Connector Solutions
R2	1	RES, 1.69 M, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW04021M69FKED	Vishay-Dale
R3, R26	2	RES, 1.00 M, 1%, 0.1 W, 0402	ERJ-2RKF1004X	Panasonic
R4	1	RES, 0, 5%, 0.063 W, 0402	RC0402JR-070RL	Yageo America
R5, R6, R7	3	RES, 1.00 k, 1%, 0.063 W, 0402	MCR01MZPF1001	Rohm
R8, R9, R12, R14, R15, R18, R20, R23	8	RES, 10.0 k, 1%, 0.063 W, 0402	RC0402FR-0710KL	Yageo America
R17, R25	2	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	RMCF0603ZT0R00	Stackpole Electronics Inc
R19	1	RES, 2.20 k, 1%, 0.1 W, 0603	RC0603FR-072K2L	Yageo
R24	1	RES, 169, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW0402169RFKED	Vishay-Dale
TP6, TP7	2	Test Point, Multipurpose, Black, TH	5011	Keystone
U1	1	Single Output LDO, 150 mA, Adjustable 1.22 to 5.25 V Output, 2.2 to 5.5 V Input, with 500 nA Quiescent Current, 5-pin SOT (DDC), -40 to 125 degC, Green (RoHS & no Sb/Br)	TPS78001DDCR	Texas Instruments
U2	1	Small, 8-Channel, 12-bit ADC with I2C Interface, GPIOs & CRC, RTE0016C_WF (WQFN-16)	ADS7128RTE	Texas Instruments
U3	1	I2C BUS EEPROM (2-Wire), TSSOP-B8	BR24G32FVT-3AGE2	Texas Instruments
U4	1	10-MHz, RRIO, CMOS Operational Amplifier for Cost-Sensitive Systems, DBV0005A (SOT-23-5)	TLV9061IDBVR	Texas Instruments

5.2 PCB Layout

Figure 26, Figure 27, Figure 28, and Figure 29 illustrate the EVM PCB layout.

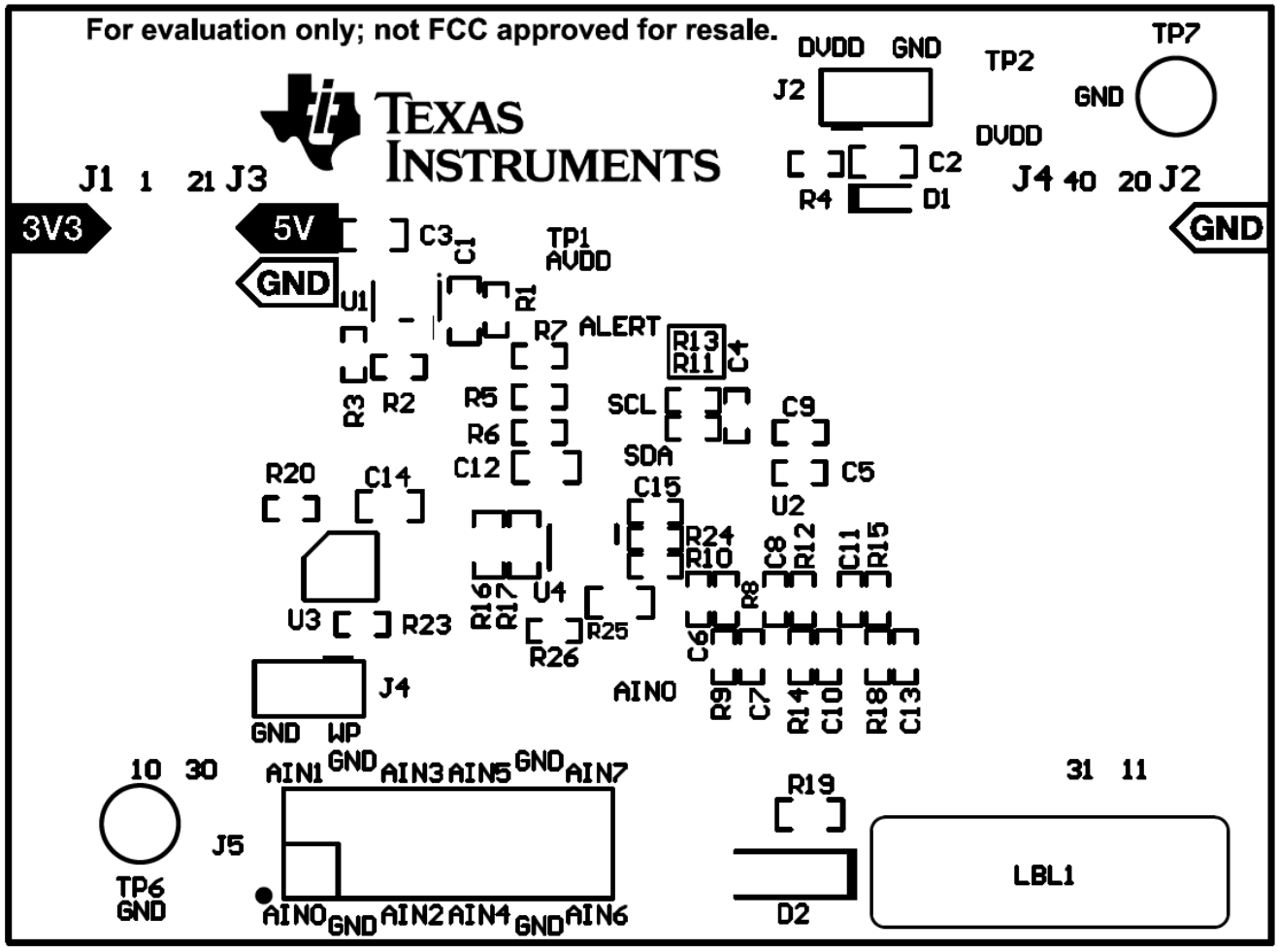

Figure 26. BP_ADS7128 PCB Top Overlay

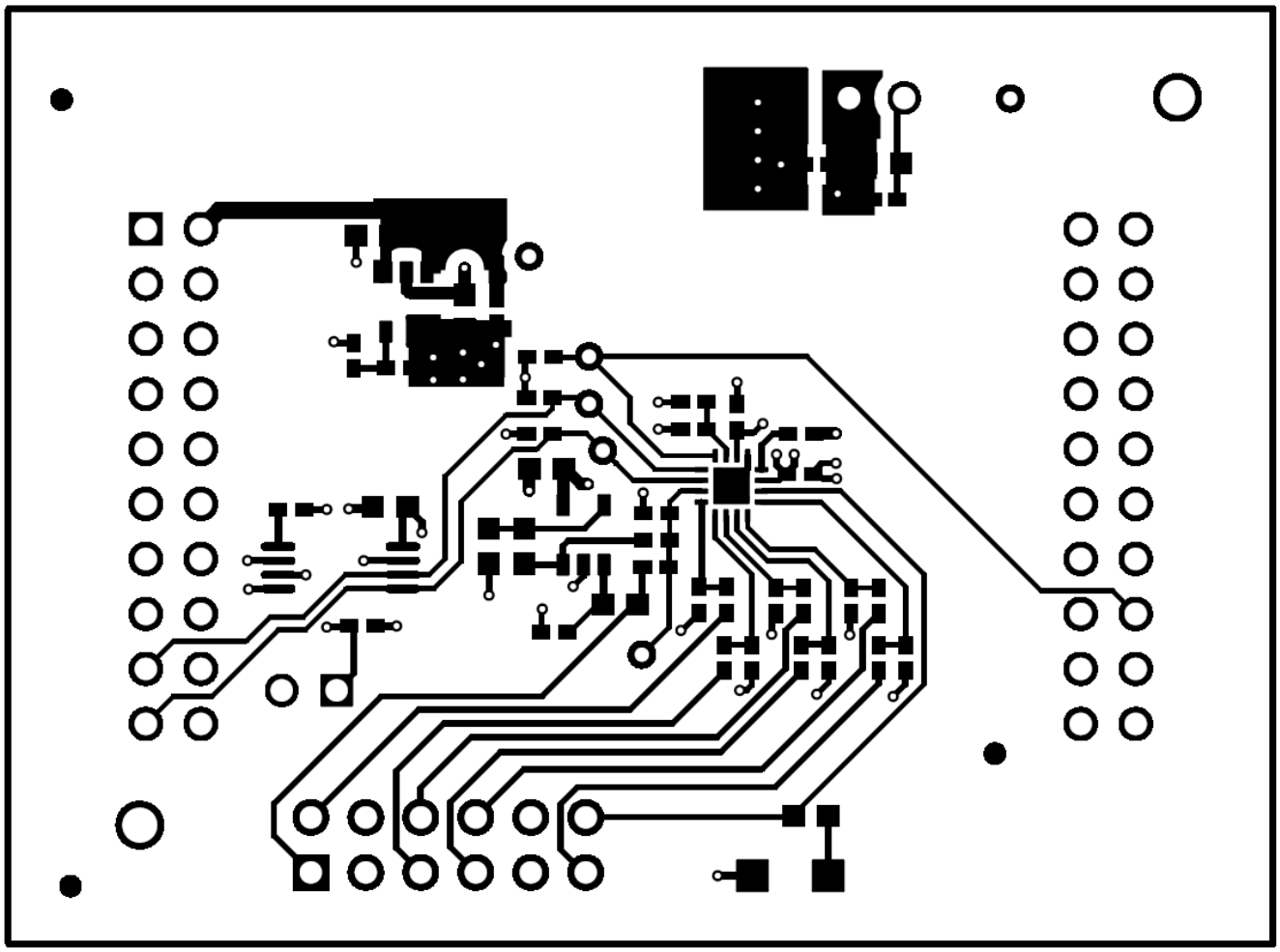

Figure 27. BP-ADS7128 Top Layer Copper and Silkscreen

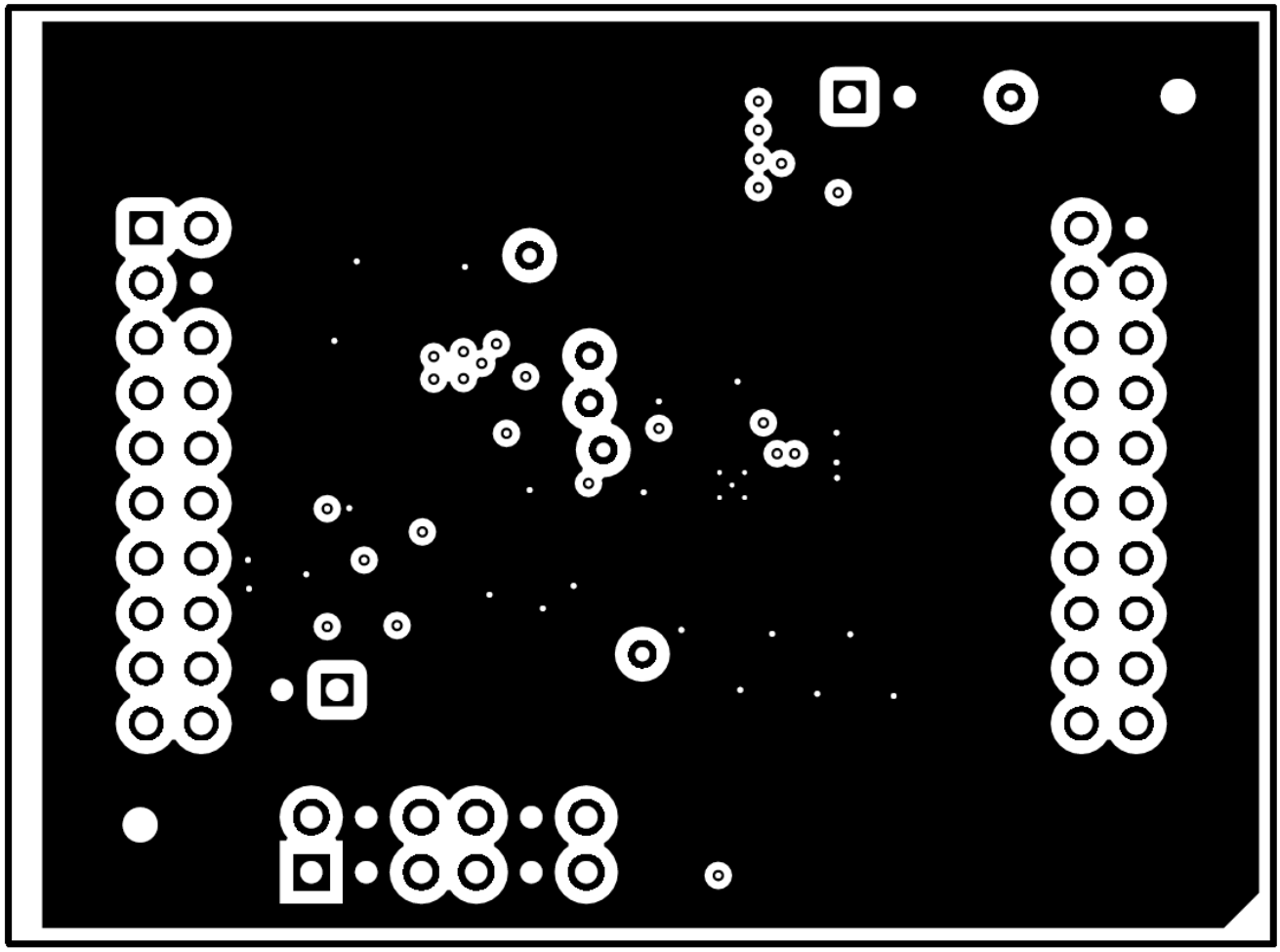

Figure 28. BP-ADS7128 Bottom Layer Copper and Silkscreen

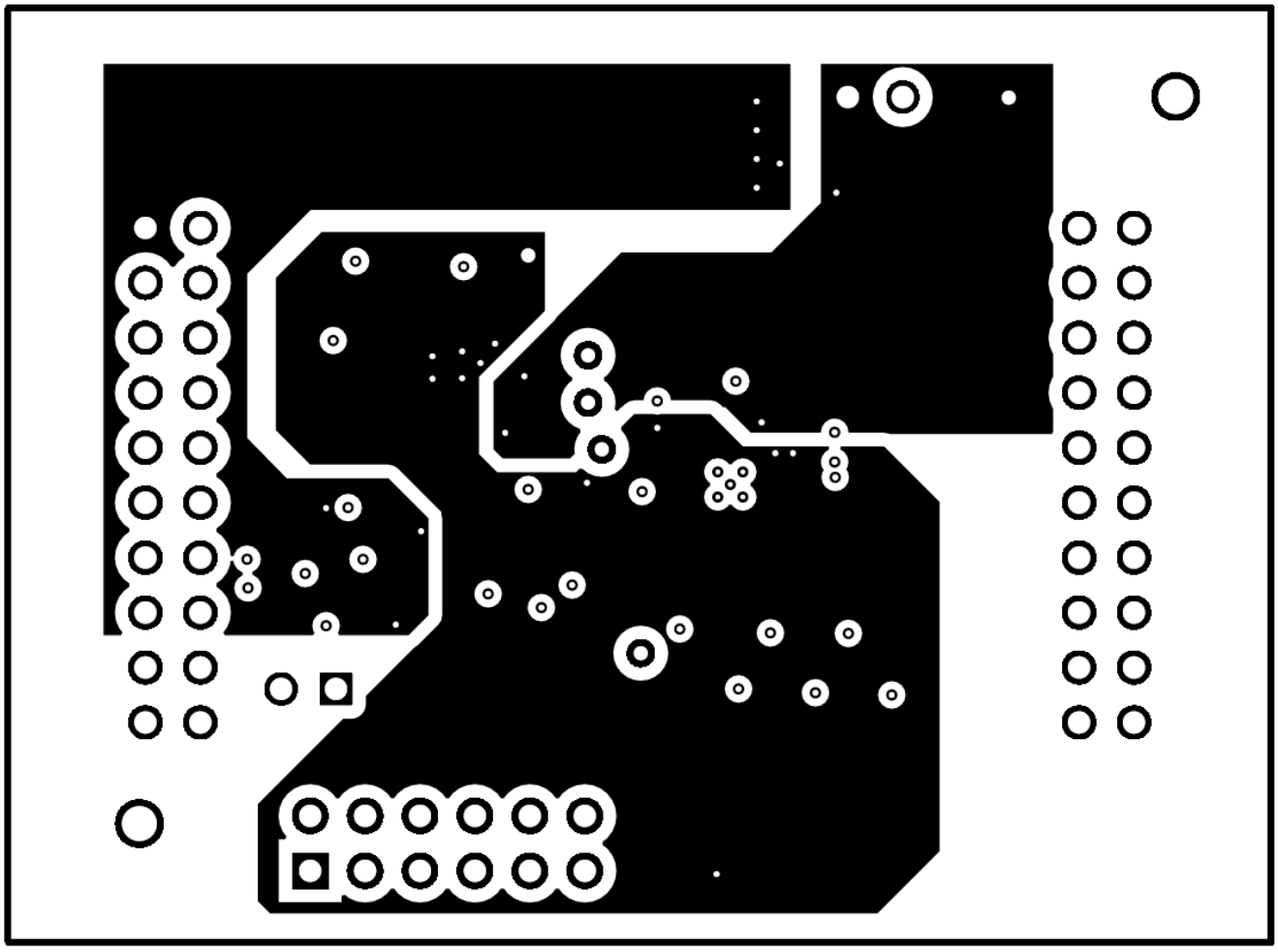

Figure 29. BP-ADS7128 Power Plane Layer

5.3 Schematics

Figure 30 illustrates the ADS7128 BoosterPack™ schematics.

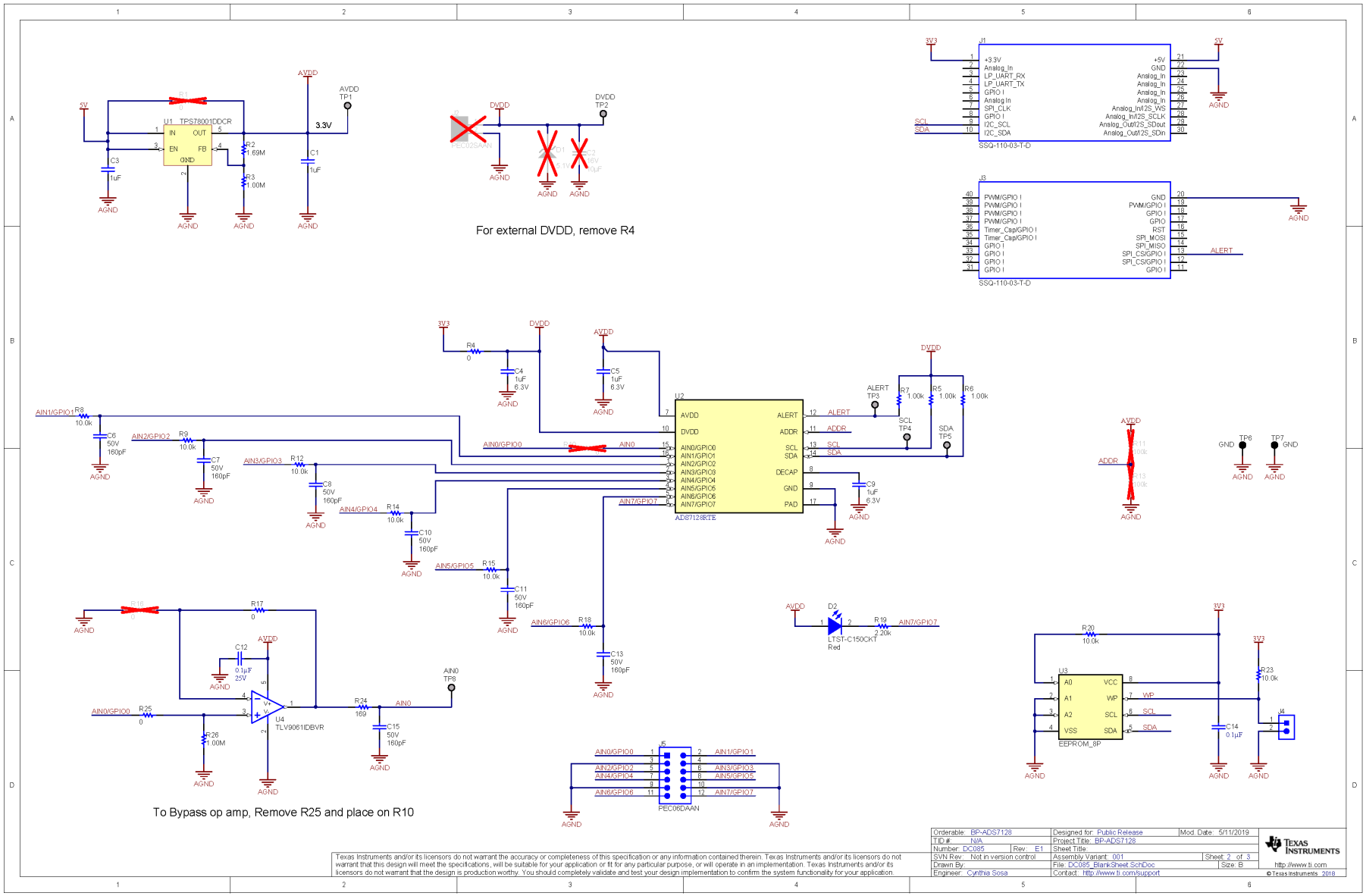

Figure 30. ADS7128 BoosterPack™ Schematic Diagram

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