PSoC™ Automotive Multitouch Generation 6L Slider

Datasheet

Features

- Automotive Electronics Council (AEC) AEC-Q100 qualified
- Multitouch capacitive slider controller
  - 32-bit Arm® Cortex® CPU
  - Register-configurable
  - Noise-suppression technologies for EMI
    - Effective 20-V drive for higher signal-to-noise ratio (SNR)[1]
    - AutoArmor improves both electromagnetic emissions and immunity
  - Water rejection and wet-finger tracking using DualSense
  - Multitouch glove with automatic mode switching
    - Ten fingers with thin glove (≤ 1-mm thick)
    - Two fingers with thick glove (≤ 5-mm thick)
  - Up to 3 TX configuration supported
  - Large object rejection
  - Supports 1 TX single layer configuration
  - Automatic baseline tracking to environmental changes
  - Low-power look-for-touch mode
  - Field upgrades via bootloader
  - Infineon Manufacturing Test Kit (MTK)
  - Slider sensor self-test
  - Low power CAPSENSE™ wake-up button with power consumption of 50 µA
- System performance (configuration dependent)
  - Up to 48 sense pins, 135 intersections (45 RX and 3TX)
  - Swipe speed of up to 1000 mm/sec
  - Reports up to ten fingers
  - Small finger support down to 4 mm
  - Support up to 10 capacitive sensing buttons
  - Refresh rate up to 250 Hz; other rates configurable
  - TX frequency up to 350 kHz

Note

1. Effective voltage when using 17 multi-phase TX and 5-V V_{CCTX} supply.

Features

- Power (configuration-dependent)
  - 1.71-V to 1.95-V and 3.0-V to 5.5-V logic and digital I/Os supply
  - 3.0-V to 5.5-V analog supply
  - 9-mW average power
  - 11-µW typical deep-sleep power
- Sensor and system design (configuration-dependent)
  - Supports a variety of slider sensors and stackups
    - Manhattan, diamond
    - Plastic (PET) and glass-sensor substrates
    - Metal mesh
- Communication interface
  - I^2C slave at 100 and 400 kbps
  - SPI slave bit rates up to 8 Mbps
- Package
  - 56-pin QFN wettable flank, 8 × 8 × 1 mm, 0.5-mm pin-pitch
  - 64-pin TQFP 10 × 10 × 1.4 mm, 0.5-mm pin-pitch
- Ambient temperature range
  - Automotive-A: –40°C to 85°C
  - Automotive-S: –40°C to 105°C

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1 Slider system overview

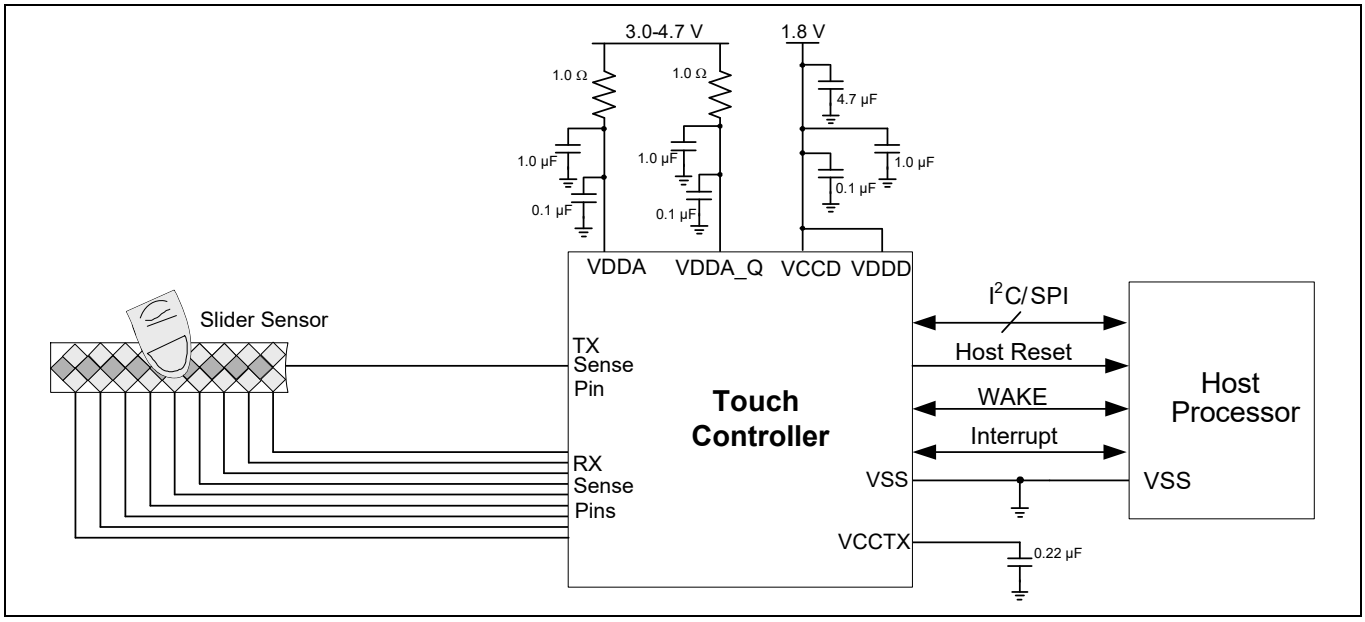


Figure 1 CYAT6165X typical system diagram

2 CYAT6165X overview

A capacitive slider detects changes in capacitance to determine the location of one or more fingers on the surface of the slider. A typical slider system consists of a capacitive slider sensor, an FPC bonded to the sensor, and the slider controller mounted on the FPC. The FPC connects the slider controller to the host processor. Users can interact with the user interface through finger movements and gestures on the surface of the slider.

CYAT6165X is a capacitive slider controller with the sensing and processing technology to resolve the locations and report the positions of up to ten fingers on the slider. The slider controller converts an array of sensor capacitances into an array of digital values, which are processed by touch-detection and position-resolution algorithms in the controller. These algorithms determine the location and signal magnitude of each finger on the slider.

Infineon provides:

- Application firmware
- Design guidance for the sensor and FPC
- Slider sensor MTK

The CYAT6165X functional block diagram is shown in **Figure 2**. This device contains a high-performance Arm® 32-bit CPU with an integrated hardware multiply unit. This CPU controls all sensing and processing of measured capacitance results to allow tracking and reporting touches. The controller is optimized for low power and fast response time, with built-in support for manufacturing test. The slider controller communicates with a host through an I^2C slave interface at up to 400 kbps or an SPI interface at up to 8 Mbps.

CYAT6165X collects the slider sensor information using the touch subsystem. This touch subsystem consists of a 5-V TX pump, TX drivers, RX channels, and a programmable transmit/receive (TX/RX) multiplexer. The multiplexer electrically connects the analog front end of each RX channel and TX driver to the appropriate row and column electrodes of the slider sensor.

The controller TX/RX multiplexer allows flexibility of chip placement on the FPC. All pins connecting to the slider sensor are programmable as either TX or RX.

Infineon reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@infineon.com**.

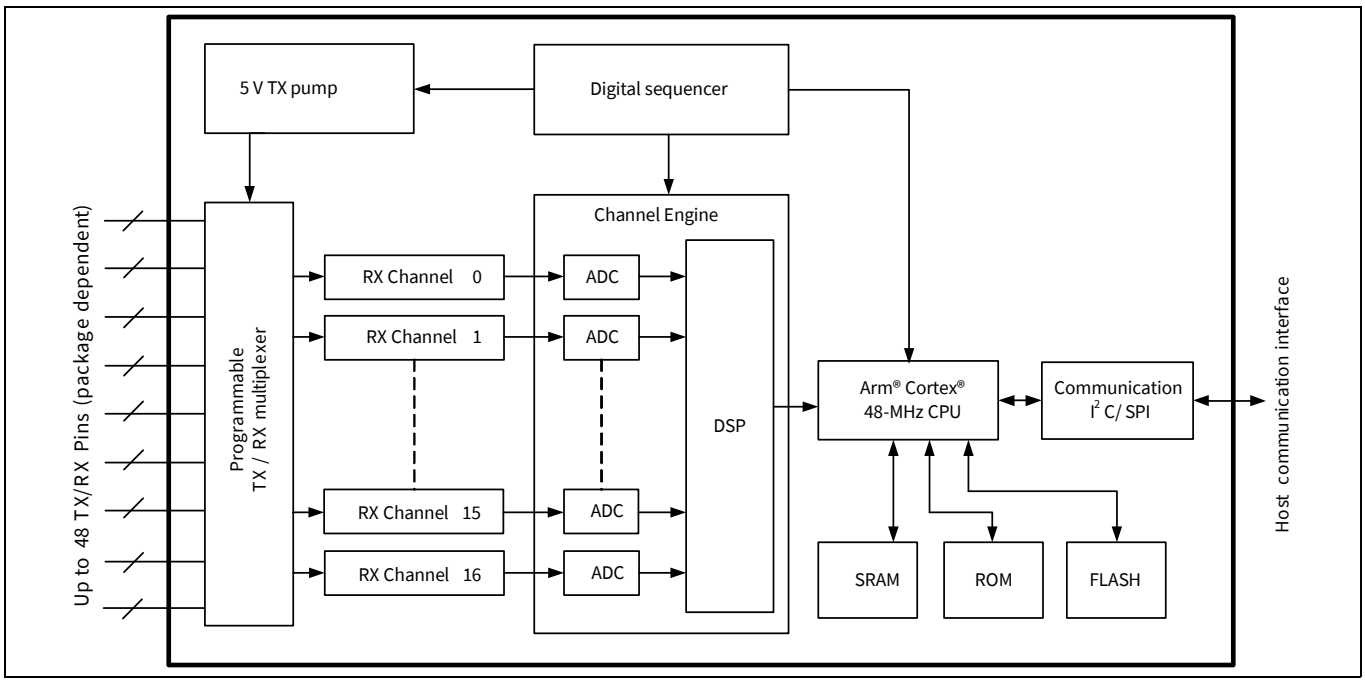


Figure 2 CYAT6165X functional block diagram

3 Features overview

3.1 AutoArmor

AutoArmor improves both electromagnetic emissions and immunity. It ensures no false finger touches when CYAT6165X is exposed to electromagnetic waves.

3.2 Water rejection

Water droplets can cause false touches to be reported. However, CYAT6165X continues to operate in the presence of water droplets or condensation. CYAT6165X enables water rejection using DualSense, Infineon's patented self- and mutual-capacitance sensing ability.

3.3 Wet-finger tracking

In a slider system, moisture on fingers can cause false touches to be reported and make tracking of fingers across the slider difficult. CYAT6165X can detect and track fingers that are wet and enable more robust functionality of the slider, using DualSense. This includes sweaty fingers touching the slider or fingers moving across a mist-covered slider.

3.4 Glove

CYAT6165X detects and tracks gloved fingers. Glove support allows navigating the slider without having to remove gloves or without the use of expensive conductive gloves. Tracking of gloved fingers is supported by automatic mode switching, which automatically transitions between tracking gloved fingers and other touch-tracking modes. Ten-finger glove-touch is supported for thin gloves (≤ 1-mm thick) and two-finger operation is supported for thick gloves (≤ 5-mm thick).

3.5 Automatic mode switching

CYAT6165X supports automatic mode switching which detects and tracks a new touch object type without requiring manual selection of the touch type from the user. Automatic mode switching allows an uninterrupted user experience when switching between a bare finger, gloved finger, fingernail, or wet finger.

3.6 Large finger tracking

A well-designed slider system must correctly report a large finger or thumb as only a single touch. If this is not supported, a large finger can incorrectly be reported as two or more touches, hampering the user experience. When an object, such as a thumb, is pressed against the slider sensor, CYAT6165X ensures that only one touch is reported at the center of the object.

3.7 Large object detection and rejection

It is important to be able to detect the presence of a large object on the slider sensor. CYAT6165X can determine the presence of a large object, such as a fist or palm, from the slider data. This presence may either be rejected or reported to the host.

3.8 Look-for-Touch

Look-for-touch is a low-power and fast-wakeup mode, in which the slider sensor is measured for an increase in self-capacitance. An increase in self-capacitance indicates that a touch is present. Because it is only necessary to detect a finger's presence, and not location, the sensing can be done at a much lower SNR, requiring less time and power. Look-for-touch sensing is used to implement multiple functions, including wake-on-touch and fast first-touch response.

4 Slider system specifications

This section specifies the slider system performance delivered by CYAT6165X. For definitions, justification of parameters, and test methodologies, refer to the Infineon specification **PSoC™ Automotive Multitouch Touchscreen Controller User Interface Performance Definitions (001-49389)**[2].

4.1 System performance specifications

The system performance specifications in **Table 1**[3] and **Table 2**[4] are valid under these conditions: $-40°C \le T_A \le 85°C$[5] for Grade-A devices, $-40°C \le T_A \le 105°C$[5] for Grade-S devices; $1.71\ V \le V_{DDD} \le 1.95\ V$ or $3.0\ V \le V_{DDD} \le 5.5\ V$, $1.71\ V \le V_{CCD} \le 1.95\ V$, $3.0\ V \le V_{DDA} \le 5.5\ V$, unless otherwise noted. Typical values are specified at $T_A = 25°C$, $V_{DDD} = V_{CCD} = 1.8\ V$, core low dropout regulator (LDO) disabled, and $V_{DDA} = 3\ V$, unless otherwise noted. Data is validated using 1 TX configuration, 5-mm electrode pitch. Contact your local Infineon sales representative for information on the system performance conditions to guarantee the specifications in **Table 1**. The performance conditions and specifications are valid only for sensors approved by Infineon for use with CYAT6165X and produced by qualified Infineon partners.

Contact **automotive@infineon.com** to discuss any deviations.

Table 1 Typical system performance specifications (Configuration dependent)

Category	Conditions	Core	Unit
Accuracy	6–12 mm diameter finger	0.5	mm
	Glove (≤ 1 mm thick)	2	
	Glove (1 < thick ≤ 5 mm)	4	

Notes

2. Infineon reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@infineon.com**.
3. Typical, as represented by 85% of the sample data measured. Accuracy is measured at points across the entire panel at 1.1-mm intervals.
4. Typical, as represented by the average values from the Infineon specification, PSoC™ Automotive Multitouch Touchscreen Controller User Interface Performance Definitions (001-49389).
5. System performance specifications are dependent on the combination of slider controller, display, slider, and environment noise and temperature. Infineon guarantees the performance of the touch controller over this temperature range, but system performance may be impacted by the response of these other elements.

Table 2 System performance specifications (Configuration dependent)

Category	Description	Conditions	Min	Typ	Max	Unit
Jitter	Delta in reported X,Y position, for non-moving finger	5–12 mm diameter finger	–	0.5	–	mm
Refresh rate	–	One finger on panel	60	200	250[6]	Hz
Response time	Active response time	First finger down	–	–	30	ms
Swipe speed	–	–	–	300	1000	mm/sec
Low power wake-up button	Power consumption	3.3 V, 100 ms scan rate	–	50	–	µA
Power	In Active state	1 finger, 60-Hz refresh rate	–	–	180	mW
	In Active look-for-touch state	–	–	–	30	
	Average power[7]	Active state for 25% of touch activity and in Deep Sleep state for 75% of touch activity.	–	9	–	
	In deepsleep state	–	–	11	–	µW

Notes

6. Requires setting TX pulses for mutual-cap and self-cap to 8 and no noise in the environment.
7. See **"Power states summary"** on page 15 for power state transition details and refresh interval configuration for each state. Average power is the power consumed during the active and deep sleep states, and is calculated using this equation: 0.25 × 120 mW + 0.75 × 0.030 mW = 30 mW.

5 System design options

5.1 CAPSENSE™ button/FPC support

The CYAT6165X controller supports a maximum of 10 physical CAPSENSE™ buttons.

Detailed FPC development guidelines, including EMI shielding, are available in the **PSoC™ Automotive Multitouch Touchscreen Controller Module Design Best Practices (001-50467).**

5.2 Sensors

Infineon supports the following sensor patterns:

- Single-solid diamond (SSD)
- Dual-solid diamond (DSD)
- Manhattan-3 (MH3)

Figure 3 through **Figure 5** show examples of SSD, DSD, and MH3 sensor patterns and unit cells.

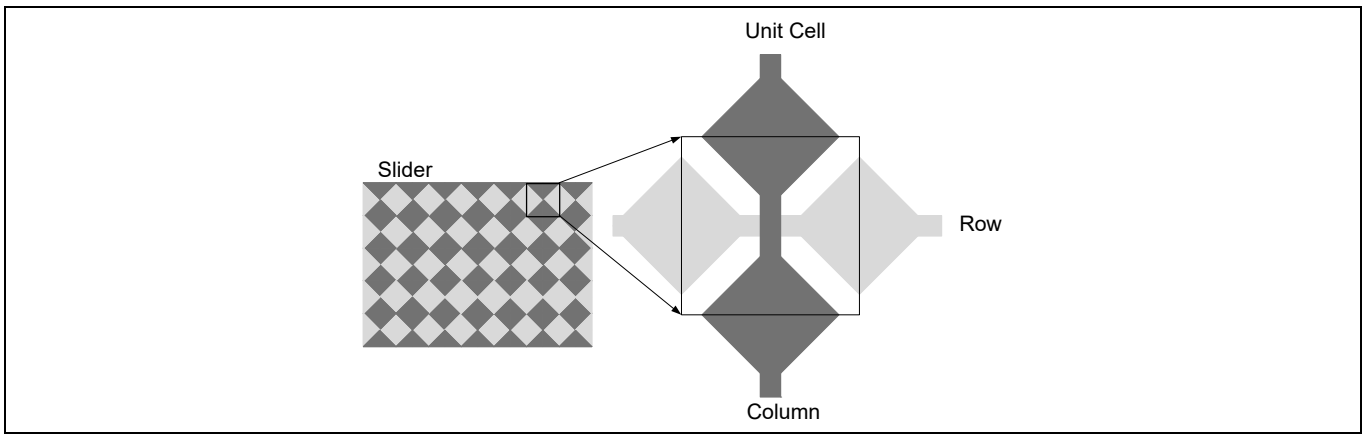


Figure 3 Single-solid diamond pattern and unit cell

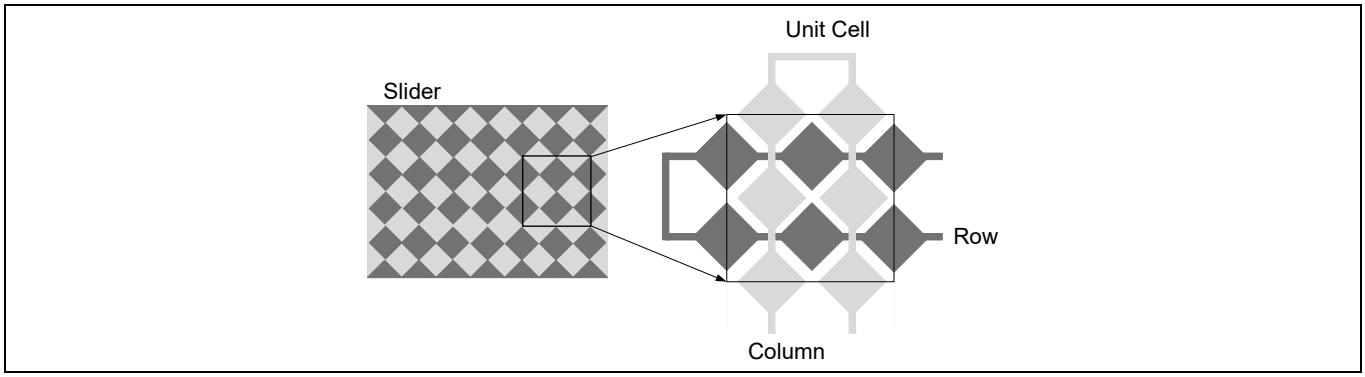


Figure 4 Dual-solid diamond unit cell

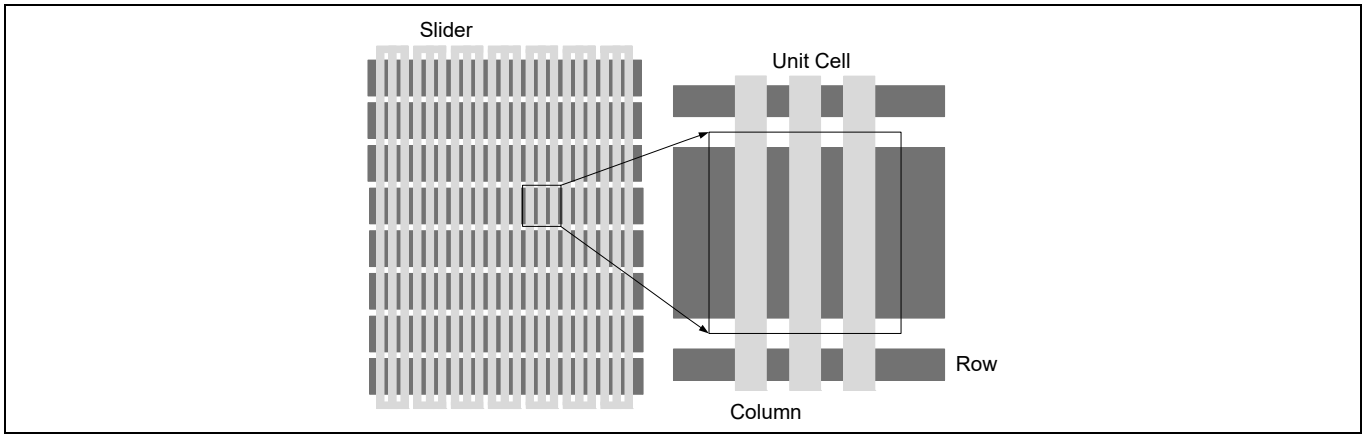


Figure 5 Manhattan-3 pattern and unit cell

Infineon continues to develop additional patterns and materials to increase performance and decrease system cost.

The specific sensor pattern used varies based on the mechanical, electrical, optical, and cost constraints; all of these factors must be considered for an optimal solution.

Following is an example:

- Overlays/lens thickness < 1 mm should not use SSD due to large signal disparity (SD).

To learn more about how to design sensors using stackups and materials, see the **PSoC™ Automotive Multitouch Touchscreen Controller Module Design Best Practices (001-50467)**.

6 Power supply information

CYAT6165X contains four power pins: VDDA, VDDA_Q, VDDD, and VCCD. VDDA supplies power to the chip's analog circuitry, TX pump, and drivers. VDDA_Q supplies power to the RX analog circuitry. VDDD supplies power to the digital I/Os, core LDO regulator, supply monitors, and external reset circuitry (XRES). VCCD supplies power to the CPU core, and may be configured as an input or output, depending on if a 1.71–1.95-V V_{DDD} supply is used.

6.1 Required external components

The touch controller requires external components for proper device operation. Quantities are dependent on the power supply configuration used. External capacitors require an X5R dielectric characteristic or better. It is recommended to use an X7R dielectric characteristic or better for high-frequency 0.1-µF/0.22-µF capacitors.

VDDA:

- 1.0-Ω, 5% tolerance resistor
- 0.1-µF capacitor
- 1-µF capacitor (2.2-µF in high low-frequency noise)

VDDA_Q:

- 1.0-Ω, 5% tolerance resistor
- 0.1-µF capacitor
- 1-µF capacitor (2.2-µF in high low-frequency noise)

VDDD:

- 0.1-µF capacitor
- 4.7-µF capacitor

VCCD:

- 0.1-µF capacitor

VCCTX:

- 0.22-µF capacitor (configurations with the VCCTX pump enabled)

6.2 Voltage coefficient

The actual capacitance of external capacitors may be reduced with higher bias voltage. Check the capacitor datasheet for the voltage coefficient. Capacitors used for power supply decoupling or filtering are operated under a continuous DC-bias. Many capacitors used with DC power across them provide less than their target capacitance, and their capacitance is not constant across their working voltage range. When selecting capacitors for use with this device verify that the selected components provide the required capacitance under the specific operating conditions of temperature and voltage used in your design. While the temperature ratings of a capacitor are normally found as part of its catalog part number (for example, X7R, C0G, Y5V), the matching voltage coefficient may only be available on the component datasheet or direct from the manufacturer. Use of components that do not provide the required capacitance under the actual operating conditions may cause the device to perform to less than the datasheet specifications.

The available power configurations, with the TX pump enabled, are shown in **Figure 6** and **Figure 8**. **Figure 7**, **Figure 9**, and **Figure 10** show power supply configurations with the TX pump disabled.

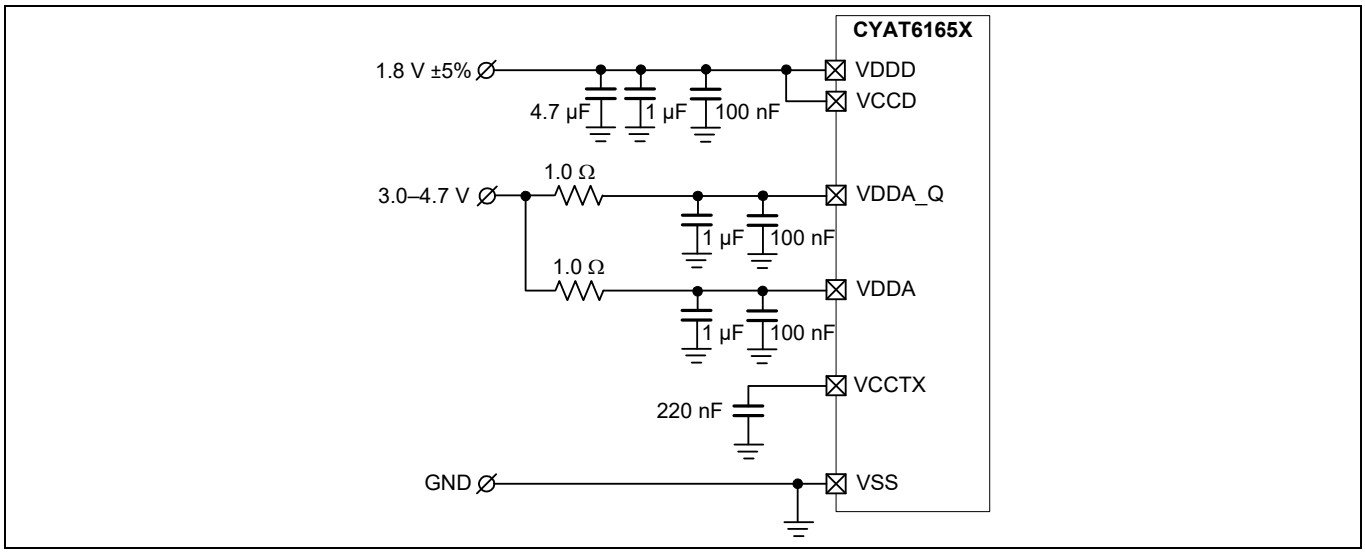


Figure 6 Dual supplies (inc. 1.8 V), TX pump enabled

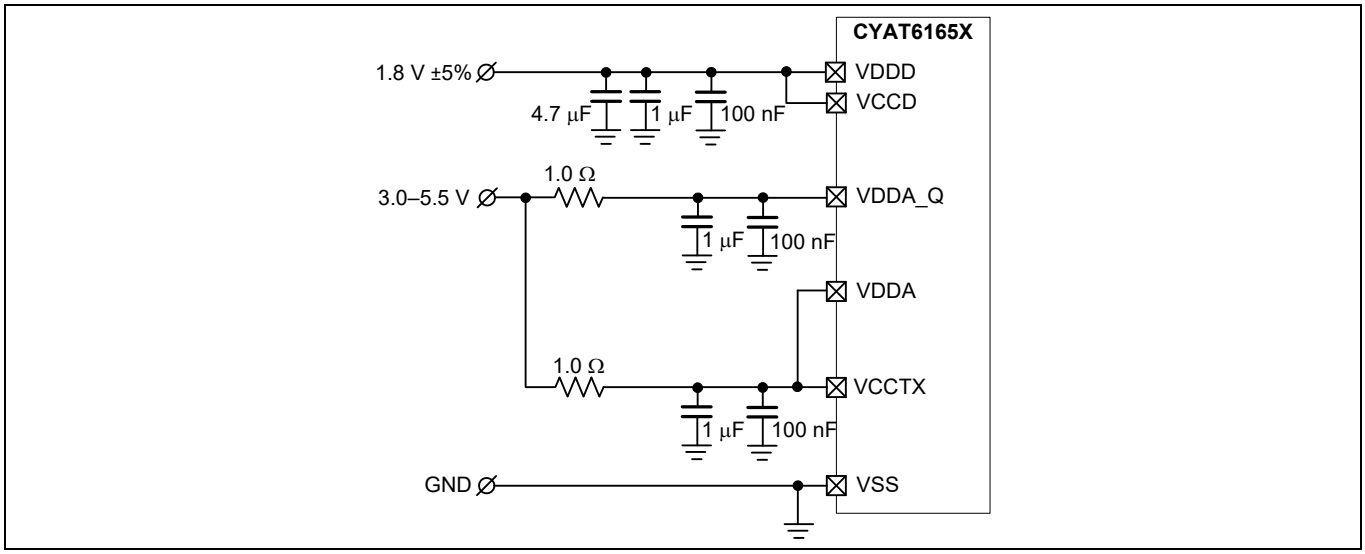


Figure 7 Dual supplies (inc. 1.8 V), TX pump disabled

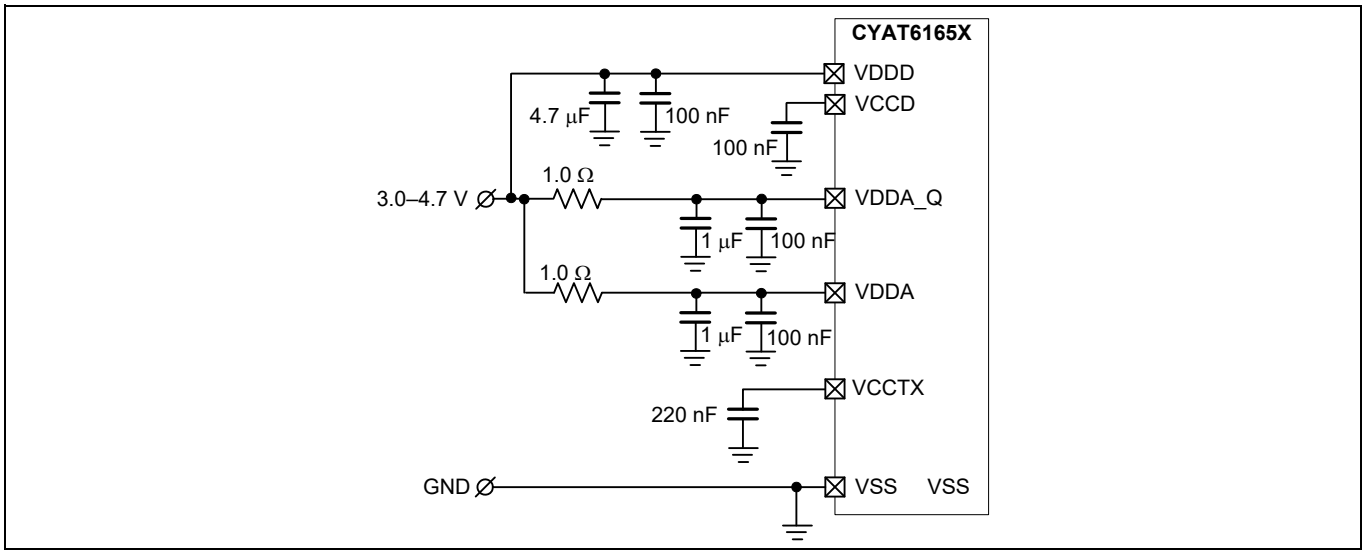


Figure 8 Single supply, TX pump enabled

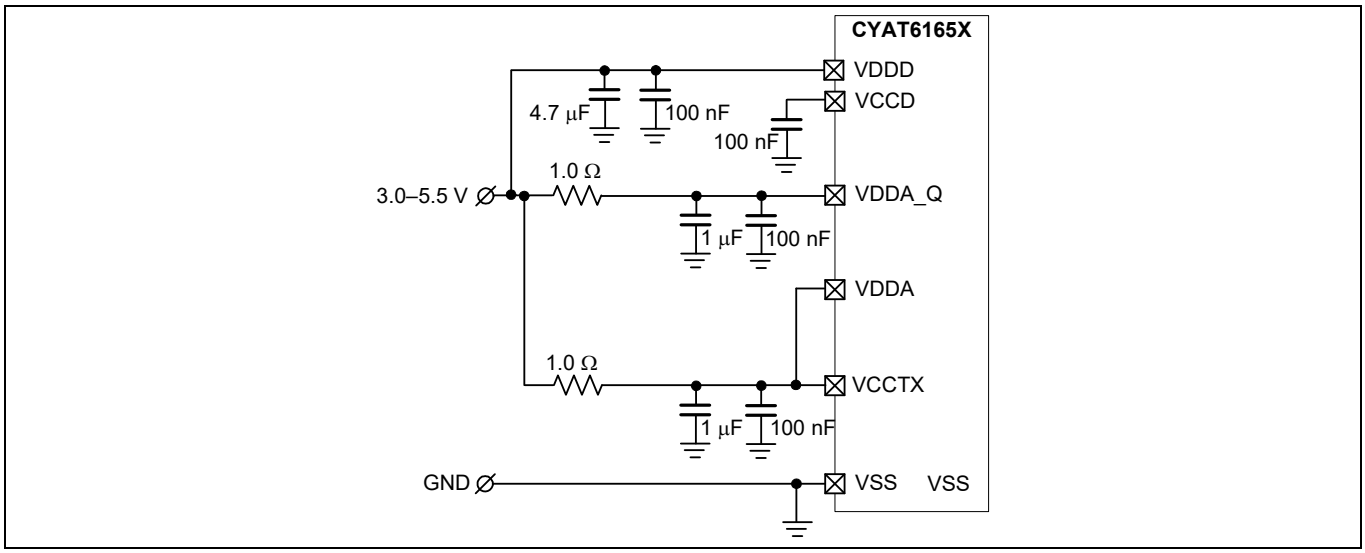


Figure 9 Single supply, TX pump disabled

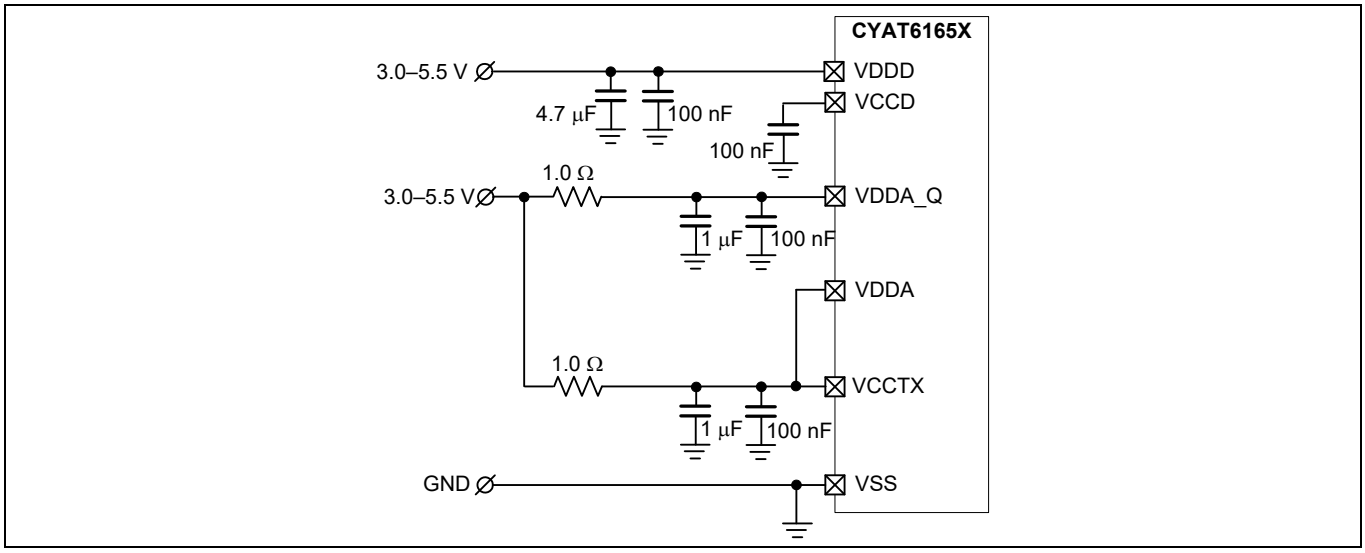


Figure 10 Dual supplies (no 1.8 V), TX pump disabled

7 Power states summary

The CYAT6165X controller has four power states, illustrated in **Figure 11**:

- Active, where the slider is actively scanned to determine the presence of a touch and identify the touch coordinates.
- Active look-for-touch, where the device performs a fast self-capacitive scan to determine if a touch exists.
- Low power, where the slider is scanned for touch presence at a much slower rate.
- Deepsleep, where the slider is not scanned and CYAT6165X is in a low power state with no processing.

The CYAT6165X controller automatically manages transitions between three power states (Active, Active Look-for-touch, and Low Power). The host can force transition in and out of the fourth power state (Deepsleep).

The active state emphasizes low refresh time for accurate finger tracking, the active look-for-touch state allows fast first-touch response, and the low power state enables low power consumption during periods of no touch activity. In all three states, the CYAT6165X controller periodically scans the panel to determine the presence of a touch. If a touch is present, the controller either enters or remains in the active state where it identifies the touch coordinates. These tasks occur at different rates in the three states and the detection of touches affects transitions between the states. Transition from active to active look-for-touch occurs when no touch is detected.

Host can request to disable low-power thus forcing CYAT61X controller to stay out of the Low-Power state at all times for the fastest response to the first touch on the panel.

The following parameters configure power states, which can be configured by the host:

- Refresh interval (register ACT_INTRVL) sets the minimum time between the start of subsequent slider scans in the active state.
- Active Look-for-touch interval (register ACT_LFT_INTRVL) sets the minimum refresh time in the active look-for-touch state.
- Active Mode Timeout (register TCH_TMOUT) sets the period of time in which no touch is detected during the active look-for-touch state before transitioning to the low power state.
- Low-Power Interval (register LP_INTRVL) sets the time in the low power state between slider scans.
- Deep Sleep is entered via a command from the host to move the device into the Deepsleep state. Automatic entry into the low power state is enabled by setting the LOW_POWER_ENABLE parameter.

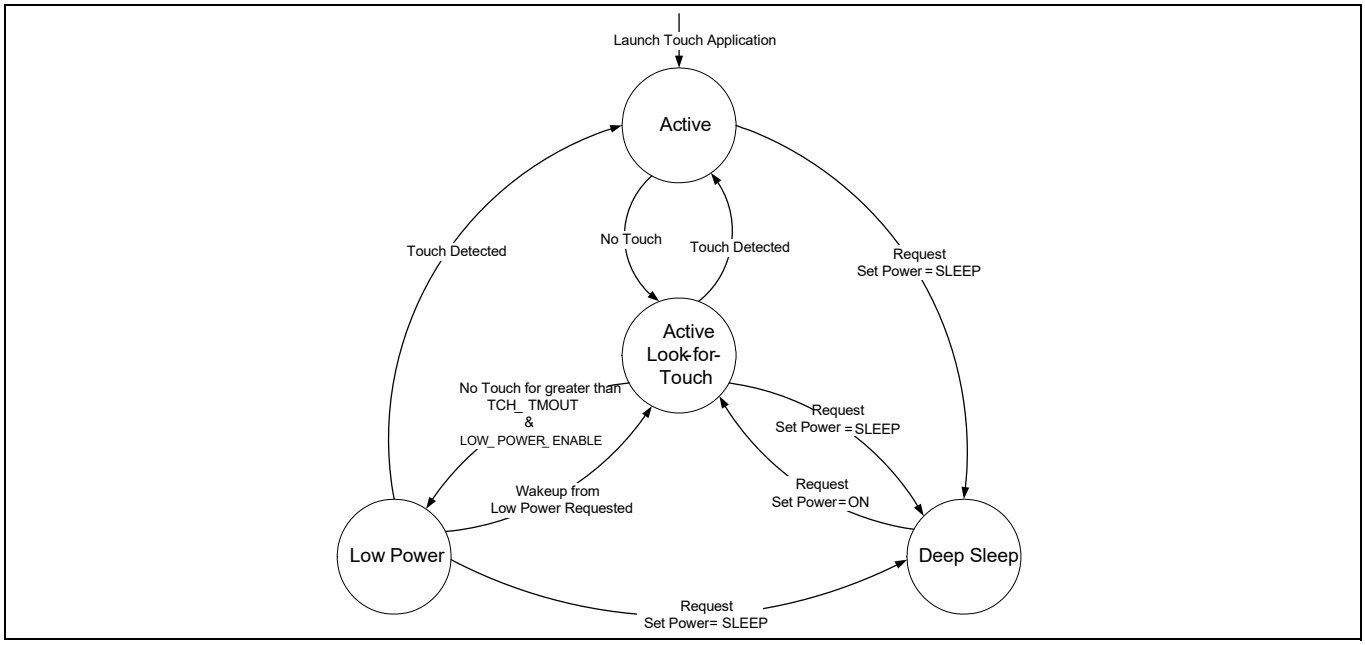


Figure 11 CYAT6165X power states and transitions

8 Pin information

CYAT6165X is available in a 56-pin QFN wettable flank package and 64-pin TQFP package. This section lists pin names, descriptions, and mappings to the physical package. Input and output pins may have more than one possible configuration. Guidance for each configuration option is provided below:

XY: XY pins may be configured as either transmit (TX) drive or receive (RX) sense, allowing each design to be optimized based on the sensor pattern and layout. See **PSoC™ Automotive Multitouch Touchscreen Controller Module Design Best Practices (001-50467)**, for guidelines. To configure the device for lowest power, leave unused XY pins unconnected. TX and RX pins are tied to VSS internally during the Deepsleep power state.

P1: Unused port 1 pin should be left unconnected.

External Reset (XRES): If the XRES pin is unused, it must be connected to V_{DDD} (either directly or through an external resistor).

SWD: Serial wire debug (SWD) is the recommended programming mode for all designs. If SWD is not used on the target board, use the bootloader to upgrade firmware.

COMM_INT: The COMM_INT pin is required. This interrupt pin is used for the host communication. If resistive mode is used, note that all I/Os are Hi-Z during chip initialization (after XRES or Bootloader Exit), so an additional external resistor is recommended.

P1[0] (WAKE): Wake pin indicates the status of the low power wake up button.

P1[1] (HOST RESET): The Host reset pin is used to send a reset pulse to the host controller on specific predefined conditions.

Pin Configurations: Multiple pin configurations are supported using the Touch Tuning Host Emulator (TTHE) software. Pins are configured using the TTHE Pin Configuration Wizard.

Table 3 56-pin QFN pin list

Pin	Name	Type		Description
		Digital	Analog	
1	XY13	–	I/O	TX/RX sense pin 13, RX channel 0
2	XY12	–	I/O	TX/RX sense pin 12, RX channel 8
3	XY11	–	I/O	TX/RX sense pin 11, RX channel 7
4	XY10	–	I/O	TX/RX sense pin 10, RX channel 6
5	XY09	–	I/O	TX/RX sense pin 09, RX channel 5
6	XY08	–	I/O	TX/RX sense pin 08, RX channel 4
7	XY07	–	I/O	TX/RX sense pin 07, RX channel 3
8	XY06	–	I/O	TX/RX sense pin 06, RX channel 2
9	XY05	–	I/O	TX/RX sense pin 05, RX channel 1
10	XY04	–	I/O	TX/RX sense pin 04, RX channel 0
11	XY03	–	I/O	TX/RX sense pin 03, RX channel 8
12	XY02	–	I/O	TX/RX sense pin 02, RX channel 7
13	XY01	–	I/O	TX/RX sense pin 01, RX channel 6
14	XY00	–	I/O	TX/RX sense pin 00, RX channel 5
15	VSS	Power		Connect to ground
16	P0[0]	I/O	–	I2C SCL / SPI SCLK
17	P0[1]	I/O	–	I2C SDA / SPI MOSI
18	XRES	I	–	External active LOW reset, no internal pull-up
19	P1[0]	I/O	–	SWDCLK / SPI MISO / EXT_START / WAKE
20	P1[1]	I/O	–	SWDIO / SPI SS / EXT_SYNC / HOST_RESET
21	P1[2]	I/O	–	ERROR - Set high when internal error is detected
22	P1[3]	I/O	–	COMM_INT
23	VCCD	Power		Digital core power supply input/output
24	VDDD	Power		Digital power supply input
25	VSS	Power		Connect to ground
26	VSS	Power		Connect to ground
27	VDDA	Power		Tx/Rx power supply input
28	VCCTX	Power		TX pump reservoir and filter capacitor connection point
29	XY40	–	I/O	TX/RX sense pin 40, RX channel 13
30	XY39	–	I/O	TX/RX sense pin 39, RX channel 12
31	XY38	–	I/O	TX/RX sense pin 38, RX channel 11
32	XY37	–	I/O	TX/RX sense pin 37, RX channel 10
33	XY36	–	I/O	TX/RX sense pin 36, RX channel 9
34	XY35	–	I/O	TX/RX sense pin 35, RX channel 16
35	XY34	–	I/O	TX/RX sense pin 34, RX channel 15
36	XY33	–	I/O	TX/RX sense pin 33, RX channel 14
37	XY32	–	I/O	TX/RX sense pin 32, RX channel 13
38	XY31	–	I/O	TX/RX sense pin 31, RX channel 12

Table 3 56-pin QFN pin list (continued)

Pin	Name	Type		Description
		Digital	Analog	
39	XY30	–	I/O	TX/RX sense pin 30, RX channel 11
40	XY29	–	I/O	TX/RX sense pin 29, RX channel 16
41	XY28	–	I/O	TX/RX sense pin 28, RX channel 15
42	XY27	–	I/O	TX/RX sense pin 27, RX channel 14
43	XY26	–	I/O	TX/RX sense pin 26, RX channel 13
44	XY25	–	I/O	TX/RX sense pin 25, RX channel 12
45	XY24	–	I/O	TX/RX sense pin 24, RX channel 11
46	XY23	–	I/O	TX/RX sense pin 23, RX channel 10
47	XY22	–	I/O	TX/RX sense pin 22, RX channel 9
48	VSS	Power		Connect to ground
49	XY21	–	I/O	TX/RX sense pin 21, RX channel 8
50	XY20	–	I/O	TX/RX sense pin 20, RX channel 7
51	XY19	–	I/O	TX/RX sense pin 19, RX channel 6
52	XY18	–	I/O	TX/RX sense pin 18, RX channel 5
53	XY17	–	I/O	TX/RX sense pin 17, RX channel 4
54	XY16	–	I/O	TX/RX sense pin 16, RX channel 3
55	XY15	–	I/O	TX/RX sense pin 15, RX channel 2
56	XY14	–	I/O	TX/RX sense pin 14, RX channel 1

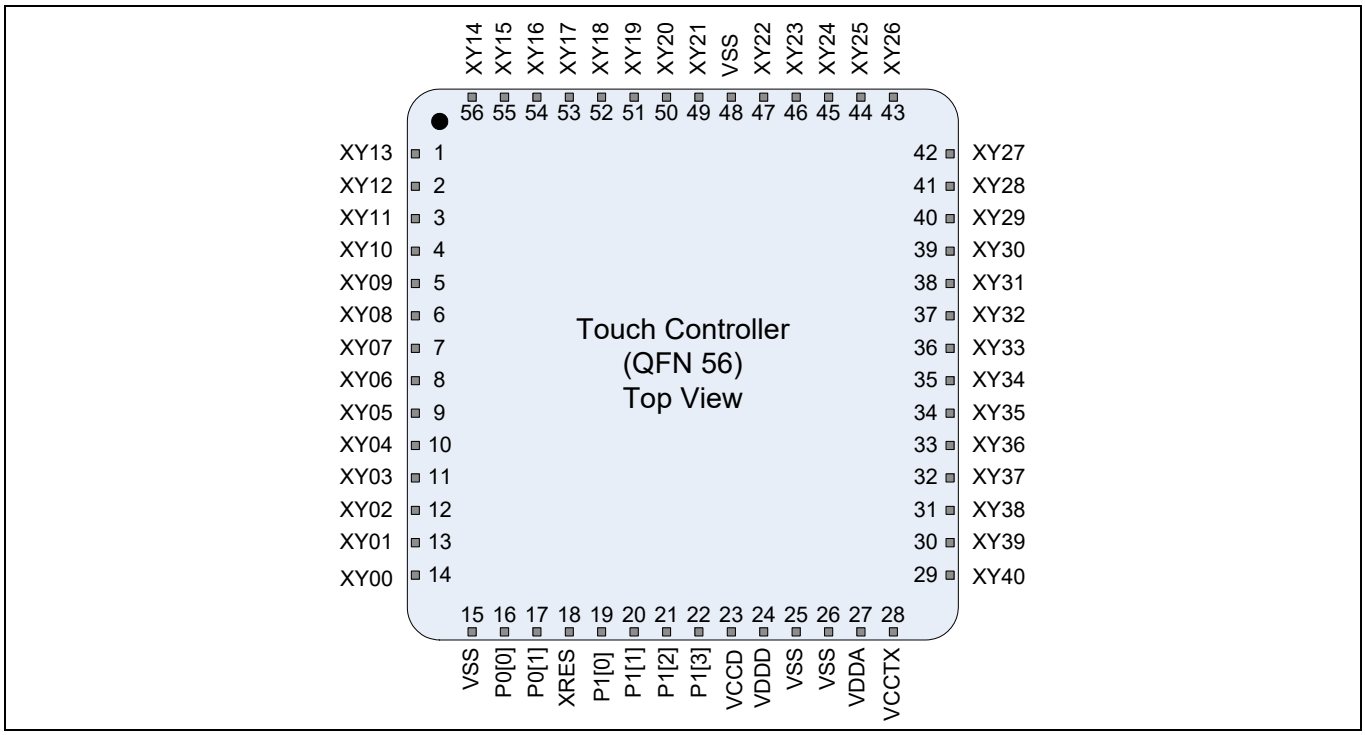


Figure 12 56-pin QFN pinout

Table 4 64-pin TQFP pin list

Pin No.	Name	Type		Description
		Digital	Analog	
1	XY17	–	I/O	TX/RX sense pin 17, Rx channel 2
2	XY16	–	I/O	TX/RX sense pin 16, Rx channel 1
3	XY15	–	I/O	TX/RX sense pin 15, Rx channel 0
4	XY14	–	I/O	TX/RX sense pin 14, Rx channel 8
5	XY13	–	I/O	TX/RX sense pin 13, Rx channel 7
6	XY12	–	I/O	TX/RX sense pin 12, Rx channel 6
7	XY11	–	I/O	TX/RX sense pin 11, Rx channel 5
8	XY10	–	I/O	TX/RX sense pin 10, Rx channel 4
9	XY09	–	I/O	TX/RX sense pin 09, Rx channel 3
10	XY08	–	I/O	TX/RX sense pin 08, Rx channel 2
11	XY07	–	I/O	TX/RX sense pin 07, Rx channel 1
12	XY06	–	I/O	TX/RX sense pin 06, Rx channel 0
13	XY05	–	I/O	TX/RX sense pin 05, Rx channel 8
14	XY04	–	I/O	TX/RX sense pin 04, Rx channel 7
15	XY03	–	I/O	TX/RX sense pin 03, Rx channel 6
16	XY02	–	I/O	TX/RX sense pin 02, Rx channel 5
17	XY01	–	I/O	TX/RX sense pin 01, Rx channel 4
18	XY00	–	I/O	TX/RX sense pin 00, Rx channel 3
19	VSS	Power		Connect to ground
20	P0[0]	I/O	–	I2C SCL / SPI SCLK
21	P0[1]	I/O	–	I2C SDA / SPI MOSI
22	XRES	I	–	External active LOW reset, no internal pull-up
23	P1[0]	I/O	–	SWDCLK / SPI MISO / EXT_START /WAKE
24	P1[1]	I/O	–	SWDIO / SPI SS / EXT_SYNC / HOST_RESET
25	P1[2]	I/O	–	ERROR - Set high when internal error is detected
26	P1[3]	I/O	–	COMM_INT
27	VCCD	Power		Digital core power supply input/output
28	VDDD	Power		Digital power supply input
29	VSS	Power		Connect to ground
30	VSS	Power		Connect to ground
31	VDDA	Power		Tx/Rx power supply input
32	VDDA_Q	Power		Tx/Rx power supply input
33	VCCTX	Power		TX pump reservoir and filter capacitor connection point
34	XY47	–	I/O	TX/RX sense pin 47, Rx channel 16
35	XY46	–	I/O	TX/RX sense pin 46, Rx channel 15
36	XY45	–	I/O	TX/RX sense pin 45, Rx channel 14
37	XY44	–	I/O	TX/RX sense pin 44, Rx channel 13
38	XY43	–	I/O	TX/RX sense pin 43, Rx channel 12

Table 4 64-pin TQFP pin list (continued)

Pin No.	Name	Type		Description
		Digital	Analog	
39	XY42	–	I/O	TX/RX sense pin 42, Rx channel 11
40	XY41	–	I/O	TX/RX sense pin 41, Rx channel 10
41	XY40	–	I/O	TX/RX sense pin 40, Rx channel 09
42	XY39	–	I/O	TX/RX sense pin 39, Rx channel 16
43	XY38	–	I/O	TX/RX sense pin 38, Rx channel 15
44	XY37	–	I/O	TX/RX sense pin 37, Rx channel 14
45	XY36	–	I/O	TX/RX sense pin 36, Rx channel 13
46	XY35	–	I/O	TX/RX sense pin 35, Rx channel 12
47	XY34	–	I/O	TX/RX sense pin 34, Rx channel 11
48	XY33	–	I/O	TX/RX sense pin 33, Rx channel 10
49	XY32	–	I/O	TX/RX sense pin 32, Rx channel 09
50	XY31	–	I/O	TX/RX sense pin 31, Rx channel 16
51	XY30	–	I/O	TX/RX sense pin 30, Rx channel 15
52	XY29	–	I/O	TX/RX sense pin 29, Rx channel 14
53	XY28	–	I/O	TX/RX sense pin 28, Rx channel 13
54	XY27	–	I/O	TX/RX sense pin 27, Rx channel 12
55	XY26	–	I/O	TX/RX sense pin 26, Rx channel 11
56	XY25	–	I/O	TX/RX sense pin 25, Rx channel 10
57	XY24	–	I/O	TX/RX sense pin 24, Rx channel 09
58	VSS	Power		Connect to ground
59	XY23	–	I/O	TX/RX sense pin 23, Rx channel 8
60	XY22	–	I/O	TX/RX sense pin 22, Rx channel 7
61	XY21	–	I/O	TX/RX sense pin 21, Rx channel 6
62	XY20	–	I/O	TX/RX sense pin 20, Rx channel 5
63	XY19	–	I/O	TX/RX sense pin 19, Rx channel 4
64	XY18	–	I/O	TX/RX sense pin 18, Rx channel 3

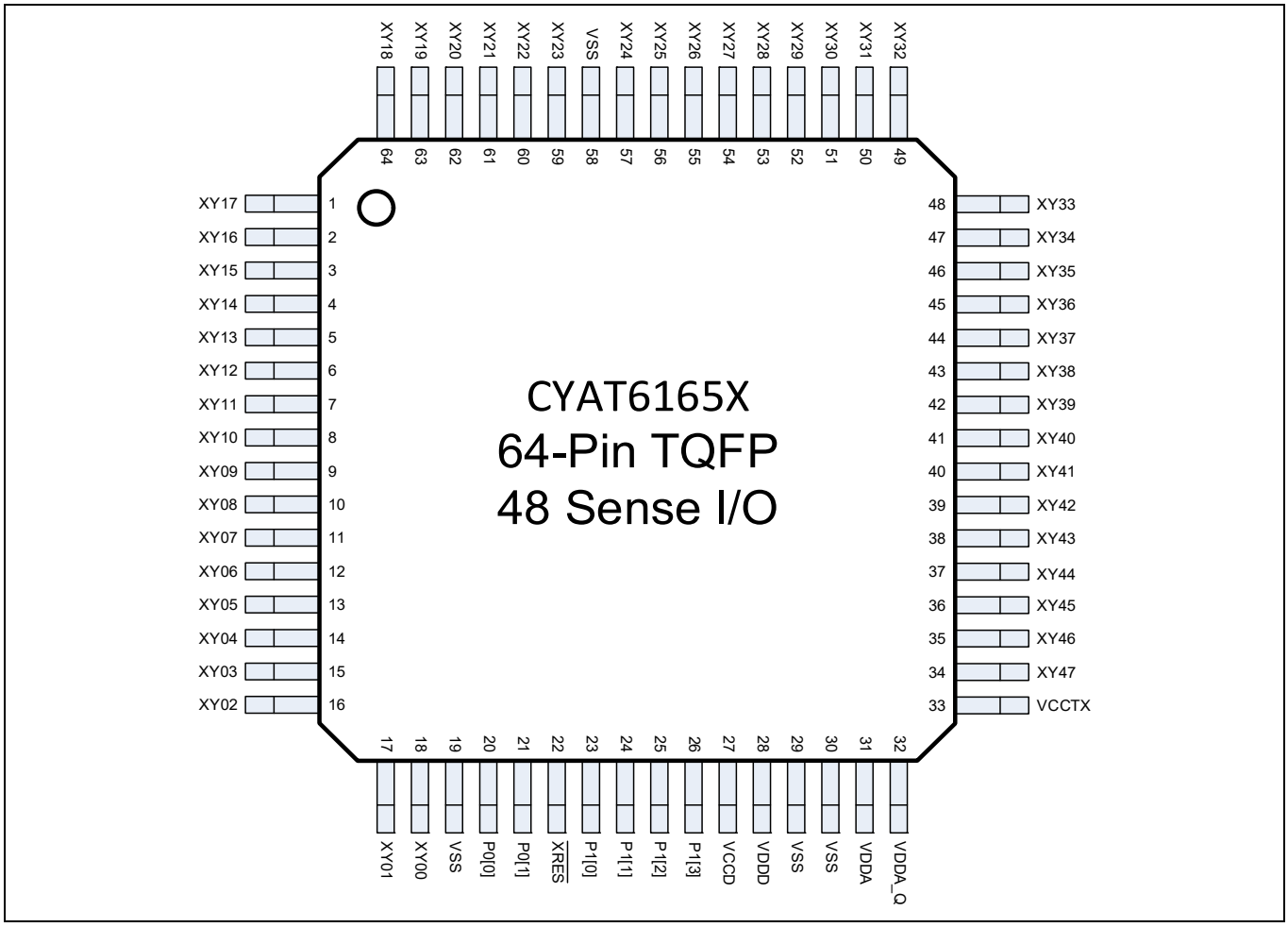


Figure 13 64-pin TQFP pinout

9 Electrical Specifications

This section lists CYAT6165X DC and AC electrical specifications.

9.1 Absolute maximum ratings

Table 5 Absolute maximum ratings

Symbol	Description	Conditions	Min	Typ	Max	Unit
T_{STG}	Storage temperature	–	–55	25	125	°C
V_{DDD}	Digital supply voltage	–	V_{SS} – 0.5	–	6	V
V_{DDA}	Analog supply voltage	–	V_{SS} – 0.5	–	6	
V_{DDDR}	Amplitude (V_{PP}) of digital (V_{DDD}) supply ripple riding on the DC voltage	DC to 20 MHz	–	–	100	mV
V_{DDAR}[8]	Amplitude (V_{PP}) of analog (V_{DDA}) supply ripple riding on the DC voltage (TX pump enabled)	DC to 20 MHz	–	–	100	
	Amplitude (V_{PP}) of analog (V_{DDA}) supply ripple riding on the DC voltage (TX pump disabled)	DC to 150 kHz[9]	–	–	15	
		150 kHz[9] to 20 MHz	–	–	15 + 20 dB/decade > 150 kHz[9]	
V_{CCD}	Core supply voltage	–	V_{SS} – 0.5	–	2.3	V
V_{GPIO}	Port 0 pin voltage	Driver enabled	V_{SS} – 0.5	–	6	
	Port 0 pin voltage	Driver disabled	V_{SS} – 0.5	–	7	
	Port 1 pin voltage	–	V_{SS} – 0.5	–	V_{DDD} + 0.5	
I_{IO}	Current into I/O pin	–	–25	–	50	mA
ESD_{CDM}	Electrostatic discharge voltage	Charge device model	1500	–	–	V
ESD_{HBM}	Electrostatic discharge voltage	Human body model	5000	–	–	

9.2 Operating temperature

Table 6 Operating temperature

Symbol	Description	Conditions	Min	Typ	Max	Unit
T_A	Ambient temperature (A-grade)	–	–40	–	85	°C
T_A	Ambient temperature (S-grade)	–	–40	–	105	

Notes

8. Analog supply ripple specifications are valid for the supply presented to the external resistor (for example, label “V” in **Figure 6**), not at the device VDDA and VDDA_Q pin.
9. If a 2.2-µF capacitor is used in place of a 1-µF capacitor, the threshold is 80 kHz.

9.3 DC specifications

The specifications in this section are valid under these conditions:
–40°C ≤ T_A ≤ 85°C for Grade-A devices, –40°C ≤ T_A ≤ 105°C for Grade-S devices.

9.3.1 Flash specifications

The specifications in **Table 7** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 7 Flash specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	10,000	–	–	cycles
$Flash_{DR}$	Flash data retention	Following maximum Flash write cycles ($Flash_{ENPB}$), T_A ≤ 55°C	20[10]	–	–	years
		Following maximum Flash write cycles ($Flash_{ENPB}$), T_A > 55°C	10[10]	–	–	

Note
10. Storing programmed devices at or above the ambient temperature specified by $Flash_{DR}$ may reduce flash data retention time. Infineon provides a retention calculator to calculate the retention lifetime based on customer's individual temperature profiles for operation over the ambient temperature range for the device's temperature rating. For more information, contact our support team at **support@infineon.com**.

9.3.2 Chip-level DC specifications

The specifications in **Table 8** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 8 Chip-level DC specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDD}	Digital supply voltage	Core LDO enabled (V_{CCD} output)	3.0	–	5.5	V
		Core LDO disabled (V_{CCD} input)[11]	1.71	1.8	1.95	
V_{CCD}	Digital core supply voltage	Core LDO enabled (V_{CCD} output)	–	1.8	–	
		Core LDO disabled (V_{CCD} input)[11]	1.71	1.8	1.95	
V_{DDA}[11]	Analog supply voltage	TX pump enabled	3.0	–	4.7	
		TX pump disabled	3.0	–	5.5	
V_{CCTX}	V_{CCTX} supply operating voltage range	Input to external low-pass filter, external V_{CCTX} configuration	3.0	–	5.5	
PSA_{RAMP}	V_{DDA} ramp rate from ground to minimum voltage	–	–	–	100	V/ms
PSD_{RAMP}	V_{DDD} ramp rate from ground to minimum voltage	–	1[12]	–	40	
$PSD_{RAMPDOWN}$	V_{DDD} ramp down rate from 1.5 V to 1.0 V	–	1[12]	–	40	
I_{DDD_ACT}	V_{DDD} active current	–	–	20	50	mA
I_{DDA_ACT}	V_{DDA} active current	–	–	15	20	
I_{DDD_DS}	V_{DDD} deep sleep current	–	–	3	–	µA
I_{DDA_DS}	V_{DDA} deep sleep current	–	–	2	–	
I_{DDD_XR}	V_{DDD} current, $\overline{XRES}$ = LOW	1.71 V ≤ V_{DDD} ≤ 1.95 V	–	5	–	
		3.0 V ≤ V_{DDD} ≤ 5.5 V	–	1	–	
I_{DDA_XR}	V_{DDA} current, $\overline{XRES}$ = LOW	–	–	25	–	
I_{DDD_P}	V_{DDD} flash programming and flash verify current	–	–	5	25	mA

Notes

11. These Min and Max limits are inclusive of noise. For proper operation, V_{DDA} or V_{DDD} with combined noise cannot go below or above the specified Min or Max limits.
12. If minimum ramp rate cannot be met, XRES should be asserted during voltage ramp (1.5 V > V_{DDD} >1.0 V for ramp-down or until voltage is stable for ramp-up). Note that a glitch on the I^2C bus could occur during voltage ramp in this case.

9.3.3 I/O port 0 (P0[0:1]) DC specifications

The port 0 specifications in **Table 9** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 9 I/O port 0 (P0[0:1]) DC specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage	CMOS mode	0.7 × V_{DDD}	–	–	V
		1.8-V mode, V_{EXT}[14] = 1.8 V, 3.0 V ≤ V_{DDD} ≤ 5.5 V	0.7 × V_{EXT}	–	–	
V_{IL}	Input low voltage	CMOS mode	–	–	0.3 × V_{DDD}	
		1.8-V mode, V_{EXT}[14] = 1.8 V, 3.0 V ≤ V_{DDD} ≤ 5.5 V	–	–	0.3 × V_{EXT}	
V_{OH}	High output voltage	Reference to V_{DDD}, I_{OH} = 1 mA, V_{DDD} = 1.8 V	V_{DDD} – 0.5	–	–	
		Reference to V_{DDD}, I_{OH} = 4 mA, V_{DDD} = 3.0 V	V_{DDD} – 0.6	–	–	
V_{OL}	Low output voltage	V_{DDD} ≥ 1.71 V, I_{OL} = 10 mA	–	–	0.6	
		V_{DDD} ≥ 1.71 V, I_{OL} = 3 mA	–	–	0.4	
V_H	Input hysteresis	–	0.1 × V_{DDD}	–	–	
T_{RISE_OV}	Output rise time Fast-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	2	–	12	ns
	Output rise time Slow-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	10	–	60	
T_{FALL_OV}	Output fall time Fast-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	1.5	–	12	
	Output fall time Slow-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	10	–	60	
I_{IL}[13]	Input leakage current (absolute value)	T_A = 25°C, V_{DDD} = 3.0 V	–	–	14	nA
		T_A = 25°C, V_{DDD} = 0.0 V	–	–	10	µA
C_{IN}	Input pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	pF
C_{OUT}	Output pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	
R_{INT}	Internal pull-up / pull-down resistance	Pin configured for internal pull-up or pull-down; note that all I/Os are Hi-Z during chip initialization (after XRES or Bootloader Exit)	3.5	5.6	8.5	kΩ

Notes
13. Gang tested with all I/Os to 1 µA.
14. V_{EXT} is the external supply used to bias the pull-up resistor when used on an I^2C bus.

9.3.4 I/O port 1 (P1[0:3]) and $\overline{\text{XRES}}$ DC specifications

The specifications in **Table 10** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 10 I/O port 1 (P1[0:3]) and $\overline{\text{XRES}}$ DC specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input voltage high threshold	1.8-V configuration	1.26	–	–	V
		CMOS configuration	0.7 × V_{DDD}	–	–	
		XRES	1.35	–	–	
V_{IL}	Input voltage low threshold	1.8-V configuration	–	–	0.54	
		CMOS configuration	–	–	0.3 × V_{DDD}	
		XRES	–	–	0.45	
V_{OH}	High output voltage	I_{OH} = 4 mA, V_{DDD} = 3.0 V	V_{DDD} – 0.6	–	–	
		I_{OH} = 1 mA, V_{DDD} = 1.8 V	V_{DDD} – 0.5	–	–	
V_{OL}	Low Output Voltage	I_{OL} = 8 mA, V_{DDD} = 3.3 V	–	–	0.6	
		I_{OL} = 4 mA, V_{DDD} = 1.8 V	–	–	0.6	
V_H	Input hysteresis voltage	–	0.1 × V_{DDD}	–	–	
T_{RISE_G}	Output rise time Fast-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	2	–	12	ns
	Output rise time Slow-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	–	–	60	
T_{FALL_G}	Output fall time Fast-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	2	–	12	
	Output fall time Slow-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	–	–	60	
I_{IL}[15]	Input leakage (absolute value)		–	–	2	nA
C_{IN}	Input pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	pF
C_{OUT}	Output pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	
R_{INT}[16]	Internal pull-up/pull-down resistance	Pin configured for internal pull-up or pull-down	3.5	5.6	8.5	kΩ

Notes
15. Gang tested with all I/Os to 1 µA.
16. $\overline{\text{XRES}}$ is input only with no internal pull-up or pull-down resistor.

9.4 AC specifications

The specifications in this section are valid under these conditions:
–40°C ≤ T_A ≤ 85°C for Grade-A devices, –40°C ≤ T_A ≤ 105°C for Grade-S devices.

9.4.1 SWD interface AC specifications

The specifications in **Table 11** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, 3.0 V ≤ V_{DDA} ≤ 5.5 V, and C_{LOAD} = 25 pF. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 11 SWD interface AC specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SWDCLK}	SWDCLK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	14	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	8	
T_{SWDI_SETUP}	SWDIO input setup before SWDCLK HIGH	T = 1 / f_{SWDCLK}	T / 4	–	–	ns
T_{SWDI_HOLD}	SWDIO input hold after SWDCLK HIGH	T = 1 / f_{SWDCLK}	T / 4	–	–	
T_{SWDO_VALID}	SWDCLK HIGH to SWDIO output valid	T = 1 / f_{SWDCLK}	–	–	T / 2	
T_{SWDO_HOLD}	SWDIO output hold after SWDCLK HIGH	T = 1 / f_{SWDCLK}	1	–	–	

9.4.2 Chip-level AC specifications

The specifications in **Table 12** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 12 Chip-level AC specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
T_{XRST}	External reset (XRES) pulse width	After V_{DDD} is valid	10	–	–	µs
T_{READY}	Time from deassertion of XRES to COMM_INT	–	–	–	35	ms
T_{CAL}	Calibration routine execution time	–	–	–	2000	
$F_{IMOTOL1}$	Frequency variation at 37 MHz and 48 MHz	–	–	–	±2	%
$T_{COMM\_EXIT\_CRC}$	Time from EXIT BTLDR command (with CRC checking) to SYS INFO MODE	POST_SHORT_OPEN_CTRL - “Disabled All” [17]	–	40	–	ms

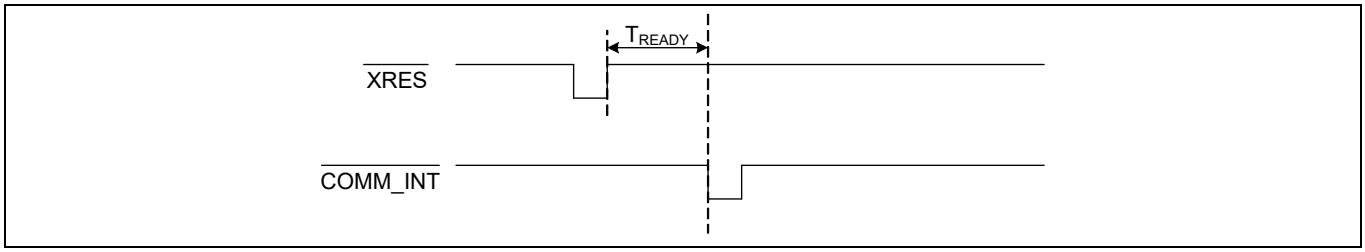


Figure 14 COMM_INT timing diagram

Note
17.For POST_SHORT_OPEN_CTRL - “Enabled All”, there will be an additional 100 ms during startup.

9.4.3 I²C specifications

The specifications in **Table 13** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V. CYAT6165X does not require a clock-stretch capable host, but is fully compatible with systems that perform clock-stretching.

To ensure proper I²C functionality in extreme bus conditions, refer to Infineon's application note **Using CY8CTMA4/5XX I²C in Systems With Slow Clock Edges (001-81514)**[18].

Important Note: The P0[0] and P0[1] pins have I/O cells optimized for use on multi-drop buses. When the touch device is powered off, the pin drivers do not load the attached bus, such that other devices attached to them may continue to communicate.

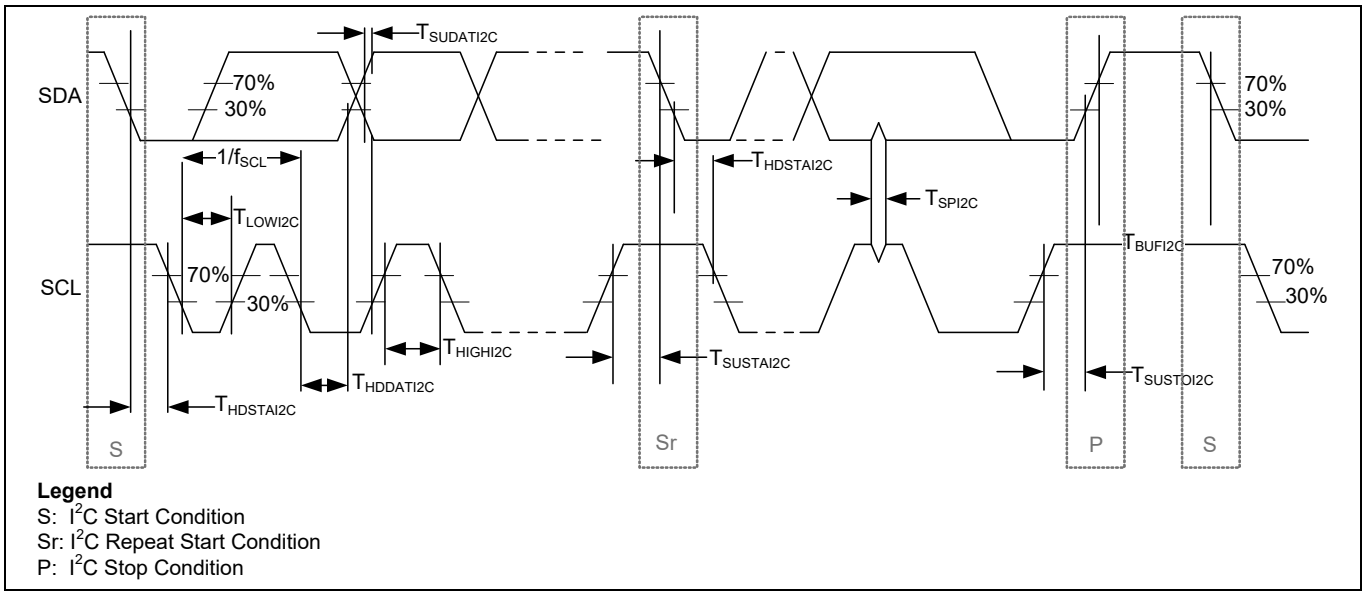


Figure 15 I²C Bus timing diagram for fast/standard mode

Note

18. Extreme bus conditions are considered to be a combination of the following conditions: High-capacitive bus load, slow SCL fall time, and fast SDA rise/fall time. Infineon reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@infineon.com**.

Table 13 AC characteristics of the I²C SDA and SCL pins

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	4	–	0.6	–	µs
T_{LOWI2C}	LOW period of SCL clock	4.7	–	1.3	–	
$T_{HIGHI2C}$	HIGH period of SCL clock	4	–	0.6	–	
$T_{SUSTAI2C}$	Setup time for repeated start condition	4.7	–	0.6	–	
$T_{HDDATI2C}$	Data hold time	0	–	0	–	
$T_{SUDATI2C}$	Data setup time	250	–	100	–	ns
$T_{VDDATI2C}$	Data valid time	–	3.45	–	0.9	µs
$T_{VDACKI2C}$	Data acknowledge time	–	3.45	–	0.9	
$T_{SUSTOI2C}$	Setup time for stop condition	4	–	0.6	–	
V_{HH}	Input hysteresis high voltage, $1.71\ V \le V_{DDD} \le 1.95\ V$ or $3.0\ V \le V_{DDD} \le 5.5\ V$	$0.1 \times V_{DDD}$	–	$0.1 \times V_{DDD}$	–	V
T_{BUFI2C}	Bus free time between a stop and start condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes that are suppressed by input filter	–	–	50	–	ns
C_{BUS}	Capacitance load for SDA or SCL	–	400	–	400	pF
V_{IL_I2C}	Input low voltage	–0.5	$0.3 \times V_{DDD}$	–0.5	$0.3 \times V_{DDD}$	V
V_{IH_I2C}	Input high voltage	$0.7 \times V_{DDD}$	–	$0.7 \times V_{DDD}$	–	
$V_{OL\_I2C\_L}$	Output low voltage ($V_{DDD} \le 2$ V, 3 mA sink)	–	$0.2 \times V_{DDD}$	–	$0.2 \times V_{DDD}$	
$V_{OL\_I2C\_H}$	Output low voltage ($V_{DDD} > 3$ V, 3 mA sink)	–	0.4	–	0.4	
I_{OL_I2C}	Output low current	–	3	–	3	mA
	Output low current $V_{OL} = 0.6$ V	–	–	–	6	
V_{H_I2C}	Input hysteresis	$0.1 \times V_{DDD}$	–	$0.1 \times V_{DDD}$	–	mV

9.4.4 SPI specifications

The specifications listed in **Table 14** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, 3.0 V ≤ V_{DDA} ≤ 5.5 V, and C_{LOAD} = 25 pF. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

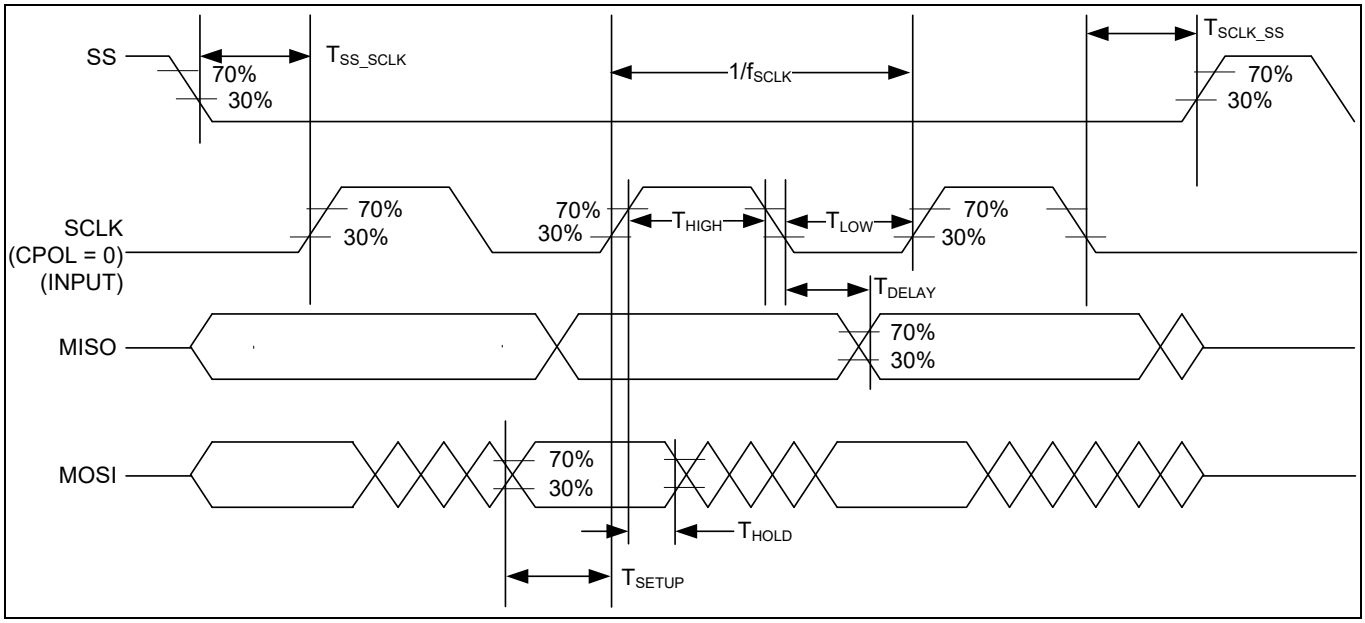


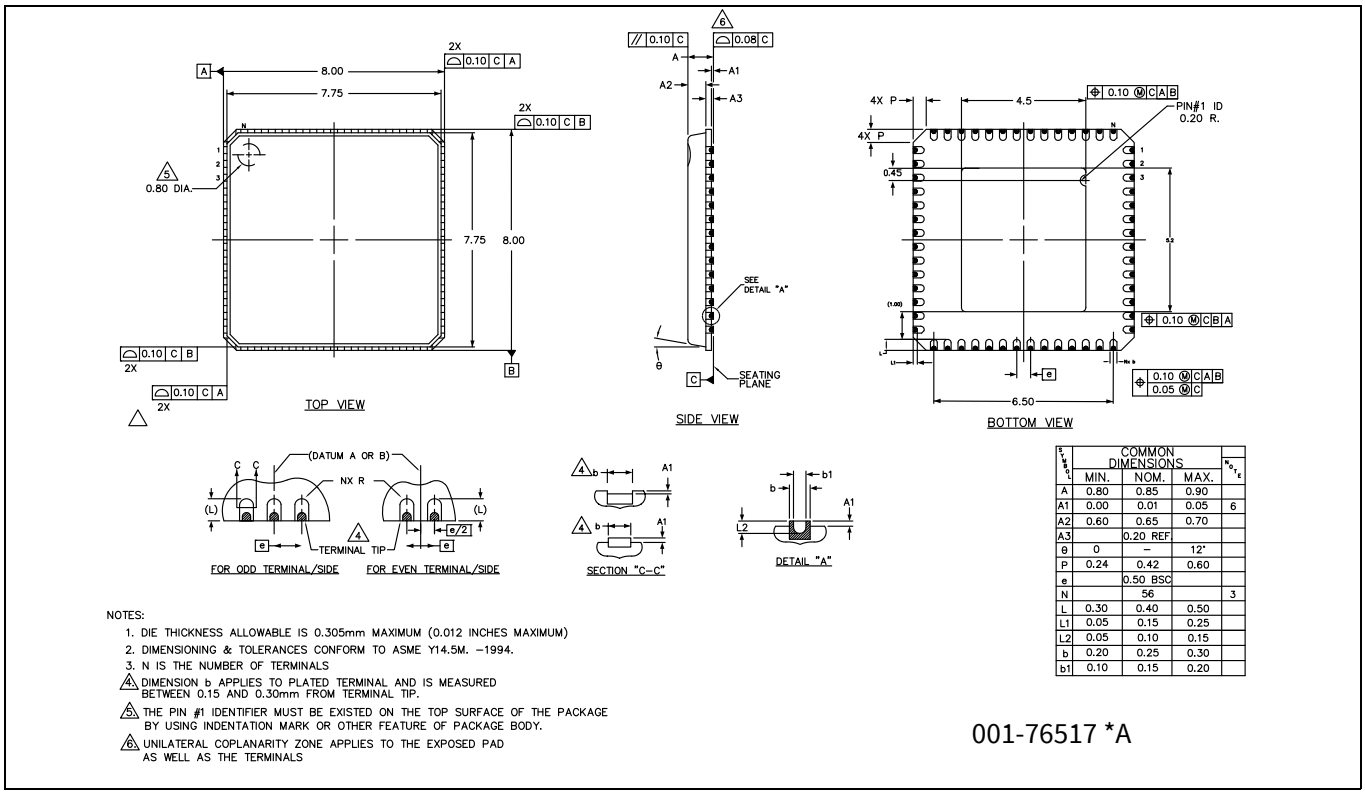
Figure 16 SPI timing diagram

Table 14 AC characteristics of SPI pins

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	–	–	–	8	MHz
$1/f_{SCLK}$	SPI SCLK cycle time (period)	–	125	–	–	ns
SDR_{SPI}	Sustained data rate for SPI transaction	–	–	–	8	Mbps
$T_{IDLESPI}$	Time between consecutive SPI transactions (duration between SS deactivation and the following SS activation)	–	125	–	–	ns
T_{LOW}	SCLK LOW time	–	50	–	–	
T_{HIGH}	SCLK HIGH time	–	50	–	–	
T_{SETUP}	MOSI setup to SCLK	–	30	–	–	
T_{HOLD}	MOSI hold from SCLK	–	30	–	–	
T_{DELAY}	MISO delay (hold) high voltage	V_{DDD} ≥ 3 V	0	–	45	
	MISO delay (hold) low voltage	V_{DDD} < 2 V	0	–	65	
T_{SS_SCLK}	Time from SS LOW to first SCLK	–	125	–	–	
T_{SCLK_SS}	Time from last SCLK to SS HIGH	–	125	–	–	

10 Packaging information

This section provides the CYAT6165X device packaging specifications.



SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	0.80	0.85	0.90	
A1	0.00	0.01	0.05	6
A2	0.60	0.65	0.70	
A3		0.20 REF.		
θ	0	–	12°	
P	0.24	0.42	0.60	
e		0.50 BSC		
N		56		3
L	0.30	0.40	0.50	
L1	0.05	0.15	0.25	
L2	0.05	0.10	0.15	
b	0.20	0.25	0.30	
b1	0.10	0.15	0.20	

Figure 17 56-pin QFN ((8 × 8 × 1.0 mm) LW56 4.5 × 5.2 E-Pad (Subcon punch type)) package outline, 001-76517

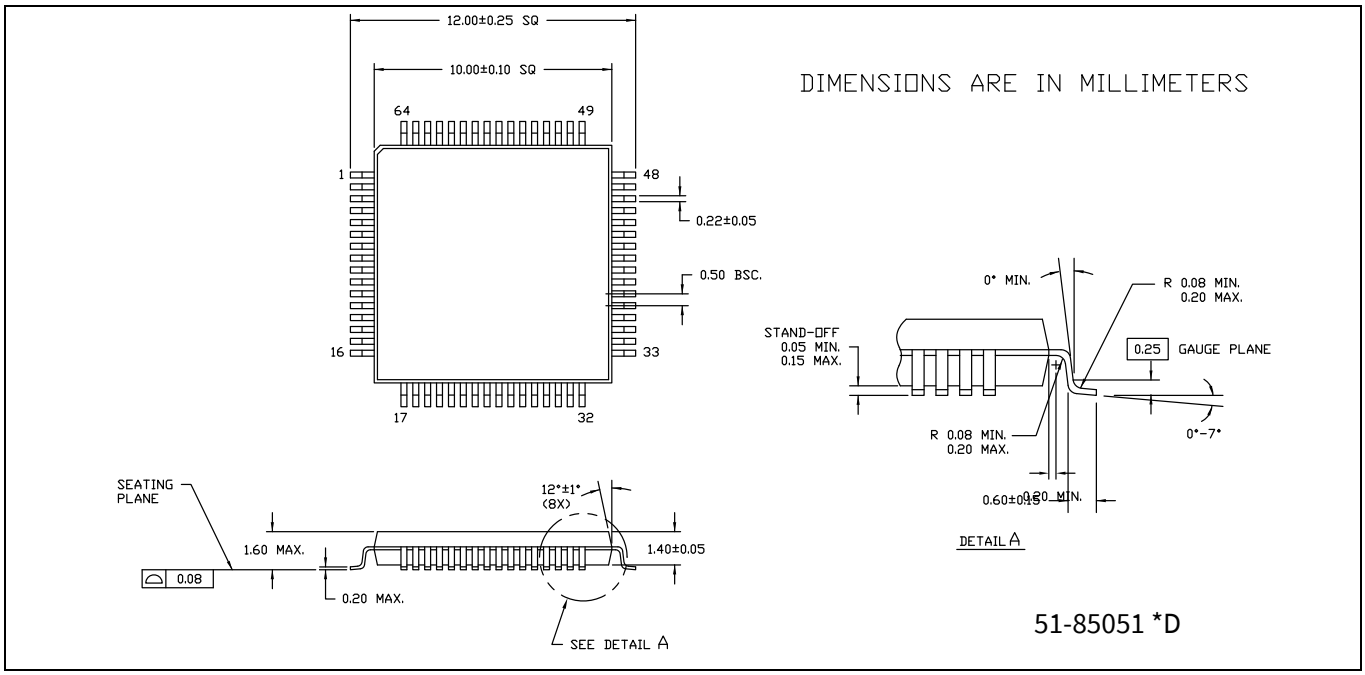


Figure 18 64-pin TQFP (10 × 10 × 1.4 mm) A64SB package outline, 51-85051

10.1 Thermal impedance and moisture sensitivity

Table 15 Thermal impedance and moisture sensitivity

Package	Typical θ_{JMAX}	Typical θ_{JA}	Typical θ_{JC}	Moisture sensitivity level
56-pin QFN	125°C	18.0°C/W [19]	3.5°C/W [19]	3
64-pin TQFP	125°C	42.8°C/W [19]	7.0°C/W [19]	3

10.2 Solder reflow specifications

Table 16 lists the maximum solder reflow peak temperature.

Important Note

Thermal ramp rate during preheat should be 3°C/s or lower. The packaged device supports Pb-free solder reflow profile as per section 5.6 of J-STD-020.D1.

Table 16 Solder reflow specifications

Package	Maximum peak temperature	Time at maximum temperature
All packages	260°C	30 seconds

Note

19.Measured at 25°C ambient on a 4-layer PCB.

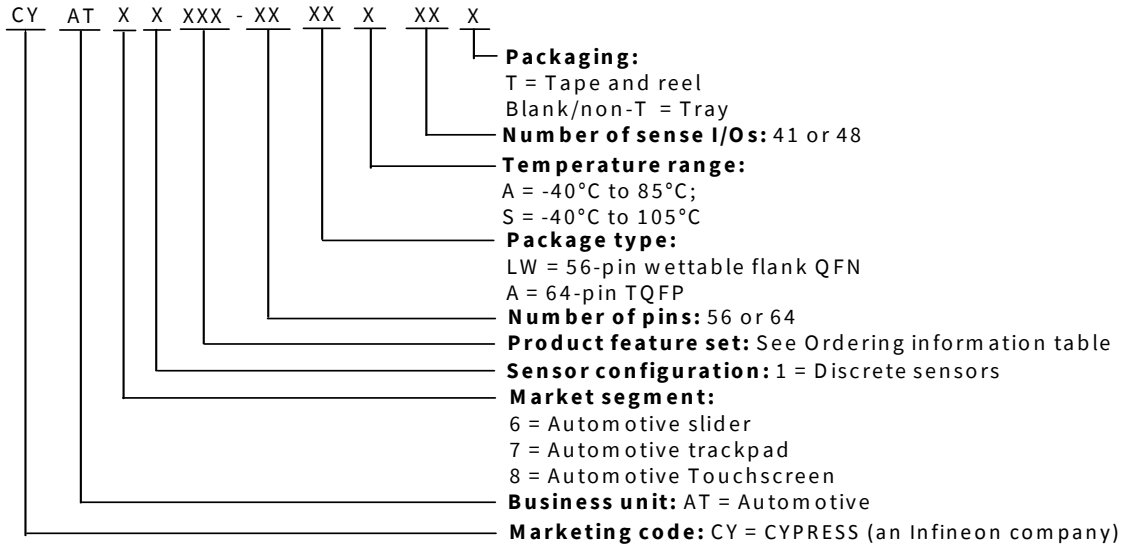
11 Ordering information

Table 17 lists the CYAT6165X slider controllers.

Table 17 Ordering information[20]

Marketing part number	Number of sense pins	Number of fingers	Slider	Wake up button support[21]	CAPSENSE™ buttons	Water rejection	Thin glove support	Gestures	Thick overlay/ thick glove support	Package
CYAT61652-56LWA41	41	10	✔	–	✔	✔	✔	–	–	56-pin QFN
CYAT61652-56LWS41	41	10	✔	–	✔	✔	✔	–	–	56-pin QFN
CYAT61658-56LWA41	41	10	✔	–	✔	✔	✔	–	✔	56-pin QFN
CYAT61658-56LWS41	41	10	✔	–	✔	✔	✔	–	✔	56-pin QFN
CYAT61659-56LWA41	41	10	✔	✔	✔	✔	✔	–	✔	56-pin QFN
CYAT61659-56LWS41	41	10	✔	✔	✔	✔	✔	–	✔	56-pin QFN
CYAT61652-64AA48	48	10	✔	–	✔	✔	✔	–	–	64-pin TQFP
CYAT61652-64AS48	48	10	✔	–	✔	✔	✔	–	–	64-pin TQFP
CYAT61658-64AA48	48	10	✔	–	✔	✔	✔	–	✔	64-pin TQFP
CYAT61658-64AS48	48	10	✔	–	✔	✔	✔	–	✔	64-pin TQFP
CYAT61659-64AA48	48	10	✔	✔	✔	✔	✔	–	✔	64-pin TQFP
CYAT61659-64AS48	48	10	✔	✔	✔	✔	✔	–	✔	64-pin TQFP

11.1 Ordering code definitions



Notes

20. All devices have the following base features: Water Rejection, DisplayArmor™, AutoArmor™, DualSense™, CAPSENSE™ buttons, and Large Object Detection and Rejection.
21. Not compatible with SPI due to pin limitations.

12 Acronyms

Table 18 Acronyms used in this document

Acronym	Description
CPU	central processing unit
DNU	do not use
DSD	dual-solid diamond pattern (**Figure 4**)
EMI	electromagnetic interference
ESD	electrostatic discharge
FPC	flexible printed circuit
I^2C	inter-integrated circuit
I/O	input/output
ITO	indium tin oxide
LDO	low dropout regulator
MH3	Manhattan-3 pattern (**Figure 5**)
MTK	manufacturing test kit
PCB	printed circuit board
PET	polyethylene terephthalate
QFN	quad flat no-lead
SCL	serial I^2C clock
SD	signal disparity
SDA	serial I^2C data
SMT	surface mount technology
SNR	signal-to-noise ratio
SSD	single-solid diamond pattern (**Figure 3**)
SWD	serial wire debug
SWDCLK	serial wire debug clock
TQFP	thin quad flat pack
TRM	technical reference manual
TTHE	touch tuning host emulator
V_{PP}	volts peak-to-peak

13 Reference documents

Infineon has created a collection of documents to support the design of PSoC™ Automotive Multitouch slider controllers.

The following list will guide you in identifying the proper document for your task:

- PCB/FPC Schematic and Layout Design
- ITO Panel Design
- Driver Development
- Manufacturing (MFG)
- System Performance Evaluation

Infineon's PSoC™ Automotive Multitouch technology is Infineon confidential information and is protected through a Non-Disclosure Agreement (NDA). These documents are not publicly available on the Infineon website. Contact your local Infineon office to request any of these documents pursuant to the aforementioned NDA. You can also direct your requests to **automotive@infineon.com**.

Table 19 Reference specifications

Document number	Document title	Description	PCB FPC	ITO panel	Driver	MFG	System
Solution specifications							
001-49389	PSoC™ Automotive Multitouch Touchscreen Controller User Interface Performance Definitions	Contains Infineon touchscreen performance parameter definitions, justification for parameters, and parameter test methodologies.	–	✔	–	–	✔
001-50467	PSoC™ Automotive Multitouch Touchscreen Controller Module Design Best Practices	A system-level design guide for building a capacitive touchscreen module, covering topics such as touchscreen traces, shielding, mechanical design, FPC/PCB design, and LCD considerations.	✔	✔	–	–	–
001-81514	AN81514 - Using I2C In Systems With Slow Clock Edges	Discusses how to ensure proper I^2C functionality in extreme bus conditions[22].	✔	–	–	–	–
001-83948	Touch Tuning Host Emulator User Guide	Describes the Touch Tuning Host Emulator Software	–	–	–	–	✔
001-63571	CY3295-MTK PSoC™ Multitouch Manufacturing Test Kit User Guide	Describes the CY3295-MTK Manufacturing Test Kit	–	–	–	✔	–
External Specifications - These specifications are not created or owned by Infineon, but directions on how to acquire or access them can be provided upon request by contacting **automotive@infineon.com**.							
UM10204	I^2C-bus specification and user manual		✔	–	–	–	✔
ISO11452	Component test methods for electrical disturbances in Road Vehicles Package		✔	–	–	–	✔
CISPR25	Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers		✔	–	–	–	✔
J-STD-020D.1	Moisture/Reflow Sensitivity	Classification for non hermetic surface mount devices	✔	–	–	–	✔

Note

22. Extreme bus conditions are considered to be a combination of the following conditions: High-capacitive bus load, slow SCL fall time, and fast SDA rise/fall time.

14 Document conventions

14.1 Units of measure

Table 20 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
µA	microampere
µF	microfarad
µs	microsecond
µW	microwatt
µ	ohm
Hz	hertz
kΩ	kilo-ohm
kbps	kilobits per second
kHz	kilohertz
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
mW	milliwatt
Mbps	megabits per second
MHz	megahertz
nA	nanoampere
ns	nanosecond
pF	picofarad
s	second

14.2 Port nomenclature

Px[y] describes a particular bit “y” available within an I/O port “x.” For example, P4[2] reads “port 4, bit 2."

Px[y:z] describes a particular range of bits “y to z” within an I/O port named “Px.” For example, P4[0:5] refers to bits 0 through 5 within an I/O port named P4.

15 Glossary

Table 21 Glossary

Term	Definition
accuracy	The maximum position error across the slider, measured in millimeters, along a straight line between the actual finger position and the reported finger position. Accuracy is measured across the core and full panel. See Infineon's **PSoC™ Automotive Multitouch Touchscreen Controller Performance Parameters (001-49389)**[23] specification for more information.
All-Points	Infineon brand name for PSoC™ Automotive Multitouch devices capable of tracking the motion of multiple fingers.
conversion	The process of measuring the capacitance of an electrode connected to a pin (self capacitance) or the capacitance between a pair of electrodes connected to different pins (mutual capacitance). The result is a number that can be processed by the channel engine and CPU.
core	That portion of the slider, responsive to touch, less a perimeter area whose width is the larger of 3.5 mm or half the width of the finger (for example, less a perimeter band 4.5-mm wide for a 9-mm finger).
core LDO	Low Drop Out Regulator that sources power to the digital core when enabled. Input to the LDO is VDDD. Output of the LDO is connected to the digital supply pin VCCD. When the core LDO is disabled, power must be externally applied to the digital core supply pin VCCD.
cover lens	The top layer in the slider stackup that provides mechanical stability and protection for the slider sensor.
mutual capacitance	The capacitance between two slider electrodes.
refresh rate	The frequency at which consecutive frames of slider data are made available in a data buffer while a finger is present on the slider. See Infineon's **PSoC™ Automotive Multitouch Touchscreen Controller Performance Parameters (001-49389)**[23] specification for more information.
RX	Receive. A slider electrode or slider controller sense pin, mapped or switched to a charge sensing circuit within the controller (known as a receive channel).
scan	The conversion of all sensor capacitances to digital values.
sense pin	A pin that can be multiplexed to RX or TX.
signal-to-noise ratio (SNR)	The ratio between a capacitive finger signal and system noise.
signal disparity (SD)	The ratio of maximum measured signal when the slider is grounded and maximum measured signal when the slider is isolated from ground.
stackup	Layers of materials, in defined assembly order, that make up a slider sensor.
TX	Transmit. A slider electrode or slider controller sense pin, mapped or switched to a charge forcing circuit within the controller. This charge forcing circuit drives a periodic waveform onto one or more slider electrodes, which are coupled through mutual capacitance to adjacent receive electrodes.

Note
23. Infineon reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@infineon.com**.

Revision history

Document revision	Date	Description of changes
**	2017-03-30	New datasheet.
*A	2018-05-03	Updated **Ordering information**: Updated **Table 17**: Updated part numbers.
*B	2019-02-22	Updated “Confidential” watermark at the bottom of page as “CONFIDENTIAL - RELEASED ONLY UNDER NONDISCLOSURE AGREEMENT (NDA)”. Updated **Reference documents**: Updated **Table 19**: Updated spec titles in “Document Title” column. Completing Sunset Review.
*C	2019-05-08	Updated **Pin information**: Updated **Table 4** (Replaced “VDDA” with “VDDA_Q” in “Name” column corresponding to pin 32). Updated **Figure 13** (Replaced “VDDA” with “VDDA_Q” corresponding to pin 32).
*D	2020-11-26	Add trackpad related information in all instances across the document. Updated **Electrical Specifications**: Updated **DC specifications**: Updated **Chip-level DC specifications**: Updated **Table 8**. Updated **AC specifications**: Updated **Chip-level AC specifications**: Updated **Table 12**. Updated **I2C specifications**: Updated **Table 13**. Updated **Packaging information**: Updated **Thermal impedance and moisture sensitivity**: Updated **Table 15**. Updated **Ordering information**: No change in part numbers. Updated **Ordering code definitions**.

Revision history

Document revision	Date	Description of changes
*E	2021-08-18	Updated **Pin information**: Updated description. Updated **Electrical Specifications**: Updated **Absolute maximum ratings**: Updated **Table 5**. Updated **DC specifications**: Updated **Chip-level DC specifications**: Updated **Table 8**. Updated **I/O port 0 (P0[0:1]) DC specifications**: Updated **Table 9**. Updated **Packaging information**: Updated **Thermal impedance and moisture sensitivity**: Updated **Table 15**. Updated **Ordering information**: No change in part numbers. Added Note 21 and referred the same note in “Wake up Button Support” column in **Table 17**.
*F	2022-05-16	Updated Document Title to read as “CYAT6165X (41/48 I/Os), PSoC™ Automotive Multitouch All-Points Slider Controller Datasheet”. Updated to the PSoC™ Automotive Multitouch branding guidelines. Updated **Power supply information**: Updated **Voltage coefficient**: Updated **Figure 6** (Updated caption only). Updated **Figure 7** (Updated caption only). Updated **Figure 8** (Updated caption only). Updated **Figure 9** (Updated caption only). Updated **Figure 10** (Updated caption only).
*G	2022-08-18	Updated Document Title to read as “CYAT6165X, PSoC™ Automotive Multitouch Generation 6L Slider Datasheet”. Migrated to Infineon template.

Revision history

Document revision	Date	Description of changes
*H	2023-05-11	Updated **Slider system specifications**: Updated **System performance specifications**: Updated description. Updated **Electrical Specifications**: Updated **DC specifications**: Added description. Updated **Flash specifications**: Updated description. Updated **Table 7**. Updated Note 10. Updated **Chip-level DC specifications**: Updated description. Updated **I/O port 0 (P0[0:1]) DC specifications**: Updated description. Updated **Table 9**. Updated **I/O port 1 (P1[0:3]) and XRES DC specifications**: Updated description. Updated **Table 10**. Updated **AC specifications**: Added description. Updated **SWD interface AC specifications**: Updated description. Updated **Chip-level AC specifications**: Updated description. Updated **I2C specifications**: Updated description. Updated **SPI specifications**: Updated description. Updated to new template. Completing Sunset Review.

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