AURIX™ TC38x variants

About this document

Scope and purpose

This document is an addendum to the TC38x Product Data Sheet and User's Manual, listing all planned product variants, key parameters such as memory size and optional features.

The User's Manual lists functions implemented on the Silicon, but this document counts functions that are pinning dependent; i.e. functions are counted that are connected to at least one package pin. As pins are overlaid with several functions the pinning needs to be checked (see Product Data Sheet) to determine the number of usable functions in an application.

Naming conventions

Prefix:

- SAK: $T_{ambient}$ Temperature Range from -40 °C up to +125 °C.
- SAL: $T_{ambient}$ Temperature Range from -40 °C up to +150 °C (packaged device).

Feature Package:

- P: Standard feature.
- E: Emulation device with all features of the emulated standard type, additionally full MCDS, overlay functionality for calibration, AGBT as trace interface for development (depending on the package).
- C,V,Z: Customer Specific.
- A: ADAS ext. Memory.
- T: ADAS + emulation.
- X: Extended Feature device. These products contain the extended memory (EMEM) of the ADAS subsystem. The ADAS peripherals SPU and RIF are not available.
- M: MotionWise software.
- F: Extended Flash.
- G: Additional Connectivity.
- H: ADAS Standard feature.
- N: Standard feature with AMU.

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1 TC38x AE step variants

The following tables list the TC38x AE step variants.

1.1 TC38x AE step (part 1)

A table listing the TC38x AE step variants.

Table 1 TC38x_AE step (part 1)

SAK-TC389QP-160F300S	SAK-TC387QP-160F300S	SAK-TC387TP-128F300S	SAK-TC387QN-160F300S	SAK-TC389QN-160F300S	SAL-TC389QP-160F300S	SAL-TC387QP-160F300S
Step						
AE	AE	AE	AE	AE	AE	AE
Production Status						
Standard	Standard	Customer Specific	Customer Specific	Customer Specific	Standard	Standard
Package Type						
PG-FBGA-516	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-FBGA-516	PG-FBGA-516	PG-LFBGA-292
Pinout						
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
Reference Silicon						
TC38x	TC38x	TC38x	TC38x	TC38x	TC38x	TC38x
Temperature Range (Ambient)						
SAK	SAK	SAK	SAK	SAK	SAL	SAL
Chip ID ***Attention:*** ***The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.***						
0x8C008984	0x8C008784	0xCB008784	0xAC008784	0xAC008984	0x8C008984	0x8C008784
Cores / Checker Cores						
4/2	4/2	3/2	4/2	4/2	4/2	4/2
Max. Freq. (MHz)						
300	300	300	300	300	300	300
Program Flash (MB)						
10	10	8	10	10	10	10
Data Flash0 (single-ended) (KB)						
512	512	512	512	512	512	512
Total SRAM (without EMEM and Cache) (KB)						
1376	1376	1152	1376	1376	1376	1376
EMEM Size (KB)						
0	0	0	0	0	0	0

1 TC38x AE step variants

Table 1 TC38x_AE step (part 1) (continued)

SAK-TC389QP-160F300S	SAK-TC387QP-160F300S	SAK-TC387TP-128F300S	SAK-TC387QN-160F300S	SAK-TC389QN-160F300S	SAL-TC389QP-160F300S	SAL-TC387QP-160F300S
DSPR (KB)						
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other
DLMU (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
PSPR (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
LMU (KB)						
128	128	128	128	128	128	128
DAM (KB)						
64	64	64	64	64	64	64
AMU[1)]						
No	No	No	Yes	Yes	No	No
ADC (Primary Groups/Channels)						
8/64	5/40	5/40	5/40	8/64	8/64	5/40
ADC (Secondary Groups/Channels)						
4/60	4/60	4/60	4/60	4/60	4/60	4/60
ADC (Fast Compare Channels)						
4	4	4	4	4	4	4
ADC (EDSADC Channels)						
10	6	6	6	10	10	6
CAN (Modules/Nodes)						
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
FlexRay (Modules/Channels)						
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules						
1	1	1	1	1	1	1
ASCLIN Modules / with ASC & LIN / with 3-wire SPI						
24/24/12	24/24/11	24/24/11	24/24/11	24/24/12	24/24/12	24/24/11
QSPI Modules / with LVDS						

1 AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

1 TC38x AE step variants

Table 1 TC38x_AE step (part 1) (continued)

SAK-TC389QP-160F300S	SAK-TC387QP-160F300S	SAK-TC387TP-128F300S	SAK-TC387QN-160F300S	SAK-TC389QN-160F300S	SAL-TC389QP-160F300S	SAL-TC387QP-160F300S
5/2	5/2	5/2	5/2	5/2	5/2	5/2
SENT Channels						
25	20	20	20	25	25	20
MSC Modules						
3	2	2	2	3	3	2
PSI5 Channels						
4	4	4	4	4	4	4
PSI5-S Module						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
SDMMC Module						
No	No	No	No	No	No	No
Max. Ethernet Availability: 1GBit/100Mbit/No						
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
MCDS Availability						
miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS
ADAS Cluster Available						
No	No	No	No	No	No	No
CIF						
No	No	No	No	No	No	No
HSM Available						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

1.2 TC38x AE step (part 2)

A continuation table listing the TC38x AE step variants.

Table 2 TC38x_AE step (part 2)

SAL-TC387TP-128F300S	SAK-TC387TP-160F300S	SAL-TC387TP-160F300S
Step		
AE	AE	AE
Production Status		
Customer Specific	Customer Specific	Customer Specific
Package Type		
PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
Pinout		
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
Reference Silicon		
TC38x	TC38x	TC38x
Temperature Range (Ambient)		
SAL	SAK	SAL
Chip ID ***Attention*: *The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.***		
0xCB008784	0xFC008784	0xFC008784
Cores / Checker Cores		
3/2	3/2	3/2
Max. Freq. (MHz)		
300	300	300
Program Flash (MB)		
8	10	10
Data Flash0 (single-ended) (KB)		
512	512	512
Total SRAM (without EMEM and Cache) (KB)		
1152	960	960
EMEM Size (KB)		
0	0	0
DSPR (KB)		
240 in CPU0&1; 96 other	160 in CPU0; 128 in CPU1; 96 other	160 in CPU0; 128 in CPU1; 96 other
DLMU (KB)		
64 per CPU	64 per CPU	64 per CPU

1 TC38x AE step variants

Table 2 TC38x_AE step (part 2) (continued)

SAL-TC387TP-128F300S	SAK-TC387TP-160F300S	SAL-TC387TP-160F300S
PSPR (KB)		
64 per CPU	64 per CPU	64 per CPU
LMU (KB)		
128	128	128
DAM (KB)		
64	64	64
AMU[2)]		
No	No	No
ADC (Primary Groups/Channels)		
5/40	5/40	5/40
ADC (Secondary Groups/Channels)		
4/60	4/60	4/60
ADC (Fast Compare Channels)		
4	4	4
ADC (EDSADC Channels)		
6	6	6
CAN (Modules/Nodes)		
3/3x4	3/3x4	3/3x4
FlexRay (Modules/Channels)		
2/2x2	2/2x2	2/2x2
HSSL Modules		
1	1	1
ASCLIN Modules / with ASC & LIN / with 3-wire SPI		
24/24/11	24/24/11	24/24/11
QSPI Modules / with LVDS		
5/2	5/2	5/2
SENT Channels		
20	20	20
MSC Modules		
2	2	2
PSI5 Channels		
4	4	4

2 AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

1 TC38x AE step variants

Table 2 TC38x_AE step (part 2) (continued)

SAL-TC387TP-128F300S	SAK-TC387TP-160F300S	SAL-TC387TP-160F300S
PSI5-S Module		
Yes	Yes	Yes
SDMMC Module		
No	No	No
Max. Ethernet Availability: 1GBit/100Mbit/No		
1Gbit/s	1Gbit/s	1Gbit/s
MCDS Availability		
miniMCDS	miniMCDS	miniMCDS
ADAS Cluster Available		
No	No	No
CIF		
No	No	No
HSM Available		
Yes	Yes	Yes

2 TC38x AD step variants

The following tables list the TC38x AD step variants.

2.1 TC38x AD step (part 1)

A table listing the TC38x AD step variants.

Table 3 TC38x_AD step (part 1)

SAL-TC389QP-160 F300S	SAL-TC387QP-160 F300S	SAK-TC389QP-160 F300S	SAK-TC387QP-160 F300S	SAK-TC387TP-128 F300S	SAL-TC387TP-128 F300S	SAK-TC387TP-160 F300S
Step						
AD	AD	AD	AD	AD	AD	AD
Production Status						
Standard	Standard	Standard	Standard	Customer Specific	Customer Specific	Customer Specific
Package Type						
PG-FBGA-516	PG-LFBGA-292	PG-FBGA-516	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292	PG-LFBGA-292
Pinout						
LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm	LFBGA 0.8 mm
Reference Silicon						
TC38x	TC38x	TC38x	TC38x	TC38x	TC38x	TC38x
Temperature Range (Ambient)						
SAL	SAL	SAK	SAK	SAK	SAL	SAK
Chip ID ***Attention:*** ***The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.***						
0x8C008983	0x8C008783	0x8C008983	0x8C008783	0xCB008783	0xCB008783	0xFC008783
Cores / Checker Cores						
4/2	4/2	4/2	4/2	3/2	3/2	3/2
Max. Freq. (MHz)						
300	300	300	300	300	300	300
Program Flash (MB)						
10	10	10	10	8	8	10
Data Flash0 (single-ended) (KB)						
512	512	512	512	512	512	512
Total SRAM (without EMEM and Cache) (KB)						
1376	1376	1376	1376	1152	1152	960
EMEM Size (KB)						
0	0	0	0	0	0	0

2 TC38x AD step variants

Table 3 TC38x_AD step (part 1) (continued)

SAL-TC389QP-160 F300S	SAL-TC387QP-160 F300S	SAK-TC389QP-160 F300S	SAK-TC387QP-160 F300S	SAK-TC387TP-128 F300S	SAL-TC387TP-128 F300S	SAK-TC387TP-160 F300S
DSPR (KB)						
240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	240 in CPU0&1; 96 other	160 in CPU0; 128 in CPU1; 96 other
DLMU (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
PSPR (KB)						
64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU	64 per CPU
LMU (KB)						
128	128	128	128	128	128	128
DAM (KB)						
64	64	64	64	64	64	64
AMU[3)]						
No	No	No	No	No	No	No
ADC (Primary Groups/Channels)						
8/64	5/40	8/64	5/40	5/40	5/40	5/40
ADC (Secondary Groups/Channels)						
4/60	4/60	4/60	4/60	4/60	4/60	4/60
ADC (Fast Compare Channels)						
4	4	4	4	4	4	4
ADC (EDSADC Channels)						
10	6	10	6	6	6	6
CAN (Modules/Nodes)						
3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4	3/3x4
FlexRay (Modules/Channels)						
2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2	2/2x2
HSSL Modules						
1	1	1	1	1	1	1
ASCLIN Modules / with ASC & LIN / with 3-wire SPI						
24/24/12	24/24/11	24/24/12	24/24/11	24/24/11	24/24/11	24/24/11
QSPI Modules / with LVDS						

3 AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

2 TC38x AD step variants

Table 3 TC38x_AD step (part 1) (continued)

SAL-TC389QP-160F300S	SAL-TC387QP-160F300S	SAK-TC389QP-160F300S	SAK-TC387QP-160F300S	SAK-TC387TP-128F300S	SAL-TC387TP-128F300S	SAK-TC387TP-160F300S
5/2	5/2	5/2	5/2	5/2	5/2	5/2
SENT Channels						
25	20	25	20	20	20	20
MSC Modules						
3	2	3	2	2	2	2
PSI5 Channels						
4	4	4	4	4	4	4
PSI5-S Module						
Yes	Yes	Yes	Yes	Yes	Yes	Yes
SDMMC Module						
No	No	No	No	No	No	No
Max. Ethernet Availability: 1GBit/100Mbit/No						
1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s	1Gbit/s
MCDS Availability						
miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS	miniMCDS
ADAS Cluster Available						
No	No	No	No	No	No	No
CIF						
No	No	No	No	No	No	No
HSM Available						
Yes	Yes	Yes	Yes	Yes	Yes	Yes

2.2 TC38x AD step (part 2)

A continuation table listing the TC38x AD step variants.

Table 4 TC38x_AD step (part 2)

	SAL-TC387TP-160F300S
Step	
	AD
Production Status	
	Customer Specific
Package Type	
	PG-LFBGA-292
Pinout	
	LFBGA 0.8 mm
Reference Silicon	
	TC38x
Temperature Range (Ambient)	
	SAL
Chip ID ***Attention:*** ***The value of SCU_CHIPID in the UCODE field contains the default value 0 not the µCode version.***	
	0xFC008783
Cores / Checker Cores	
	3/2
Max. Freq. (MHz)	
	300
Program Flash (MB)	
	10
Data Flash0 (single-ended) (KB)	
	512
Total SRAM (without EMEM and Cache) (KB)	
	960
EMEM Size (KB)	
	0
DSPR (KB)	
	160 in CPU0; 128 in CPU1; 96 other
DLMU (KB)	
	64 per CPU

2 TC38x AD step variants

Table 4 TC38x_AD step (part 2) (continued)

	SAL-TC387TP-160F300S
PSPR (KB)	
	64 per CPU
LMU (KB)	
	128
DAM (KB)	
	64
AMU[4]	
	No
ADC (Primary Groups/Channels)	
	5/40
ADC (Secondary Groups/Channels)	
	4/60
ADC (Fast Compare Channels)	
	4
ADC (EDSADC Channels)	
	6
CAN (Modules/Nodes)	
	3/3x4
FlexRay (Modules/Channels)	
	2/2x2
HSSL Modules	
	1
ASCLIN Modules / with ASC & LIN / with 3-wire SPI	
	24/24/11
QSPI Modules / with LVDS	
	5/2
SENT Channels	
	20
MSC Modules	
	2
PSI5 Channels	
	4

4 AMU is abbreviated as ASC Modeling Unit. For Additional details about AMU, Contact an Infineon Representative

2 TC38x AD step variants

Table 4 TC38x_AD step (part 2) (continued)

	SAL-TC387TP-160F300S
PSI5-S Module	
	Yes
SDMMC Module	
	No
Max. Ethernet Availability: 1GBit/100Mbit/No	
	1Gbit/s
MCDS Availability	
	miniMCDS
ADAS Cluster Available	
	No
CIF	
	No
HSM Available	
	Yes

3 Memory maps of TC38x variants

This section shows the influence of above feature variants on the memory map.

Program Flash

Variants:

- 10 MB: umbrella (3 x 3 MB, 1 x 1 MB), see User's Manual.
- 8 MB: 3 MB + 1 MB + 3 MB + 1 MB (see Figure below).

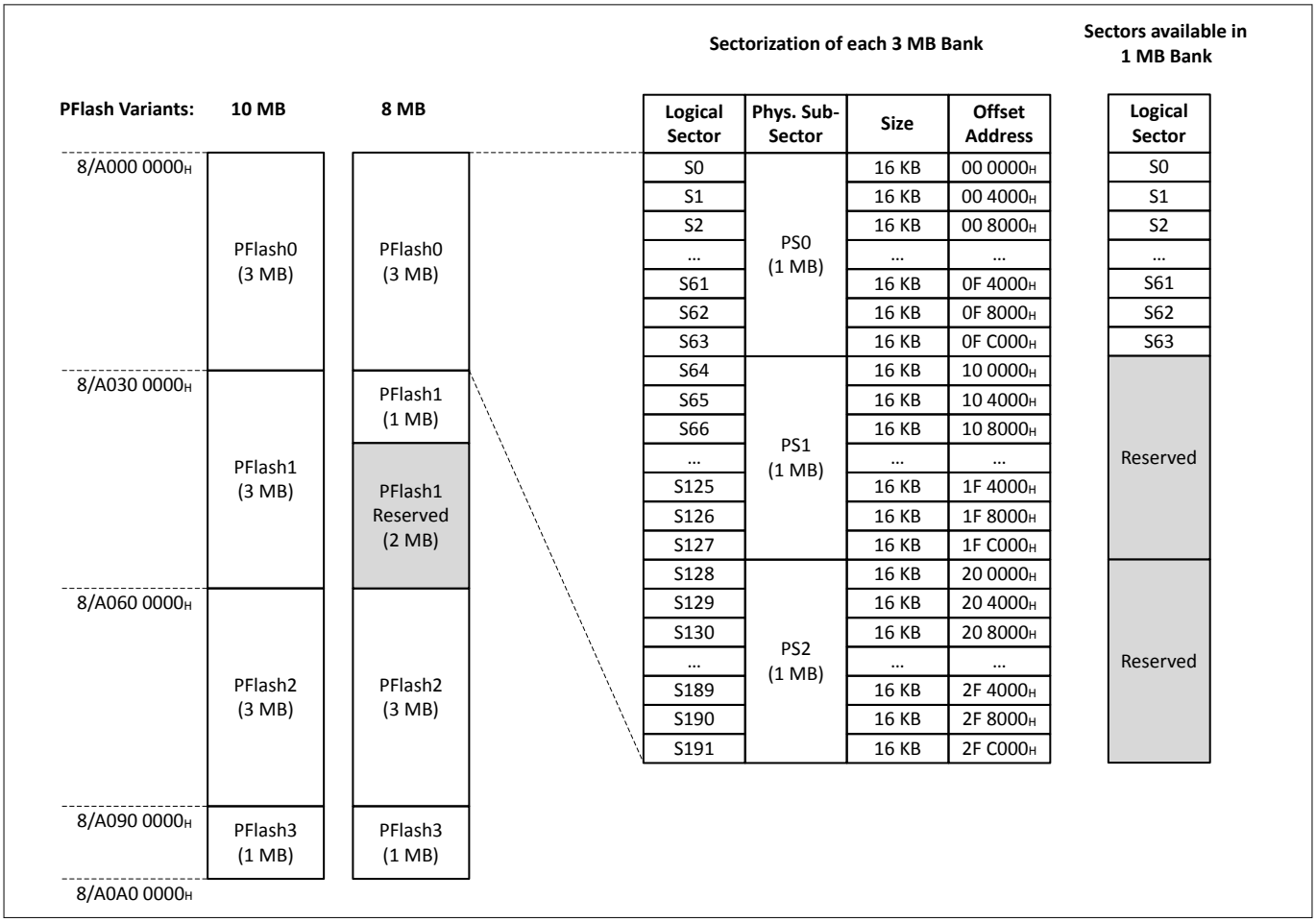

Figure 1 TC38x PFlash variants

Cores / Checker cores

Variants:

- 4/2: umbrella, see User's Manual
- 3/2: not available is CPU3 including its RAMs (DSPR, DCACHE, DTAG, PSPR, PCACHE, PTAG, DLMU)

CPU RAMs

Variants:

- DSPR: 240 KB in CPU0 & CPU1, 96 KB in CPU2 & CPU3: umbrella, see User's Manual
- DSPR: 240 KB in CPU0 & CPU1, 96 KB in CPU2: default for 3/2 Cores/Checker Cores configuration (see Figure below for available DSPR address ranges).
- DSPR: 160 KB in CPU0, 128 KB in CPU1, 96 KB in CPU2: reduced RAM variant of 3/2 Cores/Checker Cores configuration (see Figure below for available DSPR address ranges).

3 Memory maps of TC38x variants

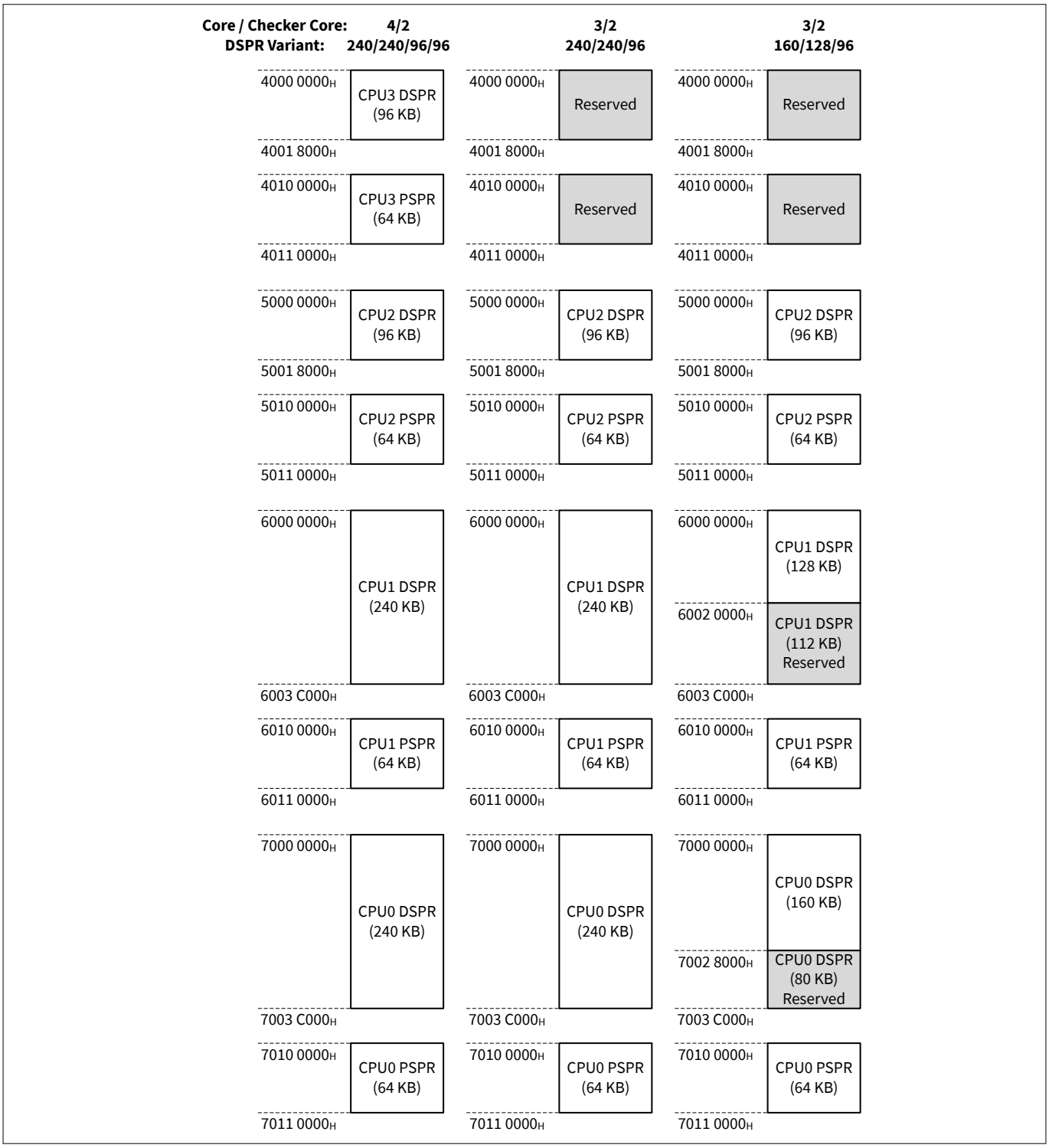

Figure 2 DSPR variants

ADC availability

- Limitation on availability of ADC channels are caused by pin limitations. See Data Sheet for the pinning table of the package.

Revision history

Document version	Date of release	Description of changes
V1.0	2018-06-08	• First release.
V1.1	2018-08-06	• Added row "Reference Silicon" (needed e.g. for TC37x) to refer user to User's Manual Appx.
V1.2	2019-02-04	• Removed from "Memory Maps" the description for LMU and DAM variations as these are not varied. • "Variant Tables": added SAL-TC387TP-128F300S
V1.3	2019-03-01	• "About this document": reduced list of described Feature Package to the used ones. • "Memory Maps": added hint to understand ADC device specific differences. • "Variant Tables": changed Production Status of several devices. • "Variant Tables": clarified Total SRAM value is without cache memories.
V1.4	2019-06-12	• Chapter 1: Added the TC38x AE step variants table. • Chapter 1 and 2: TC38x Ax step variants table format changed to fit all the contents. • Chapter 1 and 2:Added new row in the variant tables called "AMU" with the footnote for additional details. • Chapter: About this document: Feature package definitions are updated to consistent with the product naming nomenclature definition.
V1.5	2020-01-10	• Chapter 1,2: Total SRAM (without EMEM and Cache) size is corrected for SAK-TC387TP-160F300S and SAL-TC387TP-160F300S. • Page 1: About the document:Feature Package 'X' definition is updated to remove CIF. • Chapter 1 and 2:Added new row in the variant tables called "CIF" indicating the Camera Interface availability.
V1.6	2020-11-18	• Chapter 1,2: Package type name for SAK-TC389QP-160F300S, SAK-TC389QN-160F300S, SAL-TC389QP-160F300S is corrected from PG-LFBGA-516 to PG-FBGA-516. • Chapter 1 and 2:Removed Bare Die Marking variant SAL-TC380QP-160F300.

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