TPS799-Q1 200 mA, Low Quiescent Current, Ultralow Noise, High PSRR, Low Dropout, Linear Regulators

1 Features

- Qualified for Automotive Applications
- 200-mA Low-Dropout (LDO) Regulator With Enable (EN)
- Low I_Q: 40 µA
- Multiple Output Voltage Versions Available:
  - Fixed Outputs of 1.2 V to 4.5 V
  - Adjustable Outputs from 1.2 V to 6.5 V
- High PSRR: 66 dB at 1 kHz, 51 db at 10 kHz
- Ultralow Noise: 29.5 μV_{RMS}
- Fast Start-Up Time: 45 µs
- Stable With a Low ESR, 2-µF (Typical) Output Capacitance
- Excellent Load and Line Transient Response
- 2% Overall Accuracy (Load, Line, and Temperature)
- Very Low Dropout: 100 mV
- Thin SOT-23 and 2-mm × 2-mm SON-6 Packages

2 Applications

- Infotainment
- Cluster
- Advanced Driver Assistance Systems

3 Description

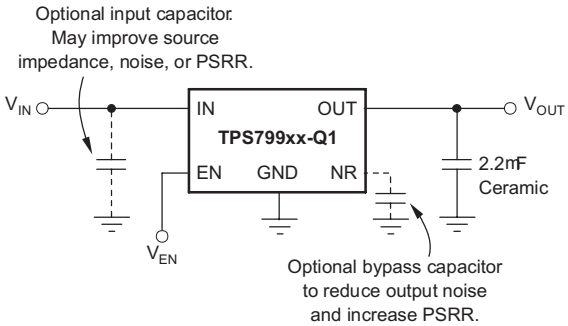
The TPS799xx-Q1 family of low-dropout (LDO) low-power linear regulators offers excellent AC performance with very low ground current. High power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient response are provided while consuming a very low 40-µA (typical) ground current. The TPS799xx-Q1 is stable with ceramic capacitors and uses an advanced BiCMOS fabrication process to yield a dropout voltage of 100 mV (typical) at 200-mA output. The TPS799xx-Q1 uses a precision voltage reference and feedback loop to achieve overall accuracy of 2% over all load, line, process, and temperature variations. It is fully specified from T_J = –40°C to 125°C and is offered in low profile thin SOT-23 and 2-mm × 2-mm SON packages, ideal for wireless handsets and WLAN cards.

Device Information(1)

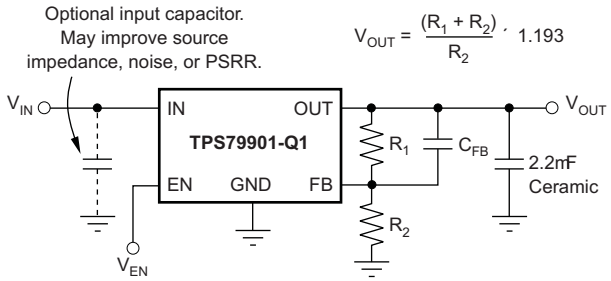
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS799-Q1	SON (6)	2.00 mm × 2.00 mm
	SOT (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit Fixed Voltage Versions



Typical Application Circuit Adjustable Voltage Version



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (January 2012) to Revision F — **Page**

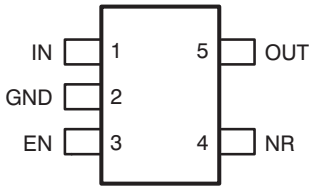
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added High PSRR: 51 db at 10 kHz ... 1

Changes from Revision D (June 2011) to Revision E — **Page**

- Changed CDM ESD rating from 500 V to 1000 V. ... 4

5 Pin Configuration and Functions

DDC Package
5-Pin SOT-23
Top View



Pin Functions

PIN			DESCRIPTION
NAME	NO. (SOT)	NO. (SON)	
IN	1	6	Input supply
GND	2	3, Pad	Ground. The pad must be tied to GND.
EN	3	4	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
NR	4	2	Fixed-voltage versions only; connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This capacitor allows output noise to be reduced to very low levels.
FB	4	2	Adjustable version only; this pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	1	Output of the regulator. A small capacitor (total typical capacitance ≥ 2 µF ceramic) is needed from this pin to ground to ensure stability.
N/C	—	5	Not internally connected. This pin must either be left open or tied to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN}	–0.3	7	V
V_{EN}	–0.3	V_{IN} + 0.3	V
V_{OUT}	–0.3	V_{IN} + 0.3	V
Peak output current	Internally limited		
Continuous total power dissipation	See *Thermal Information*		
Junction temperature, T_J	–55	150	°C
Storage junction temperature, T_{stg}	–55	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.7		6.5	V
I_{OUT}	Output current	0.5		200	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)(2)		TPS799xx-Q1		UNIT
		DRV (SON)	DDC (SOT-23)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.2	178.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.8	70.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	145.9	73.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	2.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.4	74.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.2	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

6.5 Electrical Characteristics

over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF (unless otherwise noted) For TPS79901, V_{OUT} = 3 V. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			2.7		6.5	V
V_{FB}	Internal reference (TPS79901)			1.169	1.193	1.217	V
V_{OUT}	Output voltage range (TPS79901)			V_{FB}		6.5 – V_{DO}	V
V_{OUT}	Output accuracy	Nominal, T_J = 25°C		–1%		1%	
V_{OUT}	Output accuracy(1)	Over V_{IN}, I_{OUT}, temperature, V_{OUT} + 0.3 V ≤ V_{IN} ≤ 6.5 V, 500 µA ≤ I_{OUT} ≤ 200 mA		–2%	±1%	2%	
ΔV_{OUT}%/ ΔV_{IN}	Line regulation(1)	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 6.5 V			0.02		%/V
ΔV_{OUT}%/ ΔI_{OUT}	Load regulation	500 µA ≤ I_{OUT} ≤ 200 mA			0.002		%/mA
V_{DO}	Dropout voltage(2) (V_{IN} = $V_{OUT(NOM)}$ – 0.1 V)	V_{OUT} < 3.3 V	I_{OUT} = 200 mA		100	175	mV
		V_{OUT} ≥ 3.3 V			90	160	
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$		200	400	600	mA
I_{GND}	Ground pin current	500 µA ≤ I_{OUT} ≤ 200 mA			40	60	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4 V, 2.7 V ≤ V_{IN} ≤ 6.5 V			0.15	1	µA
I_{FB}	Feedback pin current (TPS79901)			–0.5		0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.85 V, V_{OUT} = 2.85 V, C_{NR} = 0.01 µF, I_{OUT} = 100 mA	f = 100 Hz		70		dB
			f = 1 kHz		66		
			f = 10 kHz		51		
			f = 100 kHz		38		
V_N	Output noise voltage BW = 10 Hz to 100 kHz, V_{OUT} = 2.8 V	C_{NR} = 0.01 µF			10.5 V_{OUT}		μV_{RMS}
		C_{NR} = none			94 V_{OUT}		
T_{STR}	Start-up time	V_{OUT} = 2.85 V, R_L = 14 Ω, C_{OUT} = 2.2 µF	C_{NR} = 0.001 µF		45		µs
			C_{NR} = 0.047 µF		45		
			C_{NR} = 0.01 µF		50		
			C_{NR} = none		50		
$V_{EN(HI)}$	Enable high (enabled)			1.2		V_{IN}	V
$V_{EN(LO)}$	Enable low (shutdown)			0		0.4	V
$I_{EN(HI)}$	Enable pin current, enabled	V_{EN} = V_{IN} = 6.5 V			0.03	1	µA
TSD	Thermal shutdown temperature	Shutdown, temperature increasing			165		°C
		Reset, temperature decreasing			145		°C
T_J	Operating junction temperature			–40		125	°C
V_{UVLO}	Undervoltage lock-out	V_{IN} rising		1.9	2.2	2.65	V
$V_{UVLO,hys}$	Hysteresis	V_{IN} falling			70		mV

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 2.7 V, whichever is greater.
(2) V_{DO} is not measured for devices with $V_{OUT(NOM)}$ < 2.8 V because minimum V_{IN} = 2.7 V.

6.6 Typical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF (unless otherwise noted). For TPS79901, V_{OUT} = 3 V. Typical values are at T_J = 25°C.

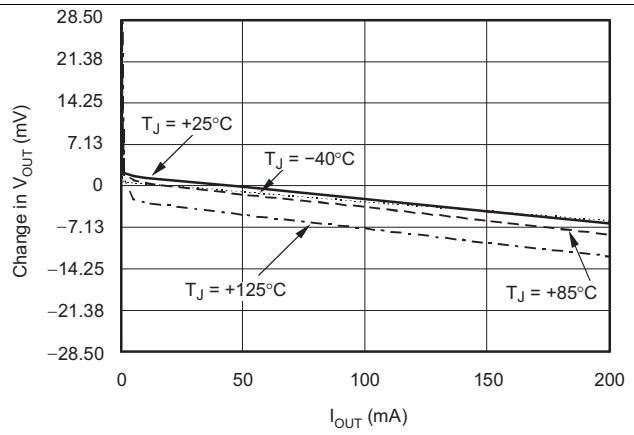


Figure 1. Load Regulation

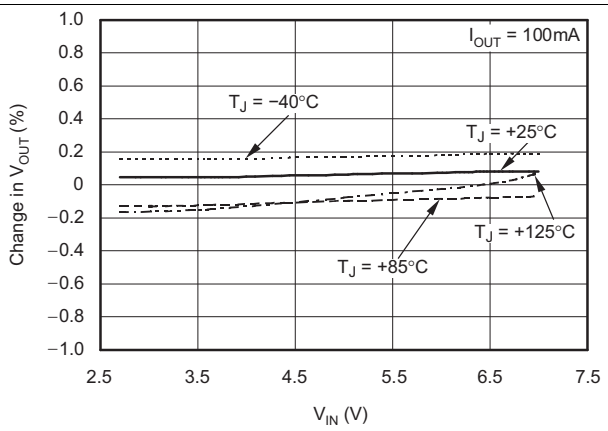


Figure 2. Line Regulation

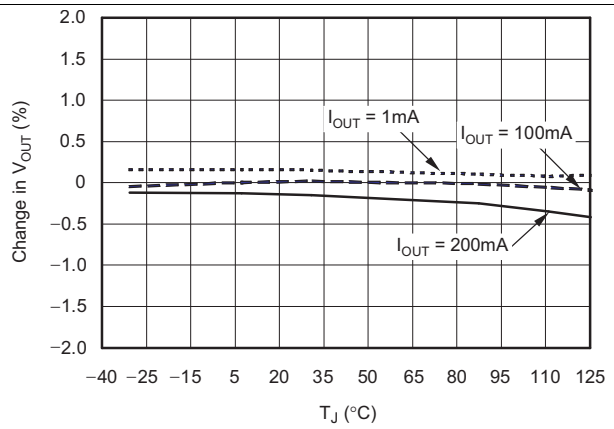


Figure 3. Output Voltage vs Junction Temperature

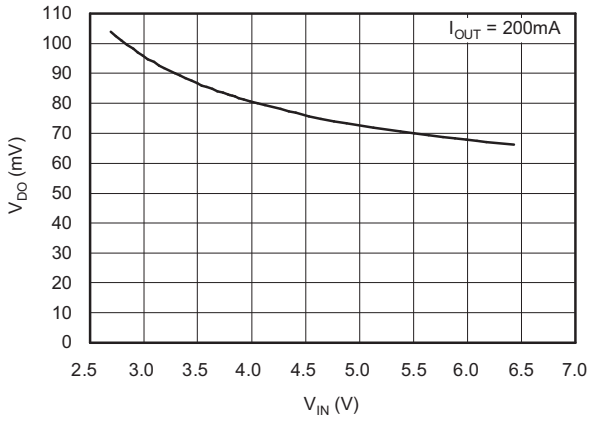


Figure 4. TPS79901 Dropout vs Input Voltage

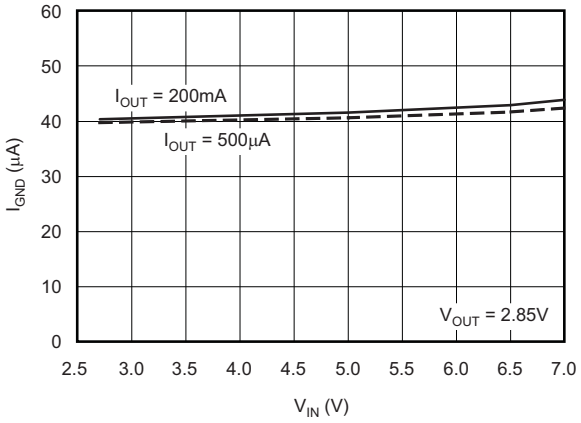


Figure 5. Ground Pin Current vs Input Voltage

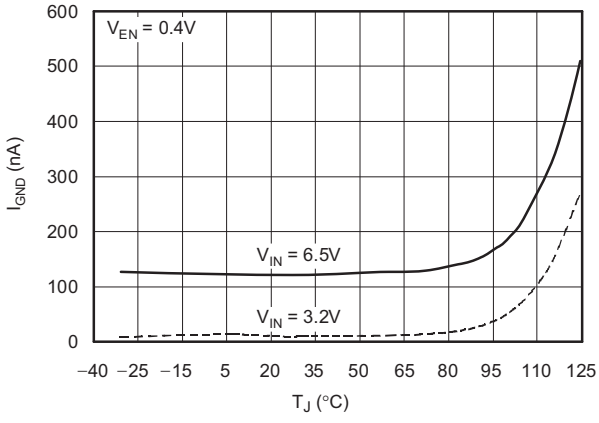


Figure 6. Ground Pin Current (Disabled) vs Junction Temperature

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.7 V, whichever is greater; I_{OUT} = 1 mA, V_{EN} = V_{IN}, C_{OUT} = 2.2 µF, C_{NR} = 0.01 µF (unless otherwise noted). For TPS79901, V_{OUT} = 3 V. Typical values are at T_J = 25°C.

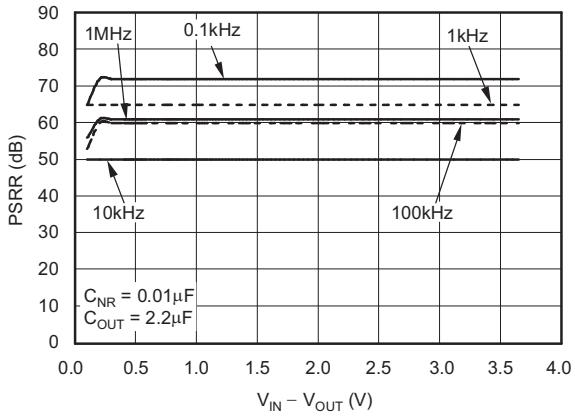


Figure 7. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}, I_{OUT} = 1 mA

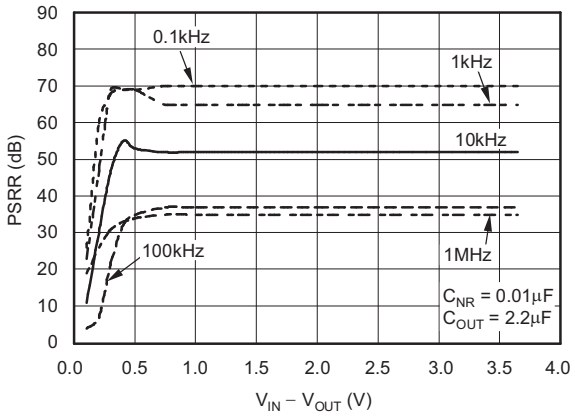


Figure 8. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}, I_{OUT} = 100 mA

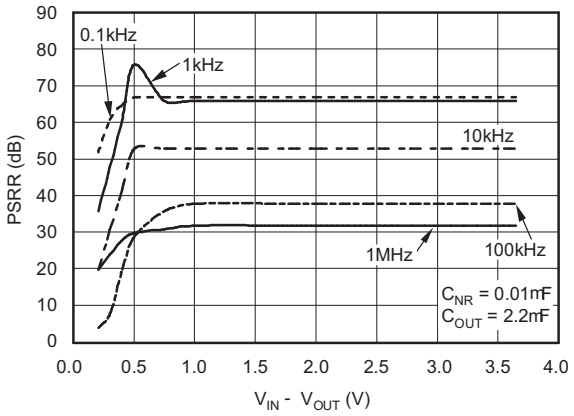


Figure 9. Power-Supply Ripple Rejection vs V_{IN} – V_{OUT}, I_{OUT} = 200 mA

7 Detailed Description

7.1 Overview

The TPS799xx-Q1 family of low-dropout (LDO) regulators combines the high performance required of many RF and precision analog applications with ultralow current consumption. High PSRR is provided by a high-gain, high-bandwidth error loop with good supply rejection at very low headroom (V_{IN} – V_{OUT}). A noise-reduction pin is provided to bypass noise generated by the band-gap reference and to improve PSRR, while a quick-start circuit quickly charges this capacitor at start-up. The combination of high performance and low ground current also make these devices an excellent choice for portable applications. All versions have thermal and overcurrent protection, and are fully specified from –40°C to 125°C.

The TPS799xx-Q1 family also features inrush current protection with an EN toggle start-up, and overshoot detection at the output. When the EN toggle is used to start the device, current limit protection is immediately activated, restricting the inrush current to the device. If voltage at the output overshoots 5% from the nominal value, a pulldown resistor reduces the voltage to normal operating conditions, as shown in *Functional Block Diagrams*.

7.2 Functional Block Diagrams

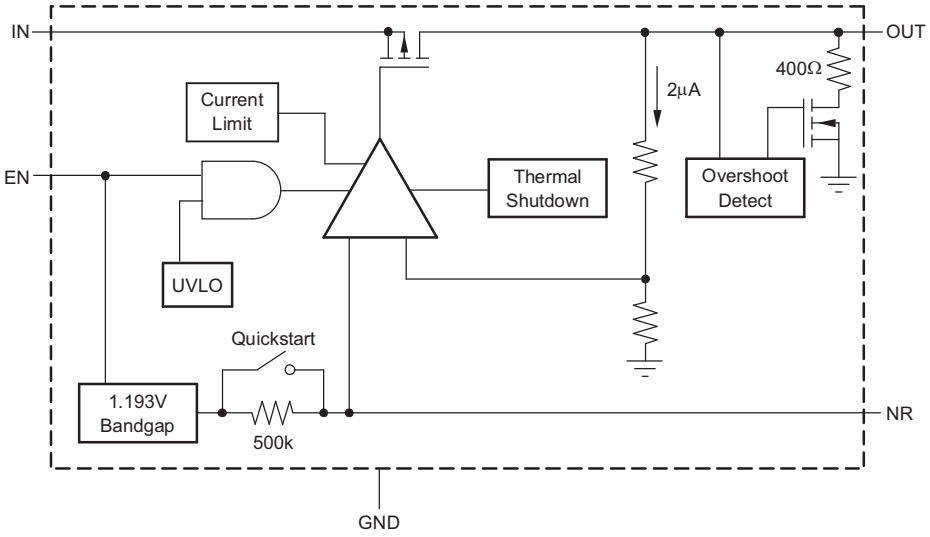


Figure 10. Fixed-Voltage Version

Functional Block Diagrams (continued)

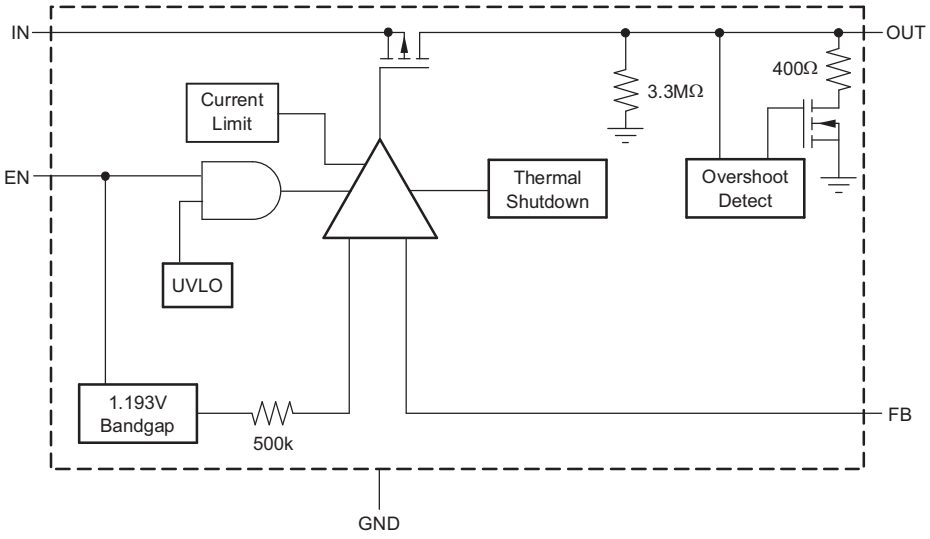


Figure 11. Adjustable-Voltage Version

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS799xx-Q1 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in current limit for extended periods of time.

The PMOS pass element in the TPS799xx-Q1 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

7.3.2 Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage TTL-CMOS levels. When shutdown capability is not required, EN can be connected to IN.

7.3.3 Dropout Voltage

The TPS799xx-Q1 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS,\ ON}$ of the PMOS pass element. Because the PMOS device behaves like a resistor in dropout, V_{DO} scales approximately with output current.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 7 through Figure 9 in the *Typical Characteristics* section.

7.3.4 Start-Up

Fixed voltage versions of the TPS799xx-Q1 use a quick-start circuit to fast-charge the noise reduction capacitor, C_{NR}, if present (see Figure 10). This allows the combination of very low output noise and fast start-up times. The NR pin is high impedance so a low leakage C_{NR} capacitor must be used; most ceramic capacitors are appropriate in this configuration.

For the fastest start-up, V_{IN} should be applied first, then the enable pin (EN) driven high. If EN is tied to IN, startup is somewhat slower. The quick-start switch is closed for approximately 135 µs. To ensure that C_{NR} is fully charged during the quick-start time, a 0.01 µF or smaller capacitor should be used.

Feature Description (continued)

7.3.5 Undervoltage Lockout (UVLO)

The TPS799xx-Q1 utilizes a UVLO circuit to keep the output shut off until internal circuitry is operating properly. The UVLO circuit has a deglitch feature so that it typically ignores undershoot transients on the input if they are less than 50-µs duration.

7.4 Device Functional Modes

Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing the operating current to 150 nA, nominal.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS799xx-Q1 family of LDO regulators combines the high performance required of many RF and precision analog applications with ultralow current consumption. High PSRR is provided by a high gain, high bandwidth error loop with good supply rejection at very low headroom ($V_{IN} – V_{OUT}$). Fixed-voltage versions provide a noise reduction pin to bypass noise generated by the bandgap reference and to improve PSRR while a quick-start circuit fast-charges this capacitor at start-up. The combination of high performance and low ground current also make the TPS799xx-Q1 an excellent choice for portable applications. All versions have thermal and overcurrent protection and are fully specified from –40°C to 125°C.

Figure 12 shows the basic circuit connections for fixed-voltage model. Figure 13 gives the connections for the adjustable output version (TPS79901). R_1 and R_2 can be calculated for any output voltage using the formula in Figure 13. Sample resistor values for common output voltages are shown in Figure 13.

8.2 Typical Application

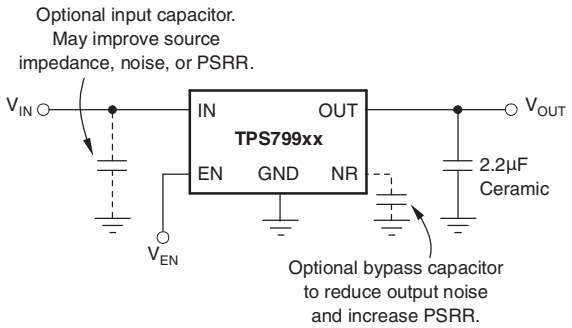


Figure 12. Typical Application Circuit for Fixed-Voltage Version

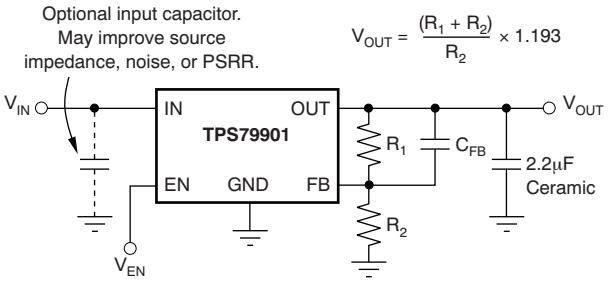


Figure 13. Typical Application Circuit for Adjustable-Voltage Version

Typical Application (continued)

8.2.1 Design Requirements

Select the desired device based on the output voltage. Provide an input supply with adequate headroom to account for dropout and output current to account for the GND terminal current, and power the load.

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The TPS799xx-Q1 is designed to be stable with standard ceramic capacitors of values 2.2 µF or larger. X5R and X7R type capacitors are best as they have minimal variation in value and ESR over temperature. Maximum ESR should be <1 Ω.

8.2.2.2 Feedback Capacitor Requirements (TPS79901 only)

The feedback capacitor, C_{FB}, shown in Figure 13 is required for stability. For a parallel combination of R_1 and R_2 equal to 250 kΩ, any value from 3 pF to 1 nF can be used. Fixed voltage versions have an internal 30-pF feedback capacitor which is quick-charged at start-up. The adjustable version does not have this quick-charge circuit, so values below 5 pF should be used to ensure fast startup; values above 47 pF can be used to implement an output voltage soft-start. Larger value capacitors also improve noise slightly. The TPS79901 device is stable in unity-gain configuration (OUT tied to FB) without C_{FB}.

8.2.2.3 Output Noise

In most LDOs, the bandgap is the dominant noise source. If a noise reduction capacitor (C_{NR}) is used with the TPS799xx-Q1, the bandgap does not contribute significantly to noise. Instead, noise is dominated by the output resistor divider and the error amplifier input. To minimize noise in a given application, use a 0.01-µF noise reduction capacitor; for the adjustable version, smaller value resistors in the output resistor divider reduce noise. A parallel combination that gives 2 µA of divider current has the same noise performance as a fixed-voltage version. To further optimize noise, equivalent series resistance of the output capacitor can be set to approximately 0.2 Ω. This configuration maximizes phase margin in the control loop, reducing total output noise by up to 10%.

Noise can be referred to the feedback point (FB pin) such that with C_{NR} = 0.01 µF, total noise is approximately given by Equation 1:

$$V_N = \frac{10.5\mu V_{RMS}}{V} \times V_{OUT} \quad (1)$$

The adjustable version of the TPS79901 device does not have the noise-reduction pin available, so ultralow noise operation is not possible. Noise can be minimized according to the previous recommendations.

8.2.2.4 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increase duration of the transient response. In the adjustable version, adding C_{FB} between OUT and FB improves stability and transient response. The transient response of the TPS799xx-Q1 is enhanced by an active pulldown that engages when the output overshoots by approximately 5% or more when the device is enabled. When enabled, the pulldown device behaves like a 350-Ω resistor to ground.

Typical Application (continued)

8.2.2.5 Minimum Load

The TPS799xx-Q1 is stable and well behaved with no output load. To meet the specified accuracy, a minimum load of 500 µA is required. Below 500 µA at junction temperatures near 125°C, the output can drift up enough to cause the output pulldown to turn on. The output pulldown limits voltage drift to 5% typically, but ground current could increase by approximately 50 µA. In typical applications, the junction cannot reach high temperatures at light loads since there is no appreciable dissipated power. The specified ground current would then be valid at no load in most applications.

8.2.3 Application Curve

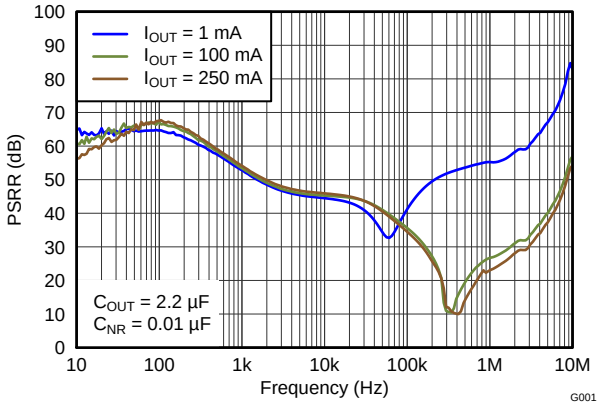


Figure 14. Power-Supply Rejection Ratio vs Frequency

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 2.7 V and 6.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply is well-regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

10.2 Layout Example

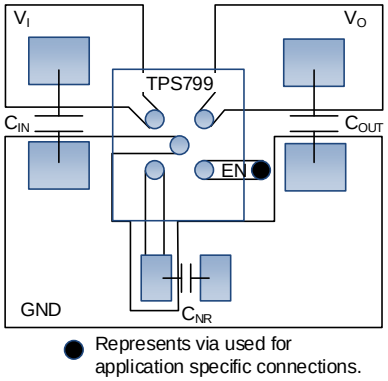


Figure 15. Layout Example

10.3 Thermal Consideration

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 145°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS799xx-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS799xx-Q1 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the head from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element, as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

10.5 Package Mounting

Solder pad footprint recommendations for the TPS799xx-Q1 are available from the TI website at www.ti.com.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Application report: *Using New Thermal Metrics*, SBVA025
- Application report: *IC Package Thermal Metrics*, SPRA953
- *TPS799xxEVM-105 User's Guide*, SLVU130

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS79901-Q1	Click here	Click here	Click here	Click here	Click here
TPS79912-Q1	Click here	Click here	Click here	Click here	Click here
TPS79915-Q1	Click here	Click here	Click here	Click here	Click here
TPS79918-Q1	Click here	Click here	Click here	Click here	Click here
TPS79925-Q1	Click here	Click here	Click here	Click here	Click here
TPS79927-Q1	Click here	Click here	Click here	Click here	Click here
TPS79933-Q1	Click here	Click here	Click here	Click here	Click here

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79901QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CFA	Samples
TPS79912QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	DAV	Samples
TPS79915QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFC	Samples
TPS79915QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RAQ	Samples
TPS79918QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CEW	Samples
TPS79925QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFM	Samples
TPS79927QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OFD	Samples
TPS79927QDRVRQ1	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFK	Samples
TPS79933QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PSEQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS799-Q1 :

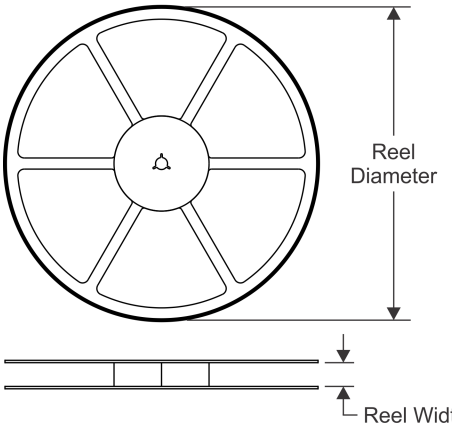
- Catalog: TPS799

NOTE: Qualified Version Definitions:

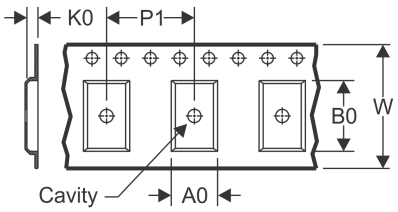
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

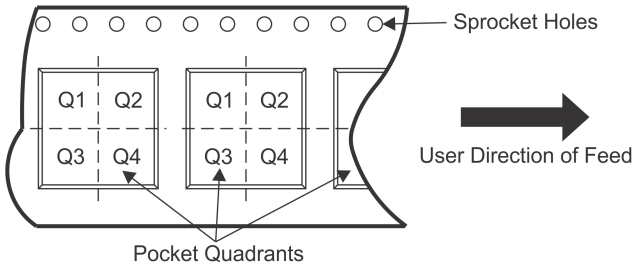


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

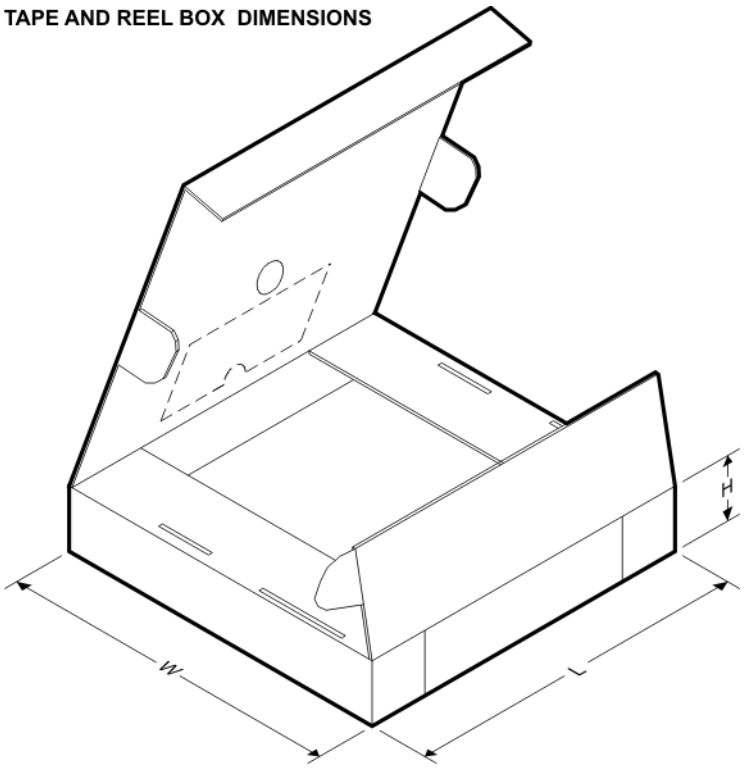
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79901QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79912QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79915QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79915QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79918QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79925QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79927QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS79927QDRVRQ1	WSON	DRV	6	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS79933QDDCRQ1	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

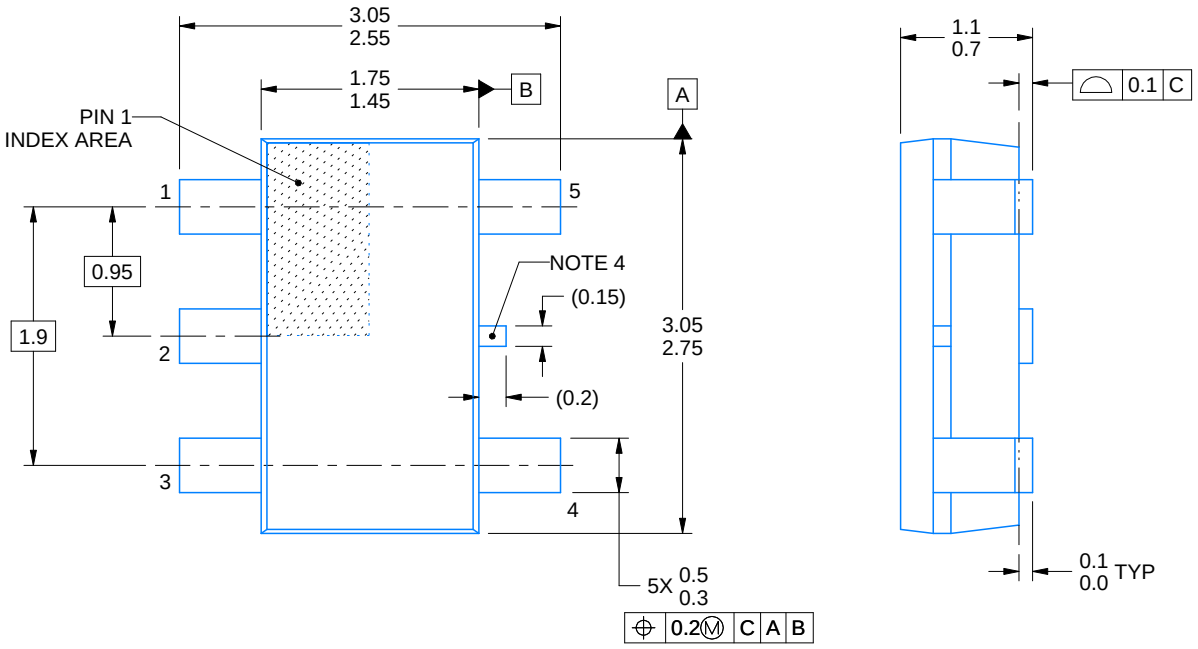
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79901QDRVRQ1	WSON	DRV	6	3000	200.0	183.0	25.0
TPS79912QDRVRQ1	WSON	DRV	6	3000	213.0	191.0	35.0
TPS79915QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79915QDRVRQ1	WSON	DRV	6	3000	213.0	191.0	35.0
TPS79918QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79925QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79927QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0
TPS79927QDRVRQ1	WSON	DRV	6	3000	213.0	191.0	35.0
TPS79933QDDCRQ1	SOT-23-THIN	DDC	5	3000	200.0	183.0	25.0

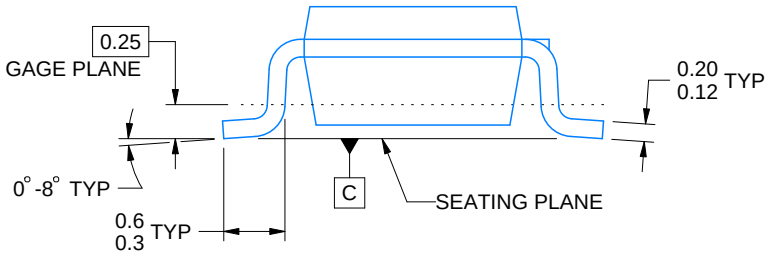
PACKAGE OUTLINE

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

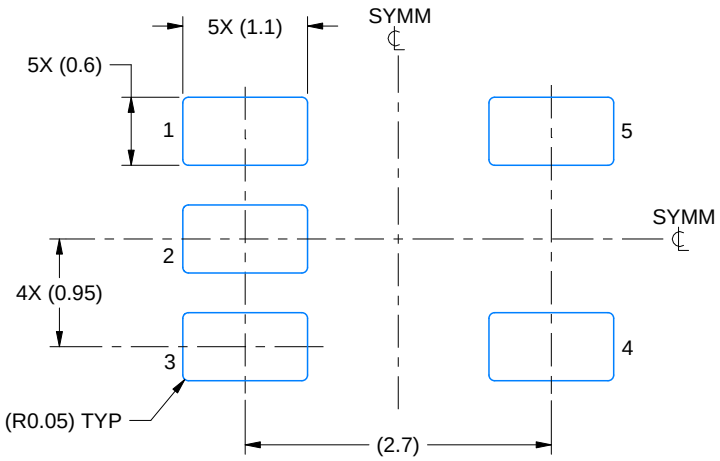




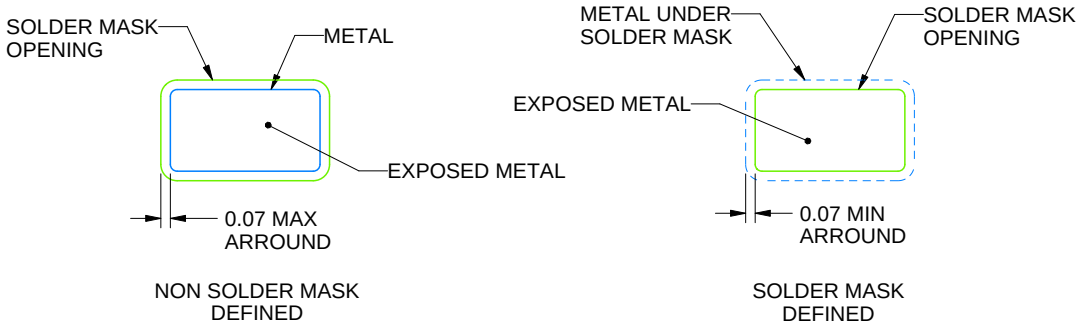
4220752/A 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X

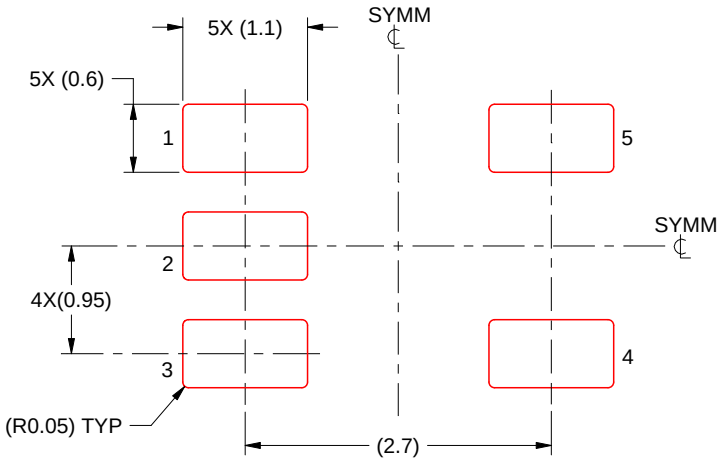


SOLDERMASK DETAILS

4220752/A 03/2023

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

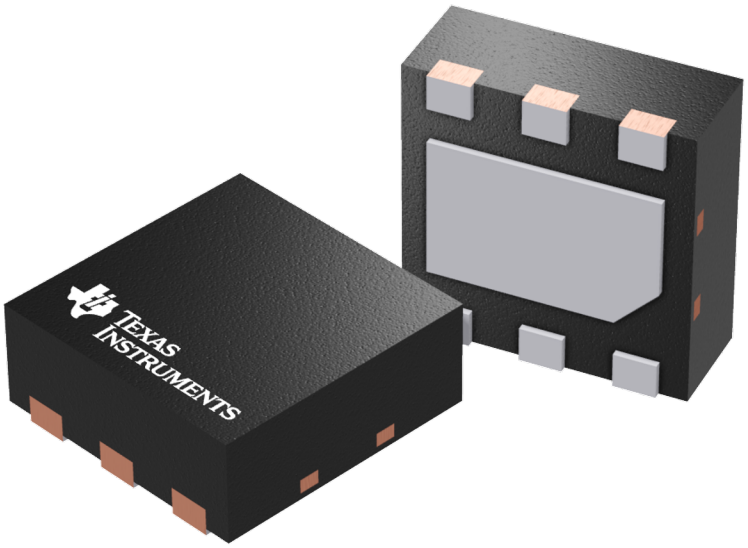
4220752/A 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



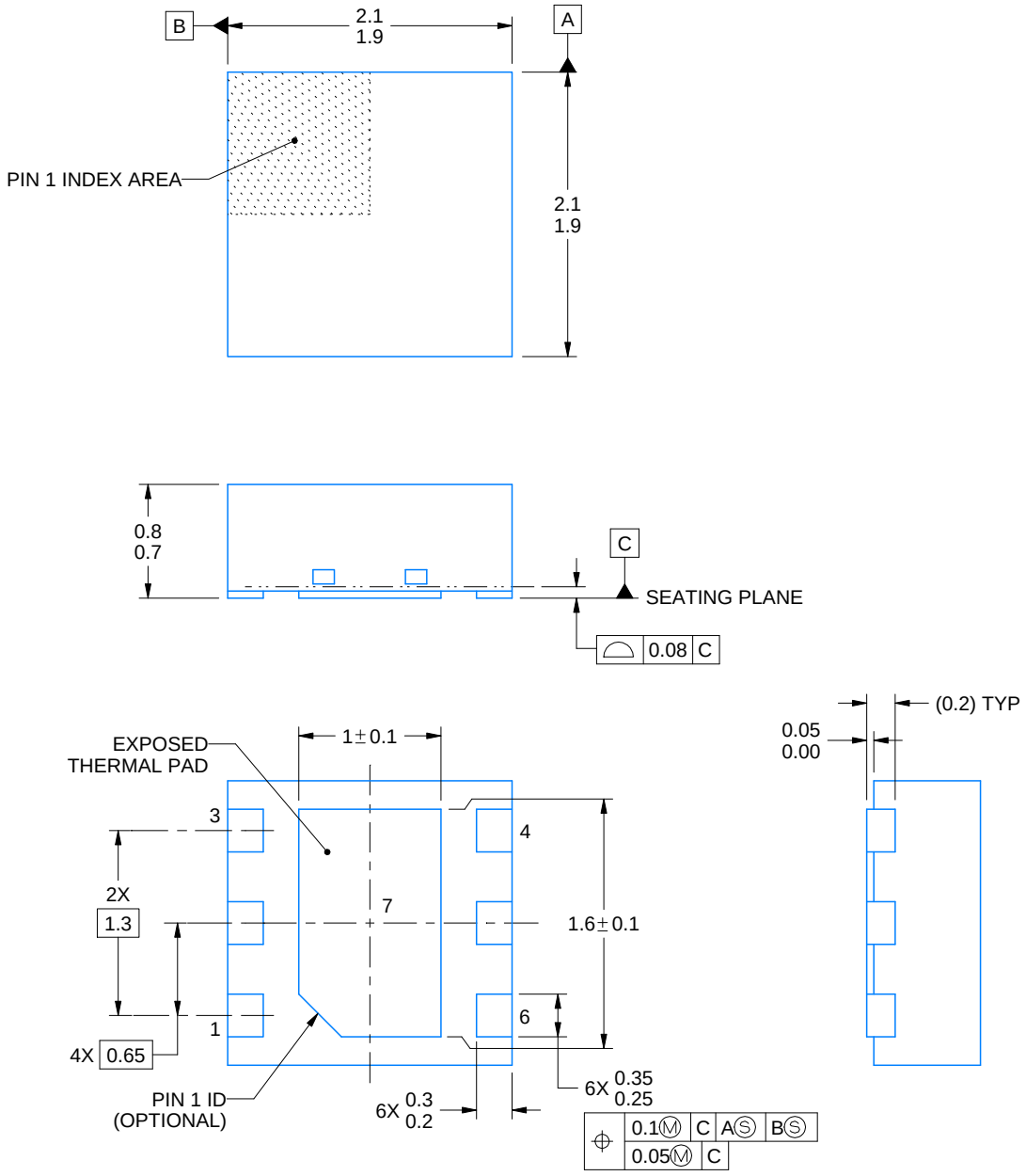
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

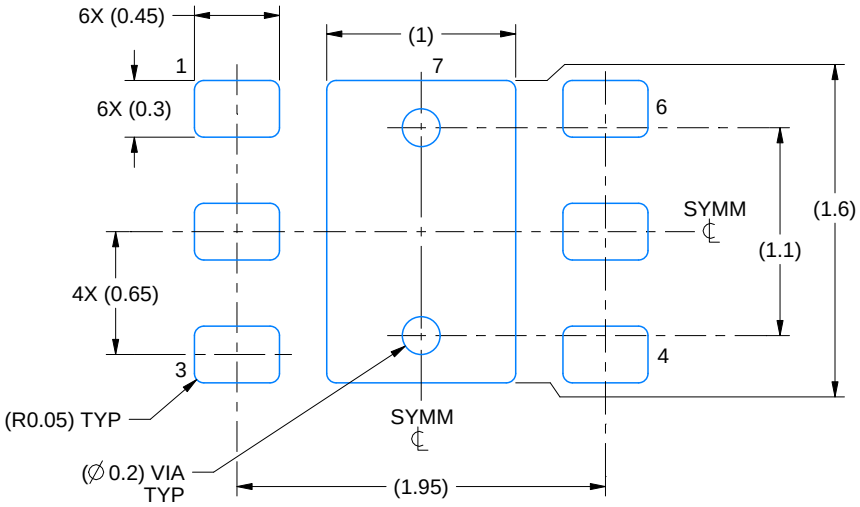
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

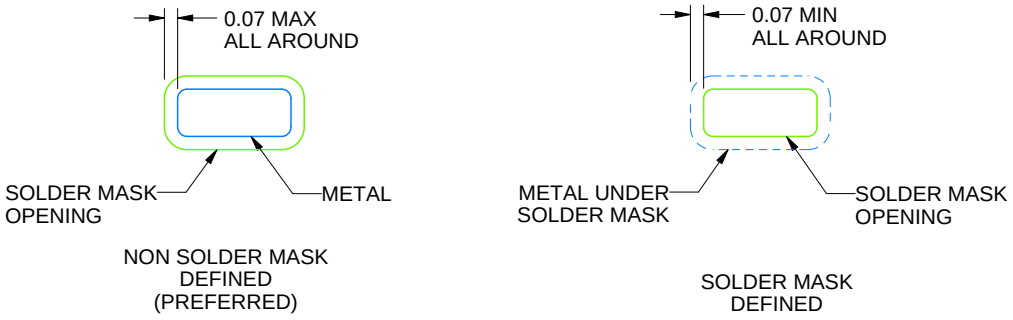


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

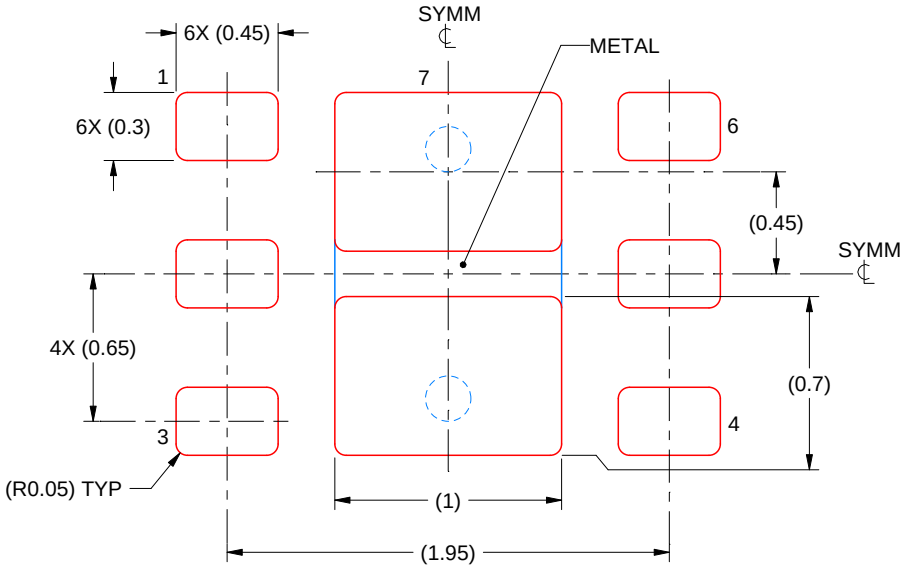
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

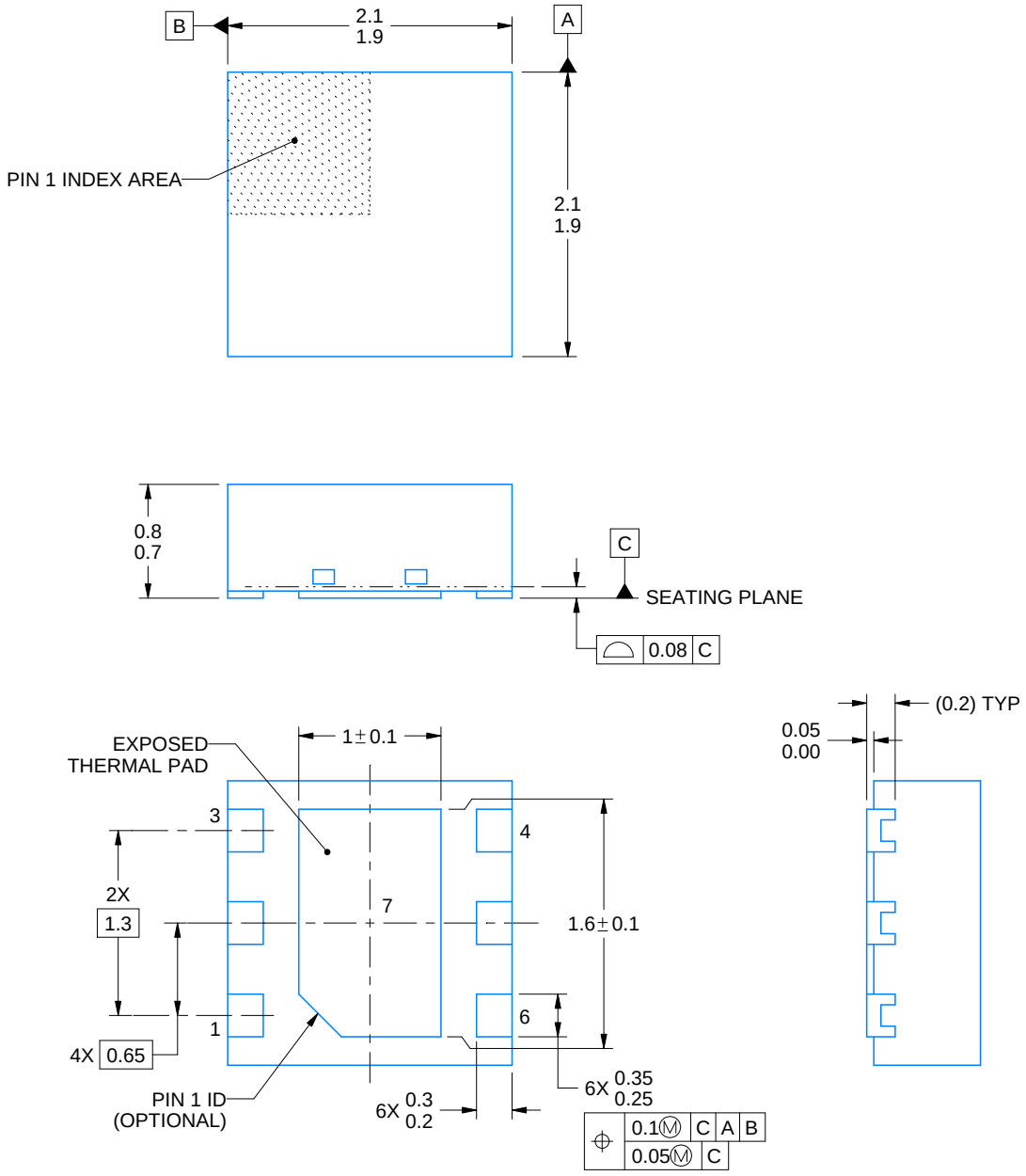
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

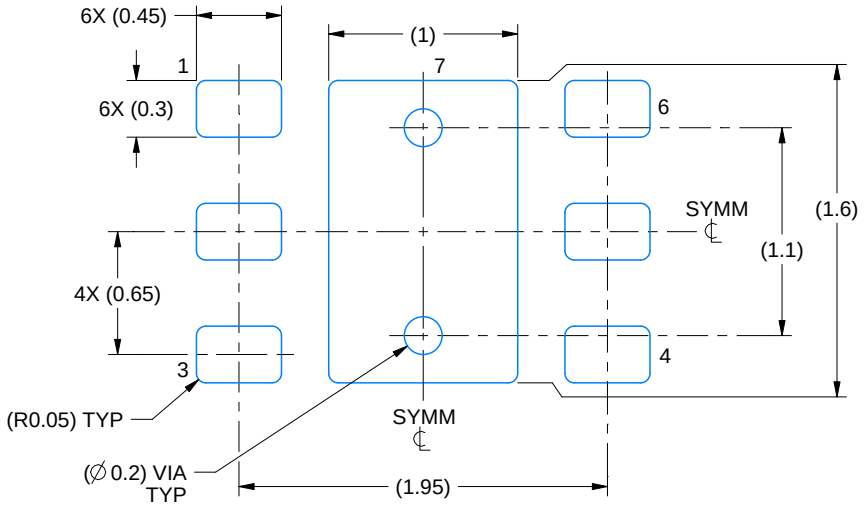
PLASTIC SMALL OUTLINE - NO LEAD



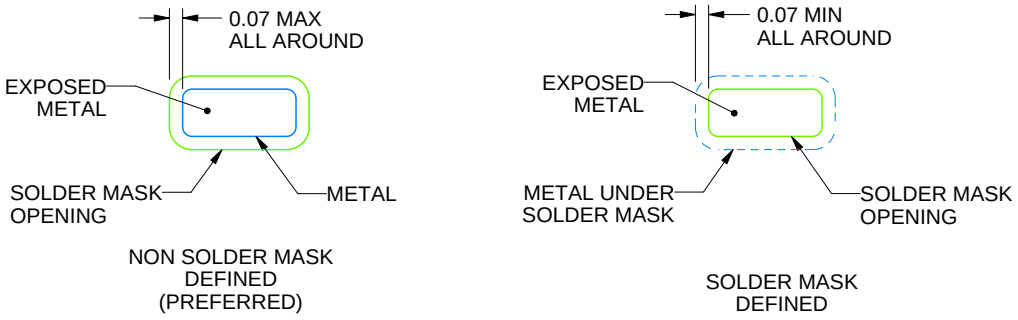
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

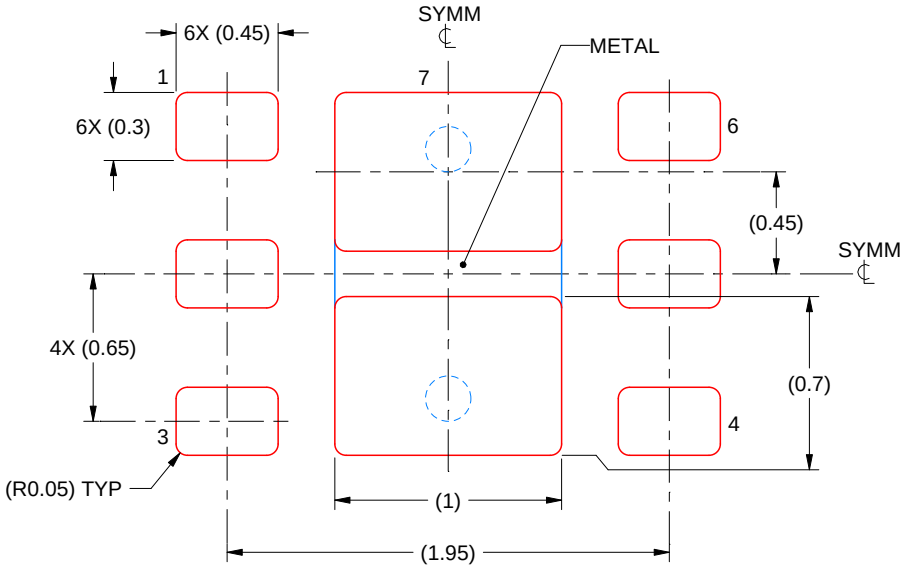


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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