*Click **here** to ask an associate for production status of specific part numbers.*

MAX20058

60V, 1A, Automotive Synchronous Step-Down DC-DC Converter

General Description

The MAX20058 is a high-efficiency, high-voltage, synchronous step-down DC-DC converter IC with integrated MOSFETs that operates over a 4.5V to 60V input. The converters can deliver up to 1A current. Output voltage is programmable from 0.8V to 90%V_{IN}. The feedback voltage regulation accuracy over -40°C to +125°C is ±1.5%.

The IC features a peak-current-mode-control architecture and can be operated in the pulse-width modulation (PWM) or pulse-frequency modulation (PFM) control schemes.

The MAX20058 is available in a 12-pin (3mm x 3mm), side-wettable TDFN package with an exposed pad for thermal heat dissipation.

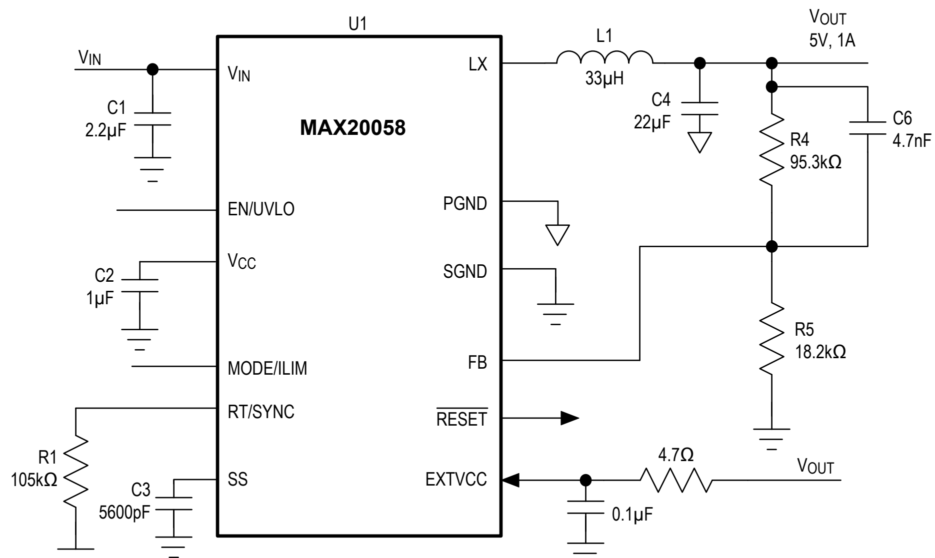
Applications

- 14V/24V Systems
- Truck Applications

Benefits and Features

- Synchronous DC-DC Converters with Integrated FETs
  - 60V Input for 14V and 24V Systems
  - Internal Compensation
- Flexibility
  - Output Adjustable from 0.8V to 90%V_{IN}
  - 200kHz to 2200kHz Adjustable Frequency with External Clock Synchronization
  - Programmable Peak Current Limit (1.14A or 1.6A)
- $\overline{\text{RESET}}$ Output and EN Input (26V, max) Simplify Power Sequencing
- Protection Features and Operating Range Ideal for Automotive Applications
  - Programmable EN/UVLO Threshold
  - Adjustable Soft-Start and Prebiased Power-Up
  - Thermal Shutdown
  - -40°C to +125°C Automotive Temperature Range
  - AEC-Q100 Qualified

Simplified Block Diagram



CIRCUIT FOR 5V OUTPUT, f_{SW} = 400kHz
(PFM MODE, 1.6A CURRENT LIMIT)

True Shutdown is a trademark of Maxim Integrated Products, Inc.

***Ordering Information** appears at end of data sheet.*

19-100263; Rev 3; 6/22

Absolute Maximum Ratings

V_{IN} to SGND .... -0.3V to +65V
EN/UVLO to SGND .... -0.3V to +26V
EXTVCC to SGND .... -0.3V to +14V
LX to PGND .... -0.3V to V_{IN} + 0.3V
FB, SS, MODE/ILIM,
RT/SYNC to SGND .... -0.3V to V_{CC} + 0.3V
PGND to SGND .... -0.3V to +0.3V
LX Total RMS Current .... ±1.2A
$\overline{RESET}$, V_{CC} to SGND .... -0.3V to +6V
Continuous Power Dissipation
(Multilayer Board) (T_A = +70°C,
derate 24.4mW/°C above +70°C) 1951.2mW
Operating Temperature Range .... -40°C to +125°C
Junction Temperature .... +150°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10s) .... +300°C
Soldering Temperature (reflow) .... +260ºC
ESD Protection – Human Body Model .... ±2kV

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 SW TDFN-EP

Package Code	TD1233Y+2
Outline Number	21-100176
Land Pattern Number	90-100072
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	41°C/W
Junction to Case (θ_{JC})	8.5°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = 24V, $V_{EN/UVLO}$ = unconnected, R_{RT} = 105kΩ, LX = unconnected, T_A = T_J = -40°C to +125°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{IN}		4.5		60	V
Input Shutdown Current	I_{IN-SH}	V_{EN} = 0V, shutdown mode	2.5	5	13	µA
Input Quiescent Current	I_{Q_PFM}	R_{ILIM} = open or 422kΩ		90		µA
	I_{Q_PWM}	R_{ILIM} = 243kΩ or 121kΩ	3	4	5	mA
ENABLE/UVLO (EN)						
EN Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.09	1.115	1.14	
	$V_{EN-TRUESD}$	$V_{EN/UVLO}$ falling, True Shutdown™		0.7		
EN Pull-up Current	I_{EN}	$V_{EN/UVLO}$ = 1.215V	2.2	2.5	2.8	µA
LDO (V_{CC})						
Output Voltage Range	V_{CC}	6V < V_{IN} < 60V, 0mA < I_{VCC} < 5mA	4.75	5	5.25	V
Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 12V	12	26	52	mA
Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 5mA			0.3	V

Electrical Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = unconnected, R_{RT} = 105kΩ, LX = unconnected, T_A = T_J = -40°C to +125°C, unless otherwise noted. (Note 1))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
UVLO	V_{CC-UVR}	V_{CC} rising	4.05	4.2	4.35	V
	V_{CC-UVF}	V_{CC} falling	3.65	3.8	3.95	
EXT LDO (EXTVCC)						
Switchover Threshold		EXTVCC rising	4.65	4.74	4.88	V
Switchover-Threshold Hysteresis				0.3		V
Dropout	EXTVCC-DO	V_{EXTVCC} = 4.75V, I_{VCC} = 5mA			0.1	V
Current Limit		V_{CC} = 4.3V, V_{EXTVCC} = 5V	15	21	34	mA
POWER MOSFETs						
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A, sourcing		0.9	1.8	Ω
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A, sinking		0.275	0.55	Ω
LX Leakage Current		T_A = +25°C			2	µA
SOFT-START						
Charging Current	I_{SS}		4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB}	R_{ILIM} = 243kΩ or 121kΩ	0.788	0.8	0.812	V
		R_{ILIM} = open or 422kΩ	0.788	0.812	0.824	
FB Input Leakage Current		V_{FB} = 1V, T_A = +25°C	-100		100	nA
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{SOURCE-LIMIT}$	R_{ILIM} = open or 243kΩ	1.4	1.6	2.0	A
		R_{ILIM} = 121kΩ or 422kΩ	0.94	1.14	1.36	
Negative Current-Limit Threshold	$I_{SINK-LIMIT}$	R_{ILIM} = open or 422kΩ		2.5		mA
		R_{ILIM} = 243kΩ	0.57	0.65	0.725	A
		R_{ILIM} = 121kΩ	0.35	0.455	0.56	
PFM Current Level	IPFM	R_{ILIM} = open	0.235	0.33	0.44	A
		R_{ILIM} = 422kΩ	0.125	0.23	0.32	
MODE						
MODE PFM Threshold		Rising	1	1.22	1.44	V
Hysteresis				0.19		V
TIMINGS						
Minimum On-Time	t_{ON-MIN}		45	70	120	ns
Maximum Duty Cycle	DMAX		89	93	97	%

Electrical Characteristics (continued)

(V_{IN} = 24V, $V_{EN/UVLO}$ = unconnected, R_{RT} = 105kΩ, LX = unconnected, T_A = T_J = -40°C to +125°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
Switching Frequency	f_{SW}	R_{RT} = 210kΩ	180	200	220	kHz
		R_{RT} = 140kΩ	270	300	330	
		R_{RT} = 105kΩ	360	400	440	
		R_{RT} = 69.8kΩ	540	600	660	
		R_{RT} = 19.1kΩ	1800	2033	2200	
SYNC Input Frequency per R_{RT}			1.15 x f_{SW}		1.4 x f_{SW}	kHz
SYNC Input Frequency Range			220		2200	kHz
SYNC Pulse Minimum Off-Time		SYNC pulse must exceed this number	40			ns
SYNC High Threshold	V_{SYNC-H}		1	1.22	1.44	V
SYNC Hysteresis	$V_{SYNC-HYS}$			0.18		V
Number of SYNC Pulses to Enable Synchronization		(Note 2)		1		cycle
$\overline{\text{RESET}}$						
UV Threshold Rising		V_{FB} rising		95		%
UV Threshold Falling		V_{FB} falling		92		%
Delay after FB Reaches 95% Regulation				2.1		ms
Output Low Level		I_{RESET} = 1mA			0.09	V
Output Leakage Current		T_A = +25°C			1	µA
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising (Note 2)		160		°C
Hysteresis		(Note 2)		20		°C

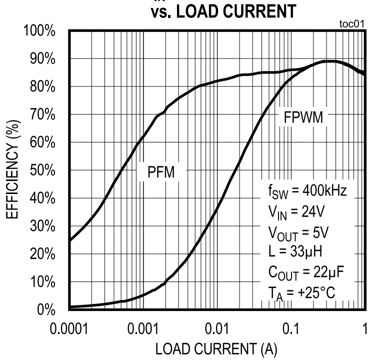
Note 1: All limits are 100% tested at +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are at T_A = +25°C.

Note 2: Guaranteed by design, not production tested.

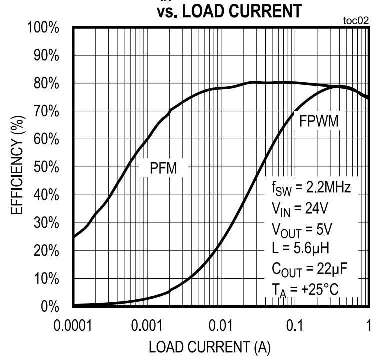
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

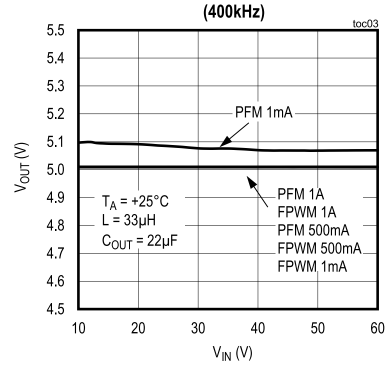
$24V_{IN}$ 400kHz EFFICIENCY vs. LOAD CURRENT



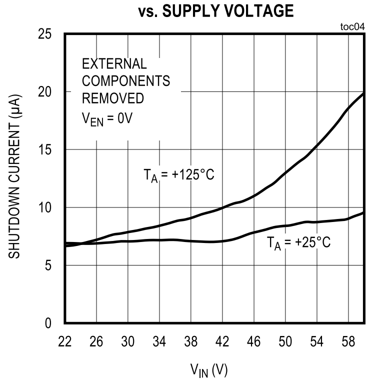
$24V_{IN}$ 2.2MHz EFFICIENCY vs. LOAD CURRENT



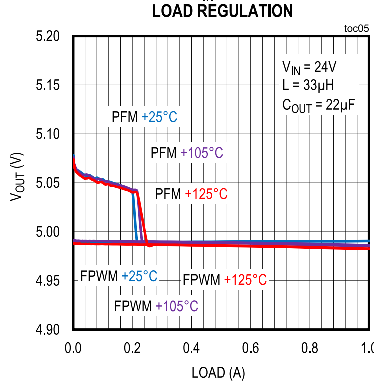
LINE REGULATION (400kHz)



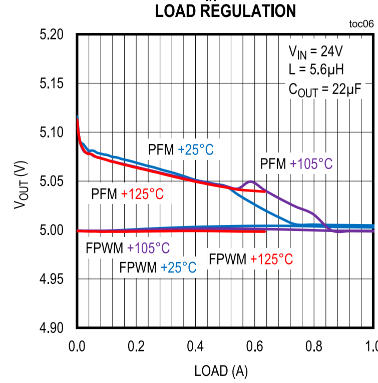
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



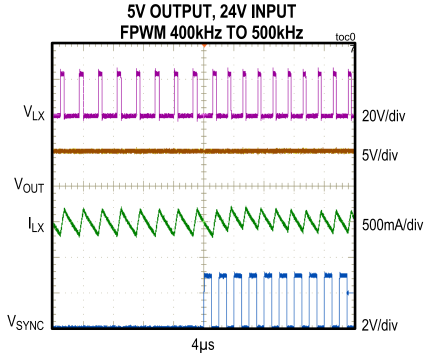
$24V_{IN}$ 400kHz LOAD REGULATION



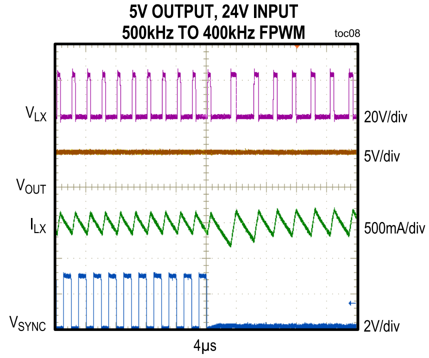
$24V_{IN}$ 2.2MHz LOAD REGULATION



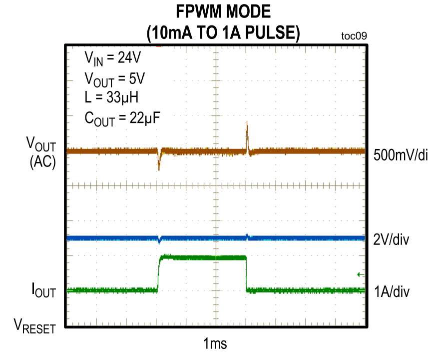
APPLICATION OF EXTERNAL CLOCK 5V OUTPUT, 24V INPUT FPWM 400kHz TO 500kHz



REMOVAL OF EXTERNAL CLOCK 5V OUTPUT, 24V INPUT 500kHz TO 400kHz FPWM



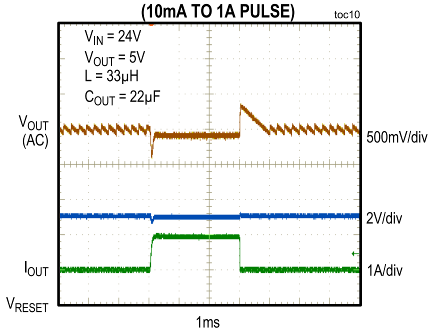
LOAD TRANSIENT FPWM MODE (10mA TO 1A PULSE)



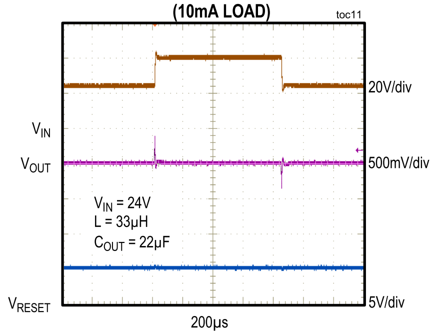
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

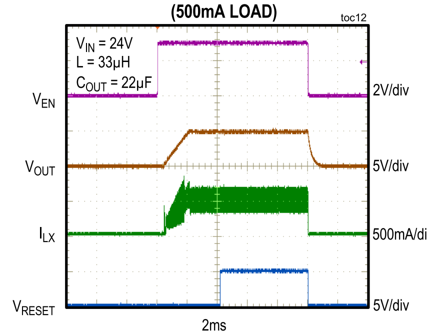
LOAD TRANSIENT PFM MODE (10mA TO 1A PULSE)



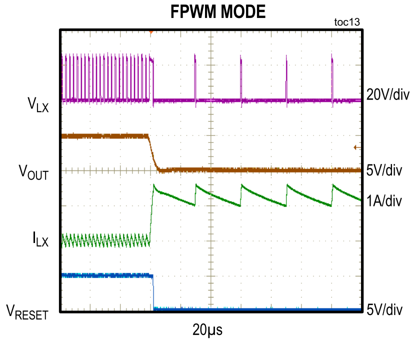
LINE TRANSIENT FPWM MODE (10mA LOAD)



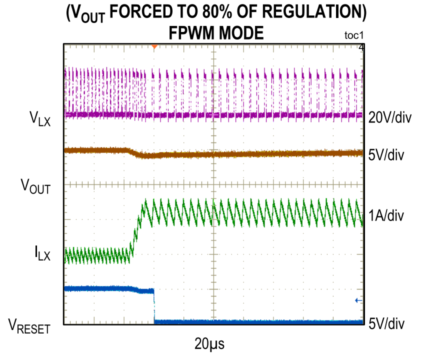
SOFT-START/SHUTDOWN FROM EN FPWM MODE (500mA LOAD)



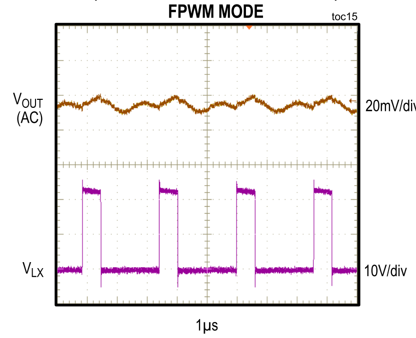
SHORT-CIRCUIT FPWM MODE



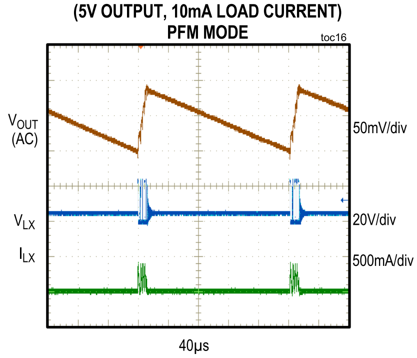
SOFT SHORT-CIRCUIT (V_{OUT} FORCED TO 80% OF REGULATION) FPWM MODE



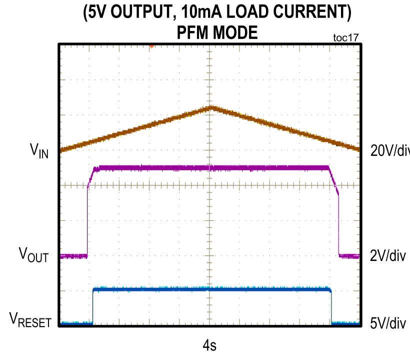
STEADY-STATE SWITCHING WAVEFORMS (5V OUTPUT, 1A LOAD CURRENT) FPWM MODE



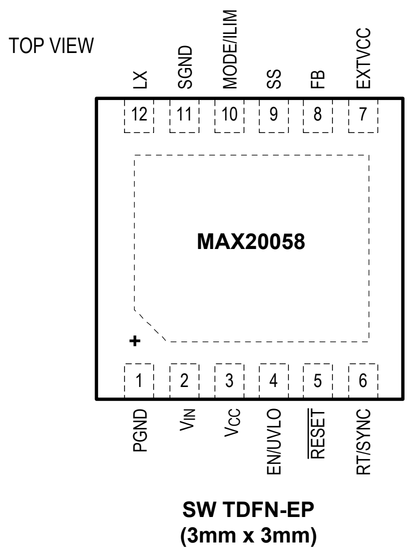
STEADY-STATE SWITCHING WAVEFORMS (5V OUTPUT, 10mA LOAD CURRENT) PFM MODE



SLOW INPUT VOLTAGE (5V OUTPUT, 10mA LOAD CURRENT) PFM MODE



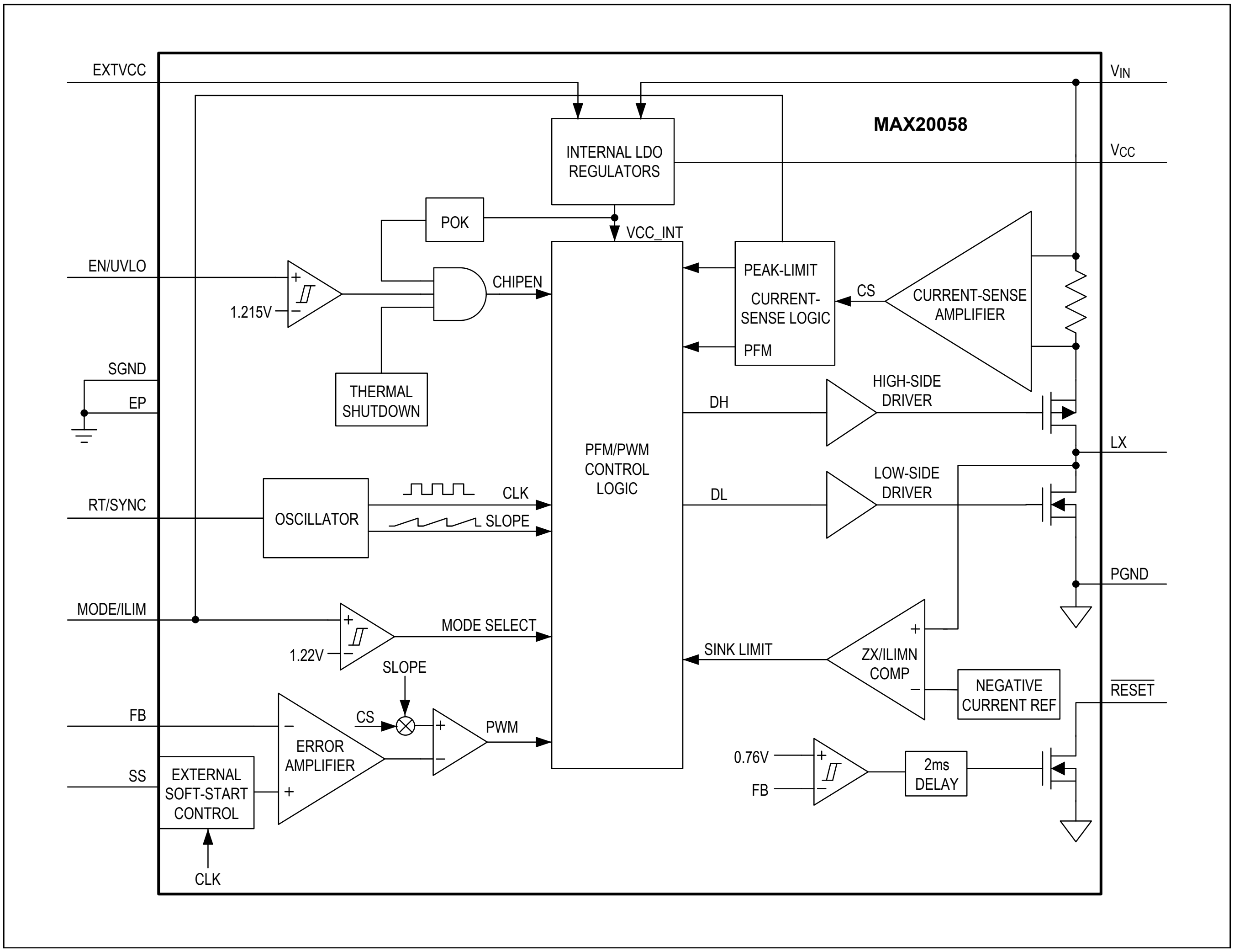
Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1	PGND	Power Ground Pin of the Converter. Connect externally to the power ground plane. Connect the SGND and PGND pins together at the ground return path of the V_{CC} bypass capacitor.
2	V_{IN}	Power-Supply Input. 4.5V to 60V input supply range. Decouple to PGND with a 2.2μF capacitor; place the capacitor close to the V_{IN} and PGND pins.
3	V_{CC}	5V LDO Output. Bypass V_{CC} with a 1μF ceramic capacitance to SGND. This LDO is intended to power internal circuits only.
4	EN/UVLO	Enable/Undervoltage Lockout Pin. Drive EN/UVLO high to enable the output. Connect to the center of the resistor-divider between V_{IN} and SGND to set the input voltage at which the part turns on. Leave the pin unconnected for always-on operation.
5	$\overline{RESET}$	Open-Drain $\overline{RESET}$ Output. The $\overline{RESET}$ output is driven low if FB drops below 92% of its set value. $\overline{RESET}$ goes high 2.1ms after FB rises above 95% of its set value.
6	RT/SYNC	Frequency-Set and Synchronization Pin. Connect a resistor from RT/SYNC to SGND to set the switching frequency of the part between 200kHz and 2000kHz. An external clock can be connected to the RT/SYNC pin to synchronize the part with an external frequency up to 2200kHz.
7	EXTVCC	External Power-Supply Input for the Internal LDO
8	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to SGND to set the output voltage.
9	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
10	MODE/ILIM	Mode and Current-Limit Set Pin. Connect a resistor from MODE/ILIM to SGND to program the peak and runaway current limits and mode of operation of the part. See the *Current Limit and Mode of Operation* section for more details.
11	SGND	Analog Ground
12	LX	Switching Node. Connect the LX pin to the switching side of the inductor.
—	EP	Exposed Pad. Connect EP to the SGND pin. Connect to a large copper plane below the IC to improve heat-dissipation capability. Add thermal vias below the exposed pad.

Functional Diagram



Detailed Description

The MAX20058 high-efficiency, high-voltage, step-down DC-DC regulator IC operates from 4.5V to 60V and delivers up to 1A load current. Feedback voltage-regulation accuracy meets ±1.5% over load, line, and temperature.

The IC uses a peak-current-mode-control scheme. An internal transconductance error amplifier generates an integrated error voltage. The error voltage sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator.

At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached or the peak current limit is detected.

During the high-side MOSFET's on-time, the inductor current ramps up. During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on and remains on until either the next rising edge of the clock arrives or sink current limit is detected. The inductor releases the stored energy as its current ramps down and provides current to the output. The internal low $R_{DS(ON)}$ pMOS/nMOS switches ensure high efficiency at full load.

The IC also integrates a switching-frequency selector pin, current-limit and mode-of-operation selector pin, enable/undervoltage lockout (EN/UVLO) pin, programmable soft-start pin, and open-drain $\overline{RESET}$ signal.

Current Limit and Mode of Operation

Table 1 lists the value of the resistors to program PWM or PFM modes of operation and 1.6A or 1.14A peak current limits.

The mode of operation cannot be changed "on-the-fly" after power-up.

Table 1. R_{ILIM} Settings

R_{ILIM} (kΩ)	PEAK CURRENT LIMIT (A)	MODE OF OPERATION
Open	1.6	PFM
422	1.14	PFM
243	1.6	PWM
121	1.14	PWM

PWM Mode of Operation

In PWM mode, the inductor current can go negative. The PWM mode of operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, PWM mode gives lower efficiency at light loads compared to PFM mode.

PFM Mode of Operation

The PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak every clock cycle until the output rises to 102% of the nominal voltage by monitoring the FB pin. Resistor tolerance will impact actual output voltage. Once the output reaches 102% of the nominal voltage, both the high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks and again commences the process of delivering pulses of energy to the output until it reaches 102% of the nominal output voltage.

The advantage of PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. However, the output-voltage ripple is higher compared to PWM mode, and switching frequency is not constant at light loads.

Linear Regulator (V_{CC})

The IC has two internal low-dropout regulators (LDOs), which power V_{CC}. One LDO is powered from the input voltage and the other LDO is powered from the EXTVCC pin. Only one of the two LDOs is in operation at a time, depending on the voltage levels present at the EXTVCC pin.

If EXTVCC rises above 4.74V (typ), V_{CC} is powered from the EXTVCC pin. If EXTVCC falls below 4.44V (typ), V_{CC} is powered from the input voltage. Powering V_{CC} from EXTVCC increases efficiency, particularly at higher input voltages. Typical V_{CC} output voltage is 5V. Bypass V_{CC} to SGND with a 1μF capacitor.

When V_{CC} falls below its undervoltage lockout (3.8V, typ), the internal step-down controller is turned off and LX switching is disabled. The LX switching is enabled again when the V_{CC} voltage exceeds 4.2V (typ). The 400mV (typ) hysteresis prevents chattering on power-up and power-down.

When powering EXTVCC from V_{OUT}, an R-C network should be placed in the path to protect the LDO from a potential negative voltage transient due to a short-circuit event. A 4.7Ω resistor and a 0.1μF capacitor are recommended (see the *Typical Application Circuit*).

Switching-Frequency Selection and External Frequency Synchronization

The RT/SYNC pin programs the switching frequency of the converter. Connect a resistor from RT/SYNC to SGND to set the switching frequency of the part at any one of five discrete frequencies: 200kHz, 300kHz, 400kHz, 600kHz, or 2MHz (see Table 2 for resistor values).

The internal oscillator of the device can be synchronized to an external clock signal on the RT/SYNC pin. The external synchronization clock frequency must be between 1.15 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the switching frequency programmed by the resistor connected from the RT/SYNC pin. The MAX20058 has been tested up to 2000kHz with a 19.1kΩ resistor.

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as shown in the following equation.

Equation 1:

$$V_{IN(MIN)} = \frac{(V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR} + 0.55)}{D_{MAX}} + (I_{OUT(MAX)} \times 1.25)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON(MIN)}}$$

where V_{OUT} is the steady-state output voltage, $I_{OUT(MAX)}$ is the maximum load current, R_{DCR} is the DC resistance of the inductor, D_{MAX} is the maximum allowable duty ratio (0.89), $f_{SW(MAX)}$ is the maximum switching frequency, and $t_{ON(MIN)}$ is the worst-case minimum switch on-time (120ns).

Table 2. RT/SYNC Resistor Settings

RT/SYNC RESISTOR VALUE (kΩ)	SWITCHING FREQUENCY (kHz)
210	200
140	300
105	400
69.8	600
19.1	2000

Overcurrent Protection

The IC is provided with a robust overcurrent-protection scheme that protects the device under overload and output short-circuit conditions. The positive current limit is triggered when the peak value of the inductor current hits a fixed threshold (ILIM_P, 1.6A/1.14A). At this point, the high-side switch is turned off and the low-side switch turned on. The low-side switch is kept on until the inductor current discharges below 0.7 x ILIM_P.

While in PWM mode, the negative current limit is triggered when the valley value of the inductor current hits a fixed threshold (ILIM_N, -0.65A/-0.455A, depending on the value of the resistor connected to the MODE/ILIM pin). At this point, the low-side switch is turned off and the high-side switch is turned on.

$\overline{RESET}$ Output

The IC includes a $\overline{RESET}$ pin to monitor the output voltage. The open-drain $\overline{RESET}$ output requires an external pull-up resistor. $\overline{RESET}$ goes high (high impedance) in 2.1ms after the output voltage increases above 95% of the nominal voltage. $\overline{RESET}$ goes low when the output voltage drops to below 92% of the nominal voltage. $\overline{RESET}$ also goes low during thermal shutdown.

Thermal-Shutdown Protection

The IC features thermal-overload protection and turns off when the junction temperature exceeds +160°C (typ). Once the device cools by 20°C (typ), it turns back on with a soft-start sequence.

Applications Information

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (ISAT) and DC resistance (RDCR). To select inductor value, the ratio of inductor peak-to-peak AC current to DC average current (LIR) must be selected first. A good compromise between size and loss is a 30% peak-to-peak ripple current to average-current ratio (LIR = 0.3). The switching frequency, input voltage, output voltage, and selected LIR then determine the inductor value as follows:

Equation 2:

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times I_{OUT} \times \text{LIR}}$$

where V_{OUT}, I_{OUT}, and f_{SW} are nominal values.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and the lowest possible DC resistance. The saturation current rating (ISAT) of the inductor must be high enough to ensure that saturation occurs only above the peak current-limit value.

Input Capacitor Selection

A low-ESR ceramic input capacitor of 4.7μF is recommended for proper device operation. This value can be adjusted based on application input-voltage-ripple requirements.

The discontinuous input current of the buck converter causes large input ripple current. The switching frequency, peak inductor current, and the allowable peak-to-peak input-voltage ripple dictate the input-capacitance requirement. Increasing the switching frequency or the inductor value lowers the peak-to-average current ratio, yielding a lower input-capacitance requirement.

The input ripple comprises of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the input capacitor). The total voltage ripple is the sum of ΔV_Q and ΔV_{ESR}. Assume that input-voltage ripple from the ESR and the capacitor discharge is equal to 50% each. The following equations show the ESR and capacitor requirement for a target voltage ripple at the input:

Equation 3:

$$\text{ESR} = \frac{\Delta V_{ESR}}{I_{OUT} + (\Delta I_{P-P} / 2)}$$

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and:

$$D = \frac{V_{OUT}}{V_{IN}}$$

where I_{OUT} is the output current, D is the duty cycle, and f_{SW} is the switching frequency. Use additional input capacitance at lower input voltages to avoid possible undershoot below the UVLO threshold during transient loading.

Output Capacitor Selection

For optimal phase margin, a 22μF output capacitor is recommended. Additional output capacitance may be needed based on application-specific, output-voltage-ripple requirements. If the total output capacitance required is > 70μF, contact the factory for an optimized solution.

The allowable output-voltage ripple and the maximum deviation of the output voltage during step-load currents determine the output capacitance and its ESR.

V_{OUT} Ripple Requirement

The output ripple comprises ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the output capacitor). Use low-ESR ceramic or aluminum electrolytic capacitors at the output. For aluminum electrolytic capacitors, the entire output ripple is contributed by ΔV_{ESR}. Use Equation 4 to calculate the ESR requirement and choose the capacitor accordingly. If using ceramic capacitors, assume the contribution to the output ripple voltage from the ESR and the capacitor discharge to be equal. The following equations show the output capacitance and ESR requirement for a specified output-voltage ripple.

Equation 4:

$$ESR = \frac{\Delta V_{ESR}}{\Delta I_{P-P}}$$

$$C_{OUT} = \frac{\Delta I_{P-P}}{8 \times \Delta V_Q \times f_{SW}}$$

where:

$$\Delta I_{P-P} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times f_{SW} \times L}$$

and:

$$V_{OUT\_RIPPLE} = \Delta V_{ESR} + \Delta V_Q$$

ΔI_{P-P} is the peak-to-peak inductor current as calculated above, and f_{SW} is the converter's switching frequency.

Transient Response Requirement

The allowable deviation of the output voltage during fast-transient loads also determines the output capacitance and its ESR. The output capacitor supplies the step-load current until the converter responds with a greater duty cycle. The response time ($t_{RESPONSE}$) depends on the closed-loop bandwidth of the converter. The high switching frequency of the devices allows for a higher closed-loop bandwidth, thus reducing $t_{RESPONSE}$ and the output-capacitance requirement. The resistive drop across the output capacitor's ESR and the capacitor discharge causes a voltage droop during a step load. Keep the maximum output-voltage deviations below the tolerable limits of the electronics being powered. When using a ceramic capacitor, assume an 80% and 20% contribution from the output-capacitance discharge and the ESR drop, respectively. Use the following equations to calculate the required ESR and capacitance value:

Equation 5:

$$ESR_{OUT} = \frac{\Delta V_{ESR}}{I_{STEP}}$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_Q}$$

where I_{STEP} is the load step and $t_{RESPONSE}$ is the response time of the converter.

Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time for the corresponding output voltage. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as shown below.

Equation 6:

$$C_{SS} \geq 30 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation.

Equation 7:

$$t_{SS} = \frac{C_{SS}}{6.25 \times 10^{-6}}$$

For example, to program a 2ms soft-start time, a 12nF capacitor should be connected from the SS pin to SGND.

Adjusting the Output Voltage

Set the output voltage with resistive voltage-dividers connected from the positive terminal of the output capacitor (V_{OUT}) to SGND (Figure 1). Connect the center node of the divider to the FB pin. To optimize efficiency and output accuracy, use the following calculations to choose the resistive divider values.

Equation 8:

$$R4 = \frac{15 \times V_{OUT}}{0.8}$$

$$R5 = \frac{R4 \times 0.8}{(V_{OUT} - 0.8)}$$

where R4 and R5 are in kΩ.

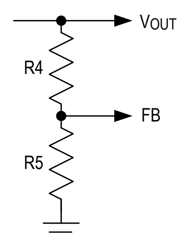


Figure 1. Setting the Output Voltage

Series R-C Selection

To achieve higher bandwidth, connect an R-C series circuit across the bottom feedback resistor (see Figure 2).

Select the R-C (R6 and C6) values using the following equations:

Equation 9:

$$R6 = \frac{R4 \times R5}{R4 + R5} \times \frac{k}{1 - 0.99k}$$

$$C6 = \frac{1.125 \times 10^6}{f_C \times R6 \times \sqrt{\frac{k}{1 - k^2}}}$$

where:

$$k = \frac{f_C \times C_{OUT} \times (1 + \frac{R4}{R5})}{3.6274}$$

And C_{OUT} is the derated capacitance value for a given bias voltage in μF, f_C is the targeted crossover frequency in Hz, (15kHz or 1/20th of f_{SW}; whichever is lower) R4 and R5 are the feedback network in kΩ, R6 is in kΩ, and C6 is in nF.

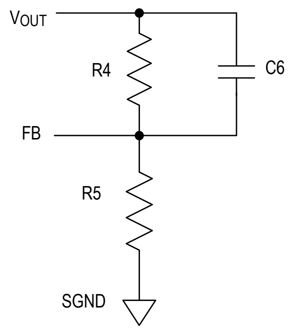


Figure 2. R-C Network for Increased Phase Margin

Setting the Undervoltage Lockout

Drive EN/UVLO high to enable the output. Leave the pin unconnected for always-on operation. Set the voltage at which each converter turns on with a resistive voltage-divider connected from V_{IN} to SGND (see Figure 3). Connect the center node of the divider to EN/UVLO pin.

Equation 10 (choose R1 as follows):

$$R1 \leq (110000 x V_{INU})$$

where V_{INU} is the input voltage at which the device is required to turn on and R1 is in Ω. Calculate the value of R2 as shown in Equation 11.

Equation 11:

$$R2 = \frac{1.215 \times R1}{(V_{INU} - 1.215 + (2.5\mu A \times R1))}$$

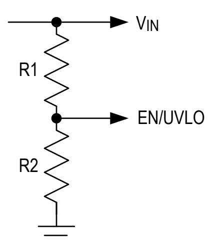


Figure 3. Undervoltage-Lockout Divider

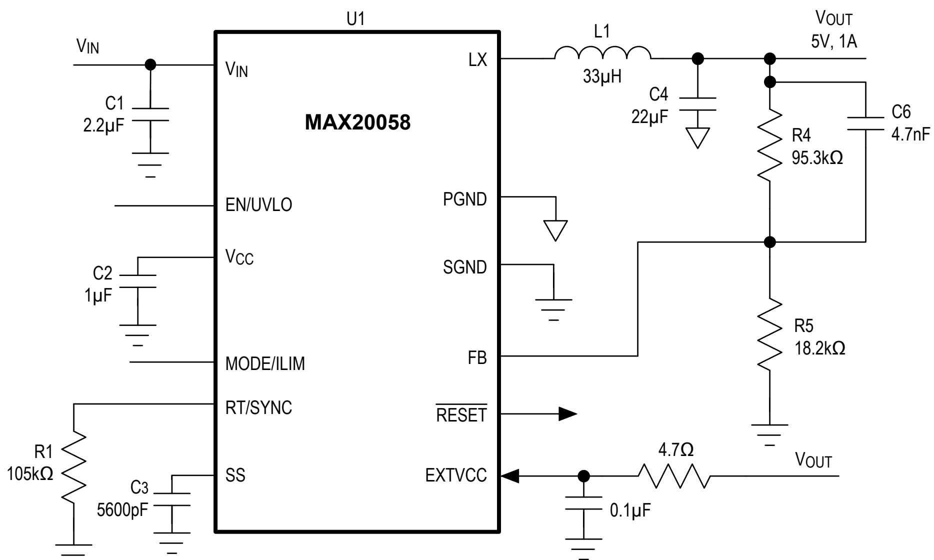
PCB Layout Guidelines

Careful PCB layout is critical to achieve low switching power losses and clean, stable operation. Use a multilayer board wherever possible for better noise immunity. Follow the guidelines below for a good PCB layout:

1. Place the input capacitor right next to the V_{IN} pin. The bypass capacitor for the V_{CC} pin should be as close as possible to the pin. The feedback trace should be routed away from the inductor.
2. Solder the exposed pad to a large copper-plane area under the device. To effectively use this copper area as heat exchanger between the PCB and ambient, expose the copper area on the top and bottom side. Add a few small vias or one large via on the copper pad for efficient heat transfer. Connect the exposed pad to PGND, ideally at the return terminal of the output capacitor.
3. Isolate the power components and high-current paths from sensitive analog circuitry.
4. Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation.

5. Connect PGND and SGND together, preferably at the return terminal of the input capacitor. Do not connect them anywhere else.
6. Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCB to enhance full-load efficiency and power-dissipation capability.
7. Route high-speed switching nodes away from sensitive analog areas. Use internal PCB layers as PGND to act as EMI shields to keep radiated noise away from the device and analog bypass capacitor.

Typical Application Circuit



CIRCUIT FOR 5V OUTPUT, f_{SW} = 400kHz
(PFM MODE, 1.6A CURRENT LIMIT)

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX20058ATCA/VY+	-40°C to +125°C	12 SW TDFN-EP*

/V Denotes an automotive-qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

SW = Side-wettable package.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—
1	6/18	Updated Output Voltage Range and last row in Switching Frequency rows in Electrical Characteristics table; replaced TOC04 and updated TOC12 in Typical Operating Characteristics section; updated Switching-Frequency Selection and External Frequency Synchronization section and the last row in Table 2	3, 4, 6, 7, 12
2	4/19	Updated Absolute Maximum Rating, Equation 6 and Series R-C Selection section	2, 14, 15
3	6/22	Updated Figure 2 and Typical Application Circuit	14, 16