Low Voltage Full Bridge Brushless DC Motor Driver with Hall Commutation and Soft Switching, and Reverse Battery, Short Circuit, and Thermal Shutdown Protection

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: March 4, 2013

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

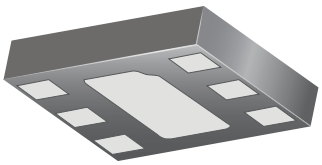
Low Voltage Full Bridge Brushless DC Motor Driver with Hall Commutation and Soft Switching, and Reverse Battery, Short Circuit, and Thermal Shutdown Protection

Features and Benefits

- Low voltage operation
- Reverse voltage protection on VDD and $\overline{\text{SLEEP}}$ pins
- Output short circuit and thermal shutdown protections
- Soft switching algorithm to reduce audible switching noise and EMI interference
- Unidirectional working mode provides motor rotation in one direction
- Hall chopper stabilization technique for precise signal response over operating range
- Sleep mode pin allowing external logic signal enable/disable to reduce average power consumption
- Antistall feature guarantees continuous rotation
- Low current consumption sleep mode
- Single-chip solution for high reliability
- Miniature MLP/DFN package

Package: 6 pin MLP/DFN (suffix EW)

1.5 mm × 2 mm, 0.40 mm maximum overall height



Approximate scale

Description

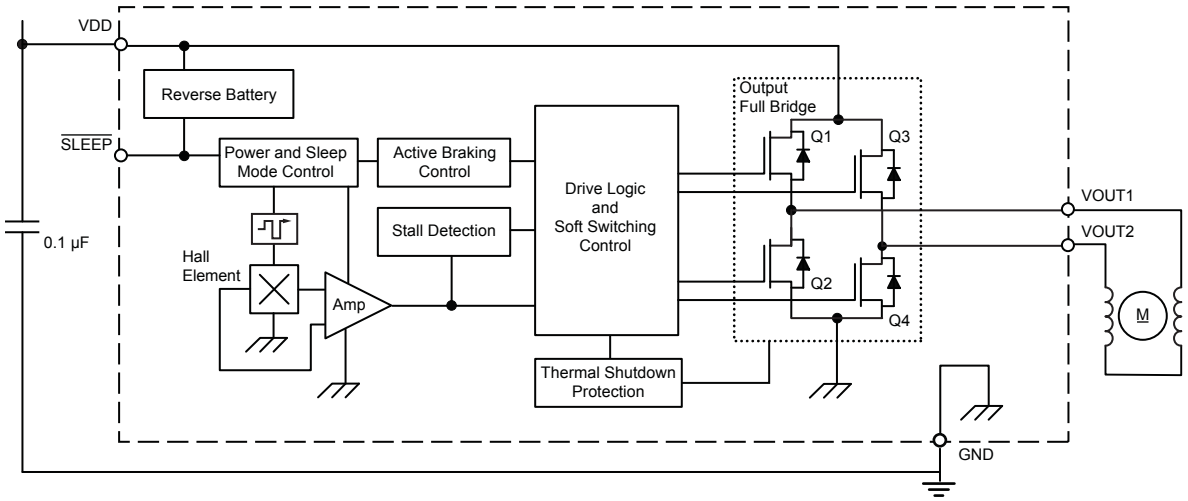
The A1442 is a full-bridge motor driver designed to drive low-voltage, brushless DC motors. Commutation of the motor is achieved by use of a single Hall element to detect the rotational position of an alternating-pole ring magnet. A high-density CMOS semiconductor process allows the integration of all the necessary electronics. This includes the Hall element, the motor control circuitry, and the full output bridge. Low-voltage design techniques have been employed to achieve full device functionality down to low V_{DD} values. This fully integrated single chip solution provides enhanced reliability (including reverse battery protection and output short circuit protection) and eliminates the need for any external support components.

The A1442 employs a soft-switching algorithm to reduce audible switching noise and EMI interference. A micropower sleep mode can be enabled by an external signal, to reduce current consumption for battery management in portable electronic devices. This feature allows the removal of a FET transistor for switching the device on and off.

The A1442 is optimized for vibration motor applications in cellular phones, pagers, electronic toothbrushes, hand-held video game controllers, and low power fan motors.

The small package outline and low profile make this device ideally suited for use in applications where printed circuit board area and component headroom are at a premium. It is available in a lead (Pb) free, 6 pin MLP/DFN microleadframe package, with an exposed pad for enhanced thermal dissipation.

Functional Block Diagram



Selection Guide

Part Number	Package[1]	Packing
A1442EEWLT-P[2]	MLP/DFN 1.5 mm × 2 mm, 0.4 mm maximum overall height	3000 pieces / 7 in. reel

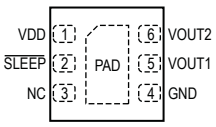
[1]Contact Allegro® for additional packing options.

[2]Allegro products sold in DFN package types are not intended for automotive applications.

Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{DD}		5.0	V
Reverse Supply Voltage	V_{RDD}		–5.0	V
Output Voltage	V_{OUT}	V_{DD} > 0 V	0 to V_{DD} + 0.3	V
Reverse Output Voltage	V_{ROUT}	V_{DD} > 0 V	–0.3	V
$\overline{\text{SLEEP}}$ Input Voltage	V_{IN}		0 to V_{DD} + 0.3	V
Peak Output Current	I_{OUTpk}	< 1 ms	±400	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
Junction Temperature	T_J(max)		165	°C
StorageTemperature	T_{stg}		–65 to 165	°C

Pin-out Diagram



Terminal List Table

Pin	Name	Function
1	VDD	Supply voltage
2	$\overline{\text{SLEEP}}$	Toggle sleep/enabled modes
3	NC	No connection
4	GND	Ground
5	VOUT1	First output
6	VOUT2	Second output

OPERATING CHARACTERISTICS valid over the full V_{DD} and T_A range unless otherwise noted

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage[1]	V_{DD}	Operating, $T_J < T_J(max)$; C_{BYP} = 0.1 µF	2.0	–	4.2	V
Supply Current	$I_{DD(ON)}$	$V_{IN} > V_{INHI,}$, T_A = 25°C, no load	–	4	6	mA
		$V_{IN} < V_{INLO}$, T_A = 25°C	–	–	10	µA
Total Output On Resistance[2,3]	$R_{DS(on)}$	V_{DD} = 2 V, I_{OUT} = 70 mA, T_A = 25°C	–	3.9	–	Ω
		V_{DD} = 3 V, I_{OUT} = 70 mA, T_A = 25°C	–	2.6	–	Ω
		V_{DD} = 4 V, I_{OUT} = 70 mA, T_A = 25°C	–	2.2	–	Ω
Reverse Battery Current	I_{RDD}	V_{RDD} = –4.2 V	–	–	–10	mA
Sleep Input Threshold	V_{INHI}		0.7×V_{DD}	–		V
	V_{INLO}		–	–	0.2×V_{DD}	V
Sleep Input Current	I_{IN}	V_{IN} = 3.0 V	–	1.0	5	µA
Reverse Sleep Current	I_{RIN}	V_{RIN} = –4.2 V	–	–	–10	mA
Restart Delay[4]	t_{RS}		–	120	–	ms
Hall Chopping Settling Time	$t_{S(CHOP)}$		–	80	–	µs
Magnetic Switchpoints[2]	B_{OP}		–	35	75	G
	B_{RP}		–75	-35	–	G
	B_{HYS}		–	70	–	G
Output Polarity	V_{OUT1}	$B < B_{RP}$	–	LOW	–	V
		$B > B_{OP}$	–	HIGH	–	V
	V_{OUT2}	$B < B_{RP}$	–	HIGH	–	V
		$B > B_{OP}$	–	LOW	–	V

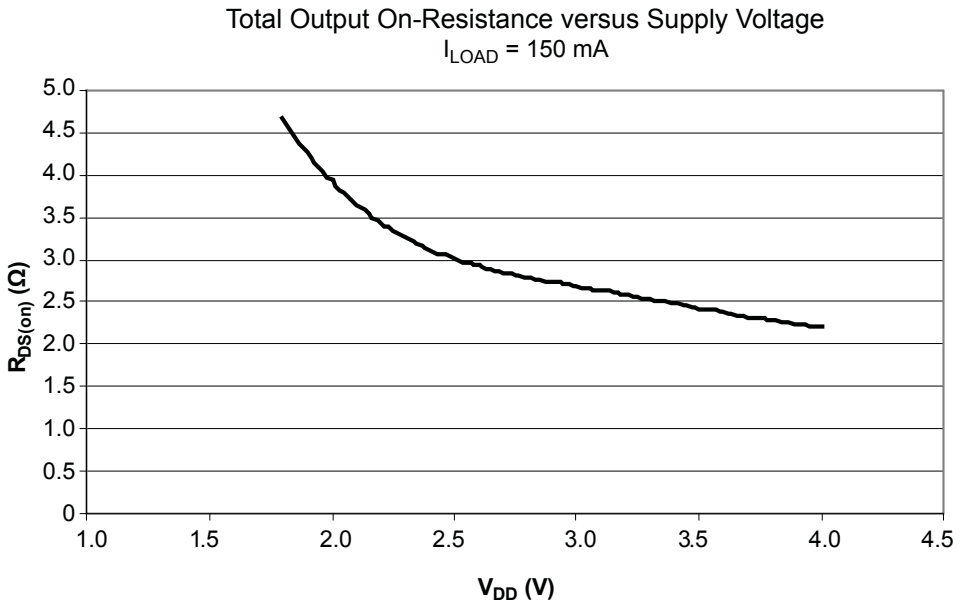
[1] A bypass capacitor of 0.1 µF is required between VDD and GND for proper device operation through the full specified voltage range.

[2] Extended V_{DD} range affects $R_{DS(on)}$ and B_x.

[3] Total On Resistance equals either $R_{DS(on)}Q1 + R_{DS(on)}Q4$ or $R_{DS(on)}Q2 + R_{DS(on)}Q3$.

[4] The Restart Delay is the time the outputs are on or off when the device is attempting a restart.

Characteristic Performance



Functional Description

Soft Switching The A1442 device includes a soft-switching algorithm that controls the output switching slew rate for both output pins. As a result the A1442 device is ideal for use in applications requiring low audible switching noise and low EMI interference.

Sleep Mode The $\overline{\text{SLEEP}}$ pin accepts an external signal that enables sleep mode. In sleep mode, the current consumption is reduced to an extremely low level, conserving battery power in portable electronics.

Antistall Algorithm If a stall condition occurs, the device will execute an antistall algorithm.

Device Start-up The start-up behavior of the device output is determined by the applied magnetic field, as specified in the Operating Characteristics table.

Application Information

Two typical application circuits are shown in figures 4 and 5. The first application circuit shows the device $\overline{\text{SLEEP}}$ pin controlled by the user. Figure 5 illustrates an application circuit where the device VDD and $\overline{\text{SLEEP}}$ pin are connected together.

Note that:

- No external diode is required for reverse battery protection because the protection is fully integrated into the IC.
- Thermal shutdown is integrated also.

A bypass capacitor of 0.1 µF is required between VDD and GND for proper device operation through the full specified supply voltage range.

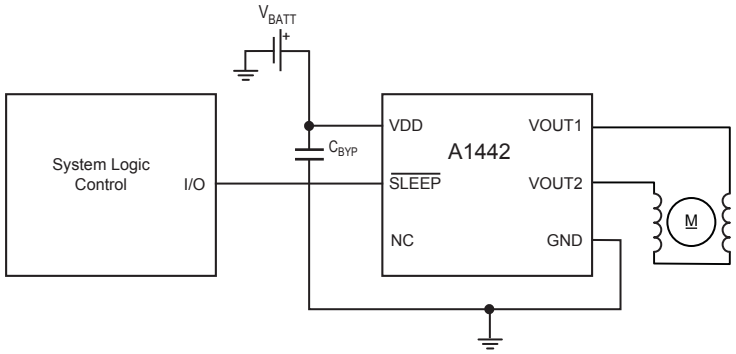


Figure 4. Application circuit showing user-controlled sleep/enable mode, while the A1442 remains powered at all times

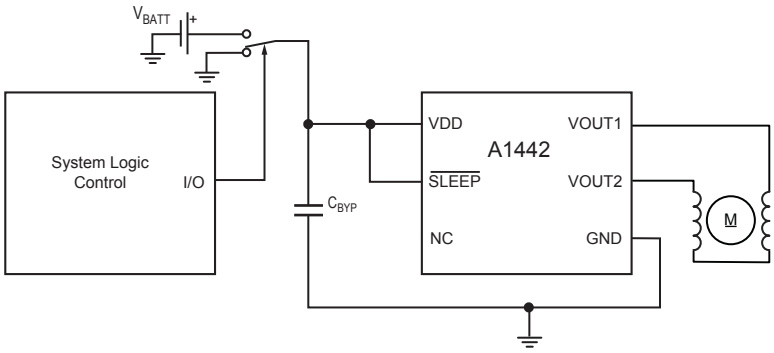


Figure 4. Application circuit showing simultaneous user control of power supply and sleep mode.

Power Derating

The device must be operated below the maximum junction temperature of the device, T_J(max). Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems Web site.) The package thermal resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the effective thermal conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, $_{TA}$, and air motion are significant external factors, damped by overmolding. The effect of varying power levels (power dissipation, P_D) can be estimated. The following formulas represent the fundamental relationships used to estimate T_J at given levels of P_D.

Given:

$$P_D = V_{IN} \times I_{IN} , \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \text{ , and} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For a load of 30 Ω, given common conditions such as: T_A= 25°C, V_{DD} = 3 V, I_{DD} = 83 mA, V_L = 2.43 V, I_L = 81 mA and $R_{\theta JA}$ = 250 °C/W, then:

$$P_D = V_{DD} \times I_{DD} - V_L I_L$$

$$= 3 \text{ V} \times 83 \text{ mA} - 2.43 \text{ V} \times 81 \text{ mA} = 52.17 \text{ mW} ,$$

$$\Delta T = P_D \times R_{\theta JA}$$

$$= 52.17 \text{ mW} \times 250 \text{ °C/W} = 13\text{°C} \text{ , and}$$

$$T_J = T_A + \Delta T = 25\text{°C} + 13\text{°C} = 38\text{°C}$$

A worst-case estimate, P_D(max), represents the maximum allowable power level, without exceeding T_J(max), at a selected $R_{\theta JA}$ and T_A.

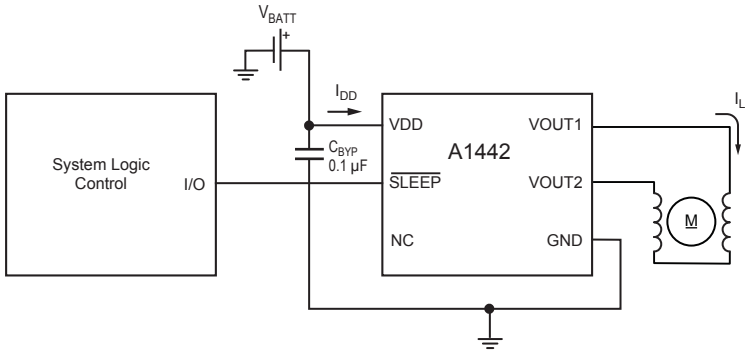
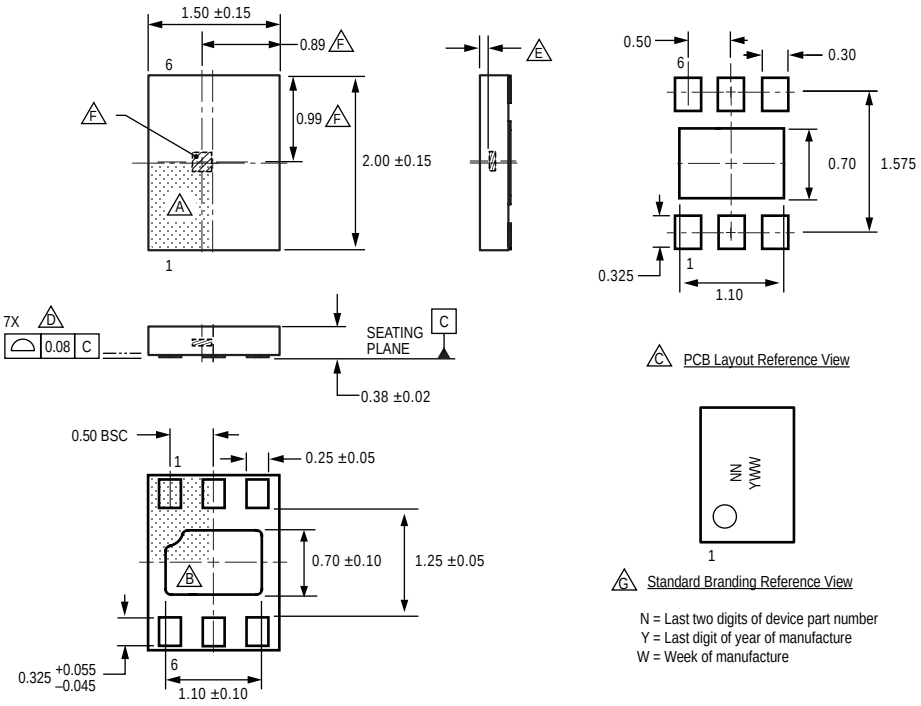


Figure 4. Typical application showing current paths

Package EW, 6 pin MLP/DFN



C PCB Layout Reference View

G Standard Branding Reference View

N = Last two digits of device part number
Y = Last digit of year of manufacture
W = Week of manufacture

For Reference Only, not for tooling use (refernce DWG-2856; similar to JEDEC Type 1, MO-229X2BCD)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P200X200X100-9M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Active Area Depth 0.15 mm REF

F Hall Element (not to scale)

G Branding scale and appearance at supplier discretion

Revision History

Revision	Revision Date	Description of Revision
Rev. 2	October 26, 2011	Update Selection Guide

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