PCN Number:	20140818000A	PCN Date:	08/29/2014
Title:	Updates to datasheet for improvement and correction and adding new device LMK04821		
Customer Contact:	PCN Manager	Phone: +1(214) 480-6037	Dept: Quality Services

Change Type:

☐	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☒	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

PCN Details

Description of Change:

The purpose of this A version is to add the LMK04821NKDT and LMK04821NKDR as PCN affected devices

Texas Instruments Incorporated is announcing an information only notification.
The product datasheet(s) is being updated as summarized in the following revision history:

Revision History

Changes from Revision AP (June 2013) to Revision AQ **Page**

• Changed data sheet flow and layout to conform with new TI standards. Added, updated, or renamed the following sections: Device Information Table, Application and Implementation; Power Supply Recommendations; Layout; Device and Documentation Support; Mechanical, Packaging, and Ordering Information 1
• Added values for LMK04821 under "Features" section. 1
• Changed LMK04820 family to LMK0482x family 1
• Added values for LMK04821 under "Device Configuration Information" section 5
• Added "holdover DAC" in Description for Pin Number 36. 7
• Changed thermal table header from LMK0482xB to LMK0482x 9
• Changed "CLKinX_BUF_TYPE" to "CLKinX_TYPE" 10
• Added values for LMK04821 under "Internal VCO Specifications" 13
• Added values for LMK04821 under "Noise Floor" 14
• Added values for LMK04821 under "CLKout Closed Loop Phase Noise Specifications a Commercial Quality VCXO".. 15
• Added 245.76 MHz as frequency for LMK04826B phase noise data $L(f)_{CLKout}$ for VCO0 16
• Added 245.76 MHz as frequency for LMK04826B phase noise data $L(f)_{CLKout}$ for VCO1 16
• Added 245.76 MHz as frequency for LMK04828B phase noise data $L(f)_{CLKout}$ for VCO0 16
• Added 245.76 MHz as frequency for LMK04828B phase noise data $L(f)_{CLKout}$ for VCO1 16
• Added values for LMK04821 under "CLKout Closed Loop Jitter Specifications a Commercial Quality VCXO" 17
• Added SDCLKoutY_HS = 0 for $ts_{JESD204B}$ in Electrical Characteristics 20
• Added "Propagation Delay from CLKin0 to SDCLKoutY" in Electrical Characteristics 20
• Added footnote that LMK04821 has no DCLKoutX or SDCLKoutY outputs on at power up, only OSCout. 20
• Changed V_{OH} TEST CONDITIONS to "= 3 or 4" and V_{OL} TEST CONDITIONS to "3, 4, or 6" under DIGITAL OUTPUTS (CLKin_SELX, Status_LDX, and RESET/GPO) subheading in Electrical Characteristics..... 23
• Changed Digital Inputs (SCK, SDIO, CS*) I_{IH} V_{IH} = VCC min line from 5 µA to -5 µA 23
• Added "4 wire mode read back has same timing as SDIO pin", "R/W bit = 0 is for SPI write", "R/W bit = 1 is for SPI read", "W1 and W0 shall be written as 0."..... 24
• Added LMK04821 phase noise graphs under "Clock Output AC Characteristics"..... 25
• Added link to AN-912 Application Report 29
• Changed from "Glitchless Half Shift" to "Glitchless Half Step"..... 32
• Changed block from SDCLKoutY_POL to DCLKoutX_POL in Figure 10 34
• Added SYSREF_CLKin0_MUX block to Figure 11 image. 35
• Changed Figure 11 to show that FB_MUX SYSREF input comes from SYSREF Divider, not SYSREF_MUX. 35
• Changed term pulsor to pulser throughout 36
• Changed DCLKout0_1_DIV to DCLKout0_DIV; DCLKout2_3_DIV to DCLKout2_DIV; DCLKout4_5_DIV to DCLKout4_DIV 37
• Added DCLKout4_DIV = 20 37

- Added DCLKout0_DDLY_PD = 0, DCLKout2_DDLY_PD = 0, DCLKout4_DDLY_PD = 0 37
- Changed text to read, "Set device clock and SYSREF divider digital delays: DCLKout0_DDLY_CNTH, DCLKout0_DDLY_CNTL, DCLKout2_DDLY_CNTH, DCLKout2_DDLY_CNTL, DCLKout4_DDLY_*CNTH,* DCLKout4_DDLY_CNTL, SYSREF_DDLY." 37
- Added "= 1" in SYSREF Request section 38
- Changed step numbers in dynamic delay and references to steps to be correct, step 8 was duplicated 41
- Added note "LMK04821 includes VCO1 divider on VCO1 output." 46
- Added note "LMK04821 includes VCO1 divider on VCO1 output." 47
- Added LMK04821 detailed block diagram 49
- Added "R/W bit = 0 is for SPI write. R/W bit = 1 is for SPI read." 51
- Added "If using LMK04821, program register 0x174" in Recommended Programming Sequence section 51
- Added SYSREF_CLKin0_MUX and VCO1_DIV to register map 53
- Added CLKin_OVERRIDE bit to register map 54
- Changed from "half shift" to "half step" 59
- Changed definition of SDCLKoutY_DDLY value of 0 from "Reserved" to "Bypass" 59
- Changed from "Sets the polarity of SYSREF clocks" to "Sets the polarity of clock on SDCLKoutY when device clock output is selected with SDCLKoutY_MUX" 62
- Changed "Sets the polarity of the device clocks" to "Sets the polarity of the device clocks from the DCLKoutX outputs" 62
- Added LMK04821 DCLKoutX_FMT power on reset values as powerdown 62
- Changed from "SYSREF" to "SYSREF Divider" in "Source" column of Register 0x13F table. 66
- Changed reserved to Off for CLKout1_OUT_MUX. 71
- Changed reserved to Off for CLKout0_OUT_MUX. 71
- Added CLKin_OVERRIDE bit 78
- Added LMK04821 register 0x174 for VCO1_DIV 93
- Deleted (LMK04828 from Core line 103
- Added VCO1 Icc including VCO1 Divider for LMK04821 103
- Changed VCO1 Icc and power dissipated for LMK04828B/26B from 6 mA to 13.5 mA and 19.8 mW to 44.55 mW 103

The datasheet number will be changing.

Device Family	Change From:	Change To:
LMK0482	SNAS605AP	**SNAS605AQ**

These changes may be reviewed at the datasheet links provided.

http://www.ti.com/product/lmk04821?keyMatch=LMK04821&tisearch=Search-EN

Reason for Change:
Adding new device in family, typo in electrical characteristics, exposing extra bits for improved performance, correction of information.
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):
Electrical specification performance changes as indicated above.
Changes to product identification resulting from this PCN:
None.
Product Affected:

LMK04826BEVM	LMK04826BISQX/NOPB	LMK04828BISQE/NOPB
LMK04826BISQ/NOPB	LMK04828BISQ/NOPB	LMK04828BISQX/NOPB
LMK04826BISQE/NOPB	LMK04821NKDR	LMK04821NKDT

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