



SST25VF064C to SST26VF064B/064BA Migration

1.0 INTRODUCTION

The Serial Quad I/O™ (SQI™) family of flash-memory devices features a six-wire, 4-bit I/O interface that allows for low-power, high-performance operation in a low pin-count package. SST26VF064B/064BA also supports full command-set compatibility to traditional Serial Peripheral Interface (SPI) protocol.

This document lists all the firmware and hardware changes required to migrate from SST25VF064C to SST26VF064B/064BA. Refer to the SST26VF064B/064BA data sheet (DS20005119) for more information.

TABLE 1-1: SUMMARY OF CHANGES REQUIRED FOR ALL PART NUMBERS AND PACKAGES

Current Part	Recommended Upgrade	Board Layout/ Footprint Change	Firmware Change
SST25VF064C-80-4I-SCE (16-lead SOIC)	SST26VF064B-104I/SO (16-lead SOIC)	No	Yes
SST25VF064C-80-4I-S3AE (8-lead SOIC)	SST26VF064B-104I/SM (8-lead SOIC)	No	Yes
SST25VF064C-80-4I-Q2AE (WSON)	SST26VF064B-104I/MN (WDFN) ¹	No	Yes
Any SST25VF064C	SST26VF064B-104I/TD (TBGA) ²	Yes	Yes

1. WSON and WDFN are different designators for the same package
2. TBGA is a new package available for SST26VF064B/064BA

**TABLE 1-2: PIN LAYOUT COMPARISON,
16-LEAD SOIC**

Pin No.	SST25VF064C	SST26VF064B/ 064BA
1	RST#/HOLD# ¹	HOLD#/SOI3
2	VDD	VDD
3	NC	NC
4	NC	NC
5	NC	NC
6	NC	NC
7	CE#	CE#
8	SO/SIO1	SO/SIO1
9	WP#	WP#/SIO2
10	VSS	VSS
11	NC	NC
12	NC	NC
13	NC	NC
14	NC	NC
15	SI/SIO0	SI/SIO0
16	SCK	SCK

1. For SST25VF064C, Pin 1 is RST# pin at power-up. For SST26VF064B/064BA, Pin 1 is HOLD# pin at power-up.

**TABLE 1-3: PIN LAYOUT COMPARISON,
8-LEAD SOIC**

Pin No.	SST25VF064C	SST26VF064B/ 064BA
1	CE#	CE#
2	SO/SIO1	SO/SIO1
3	WP#	WP#/SIO2
4	VSS	VSS
5	SI/SIO0	SI/SIO0
6	SCK	SCK
7	RST#/HOLD# ¹	HOLD#/SOI3
8	VDD	VDD

1. For SST25VF064C, Pin 7 is RST# pin at power-up. For SST26VF064B/064BA, Pin 7 is HOLD# pin at power-up.

SST25VF064C TO SST26VF064B/064BA

2.0 MIGRATION CONSIDERATIONS

The following topics should be considered when migrating from SST25VF064C to SST26VF064B/064BA.

2.1 Reset Pin Function at Power-Up

SST25VF064C powers up with the Reset-pin function enabled. Reset-pin function is not supported by SST26VF064B/064BA. SST26VF064B/064BA executes a Reset by software reset using Reset Enable (66H) or Reset memory (99H) software instruction commands.

2.2 Status and Configuration Register

The status register of the SST25VF064C differs from the Status register of SST26VF064B/064BA. [Table 2-1](#) shows the Status register of SST25VF064C and [Table 2-2](#) shows the Status register of SST26VF064B/064BA. SST26VF064B/064BA also has an additional Configuration register used to configure device operations and setup defaults on I/O configuration and Block Protection state, see [Table 2-3](#).

TABLE 2-1: STATUS REGISTER SST25VF064C

Bit	Name	Function	Default at Power-up	Read/Write
0	BUSY	1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	1 = Device is memory Write enabled 0 = Device is not memory Write enabled	0	R
2	BP0	Indicate current level of block write protection	1	R/W
3	BP1	Indicate current level of block write protection	1	R/W
4	BP2	Indicate current level of block write protection	1	R/W
5	BP3	Indicate current level of block write protection	1	R/W
6	SEC ¹	Security ID status 1 = Security ID space locked 0 = Security ID space not locked	01	R
7	BPL	1 = BP3, BP2, BP1, BP0 are read-only bits 0 = BP3, BP2, BP1, BP0 are readable/writable	0	R/W

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1. The Security ID status will always be '1' at power-up after a successful execution of the Lockout SID instruction; otherwise, the default at power up is '0'.

TABLE 2-2: STATUS REGISTER SST26VF064B/064BA

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
0	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R
1	WEL	Write-Enable Latch status 1 = Device is write-enabled 0 = Device is not write-enabled	0	R
2	WSE	Write Suspend-Erase status 1 = Erase suspended 0 = Erase is not suspended	0	R
3	WSP	Write Suspend-Program status 1 = Program suspended 0 = Program is not suspended	0	R
4	WPLD	Write Protection Lock-Down status 1 = Write Protection Lock-Down enabled 0 = Write Protection Lock-Down disabled	0	R
5	SEC ¹	Security ID status 1 = Security ID space locked 0 = Security ID space not locked	0 ¹	R

SST25VF064C TO SST26VF064B/064BA

TABLE 2-2: STATUS REGISTER SST26VF064B/064BA (CONTINUED)

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
6	RES	Reserved for future use	0	R
7	BUSY	Write operation status 1 = Internal Write operation is in progress 0 = No internal Write operation is in progress	0	R

1. The Security ID status will always be '1' at power-up after a successful execution of the Lockout Security ID instruction, otherwise default at power-up is '0'.

TABLE 2-3: CONFIGURATION REGISTER SST26VF064B/064BA

Bit	Name	Function	Default at Power-up	Read/Write (R/W)
0	RES	Reserved	0	R
1	IOC	I/O Configuration for SPI Mode 1 = WP# and HOLD# pins disabled 0 = WP# and HOLD# pins enabled	0 ¹	R/W
2	RES	Reserved	0	R
3	BPNV	Block-Protection Volatility State 1 = No memory block has been permanently locked 0 = Any block has been permanently locked	1	R
4	RES	Reserved	0	R
5	RES	Reserved	0	R
6	RES	Reserved	0	R
7	WPEN	Write-Protection Pin (WP#) Enable 1 = WP# enabled 0 = WP# disabled	0 ²	R/W

1. SST26VF064B default at Power-up is '0'
SST26VF064BA default at Power-up is '1'

2. Factory default setting. This is a non-volatile bit; default at power-up will be the setting prior to power-down.

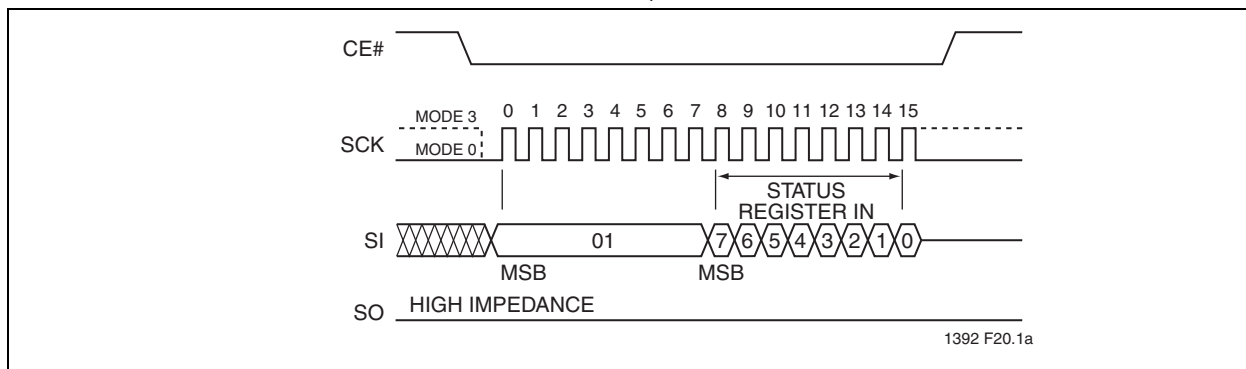
The Read-Status-Register (RDSR) instructions allows the device to read the Status register for SST25VF064C or SST26VF064B/064BA. The Read-Configuration-Register (RDCR) enables the device to read the Configuration register for SST26VF064B/064BA.

The Write-Status-Register (WRSR) instruction writes to the Status and Configuration registers. Write-Enable (WREN) instruction must be issued prior to WRSR instruction. The WRSR sequence that allows the device

to write to the Status register of SST25VF064C is shown in [Figure 2-1](#). The WRSR sequence that allows the device to write to the Status and Configuration registers of SST26VF064B/064BA is shown in [Figure 2-2](#).

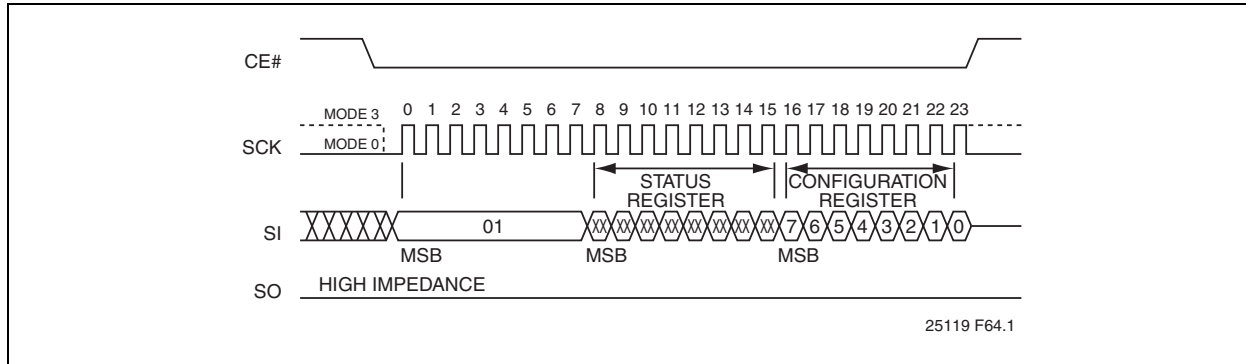
The default I/O state factory settings are the same between SST25VF064C and SST26VF064B. The SST26VF064BA factory default setting for I/O WP# and HOLD# are disabled and different from the SST25VF064C.

FIGURE 2-1: WRITE-STATUS-REGISTER SEQUENCE SST25VF064C



SST25VF064C TO SST26VF064B/064BA

FIGURE 2-2: WRITE-STATUS-REGISTER SEQUENCE SST26VF064B/064BA



2.3 Device Protection

SST26VF064B/064BA employs a new protection scheme that allows for more flexibility and a higher level of protection in comparison to the SST25VF064C. SST25VF064C offers traditional memory protection via block protection bits in the Status Register, whereas SST26VF064B/064BA supports individual block protection via Block Protection Register instructions.

Both SST25VF064C and SST26VF064B/064BA power up with memory protected. To execute Program or Erase commands, remove the protection.

To remove the memory protection of SST25VF064C, clear the protection bits in the status register. The status register contains protection bits BP0, BP1, BP2, and BP3, all of which are set to 0 to clear all protection.

SST26VF064B/064BA supports the Global Block-protection Unlock command (98H) to unlock the entire memory. Table 2-4 lists all block protection commands for SST26VF064B/064BA.

TABLE 2-4: BLOCK PROTECTION COMMANDS SST26VF064B/064BA

Instruction	OpCode
Read Block Protection Register	72H
Write Block Protection Register	42H
Lock Down Block Protection Register	8DH
non-Volatile Write Lock-Down Register	E8H
Global Block Protection Unlock	98H

2.4 Device ID

SST25VF064C and SST26VF064B/064BA use different device IDs. The device ID of SST25VF064C is BF254BH. BFH is manufacturer ID, 25H is memory type and 4BH is device ID. The device ID of SST26VF064B/064BA is BF2643H. BFH is manufacturer ID, 26H is memory type and 43H is device ID.

The device IDs for both devices are accessed with the same operation command and protocol, but the return data will be different for each device. See Table 2-5 for more information about the operation commands.

SST26VF064B/064BA supports JEDEC's Serial Flash Discoverable Parameters (SFDP) v1.1 as an additional method of device identification.

2.5 Communication Protocol

SST25VF064C only utilizes SPI protocol, but SST26VF064B/064BA can use either SPI and SQI protocol. SST26VF064B/064BA will work with a host controller that only supports SPI. If the host controller supports both SPI and SQI, then all the features of SST26VF064B/064BA are available.

SST25VF064C supports a clock frequency up to 80MHz and SST26VF064B/064BA supports a clock frequency up to 104MHz.

SST25VF064C TO SST26VF064B/064BA

2.6 Host Controller Supports SPI

Most operation commands of SST25VF064C are compatible with SST26VF064B with minimal changes required. See [Table 2-5](#).

TABLE 2-5: OPERATION COMMAND COMPATIBILITY

SST25VF064C Device Operation Instructions	OpCode	Compatible with SST26VF064B/064BA	Comments
Read	03H	Yes	
Fast-Read Dual I/O	BBH	Yes	
Fast-Read Dual Output	3BH	Yes	
High-Speed Read	0BH	Yes	
Sector-Erase	20H	Yes	
32KByte Block Erase	52H	Change Required	This command is not supported in the SST26VF064B/064BA. For 32 KByte Block Erase, use D8H.
64KByte Block Erase	D8H	Change Required	The memory maps of SST25VF064C and SST26VF064B/064BA are different. Refer to data sheet.
Chip-Erase	60H or C7H	Change Required	SST26VF064B/064BA supports C7H but not 60H instruction
Page-Program	02H	Yes	
Dual-Input Page Program	A2H	No	Not supported by SST26VF064B/064BA
RDSR	05H	Yes	With the exception of bit 0 (BUSY) and bit 1 (WEL), all other bits in the Status register are different between the two devices. Status register on SST26VF064B/064BA is read-only.
EWSR	50H	No	Not supported by SST26VF064B
WRSR	01H	Change Required	The two parts use different block protection schemes and the block protection bits in the Status Register are removed from SST26VF064B/064BA. WRSR instructions for SST26VF064B/064BA ignore Write to the 1st data byte to the Status Register, and only accept Write to the 2nd data byte for the Configuration Register.
WREN	06H	Yes	
WRDI	04H	Yes	
RDID	90H or ABH	No	Not supported by SST26VF064B/064BA
JEDEC-ID	9FH	Yes	Device Id is different between two parts.
EHLID	AAH	No	Not supported by SST26VF064B/064BA
Read SID	88H	No	SST26VF064B Read SID and Program SID have 2 bytes for address cycles. The security memory space increases from 256 Bytes on SST25VF064C to 2048 Bytes on SST26VF064B/064BA.
Program SID	A5H	No	
Lockout SID	85H	Yes	

SST25VF064C TO SST26VF064B/064BA

2.7 Host Controller Supports Both SPI and SQI

If the host controller can support both SPI and SQI protocol than the above changes described are still relevant and in addition all features of SST26VF064B/064BA are now available for use. A review of the current methods/code to perform read and program must be done and the firmware should be upgraded to take advantage of all the features available as described in the data sheet.

SST26VF064B/064BA supports higher functionality and performance such as:

- up to 104 MHz operating frequency
- multi-I/O read/program capability
- enhanced security and OTP security memory area outside of the main memory array
- JEDEC Serial Flash Discoverable Parameters (SFDP)
- Suspend Program/Erase capability.

Refer to the SST26VF064B/064BA data sheet for detailed instructions.

2.8 Conclusion

This document describes the aspects to consider when migrating from SST25VF064C to SST26VF064B/064BA. SST26VF064B/064BA is a great choice because it supports higher clock frequency, uses both SPI and SQI protocol, and continues to provide the superior reliability represented by SuperFlash® technology.

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ISBN: 978-1-5224-2456-7



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