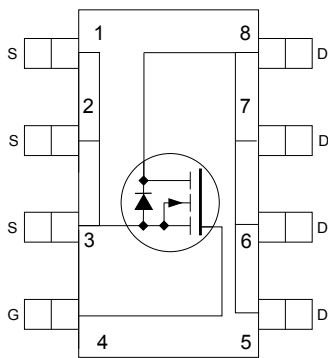
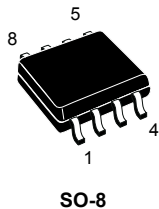


N-channel 20 V, 30 mΩ typ., 6 A, 2.7 V drive, STripFET II Power MOSFET in an SO-8 package



SC12830N

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STS6NF20V	20 V	40 mΩ (@4.5 V)	6 A
		45 mΩ (@2.7 V)	

- Ultra low threshold gate drive
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status link

[STS6NF20V](#)

Product summary

Order code	STS6NF20V
Marking	6F20V-
Package	SO-8
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate-source voltage	±12	V
I_D	Drain current (continuous) at $T_{amb} = 25\text{ °C}$	6	A
	Drain current (continuous) at $T_{amb} = 100\text{ °C}$	3.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	24	A
P_{TOT}	Total power dissipation at $T_{amb} = 25\text{ °C}$	2.5	W
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		°C

1. Pulse width limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance junction-ambient	50	°C/W

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified

Table 3. On-/off-states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	20			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$ $T_C = 125\text{ }^\circ\text{C}$ (1)			10	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DD} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	0.6			V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 4.5\text{ V}, I_D = 3\text{ A}$		30	40	m Ω
		$V_{GS} = 2.7\text{ V}, I_D = 3\text{ A}$		37	45	
		$V_{GS} = 1.95\text{ V}, I_D = 0.9\text{ A}$			90	

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance		6.5	10	15	S
C_{iss}	Input capacitance	$V_{DS} = 15\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0\text{ V}$	320	460	640	pF
C_{oss}	Output capacitance		130	200	280	pF
C_{rss}	Reverse transfer capacitance		33	50	68	pF
Q_g	Total gate charge	$V_{DD} = 16\text{ V}, I_D = 6\text{ A}$	5.5	8.5	11.5	nC
Q_{gs}	Gate-source charge	$V_{GS} = 0\text{ to }4.5\text{ V}$	1.2	1.8	2.5	nC
Q_{gd}	Gate-drain charge	(see Figure 12. Test circuit for gate charge behavior)	1.6	2.4	3.4	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10\text{ V}, I_D = 3\text{ A},$	-	7	20	ns
t_r	Rise time	$R_G = 4.7\text{ }\Omega, V_{GS} = 4.5\text{ V}$	-	33	45	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 11. Test circuit for resistive load switching times and Figure 16. Switching time waveform)	-	27	40	ns
t_f	Fall time		-	10	20	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		24	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 10\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 16. Switching time waveform)	-	26		ns
Q_{rr}	Reverse recovery charge		-	13		nC
I_{RRM}	Reverse recovery current		-	1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

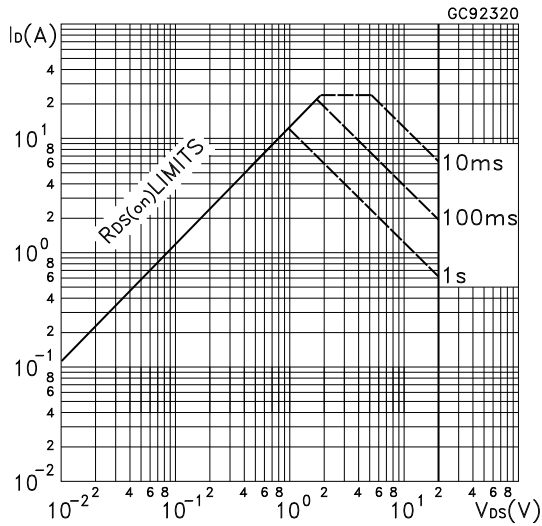


Figure 2. Thermal impedance

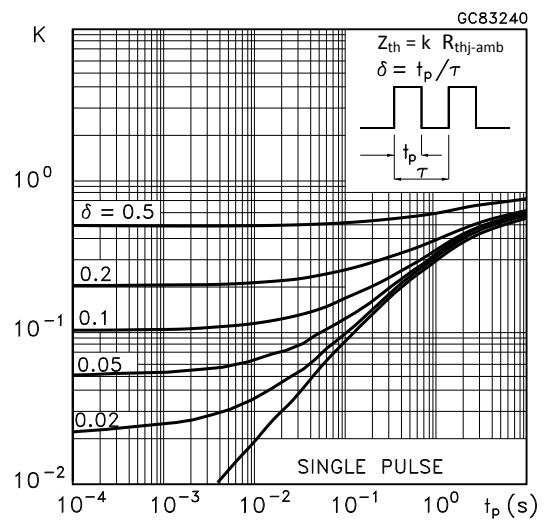


Figure 3. Output characteristics

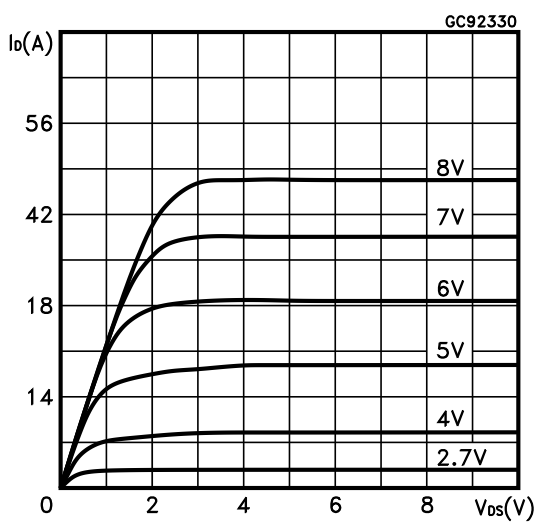


Figure 4. Transfer characteristics

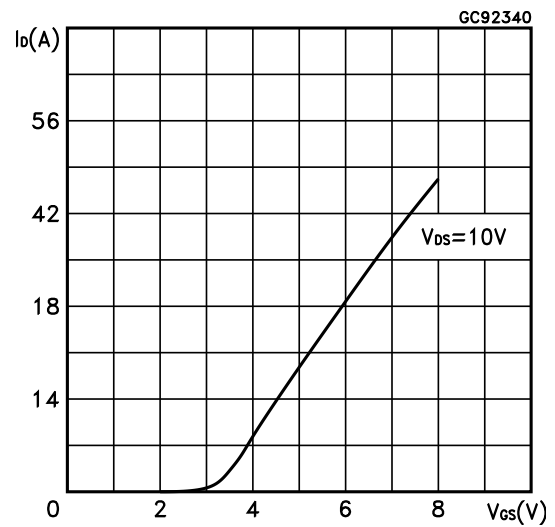


Figure 5. Source-drain diode forward characteristics

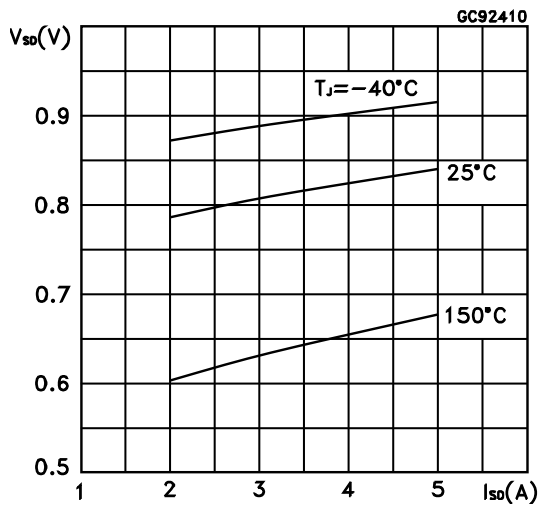


Figure 6. Static drain-source on-resistance

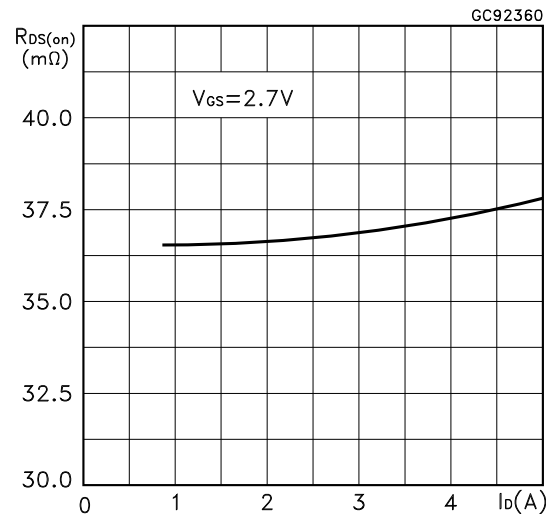


Figure 7. Gate charge vs gate-source voltage

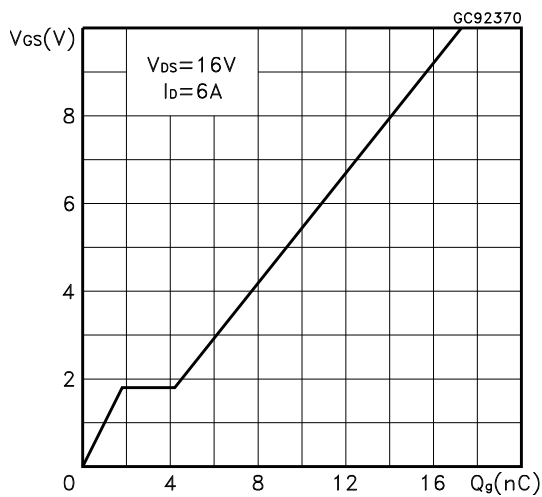


Figure 8. Capacitance variations

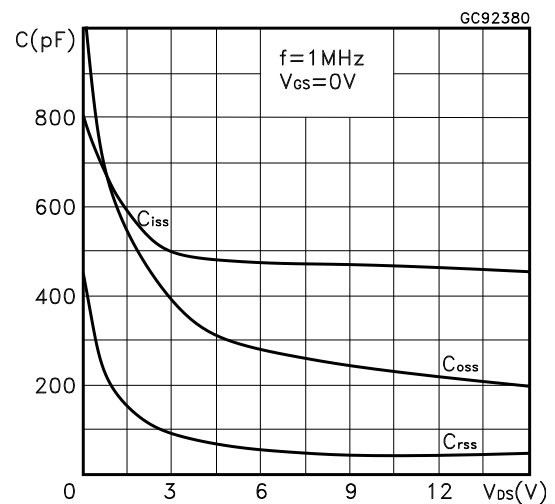


Figure 9. Normalized gate threshold voltage vs temperature

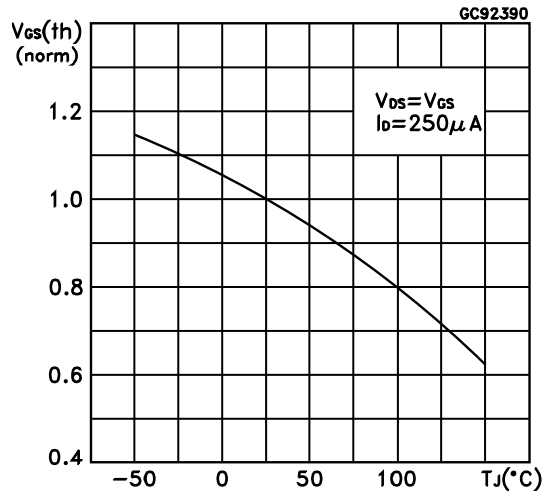
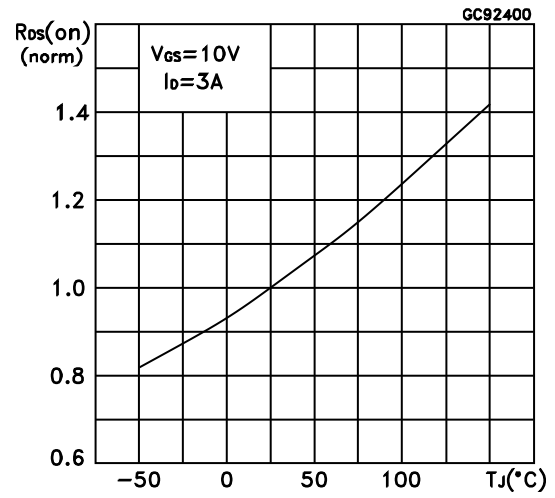
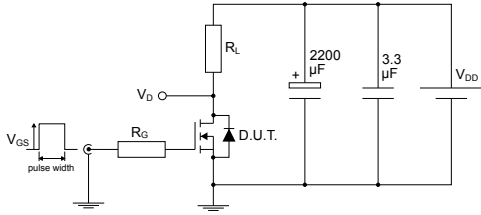


Figure 10. Normalized on-resistance vs temperature



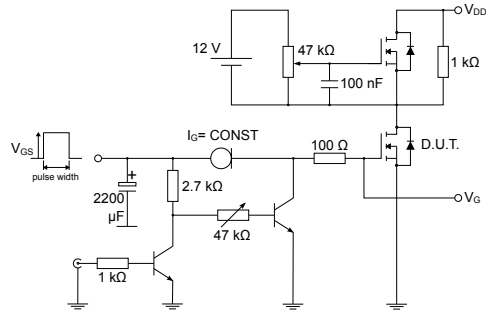
3 Test circuits

Figure 11. Test circuit for resistive load switching times



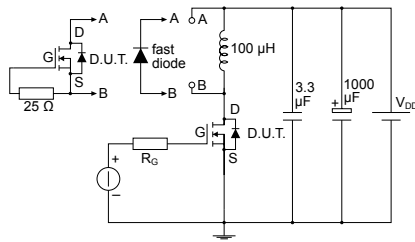
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Figure 12. Test circuit for gate charge behavior



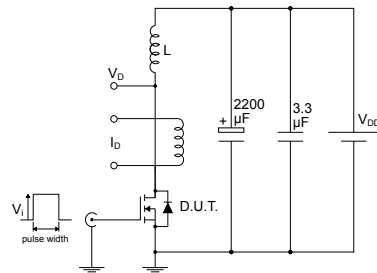
AM01469v1

Figure 13. Test circuit for inductive load switching and diode recovery times



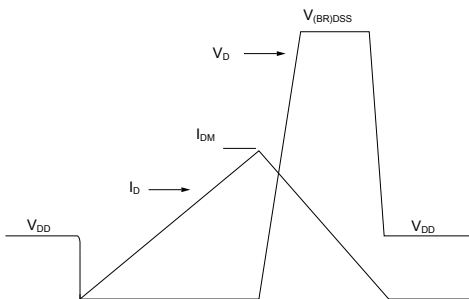
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Figure 14. Unclamped inductive load test circuit



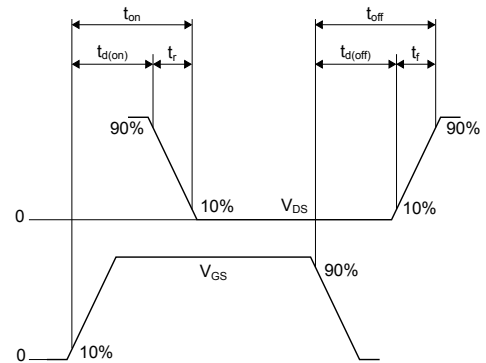
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Figure 15. Unclamped inductive waveform



AM01472v1

Figure 16. Switching time waveform



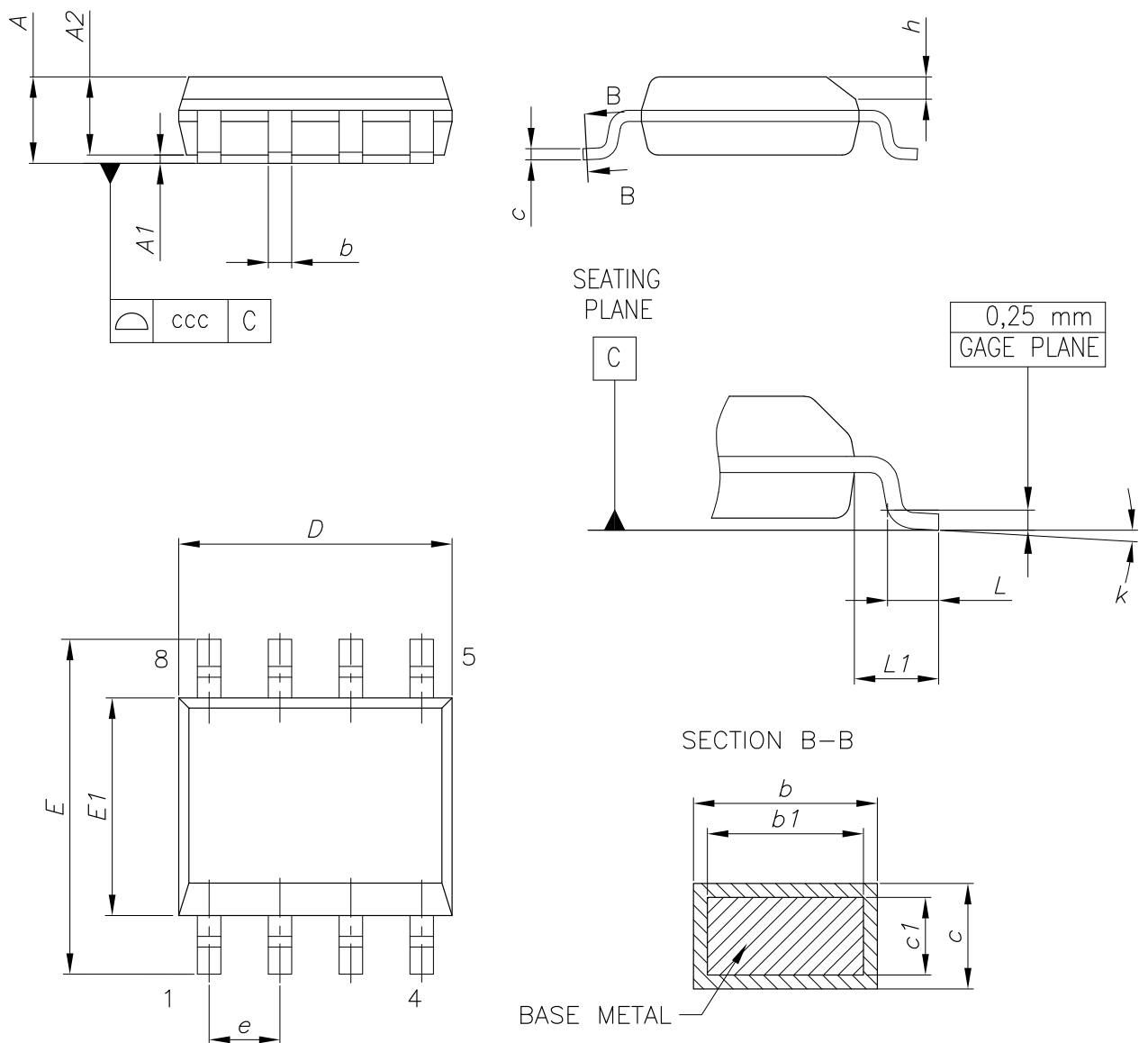
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 SO-8 package information

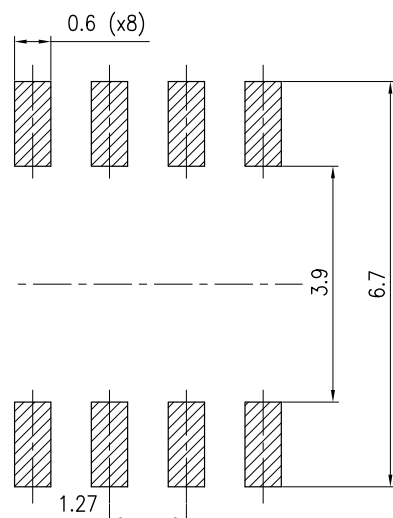
Figure 17. SO-8 package outline



0016023_So-807_fig2_Rev10

Table 7. SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 18. SO-8 recommended footprint (dimensions are in mm)


0016023_So-807_footprint_Rev10

4.2 SO-8 packing information

Figure 19. SO-8 tape and reel dimensions

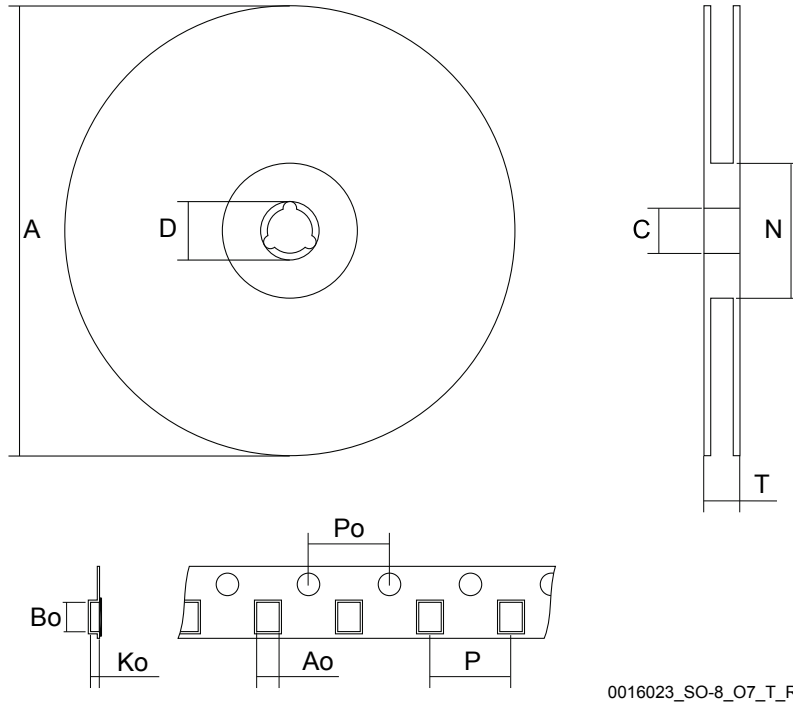


Figure 20. Tape orientation

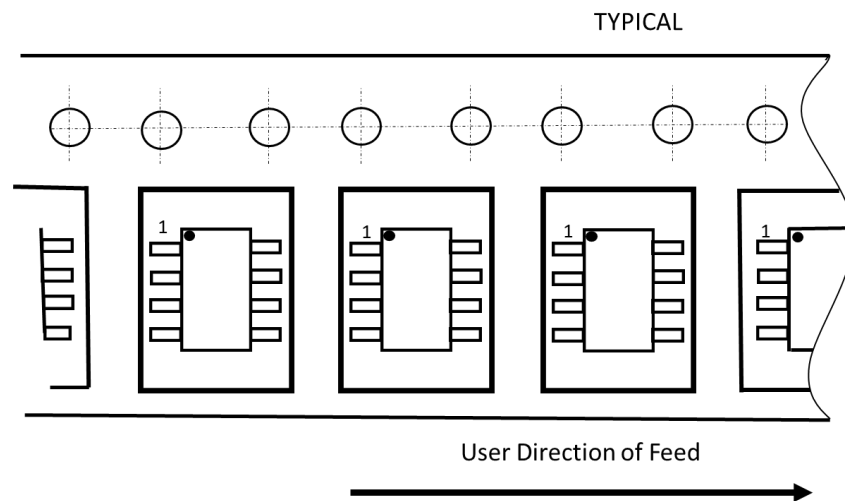


Table 8. SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	6.5	-	6.7
Bo	5.4		5.6
Ko	2.0		2.2
Po	3.9		4.1
P	7.9		8.1

Revision history

Table 9. Document revision history

Date	Version	Changes
07-Feb-2008	1	Initial release.
18-Nov-2009	2	Added new RDS(on) value on <i>Table 4: On /off states</i>
29-Nov-2012	3	Max values have been added in <i>Table 5: Dynamic</i> and <i>Table 6: Switching times</i> . <i>Section 4: Package mechanical data</i> has been updated. Minor text changes.
04-Apr-2018	4	Removed maturity status indication from cover page. The document status is production data. Updated product marking on cover page. Updated <i>Table 3. On-/off-states</i> . Updated <i>Section 4 Package information</i> . Minor text changes
05-Nov-2020	5	Updated Section 4.2 SO-8 packing information . Minor text changes.

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