

74AHC1G4208-Q100

8-stage divider and oscillator

Rev. 1 — 3 September 2019

Product data sheet

1. General description

74AHC1G4208-Q100 is a 8-stage divider and oscillator. It consists of a chain of 8 flip-flops. Each flip-flop divides the frequency of the previous flip-flop by two, consequently the 74AHC1G4208-Q100 counts up to $2^8 = 256$. The single inverting stage (X1 to X2) functions as a crystal oscillator or an input buffer for an external oscillator. When used as a buffer the output X2 should be left floating. The frequency of the output (Q) is the frequency applied to X1 divided by 256. The divider advances on the negative-going transition of X1.

The X1 input is overvoltage tolerant. This feature allows the use of this device as a voltage level translator in mixed voltage environments.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- ESD protection:
 - HBM: ANSI/ESDA/Jedec JS-001 exceeds 2000 V
 - CDM: ANSI/ESDA/Jedec JS-002 exceeds 1000 V
 - MIL-STD-883, method 3015 exceeds 2000 V
- Latch-up performance exceeds 100 mA per JESD 78 Class II

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|--------------------|-------------------|--------|--|----------|
| | Temperature range | Name | Description | Version |
| 74AHC1G4208GW-Q100 | -40 °C to +125 °C | TSSOP5 | plastic thin shrink small outline package; 5 leads; body width 1.25 mm | SOT353-1 |

4. Marking

Table 2. Marking codes

| Type number | Marking[1] |
|--------------------|------------|
| 74AHC1G4208GW-Q100 | C5 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

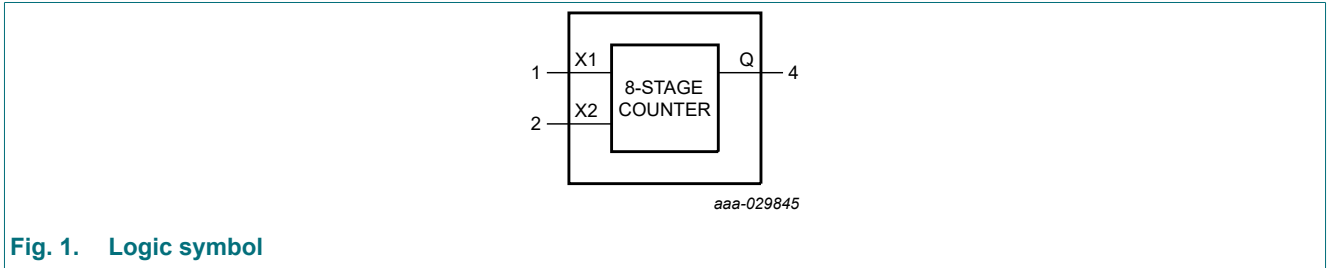


Fig. 1. Logic symbol

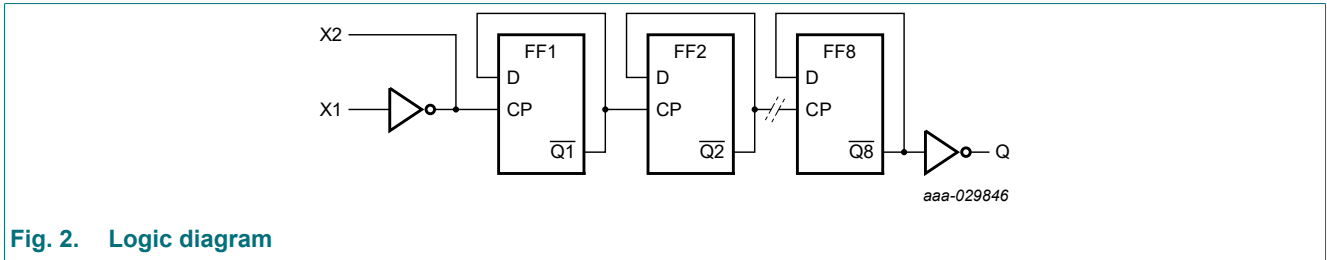


Fig. 2. Logic diagram

6. Pinning information

6.1. Pinning

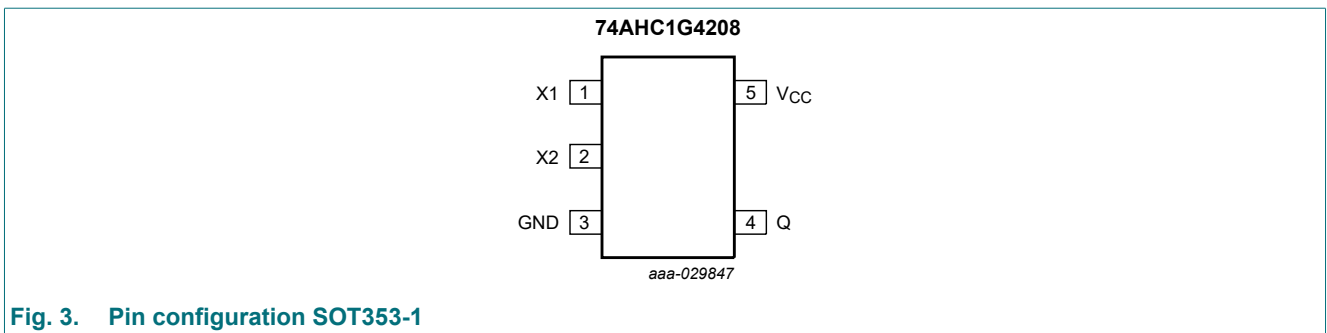


Fig. 3. Pin configuration SOT353-1

6.2. Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|-----|----------------------------|
| X1 | 1 | clock input/oscillator pin |
| X2 | 2 | oscillator pin |
| GND | 3 | ground (0 V) |
| Q | 4 | divider output |
| V _{CC} | 5 | supply voltage |

7. Functional description

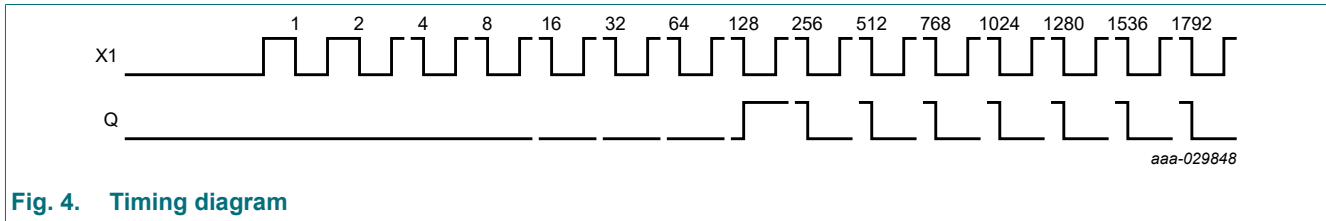


Fig. 4. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | | -0.5 | +7.0 | V |
| I_{IK} | input clamping current | $V_I < -0.5$ V | -20 | - | mA |
| I_{OK} | output clamping current | $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1] | - | ±20 | mA |
| I_O | output current | -0.5 V < $V_O < V_{CC} + 0.5$ V | - | ±25 | mA |
| I_{CC} | supply current | | - | 75 | mA |
| I_{GND} | ground current | | -75 | - | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to +125 °C [2] | - | 250 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: above 74 °C the value of P_{tot} derates linearly with 3.3 mW/K.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|--------------------------|-----|-----|----------|------|
| V_{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | | 0 | - | V_{CC} | V |
| T_{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 3.3$ V ± 0.3 V | - | - | 100 | ns/V |
| | | $V_{CC} = 5.0$ V ± 0.5 V | - | - | 20 | ns/V |

10. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|---------------------------|---|-------|-----|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | X1 | | | | | | | | |
| | | V _{CC} = 2.0 V | 1.7 | - | - | 1.7 | - | 1.7 | - | V |
| | | V _{CC} = 3.0 V | 2.4 | - | - | 2.4 | - | 2.4 | - | V |
| | | V _{CC} = 5.5 V | 4.4 | - | - | 4.4 | - | 4.4 | - | V |
| V _{IL} | LOW-level input voltage | X1 | | | | | | | | |
| | | V _{CC} = 2.0 V | - | - | 0.3 | - | 0.3 | - | 0.3 | V |
| | | V _{CC} = 3.0 V | - | - | 0.6 | - | 0.6 | - | 0.6 | V |
| | | V _{CC} = 5.5 V | - | - | 1.1 | - | 1.1 | - | 1.1 | V |
| V _{OH} | HIGH-level output voltage | Q; V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -50 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | | I _O = -8.0 mA; V _{CC} = 4.5 V | 3.94 | - | - | 3.8 | - | 3.70 | - | V |
| | | X2; V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -50 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | I _O = -50 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -2.0 mA; V _{CC} = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| I _O = -3.0 mA; V _{CC} = 4.5 V | 3.94 | - | - | 3.8 | - | 3.70 | - | V | | |
| V _{OL} | LOW-level output voltage | Q; V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 50 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | I _O = 8.0 mA; V _{CC} = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | X2; V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 50 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 2.0 mA; V _{CC} = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _O = 3.0 mA; V _{CC} = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V | | |
| I _I | input leakage current | X1; V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 1.0 | - | 10 | - | 40 | μA |
| C _I | input capacitance | X1 | - | 3 | 8 | - | 8 | - | 8 | pF |

11. Dynamic characteristics

Table 7. Dynamic characteristics

$GND = 0\text{ V}$; $t_r = t_f = \leq 3.0\text{ ns}$. For test circuit see Fig. 7. For waveforms see Fig. 5 and Fig. 6.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|----------------------|-------------------------------|--|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t_{pd} | propagation delay | X1 to X2 [1] | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2] | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 3 | 7 | 1 | 11 | 1 | 13 | ns |
| | | $C_L = 50\text{ pF}$ | - | 7 | 13 | 1 | 16 | 1 | 18 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3] | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 2 | 5 | 1 | 7 | 1 | 9 | ns |
| | | $C_L = 50\text{ pF}$ | - | 6 | 10 | 1 | 11 | 1 | 12 | ns |
| | | X1 to Q [1] | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ [2] | | | | | | | | |
| | | $C_L = 15\text{ pF}$ | - | 19 | 32 | 1 | 42 | 1 | 49 | ns |
| | | $C_L = 50\text{ pF}$ | - | 21 | 36 | 1 | 46 | 1 | 55 | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ [3] | | | | | | | | |
| $C_L = 15\text{ pF}$ | - | 14 | 23 | 1 | 29 | 1 | 34 | ns | | |
| $C_L = 50\text{ pF}$ | - | 16 | 25 | 1 | 32 | 1 | 38 | ns | | |
| t_W | pulse width | X1 HIGH or LOW | | | | | | | | |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$ | 4 | - | - | 5 | - | 7 | - | ns |
| | | $V_{CC} = 4.5\text{ V to }5.5\text{ V}$ | 3 | - | - | 4 | - | 5 | - | ns |
| f_{max} | maximum frequency | X1 | | | | | | | | |
| | | $V_{CC} = 3.3\text{ V}$ | 125 | - | - | 100 | - | 70 | - | MHz |
| | | $V_{CC} = 5\text{ V}$ | 165 | - | - | 125 | - | 100 | - | MHz |
| C_{PD} | power dissipation capacitance | $C_L = 50\text{ pF}$; $f_i = 1\text{ MHz}$; $V_I = GND\text{ to }V_{CC}$ [4] | | | | | | | | |
| | | $V_{CC} = 3.3\text{ V}$ | - | 4 | - | - | - | - | - | pF |
| | | $V_{CC} = 5\text{ V}$ | - | 5 | - | - | - | - | - | pF |

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] Typical values are measured at $V_{CC} = 3.3\text{ V}$.

[3] Typical values are measured at $V_{CC} = 5.0\text{ V}$.

[4] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + C_L \times V_{CC}^2 \times f_i/256 \text{ where:}$$

f_i = input frequency in MHz; C_L = output load capacitance in pF; V_{CC} = supply voltage in Volt.

11.1. Waveforms and test circuit

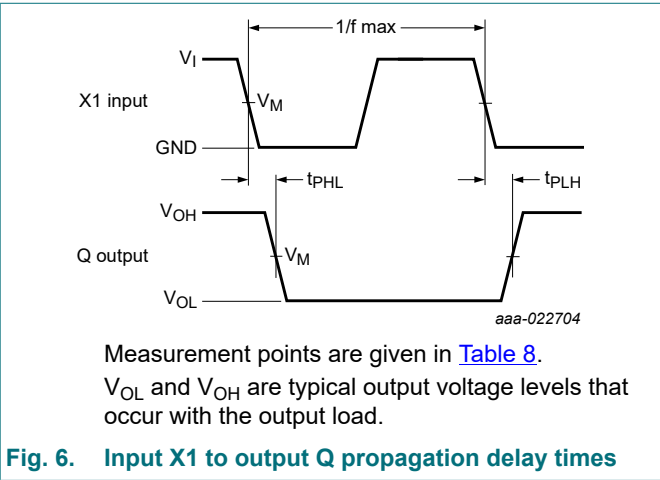
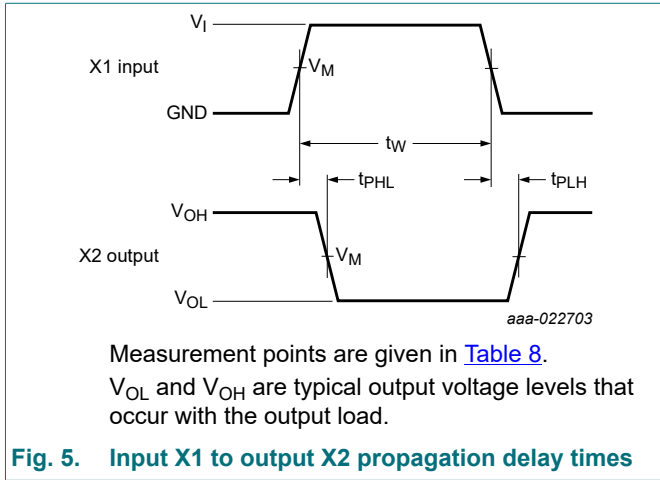
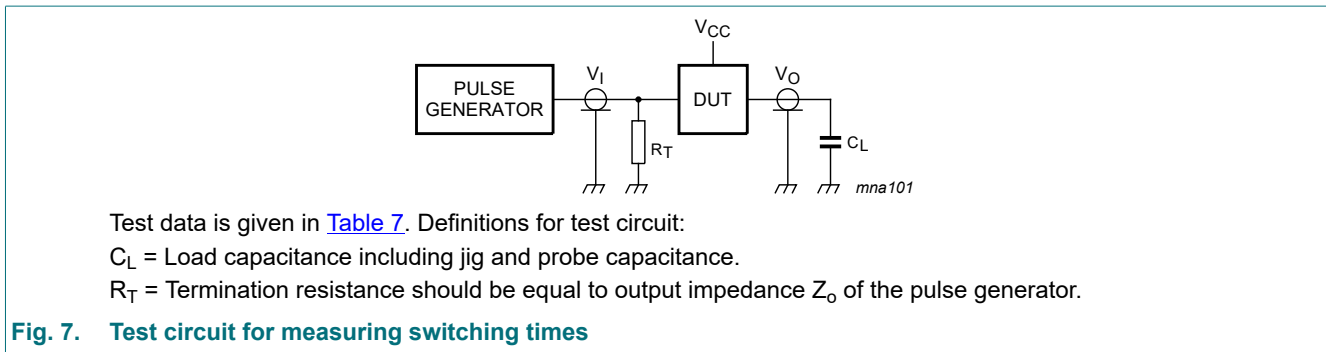


Table 8. Measurement points

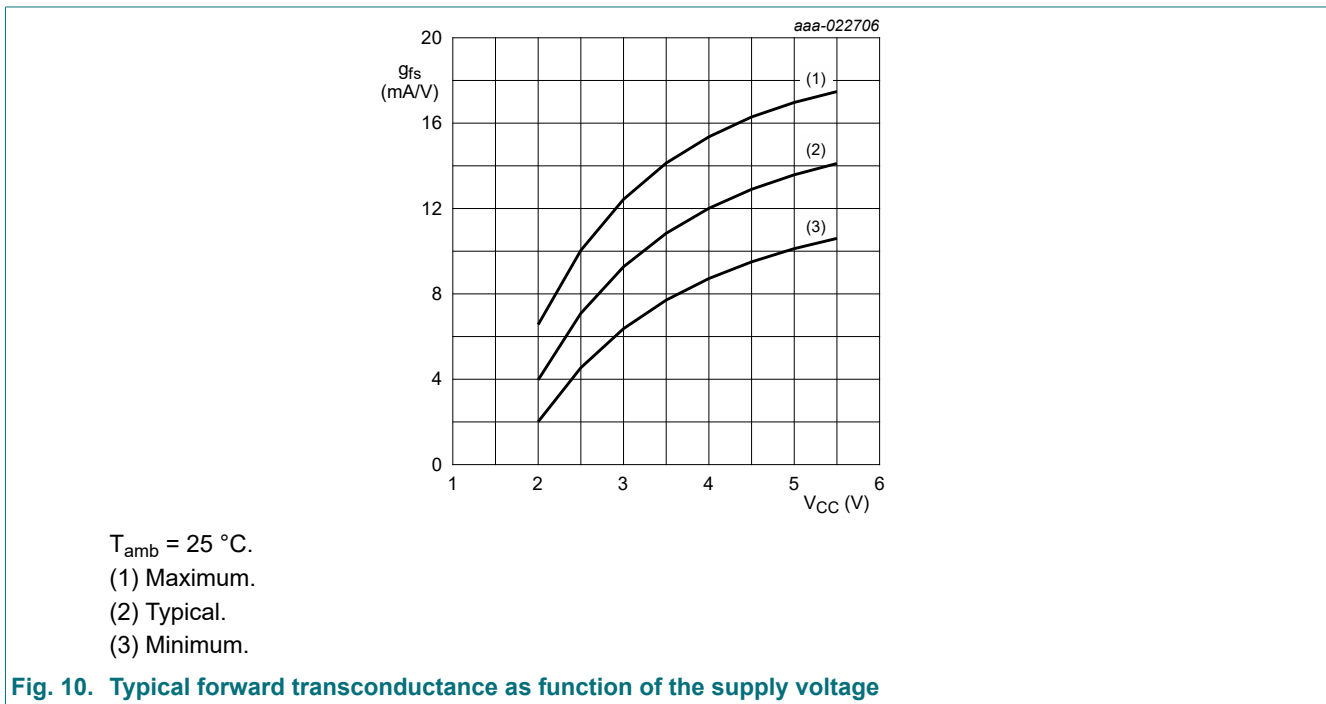
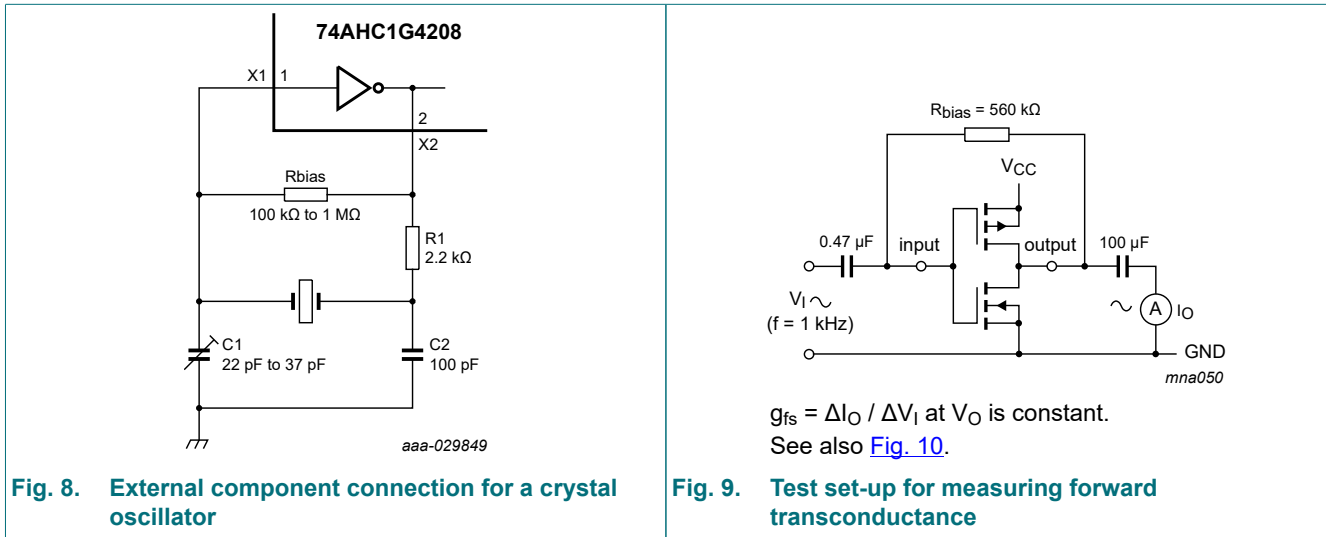
| Inputs | | Output |
|-----------------|---------------------|---------------------|
| V_I | V_M | V_M |
| GND to V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |



12. Crystal oscillator

12.1. Typical crystal oscillator circuit

A typical crystal oscillator schematic is shown in Fig. 8. R1 is the power limiting resistor, its value depends on the frequency and required stability against changes in V_{CC} or average I_{CC} . For starting and maintaining oscillation a minimum transconductance is necessary, so R1 should not be too large. A practical value for R1 is 2.2 k Ω .



13. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | e ₁ | H _E | L | L _p | v | w | y | z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|----------------|-------|----------------|-----|-----|-----|------------------|----------|
| mm | 1.1 | 0.1 0 | 1.0 0.8 | 0.15 | 0.30 0.15 | 0.25 0.08 | 2.25 1.85 | 1.35 1.15 | 0.65 | 1.3 | 2.25 2.0 | 0.425 | 0.46 0.21 | 0.3 | 0.1 | 0.1 | 0.60 0.15 | 7° 0° |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|--------|--------|--|---------------------|------------------------|
| | IEC | JEDEC | JEITA | | | |
| SOT353-1 | | MO-203 | SC-88A | | | -00-09-01- 03-02-19 |

Fig. 11. Package outline SOT353-1 (TSSOP5)

14. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|-------------------------|
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MIL | Military |
| MM | Machine Model |

15. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------------|--------------|--------------------|---------------|------------|
| 74AHC1G4208_Q100 v.1 | 20190903 | Product data sheet | - | - |

16. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
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