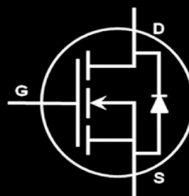
EPC2010C – Enhancement Mode Power Transistor

V_{DSS} , 200 V
$R_{DS(on)}$, 25 mΩ
I_D , 22 A

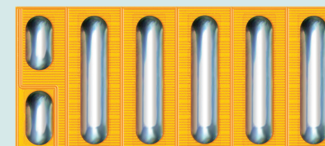
NEW PRODUCT



Halogen-Free

Gallium Nitride is grown on Silicon Wafers and processed using standard CMOS equipment leveraging the infrastructure that has been developed over the last 55 years. GaN's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
I_D	Continuous (T_A =25˚C, $R_{\theta JA}$ = 5.3)	22	A
	Pulsed (25˚C, T_{Pulse} = 300 µs)	90	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	



EPC2010C eGaN® FETs are supplied only in passivated die form with solder bars

Applications

- High Speed DC-DC conversion
- Class D Audio
- High Frequency Hard-Switching and Soft-Switching Circuits

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra low Q_G
- Ultra small footprint

www.epc-co.com/epc/Products/eGaNFETs/EPC2010C.aspx

Static Characteristics (T_J= 25˚C unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 200 µA	200			V
I_{DSS}	Drain Source Leakage	V_{DS} = 160 V, V_{GS} = 0 V		50	150	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		1	3	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		50	150	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{GS}, I_D = 3 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 12 A		18	25	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.7		V

All measurements were done with substrate shorted to source.

Thermal Characteristics			
		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.1	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	2.7	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1)	56	˚C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See http://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Dynamic Characteristics (T_J = 25˚C unless otherwise stated)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance			380	540	
C_{OSS}	Output Capacitance	V_{GS} = 0 V, V_{DS} = 100 V		240	320	pF
C_{RSS}	Reverse Transfer Capacitance			1.8	2.7	
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{DS} = 100 V, I_D = 12 A, V_{GS} = 5 V		3.7	5.3	
Q_{GS}	Gate to Source Charge			1.3		
Q_{GD}	Gate to Drain Charge	V_{DS} = 100 V, I_D = 12 A		0.7	1.3	nC
$Q_{G(TH)}$	Gate Charge at Threshold			0.9		
Q_{OSS}	Output Charge	V_{DS} = 100 V, V_{GS} = 0 V		40	52	
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.

Figure 1: Typical Output Characteristics at 25°C

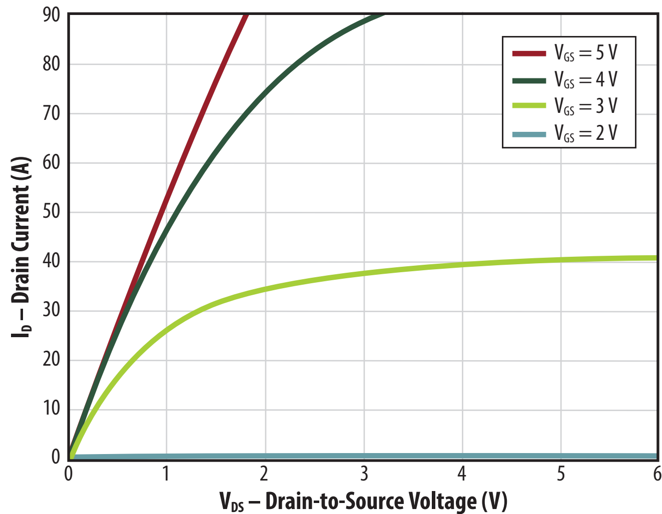


Figure 2: Transfer Characteristics

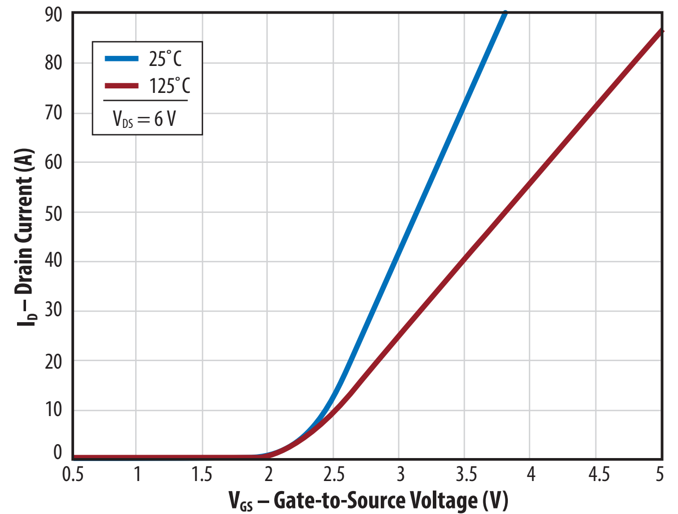


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Current

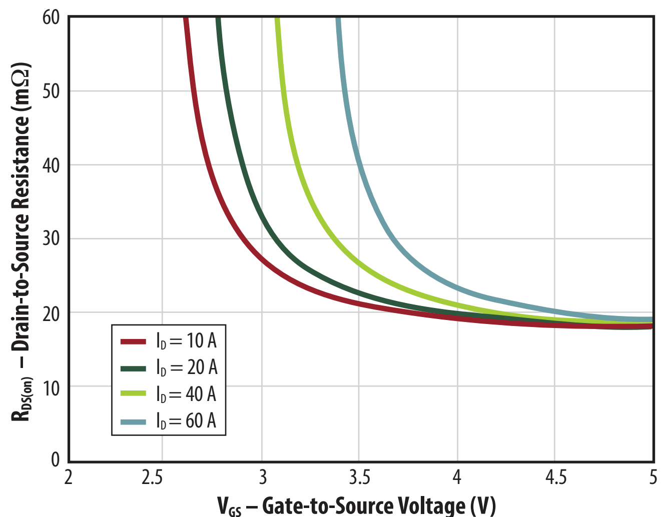
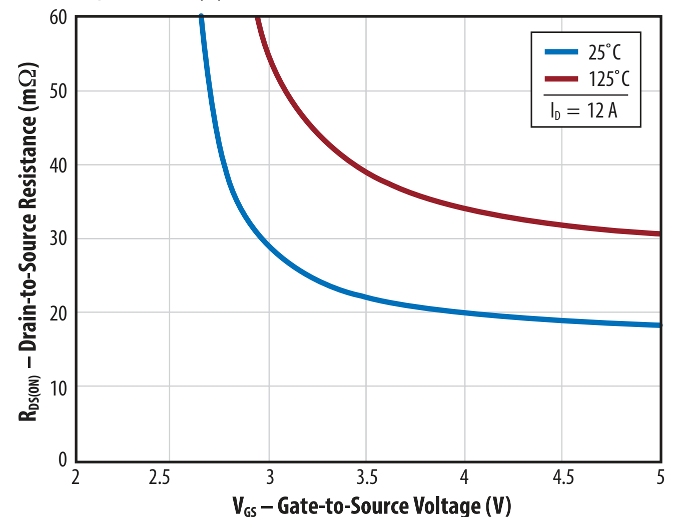
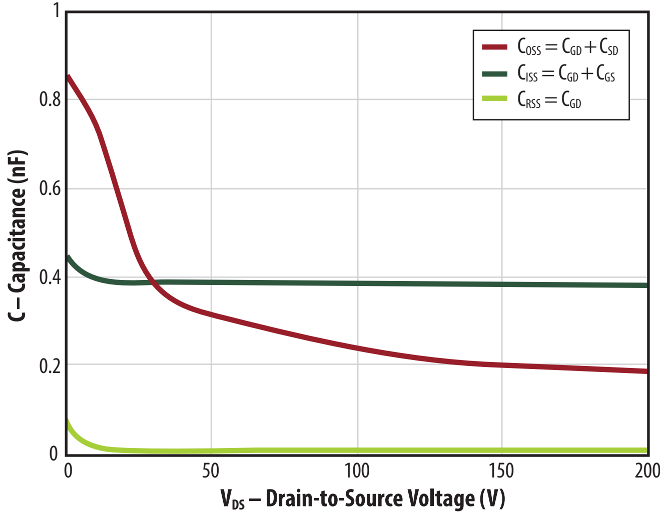
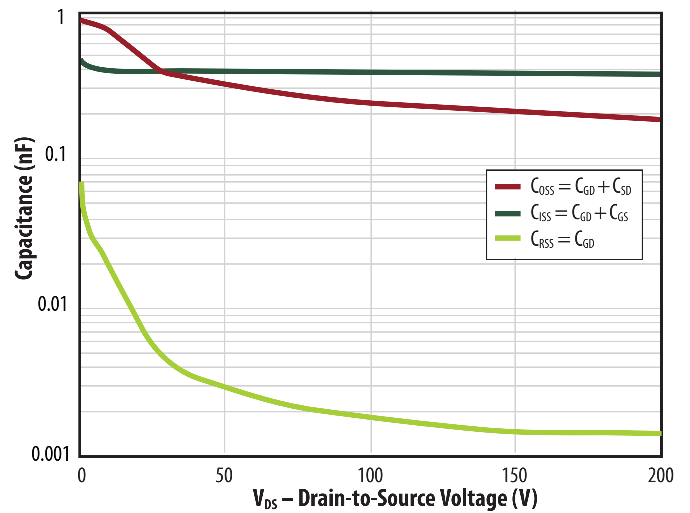
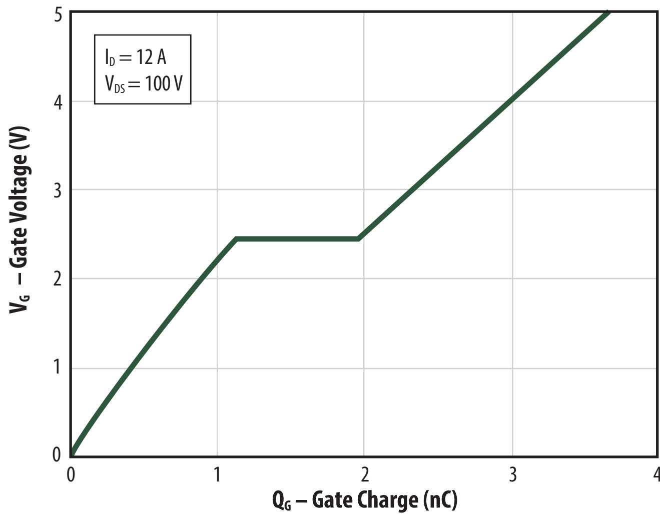


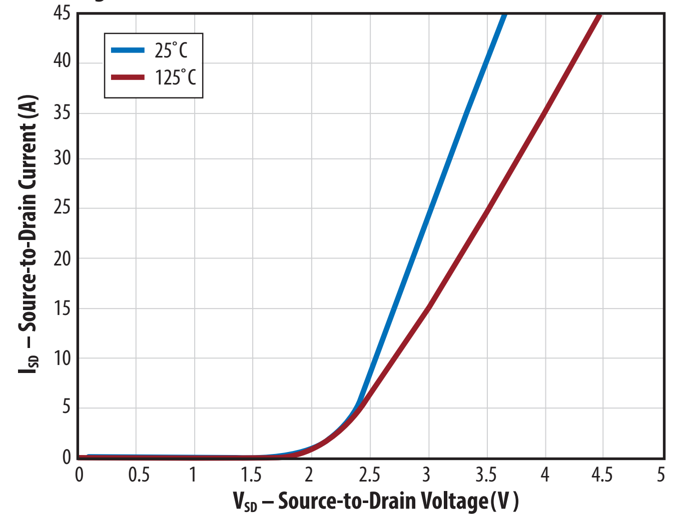
Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

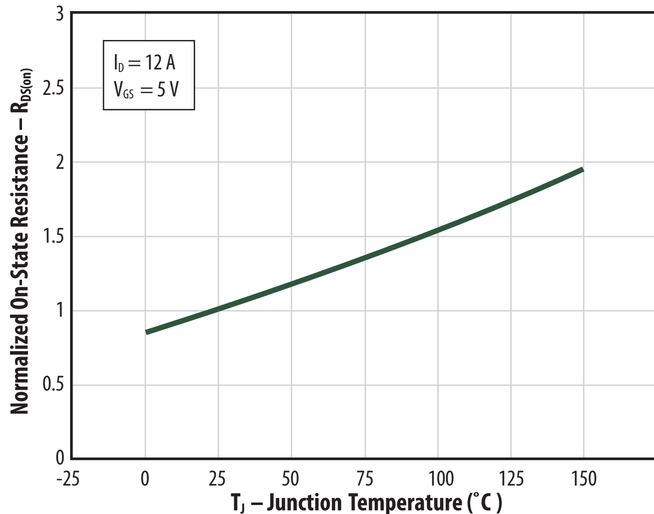


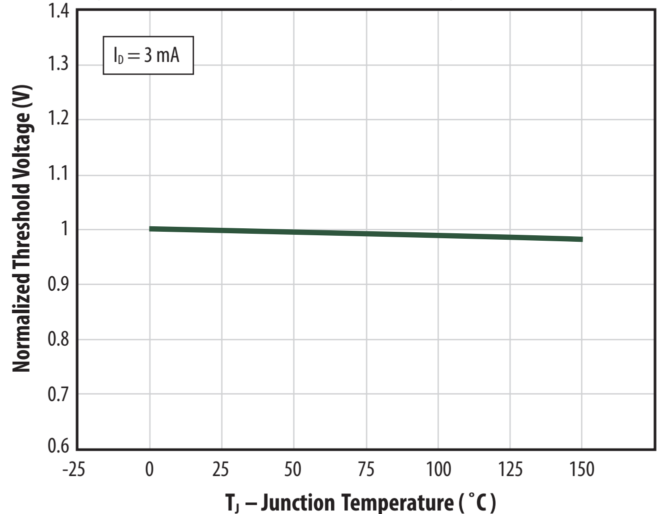












All measurements were done with substrate shortened to source.

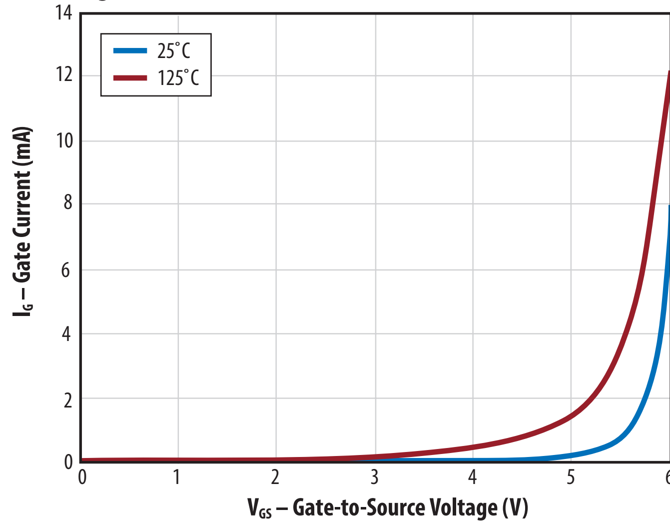
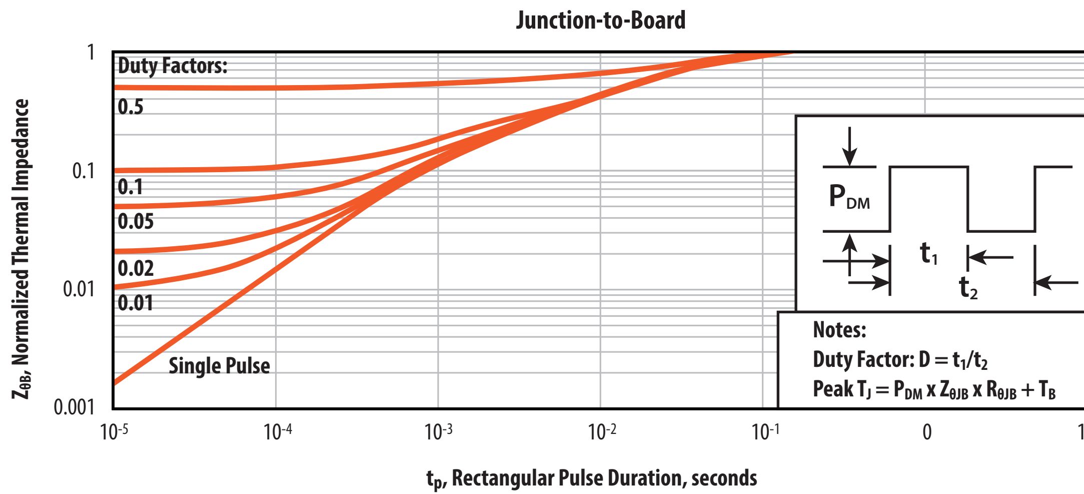


Figure 11: Transient Thermal Response Curves



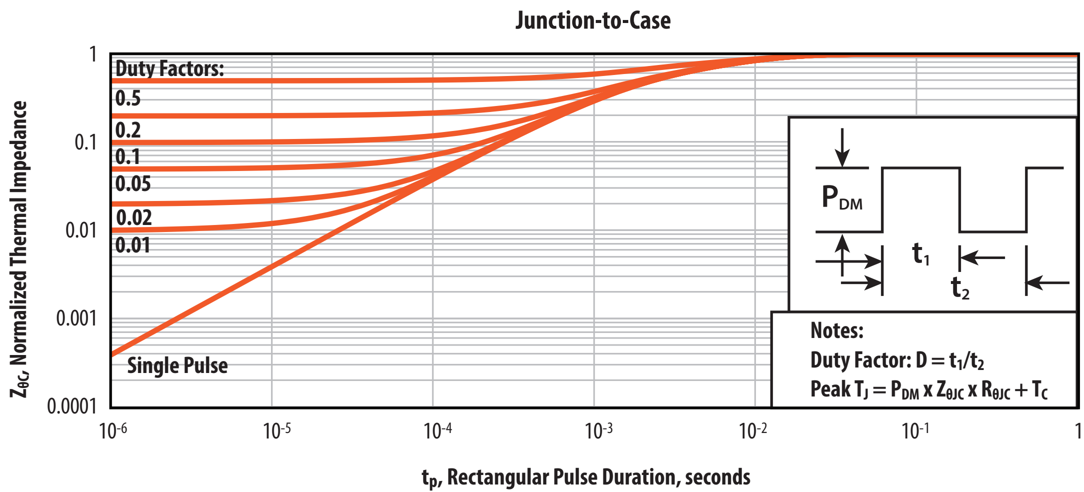
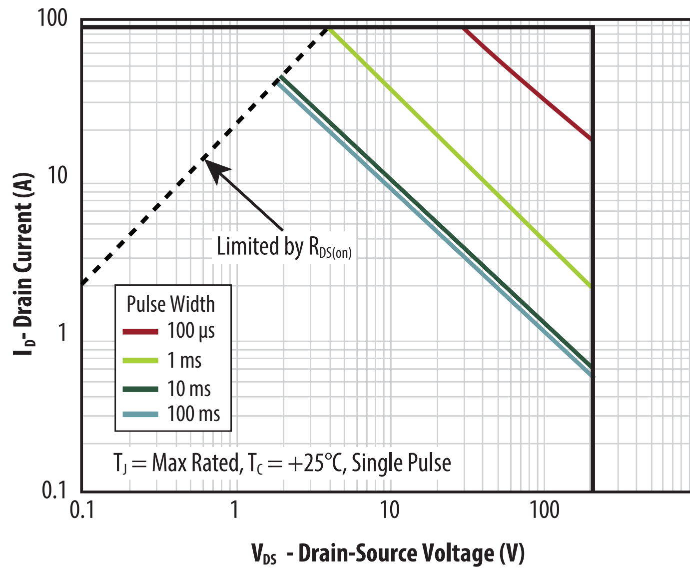
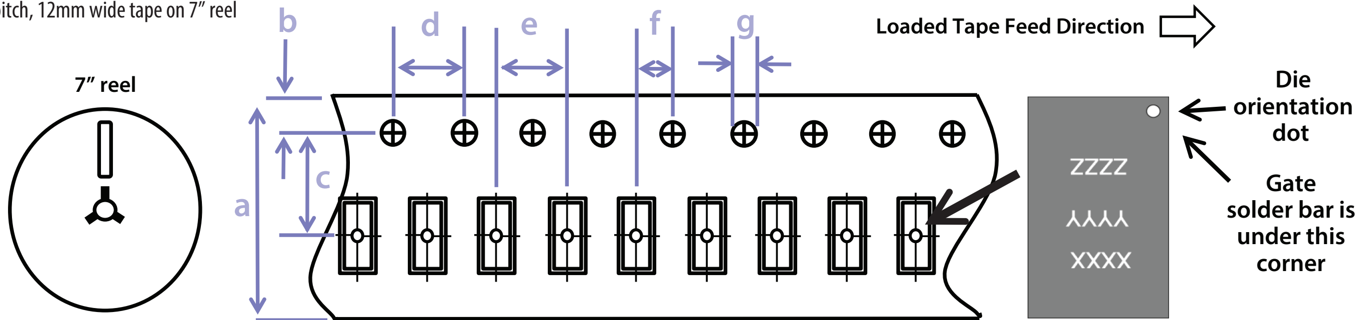


Figure 12: Safe Operating Area



TAPE AND REEL CONFIGURATION

4mm pitch, 12mm wide tape on 7" reel

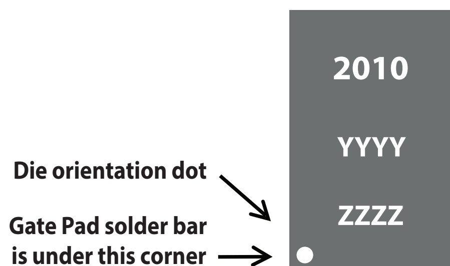


Die is placed into pocket solder bar side down (face side down)

	EPC2010C (note 1)		
Dimension (mm)	target	min	max
a	12.0	11.9	12.3
b	1.75	1.65	1.85
c (note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (note 2)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

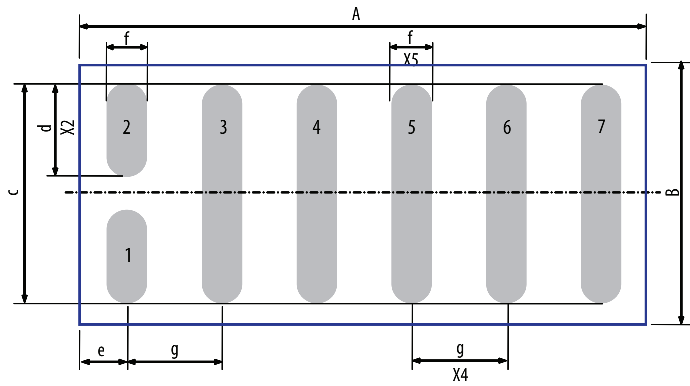
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2010C	2010	YYYY	ZZZZ

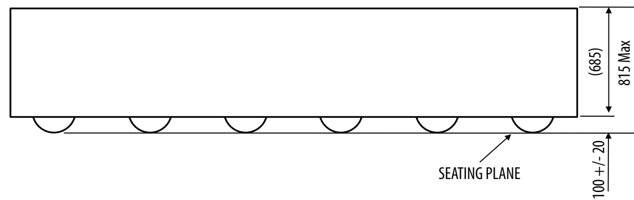
DIE OUTLINE

Solder Bar View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	3524	3554	3584
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	262	277	292
f	245	250	255
g	600	600	600

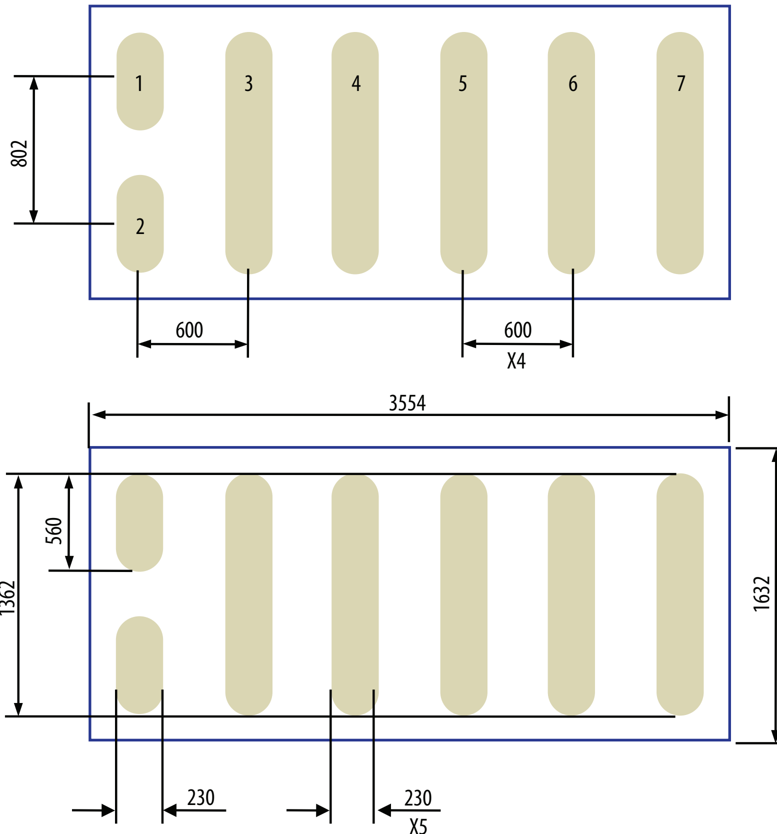
Side View



RECOMMENDED LAND PATTERN

(units in µm)

The land pattern is solder mask defined.



Pad no. 1 is Gate;

Pads no. 3, 5, 7 are Drain;

Pads no. 4, 6 are Source;

Pad no. 2 is Substrate

For assembly recommendations please visit http://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

Efficient Power Conversion Corporation (EPC) reserves the right to make changes without further notice to any products herein to improve reliability, function or design. EPC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

eGaN® is a registered trademark of Efficient Power Conversion Corporation.

U.S. Patents 8,350,294; 8,404,508; 8,431,960; 8,436,398; 8,785,974; 8,890,168; 8,969,918; 8,853,749; 8,823,012

Information subject to change without notice.

Revised September, 2015