



PMDPB95XNE2

30 V, dual N-channel Trench MOSFET

14 June 2016

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Very fast switching
- Trench MOSFET technology
- Leadless medium power SMD plastic package: 2 × 2 × 0.65 mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Charging switch for portable devices
- DC-to-DC converters
- Small brushless DC motor drive
- Power management in battery-driven portables
- Hard disk and computing power management

4. Quick reference data

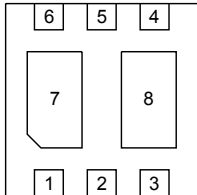
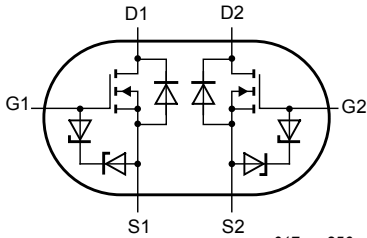
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_J = 25\text{ °C}$	-	-	30	V
V_{GS}	gate-source voltage		-12	-	12	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	3	A
Static characteristics (per transistor)						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 2.8\text{ A}; T_J = 25\text{ °C}$	-	77	99	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view DFN2020-6 (SOT1118)</p>	 <p>017aaa256</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB95XNE2	DFN2020-6	DFN2020-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

7. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB95XNE2	3B

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	30	V
V_{GS}	gate-source voltage			-12	12	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	3	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	2.7	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	1.7	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	11	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	510	mW
			[1]	-	1.165	W
		$T_{sp} = 25\text{ °C}$		-	8.33	W
Per device						
T_j	junction temperature			-55	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
Source-drain diode						
I_S	source current	$T_{amb} = 25\text{ °C}$	[1]	-	1.1	A

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

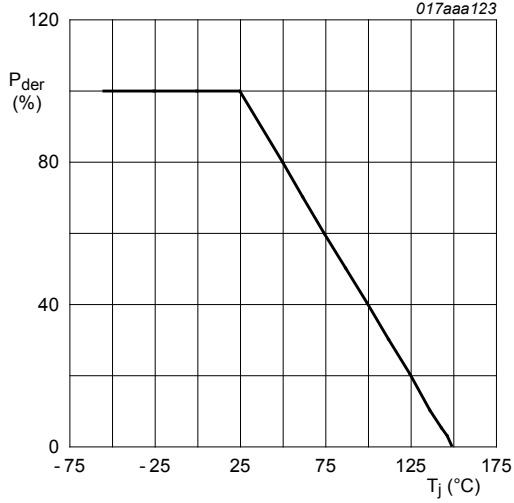


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

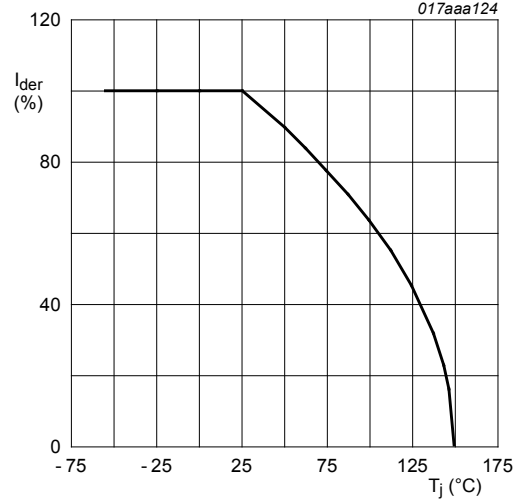


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

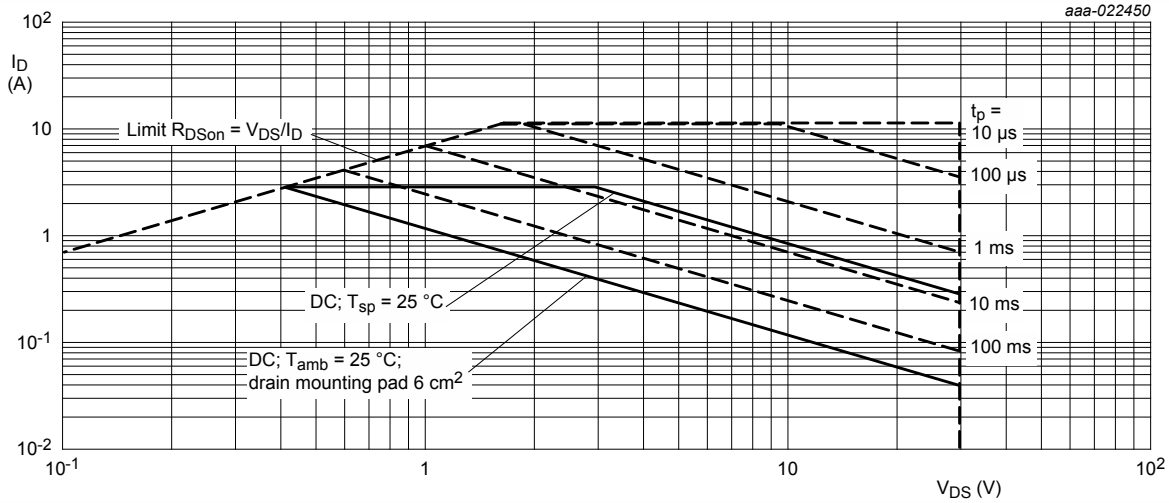


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor							
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	224	257	K/W
			[2]	-	95	109	K/W
		in free air; t ≤ 5 s	[2]	-	55	64	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	12	15	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

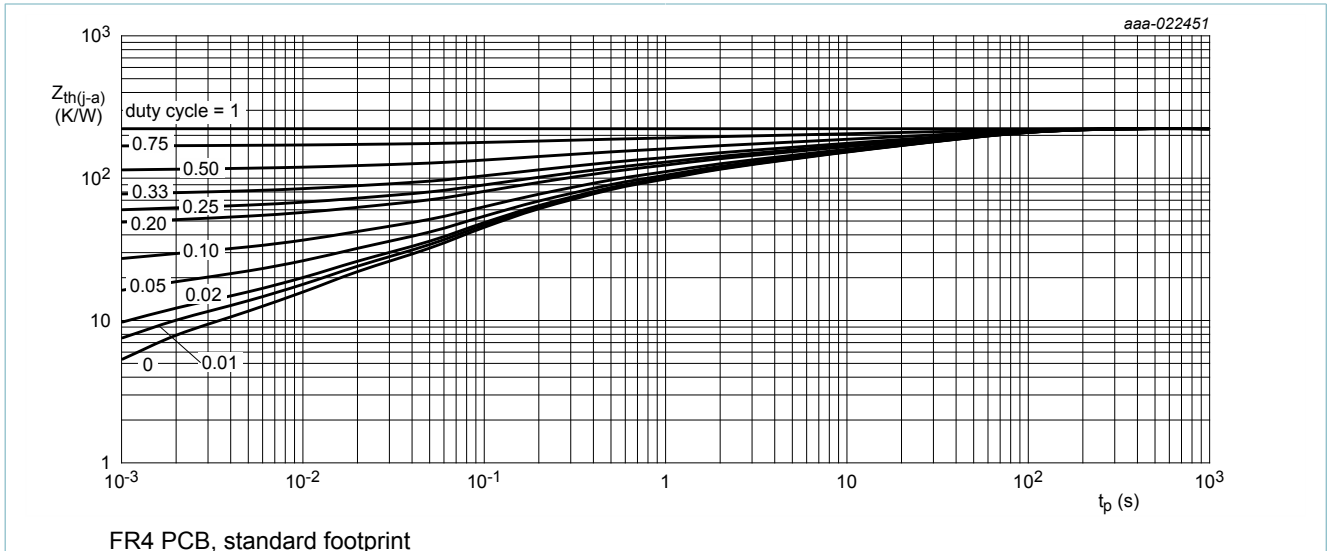


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

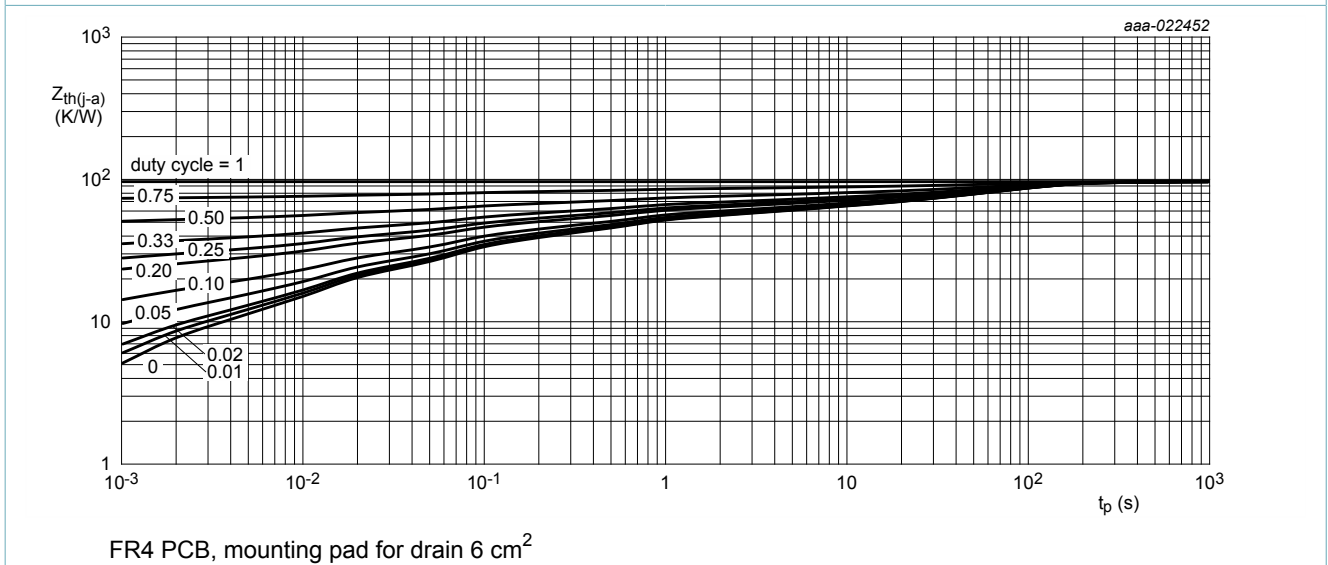


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics (per transistor)						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu\text{A}$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	0.75	1	1.25	V
I_{DSS}	drain leakage current	$V_{DS} = 30 \text{ V}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 12 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	10	μA
		$V_{GS} = -12 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-10	μA
		$V_{GS} = 4.5 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	2	μA
		$V_{GS} = -4.5 \text{ V}$; $V_{DS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-2	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}$; $I_D = 2.8 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	77	99	m Ω
		$V_{GS} = 4.5 \text{ V}$; $I_D = 2.8 \text{ A}$; $T_j = 150 \text{ }^\circ\text{C}$	-	126	170	m Ω
		$V_{GS} = 2.5 \text{ V}$; $I_D = 2.5 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	92	117	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10 \text{ V}$; $I_D = 2.8 \text{ A}$; $T_j = 25 \text{ }^\circ\text{C}$	-	8.6	-	S
R_G	gate resistance	$T_j = 25 \text{ }^\circ\text{C}$; $f = 1 \text{ MHz}$	-	9.2	-	Ω
Dynamic characteristics (per transistor)						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 \text{ V}$; $I_D = 3 \text{ A}$; $V_{GS} = 4.5 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	2.9	4.5	nC
Q_{GS}	gate-source charge		-	0.4	-	nC
Q_{GD}	gate-drain charge		-	0.8	-	nC
C_{iss}	input capacitance	$V_{DS} = 15 \text{ V}$; $f = 1 \text{ MHz}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	258	-	pF
C_{oss}	output capacitance		-	31	-	pF
C_{riss}	reverse transfer capacitance		-	23	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 15 \text{ V}$; $I_D = 3 \text{ A}$; $V_{GS} = 4.5 \text{ V}$; $R_{G(ext)} = 6 \text{ } \Omega$; $T_j = 25 \text{ }^\circ\text{C}$	-	9	-
t_r	rise time	-		10	-	ns
$t_{d(off)}$	turn-off delay time	-		20	-	ns
t_f	fall time	-		8	-	ns
Source-drain diode (per transistor)						
V_{SD}	source-drain voltage	$I_S = 1.1 \text{ A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	0.7	1.2	V

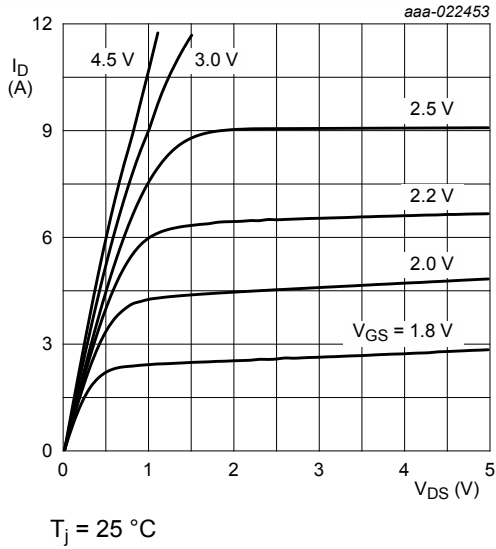


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

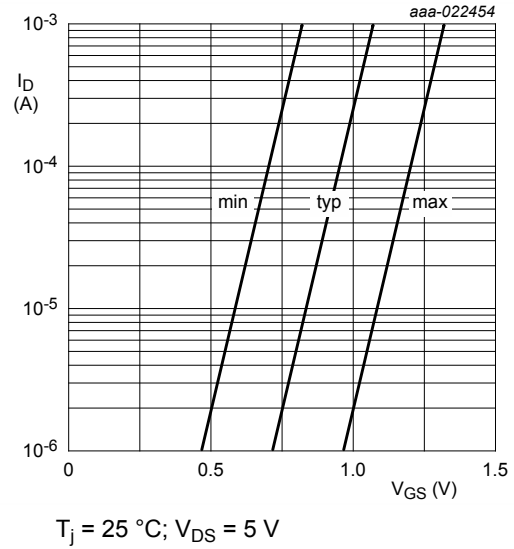


Fig. 7. Subthreshold drain current as a function of gate-source voltage

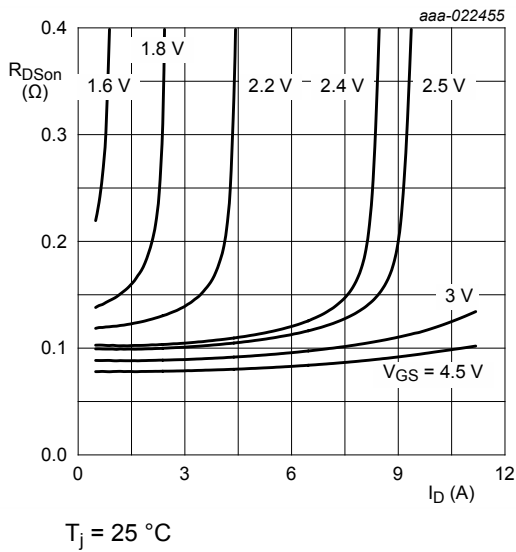


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

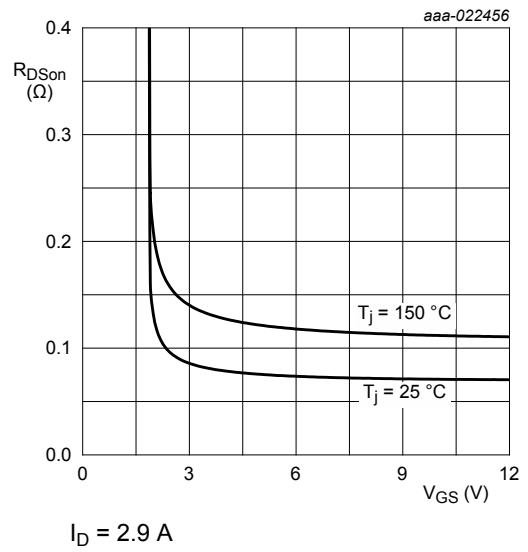
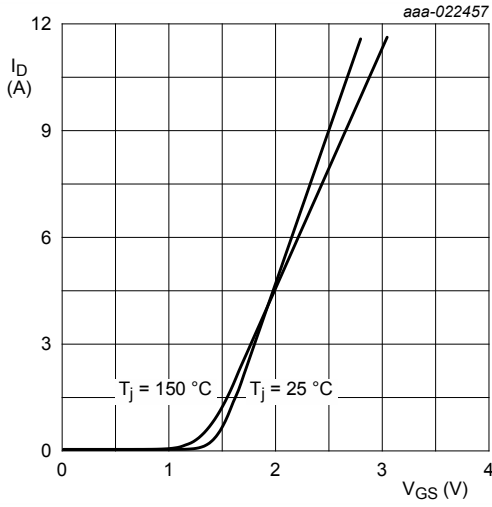


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

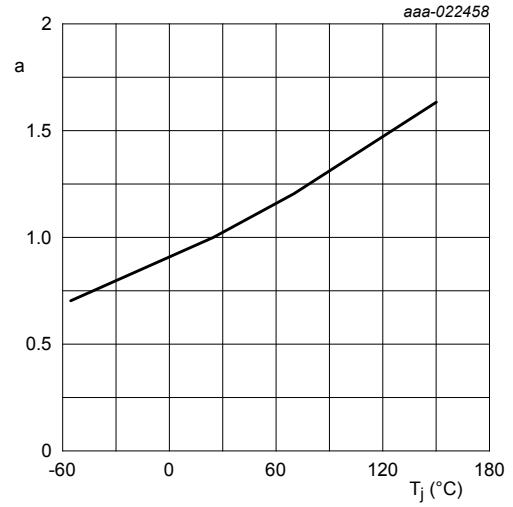
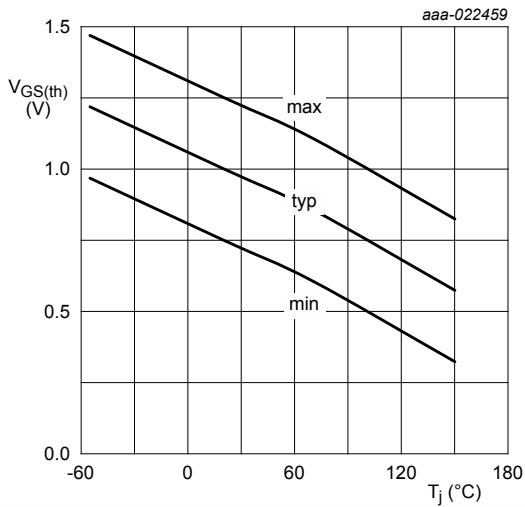


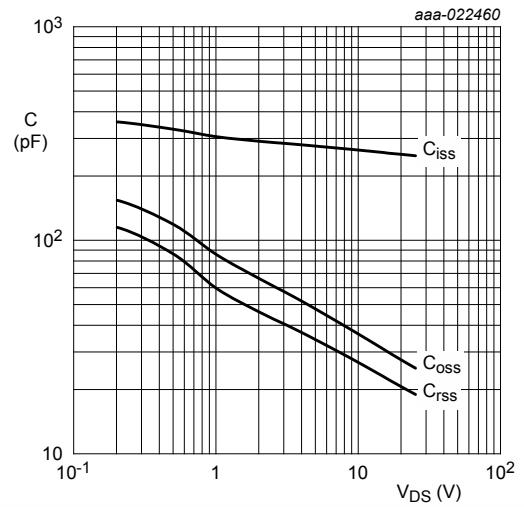
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$



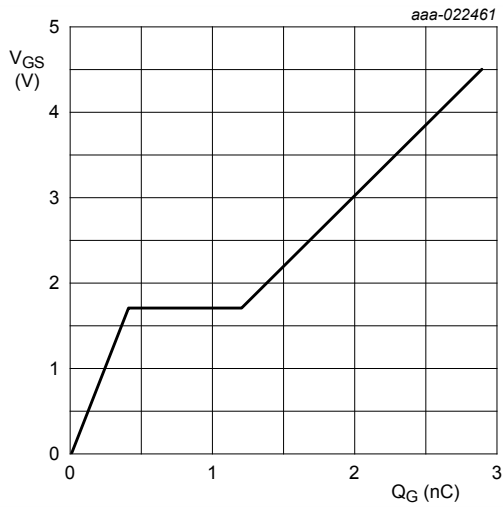
$$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 2.8 \text{ A}; V_{DS} = 15 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

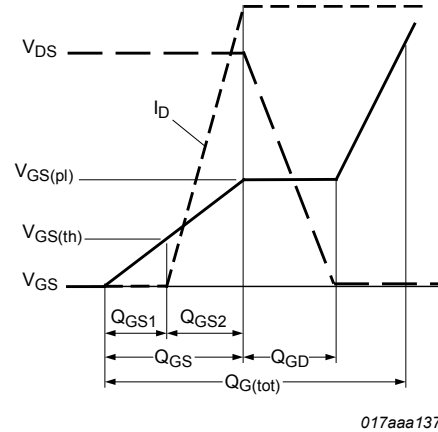
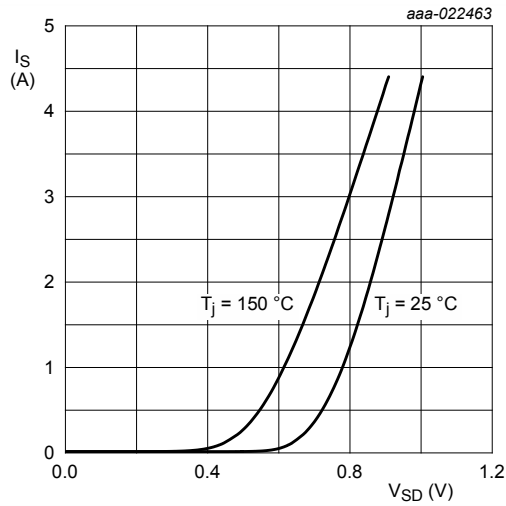


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

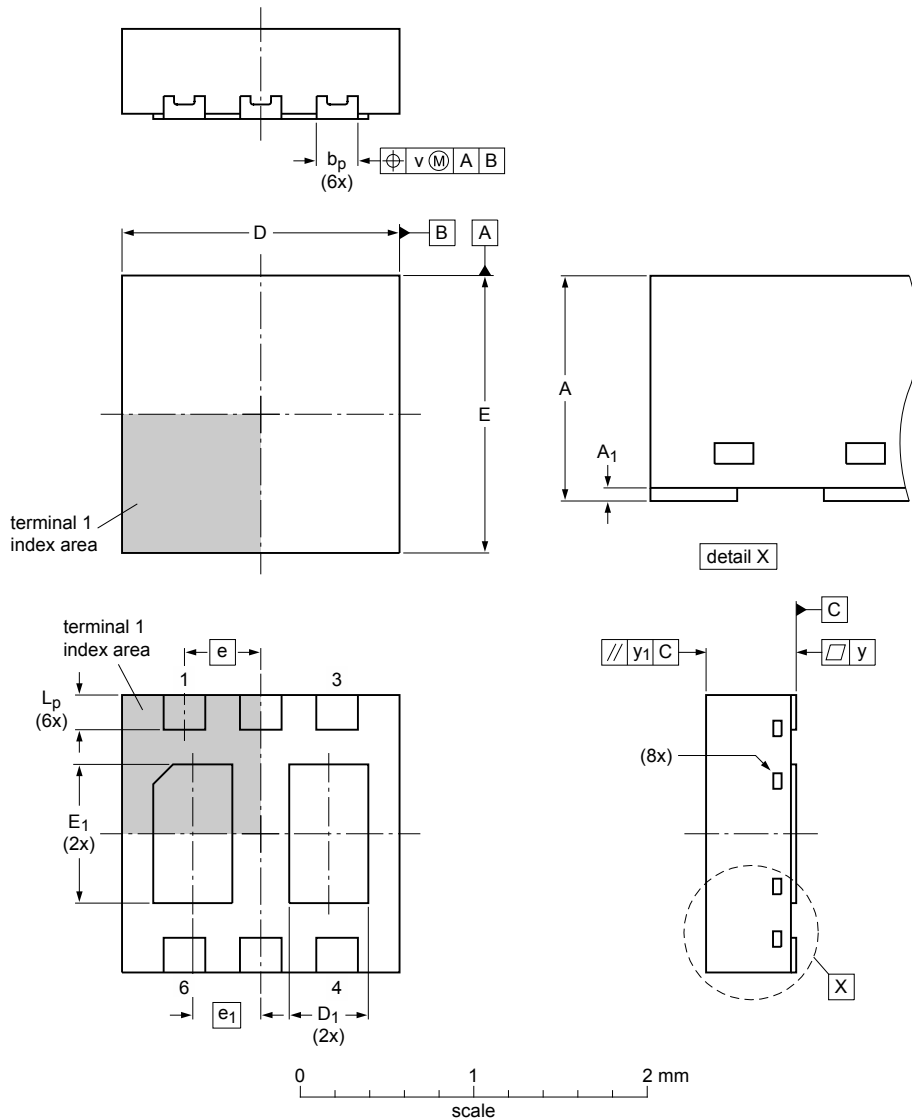


Fig. 17. Duty cycle definition

12. Package outline

HUSON6: plastic, thermal enhanced ultra thin small outline package; no leads;
6 terminals; body 2 x 2 x 0.65 mm

SOT1118



Dimensions

Unit	A ⁽¹⁾	A ₁	b _p	D	D ₁	E	E ₁	e	e ₁	L _p	v	y	y ₁
max	0.65	0.04	0.35	2.1	0.77	2.1	1.1	0.54	0.3				
nom								0.65		0.1	0.05	0.05	
min			0.25	1.9	0.57	1.9	0.9	0.44	0.2				

Note

1. Dimension including plating thickness.

sot1118_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1118		---			10-08-16 13-06-06

Fig. 18. Package outline DFN2020-6 (SOT1118)

13. Soldering

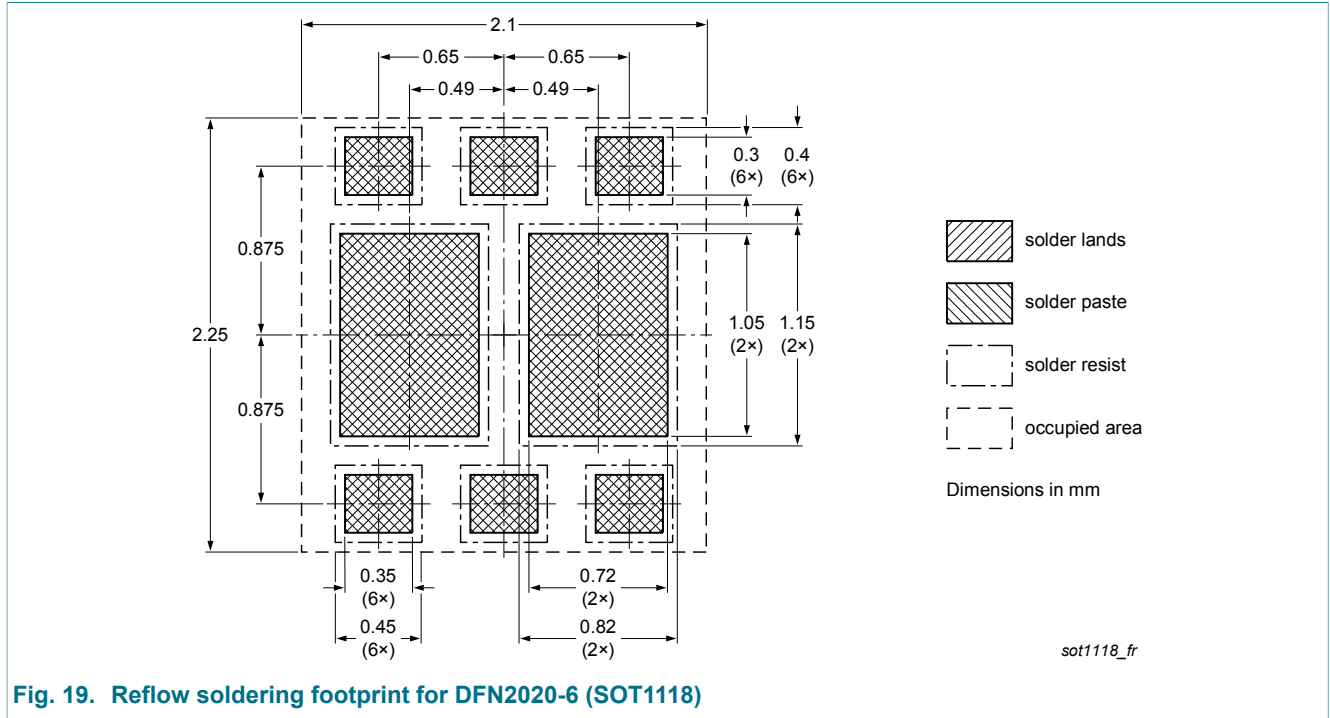


Fig. 19. Reflow soldering footprint for DFN2020-6 (SOT1118)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB95XNE2 v.2	20160614	Product data sheet	-	PMDPB95XNE2 v.1
Modifications:	<ul style="list-style-type: none">• Values of I_D and R_{DSon} corrected			
PMDPB95XNE2 v.1	20160419	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 14 June 2016