

MOSFET - Power, N-Channel, PowerTrench® Power Clip, Symmetric Dual 30 V NTTFD4D1N03P1E

Features

- Latest 30 V MOSFET Technology with Optimized Figure-of-Merit
- Less Junction Capacitance for High Switching Frequency Application
- Lower Q_{GD}/Q_{GS} for Shoot-Through Preventing
- Small Footprint (3.3mm x 3.3mm) for Compact Design
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- DC-DC Converters
- System Voltage Rails

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

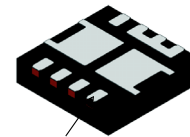
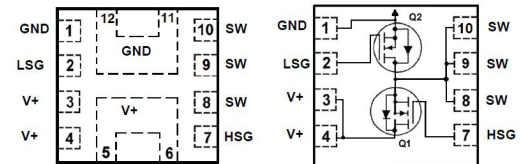
Parameter		Symbol	Q1	Q2	Unit	
Drain-to-Source Voltage		V _{DSS}	30	30	V	
Gate-to-Source Voltage		V _{GS}	+16 -12	+16 -12	V	
Continuous Drain Current R _{θJC} (Note 3)	Steady State	T _C = 25°C	I _D	54	54	A
		T _C = 85°C		38	38	
Power Dissipation R _{θJC} (Note 3)		T _C = 25°C	P _D	20	20	W
Continuous Drain Current R _{θJA} (Notes 1, 3)	Steady State	T _A = 25°C	I _D	15	15	A
		T _A = 85°C		11	11	
Power Dissipation R _{θJA} (Notes 1, 3)		T _A = 25°C	P _D	1.7	1.7	W
Continuous Drain Current R _{θJA} (Notes 2, 3)	Steady State	T _A = 25°C	I _D	12	12	A
		T _A = 85°C		8	8	
Power Dissipation R _{θJA} (Notes 2, 3)		T _A = 25°C	P _D	1.0	1.0	W
Pulsed Drain Current	T _A = 25°C, t _p = 10 μs	I _{DM}	408	408	A	
Single Pulse Drain-to-Source Avalanche Energy Q1: I _L = 7 A _{pk} , L = 3 mH (Note 4) Q2: I _L = 7 A _{pk} , L = 3 mH (Note 4)		E _{AS}	74	74	mJ	
Operating Junction and Storage Temperature		T _J , T _{stg}	-55 to + 150		°C	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T _L	260		°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in² pad size, 2 oz. Cu pad.
2. Surface-mounted on FR4 board using minimum pad size, 2 oz. Cu pad.
3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted. Actual continuous current will be limited by thermal & electro-mechanical application board design. R_{θJC} is determined by the user's board design.
4. Q1 100% UIS tested at L = 3 mH, IAS = 7 A.
Q2 100% UIS tested at L = 3 mH, IAS = 7 A.
5. This device is Class 1B ESD HBM Rating.

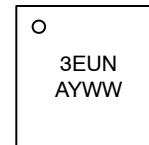
FET	V _{(BR)DSS}	R _{DS(ON) MAX}	I _{D MAX}
Q1	30 V	4.3 mΩ @ 10 V	54 A
		5.4 mΩ @ 4.5 V	
Q2	30 V	3.5 mΩ @ 10 V	54 A
		4.5 mΩ @ 4.5 V	

ELECTRICAL CONNECTION



PIN1
WQFN12
3.3X3.3, 0.65P
CASE 510CJ

MARKING DIAGRAM



3EUN = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping†
NTTFD4D1N03P1E	WQFN12 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Q1 Max	Q2 Max	Unit
Junction-to-Case – Steady State (Notes 1, 3)	$R_{\theta JC}$	6.0	6.0	°C/W
Junction-to-Ambient – Steady State (Notes 1, 3)	$R_{\theta JA}$	70	70	
Junction-to-Ambient – Steady State (Notes 2, 3)	$R_{\theta JA}$	120	120	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	FET	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$		Q1	30		V
		$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$		Q2	30		
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 1\text{ mA}, \text{ ref to } 25^\circ\text{C}$		Q1		17	mV/°C
		$I_D = 1\text{ mA}, \text{ ref to } 25^\circ\text{C}$		Q2		17	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$	Q1		1.0	μA
				Q2		1.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V} / -12\text{ V}$		Q1		± 100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V} / -12\text{ V}$		Q2		± 100	

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 270\text{ }\mu\text{A}$		Q1	1.2	1.61	2.2	V
		$V_{GS} = V_{DS}, I_D = 270\text{ }\mu\text{A}$		Q2	1.2	1.64	2.2	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 270\text{ }\mu\text{A}, \text{ ref to } 25^\circ\text{C}$		Q1		4.5		mV/°C
		$I_D = 270\text{ }\mu\text{A}, \text{ ref to } 25^\circ\text{C}$		Q2		4.5		
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		Q1		3.8	4.3	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$					4.7	
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		Q2		2.9	3.5	
		$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$					3.9	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 10\text{ A}$		Q1		52		S
		$V_{DS} = 5\text{ V}, I_D = 10\text{ A}$		Q2		57		
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		Q1		0.8		Ω
				Q2		0.8		

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$	Q1		1103		pF
			Q2		972		
Output Capacitance	C_{OSS}		Q1		335		pF
			Q2		309		
Reverse Transfer Capacitance	C_{RSS}		Q1		19		pF
			Q2		25		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

7. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	FET	Min	Typ	Max	Unit
CHARGES AND CAPACITANCES							
Total Gate Charge	Q _{G(TOT)}	Q1: V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 10 A Q2: V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 10 A	Q1		6.7		nC
			Q2		6.3		
Gate-to-Drain Charge	Q _{GD}		Q1		1.4		nC
			Q2		1.4		
Gate-to-Source Charge	Q _{GS}		Q1		2.8		nC
			Q2		2.5		
Total Gate Charge	Q _{G(TOT)}	Q1: V _{GS} = 10 V, V _{DS} = 15 V; I _D = 10 A	Q1		15		nC
		Q2: V _{GS} = 10 V, V _{DS} = 15 V; I _D = 10 A	Q2		14		

SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 7)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V Q1: I _D = 10 A, V _{DD} = 15 V, R _G = 6 Ω Q2: I _D = 10 A, V _{DD} = 15 V, R _G = 6 Ω	Q1		12		ns
			Q2		11		
Rise Time	t _r		Q1		7.5		ns
			Q2		5.2		
Turn-Off Delay Time	t _{d(OFF)}		Q1		16		ns
			Q2		14.3		
Fall Time	t _f	Q1		5.2		ns	
		Q2		4.9			

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 7)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V Q1: I _D = 10 A, V _{DD} = 15 V, R _G = 6 Ω Q2: I _D = 10 A, V _{DD} = 15 V, R _G = 6 Ω	Q1		8.3		ns
			Q2		7.5		
Rise Time	t _r		Q1		2.0		ns
			Q2		1.8		
Turn-Off Delay Time	t _{d(OFF)}		Q1		22		ns
			Q2		20		
Fall Time	t _f	Q1		3.2		ns	
		Q2		3.0			

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 10 A	T _J = 25°C	Q1		0.80	1.2	V
			T _J = 125°C			0.65		
		V _{GS} = 0 V, I _S = 10 A	T _J = 25°C	Q2		0.79	1.2	
			T _J = 125°C			0.65		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, V _{DD} = 15 V Q1: I _S = 10 A, dI _S /dt = 100 A/μs Q2: I _S = 10 A, dI _S /dt = 100 A/μs	Q1		23		ns	
	Q2			22				
Reverse Recovery Charge	Q _{RR}		Q1		9.4		nC	
			Q2		9.0			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

7. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS – Q1

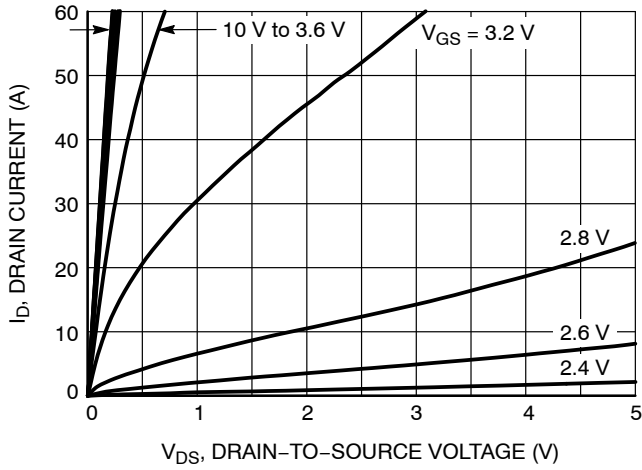


Figure 1. On-Region Characteristics

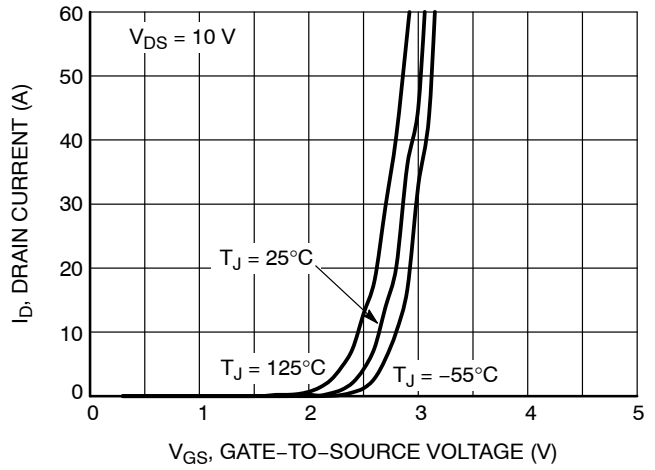


Figure 2. Transfer Characteristics

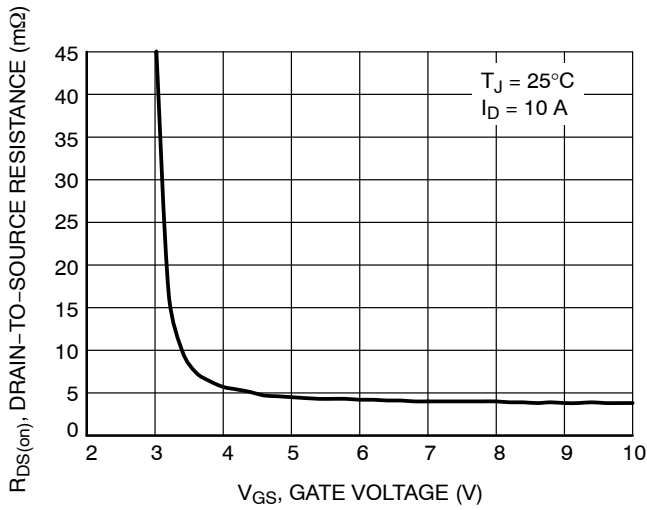


Figure 3. On-Resistance vs. Gate-to-Source Voltage

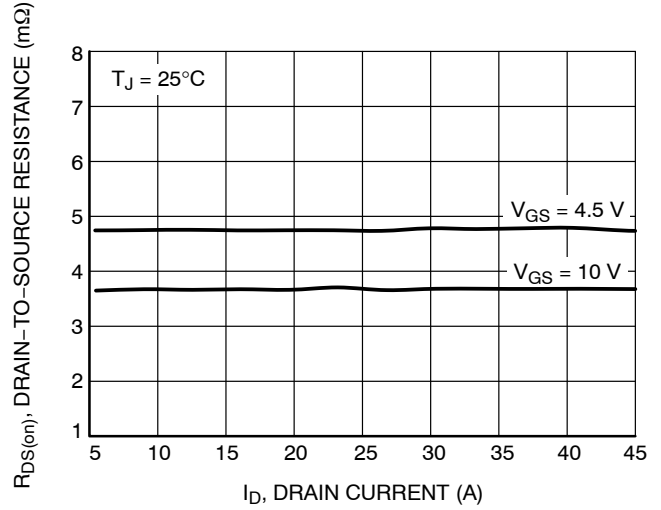


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

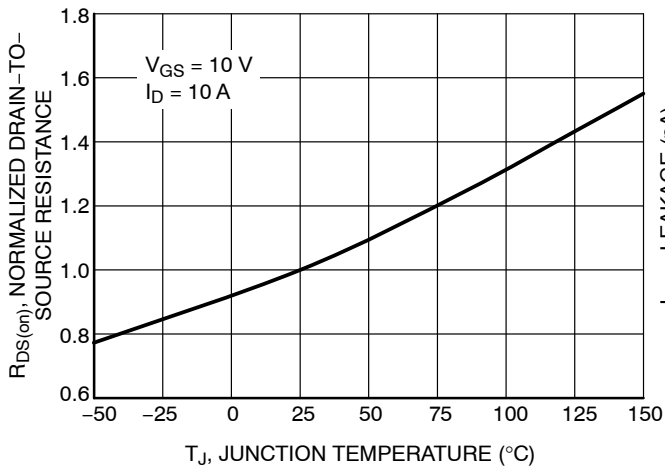


Figure 5. On-Resistance Variation with Temperature

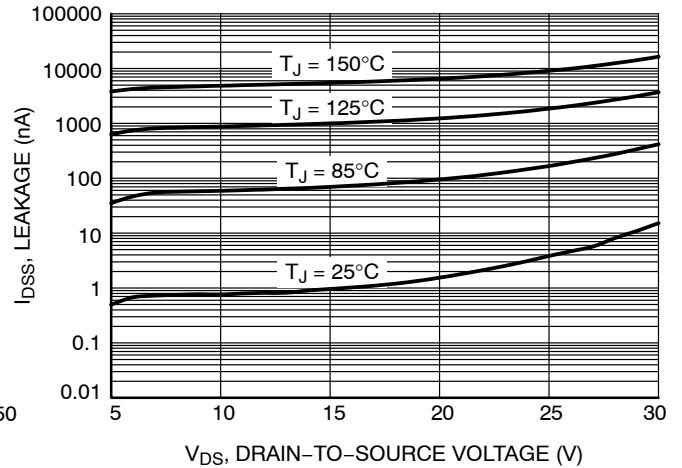


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS – Q1

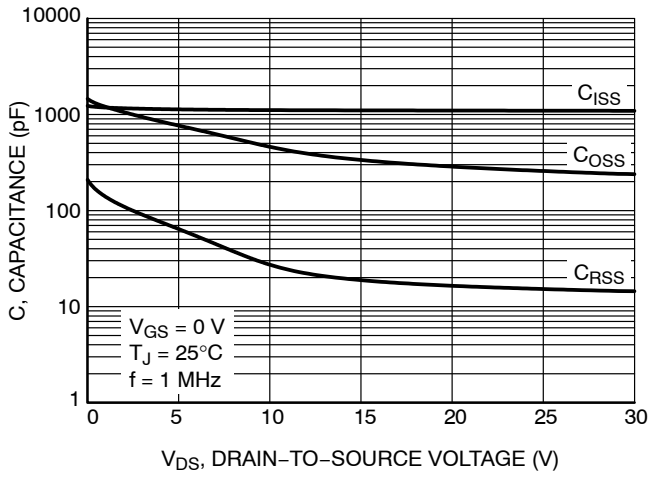


Figure 7. Capacitance Variation

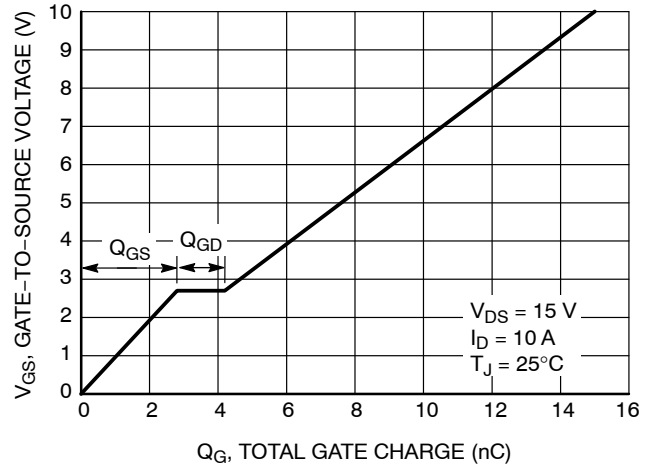


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

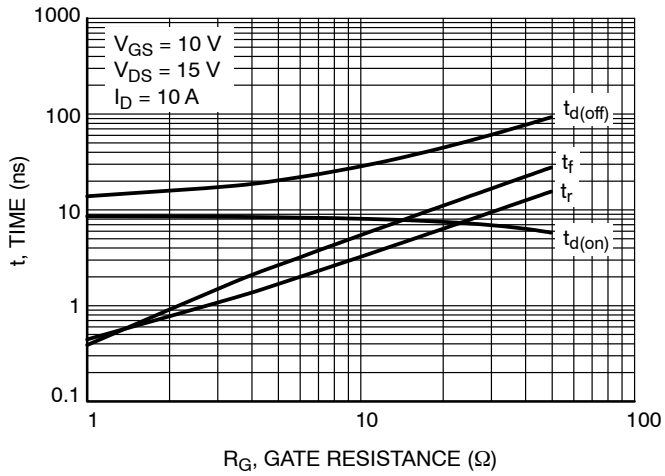


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

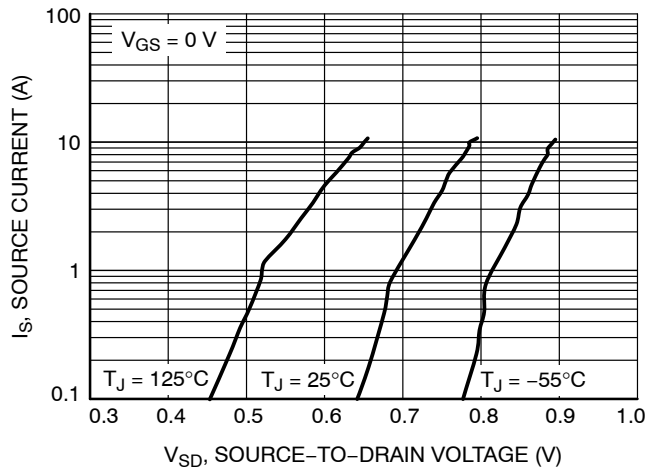


Figure 10. Diode Forward Voltage vs. Current

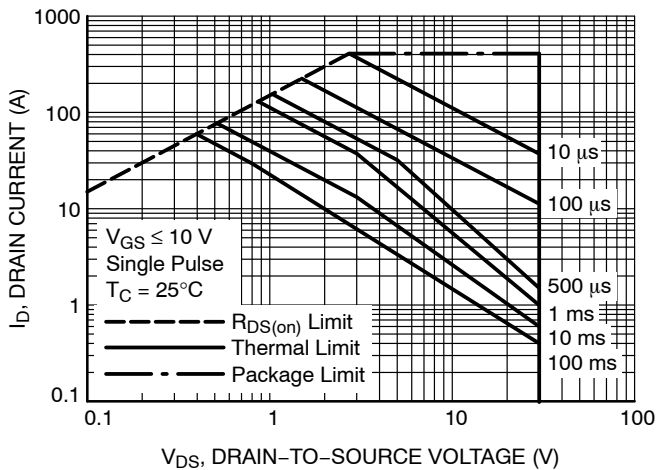


Figure 11. Maximum Rated Forward Biased Safe Operating Area

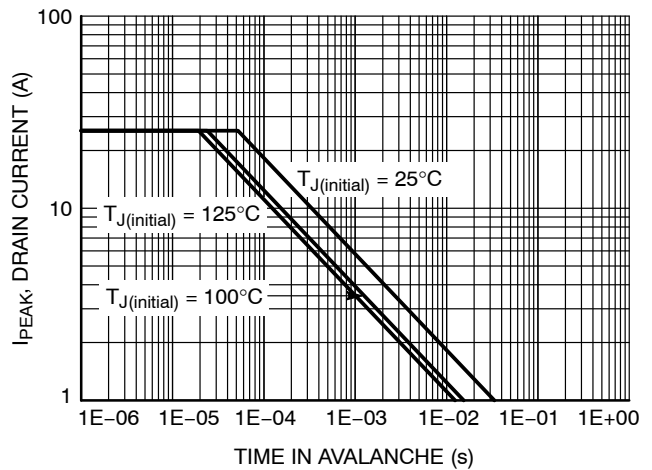


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS – Q1

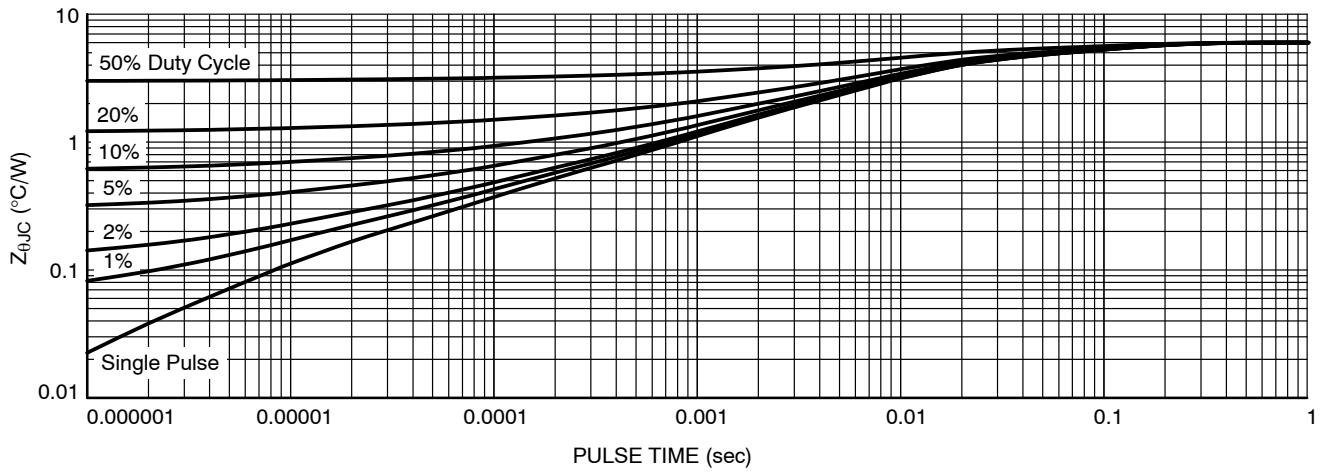


Figure 13. Thermal Characteristics

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TYPICAL CHARACTERISTICS – Q2

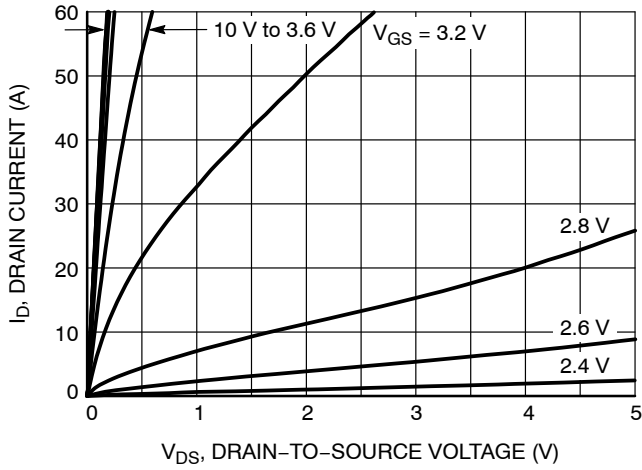


Figure 14. On-Region Characteristics

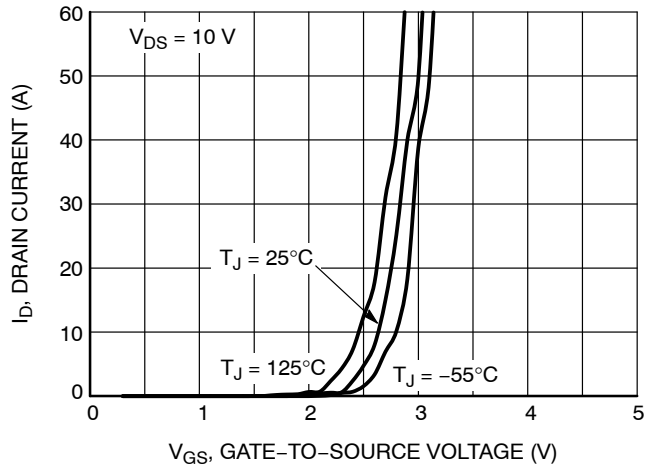


Figure 15. Transfer Characteristics

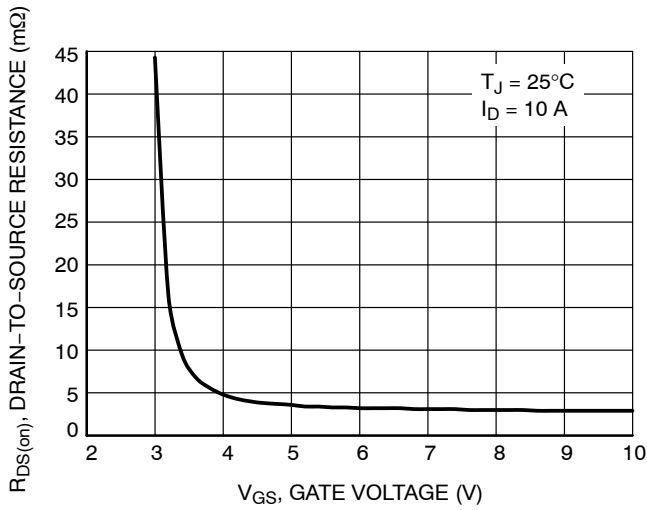


Figure 16. On-Resistance vs. Gate-to-Source Voltage

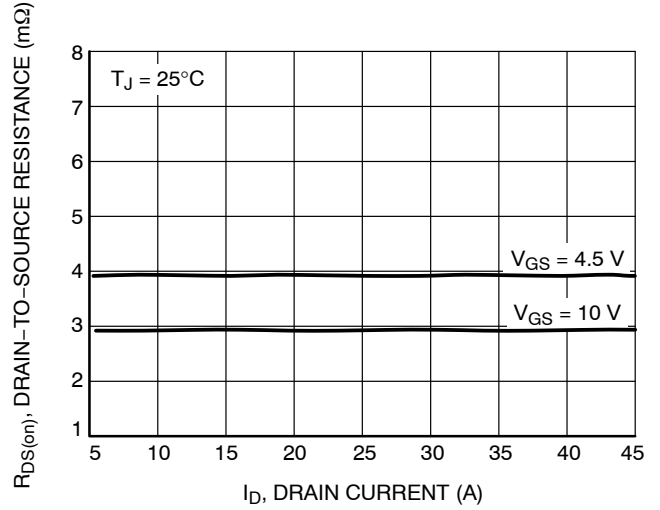


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

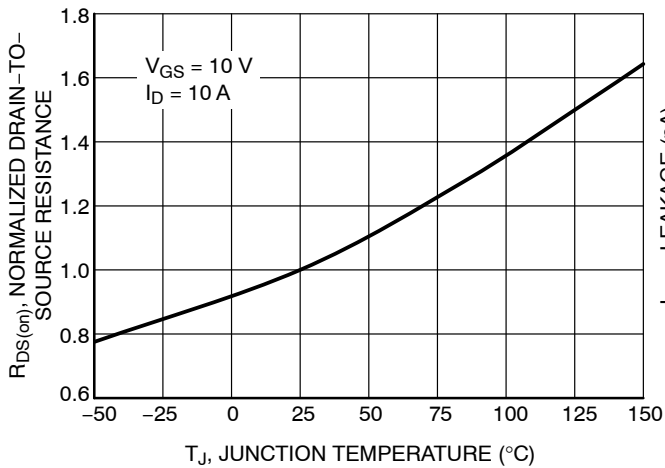


Figure 18. On-Resistance Variation with Temperature

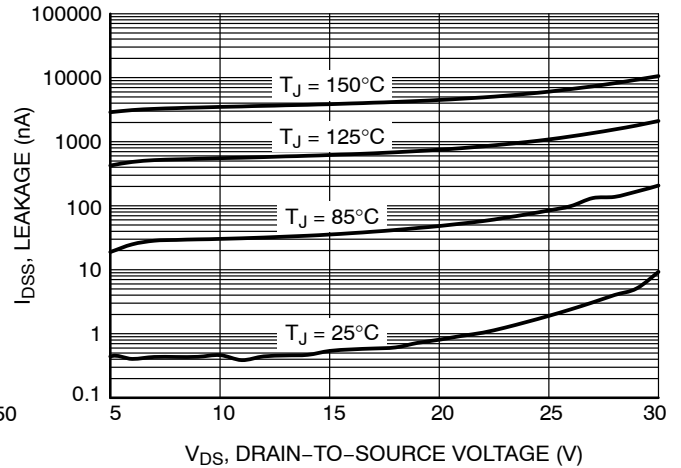


Figure 19. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS – Q2

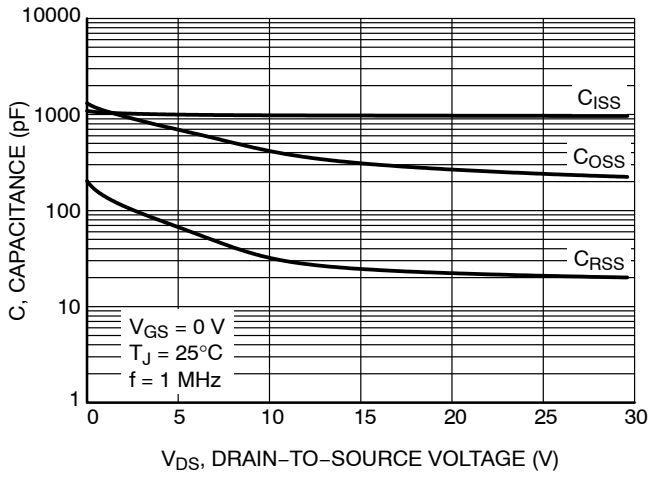


Figure 20. Capacitance Variation

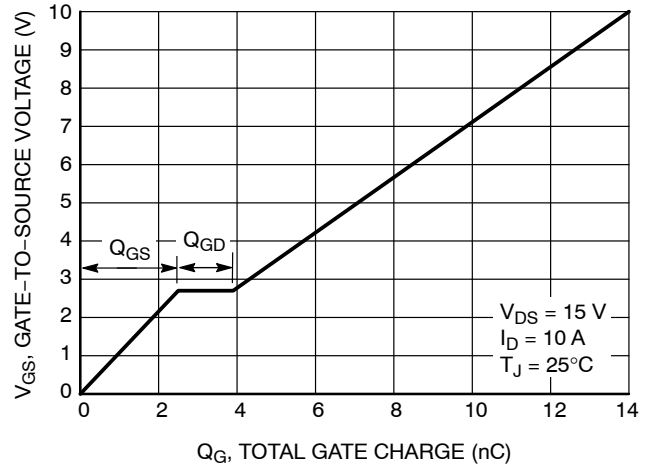


Figure 21. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

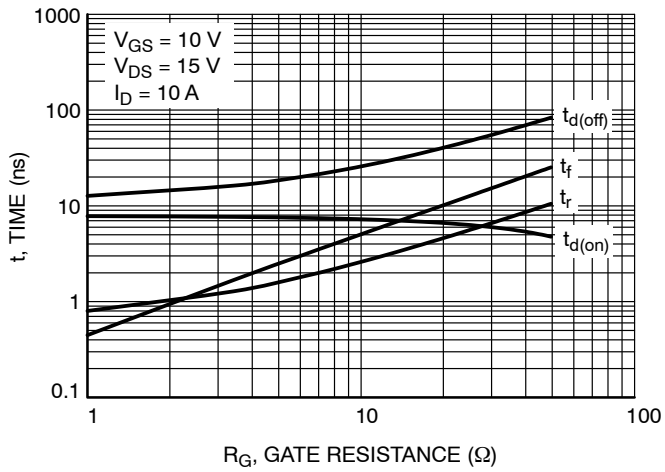


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

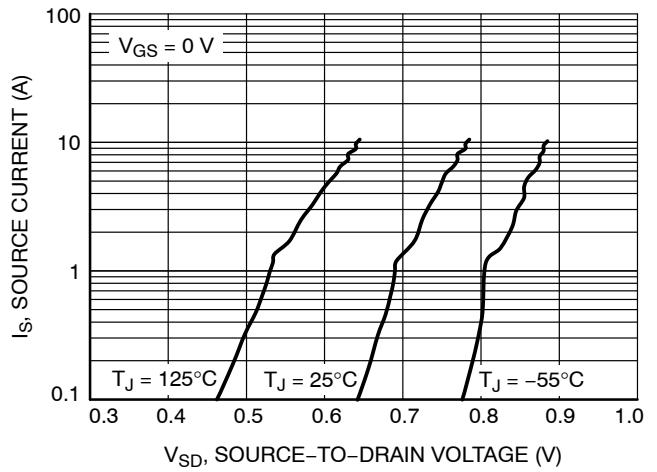


Figure 23. Diode Forward Voltage vs. Current

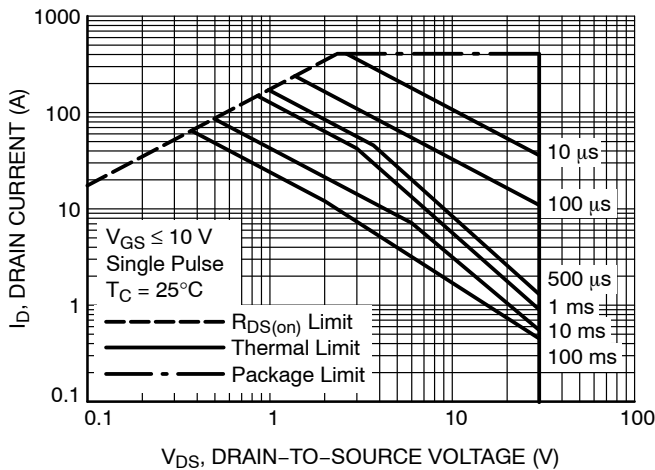


Figure 24. Maximum Rated Forward Biased Safe Operating Area

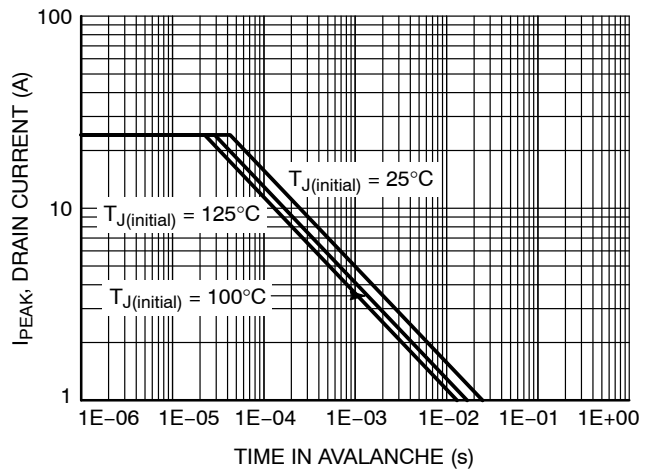


Figure 25. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS – Q2

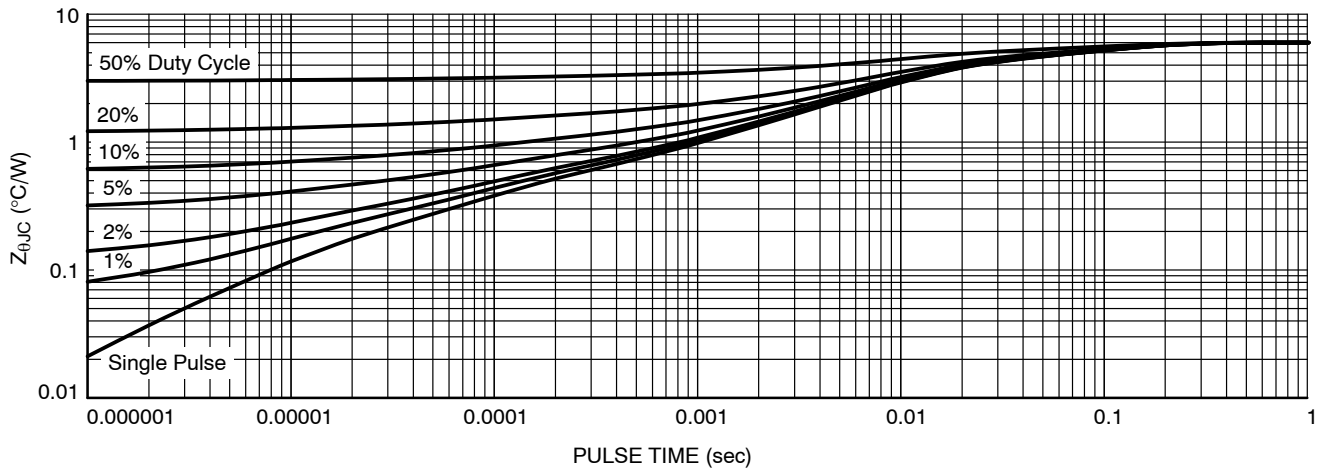
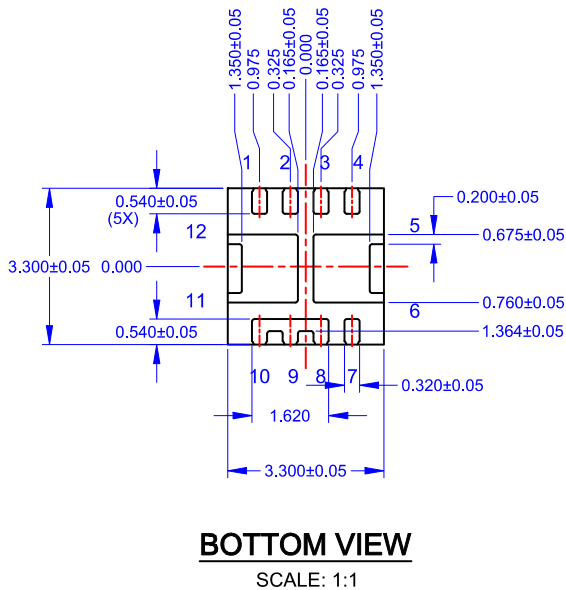
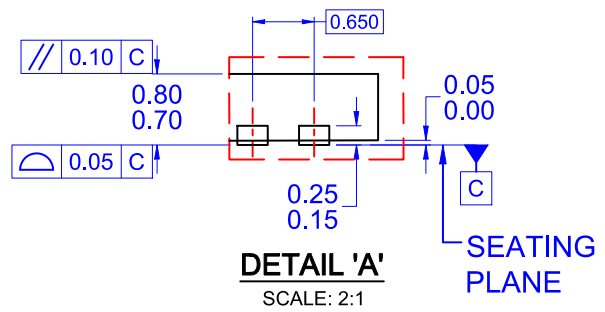
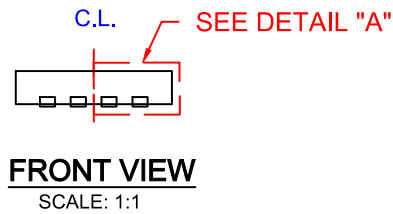
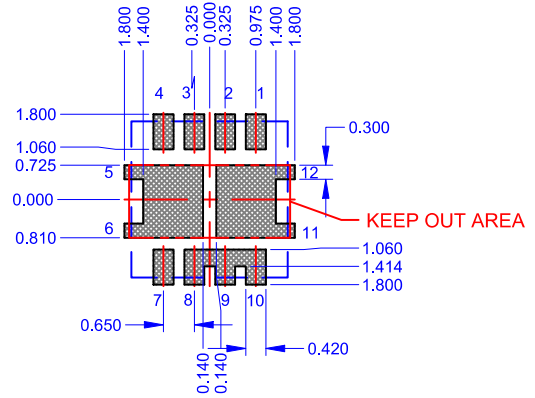
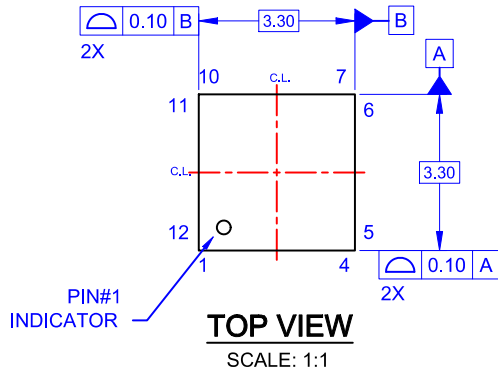


Figure 26. Thermal Characteristics

NTTFD4D1N03P1E

PACKAGE DIMENSIONS

WQFN12 3.3X3.3, 0.65P
CASE 510CJ
ISSUE O



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-220, VARIATION WECC-1
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.

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