NR421A

DATA SHEET

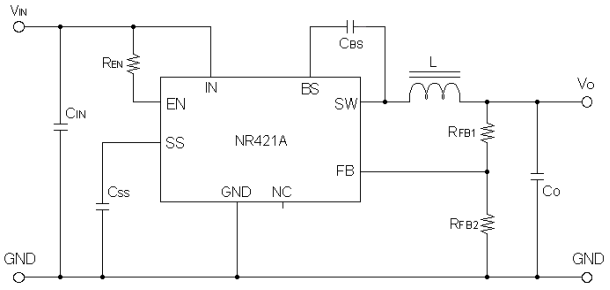
General Descriptions

The NR421A is Synchronous Rectification buck regulator ICs integrates PowerMOSFETs. With the current mode control, low ESR capacitors such as ceramic capacitors can be used. It has achieved a high efficiency by the synchronous rectification system. The ICs have protection functions such as Over-Current Protection (OCP), Under-Voltage Lockout (UVLO) and Thermal Shutdown (TSD). Soft starting time can be set up by selecting an external capacitor value. The ON/OFF pin (EN Pin) turns the regulator ON/OFF. The NR421A is available in an 8-pin HSOP package with an exposed thermal pad on the back side.

Features & Benefits

- For excellent heat dissipation, HSOP8 package with the heat-slug is adopted.
- Current mode PWM control
- Up to 94% efficiency
- Stable with low ESR ceramic output capacitors
- Built-in protection function
  Drooping type Over Current Protection (OCP) with Auto-restart
  Thermal Shutdown (TSD) with Auto-restart
  Under Voltage Lockout(UVLO)
- By the internal Phase Compensation, external component count reduction
- Adjustable Soft-Start with an external capacitor
- Output ON/OFF function (Enable)

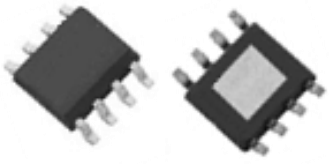
Basic Circuit Connection



NR421A

Package

- HSOP8
  Thermally enhanced 8-Pin package



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Electrical Characteristics

- Input voltage range V_{IN} = 4.5 to 18V
- Output voltage range V_O=0.8V to 14V
- Operation Frequency F_{SW}= 350kHz Fixed

Applications

- LCD-TV
- Blu-ray
- Power supply for digital consumer

CONTENTS

1. Electrical Characteristics

1.1 Absolute Maximum Ratings

- The polarity value for current specifies a sink as "+" and a source as "−", referencing the IC.
- Ta=25°C,unless otherwise noted.

Parameter		Symbol	Ratings	Units	Conditions
DC input voltage		V_{IN}	−0.3 to 20	V	
BS terminal voltage		V_{BS}	−0.3 to 25.5	V	
BS to SW voltage		V_{BS-SW}	−0.3 to 6.0	V	DC
			7.5	V	* Pulse Width Limitation ≦30[ns]
SW terminal voltage		V_{SW}	−1 to 20	V	DC
			−2 to 20		* Pulse Width Limitation ≦100[ns]
			−4 to 20		* Pulse Width Limitation ≦10[ns]
FB terminal voltage		V_{FB}	−0.3 to 5.5	V	
EN terminal voltage		V_{EN}	−0.3 to20	V	
SS terminal voltage		V_{SS}	−0.3 to 3.5	V	
Power dissipation	(1)	P_D	2.97	W	Glass-epoxy board mounting in a 40×40mm. * The implementation in our Demo- Board, Tj=150°C
Junction temperature	(2)	T_J	−40 to 150	°C	
Storage temperature		T_{stg}	−40 to 150	°C	
Thermal resistance (Junction to GND Lead)		θ_{JP}	11	°C /W	
Thermal resistance (Junction to Ambient air)		θ_{JA}	42	°C /W	Glass-epoxy board mounting in a 40×40mm. * The implementation in our Demo- Board.

(1) Limited by thermal shutdown.
(2) The temperature detection of thermal shutdown is about 165°C.

1.2 Recommended Operating Conditions

Operating IC in recommended operating conditions is required for normal operating of circuit functions shown in the electrical characteristics.

Parameter		Symbol	Ratings		Units	Conditions
			MIN	MAX		
DC input voltage range	(3)	V_{IN}	V_O+3	18	V	
DC output voltage range		V_O	0.8	14	V	
DC output current range	(4) (5)	I_O	0	3.0	A	
Operating ambient temperature	(5)	Ta	−40	85	°C	

(3) The minimum value of input voltage is taken as the larger one of either 4.5V or V_O +3V.
In the case of V_{IN}=V_O +1 to V_O +3V , it is set to I_O = Max. 2A.
(4) Refer to typical Application Circuit (Fig3-1).
(5) To be used within the allowable package power dissipation characteristics (Fig4-1).

1.3 Electrical Characteristics

- The polarity value for current specifies a sink as "+" and a source as "−", referencing the IC.
- Ta=25°C,unless otherwise noted.

Parameter			Symbol	Ratings			Units	Test conditions
				MIN	TYP	MAX		
Reference voltage			V_{REF}	0.784	0.800	0.816	V	V_{IN} = 12V, I_o = 0.1A
Reference voltage temperature coefficient			$\triangle V_{REF}/\triangle T$	—	±0.05	—	mV/°C	V_{IN} = 12V, I_o = 1.0A -40°C to +85°C
Switching frequency			fsw	280	350	420	kHz	V_{IN}=12V, Vo=3.3V, I_O=1A
Line regulation		(5)	V_{Line}	—	50	—	mV	V_{IN}= 6.3V to 18V, Vo=3.3V, I_O=1A
Load regulation		(5)	V_{Load}	—	50	—	mV	V_{IN}=12V, Vo=3.3V, I_O=0.1A to 3.0A
Over current protection threshold			I_S	3.1		6.0	A	V_{IN}=12V, Vo=3.3V
Supply Current			I_{IN}	—	6	—	mA	V_{IN}= 12V, EN: 10kΩ Pull up toV_{IN})
Shutdown Supply Current			$I_{IN(off)}$	0		10	μA	V_{IN}=12V, V_{EN}=0V, Io=0A
Input UVLO Threshold			Vuvlo		4	4.4	V	V_{IN} Rising
SS terminal	Source current at low level voltage		I_{SS}	6	10	14	μA	V_{SS}=0V, V_{IN}=12V
	Open voltage		V_{SSH}	—	3.0	—	V	V_{IN}=12V
EN terminal	Sink current		I_{EN}	—	50	100	μA	V_{EN}= 10V
	Threshold voltage		V_{EN}	0.7	1.4	2.1	V	V_{IN}=12V
Maximum ON duty		(6)	D_{MAX}	—	90	—	%	V_{IN}=12V
Minimum ON time		(6)	$T_{ON(MIN)}$	—	150	—	nsec	V_{IN}=12V
Thermal shutdown threshold temperature		(6)	TSD	151	165	—	°C	V_{IN}=12V
Thermal shutdown restart temperature hysteresis		(6)	TSD_hys	—	20	—	°C	V_{IN}=12V
On-resistance of Hi-side MOSFET		(6)	RonH	—	110	—	mΩ	V_{IN}=12V
On-resistance of Lo-side MOSFET		(6)	RonL	—	85	—	mΩ	V_{IN}=12V

(6) Guaranteed by design,not tested.

2. Block Diagram & Pin Functions

2.1 Block Diagram

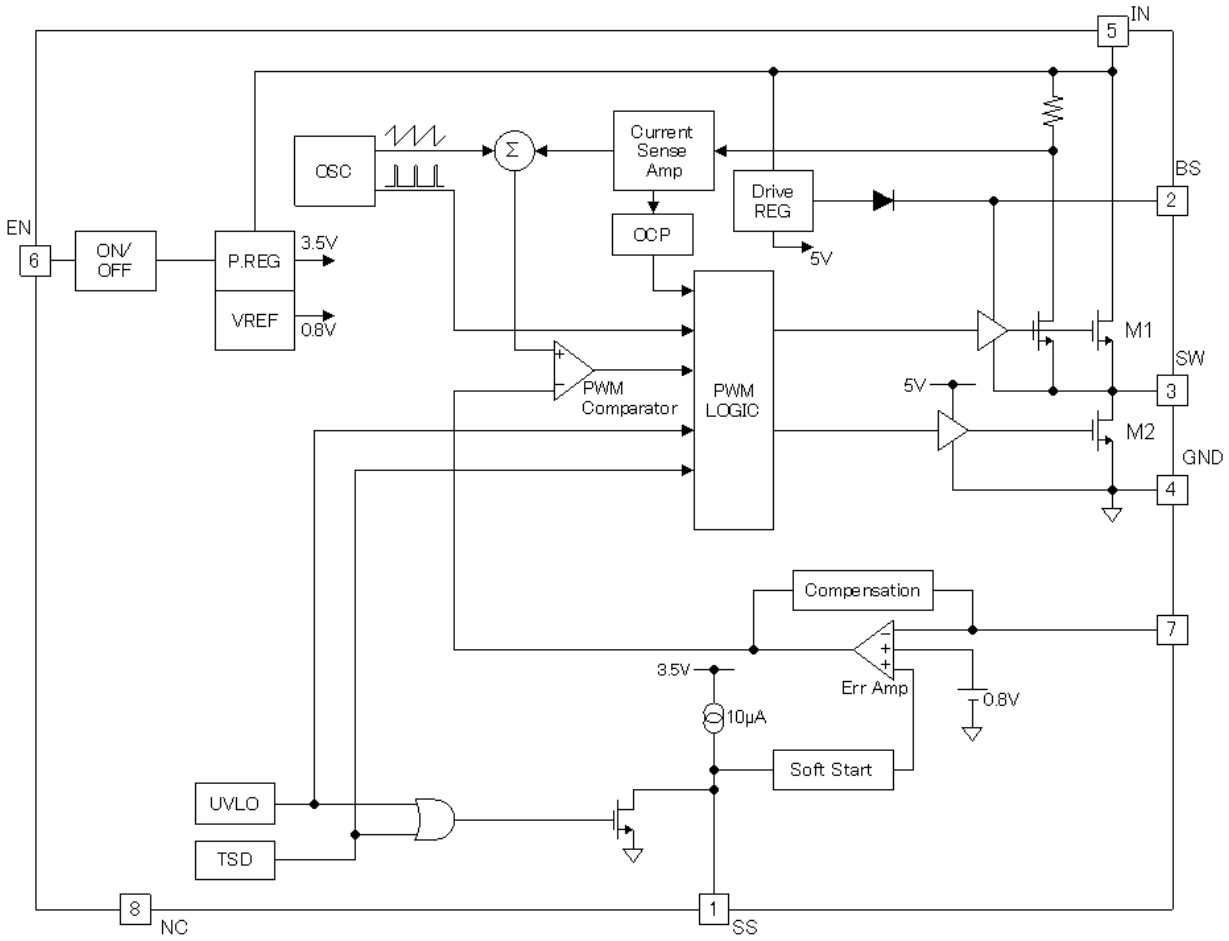


Fig. 2-1 NR421A Block diagram

2.2 Pin Asignments & Functions

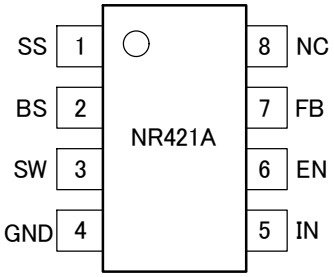


Fig. 2-2 Pin Assignments

Pin No.	Symbol	Functions
1	SS	Soft-Start control input. To set the soft-start period, connect to a capacitor between GND.
2	BS	Hi-side Boost Input. A BS terminal supplies the drive power of the internal PowerMOSFET. Connect a capacitor between the SW terminal and the BS terminal.
3	SW	Power switching output. SW supplies power to the output. Connect the LC filter from SW to the output.
4	GND	Ground. *Connect the exposed pad of back side to Pin No.4.
5	IN	Power input. V_{IN} supplies the power to the internal control circuit and the powerMOSFET.
6	EN	Enable control input. By setting the EN pin to high level, the regulator turns on. By setting to low level, it turns off.
7	FB	Feedback input Pin for compare Reference Voltage. The feedback threshold voltage (V_{REF}) is 0.8V. To set the output voltage, the FB pin requires to connect voltage divider resistor R_{FB1} and R_{FB2}.
8	NC	No connection

3. Typical Application Circuit

Standard connection is shown in Fig3-1.

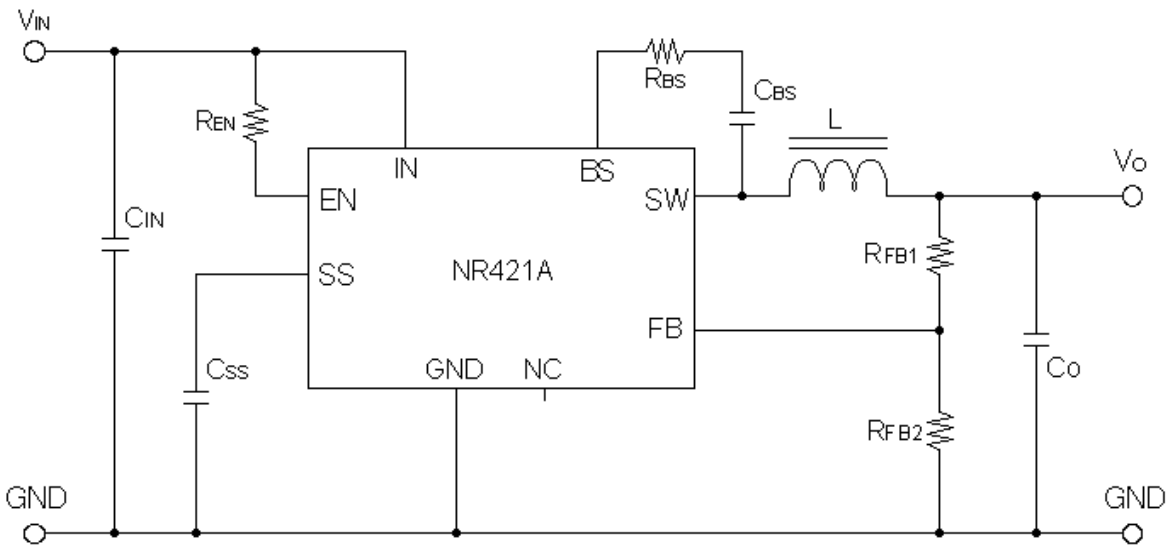


Fig. 3-1 NR421A Standard connection

C_{IN}: 2×10μF / 25V
C_O: 2×22μF / 16V
C_{BS}: 0.1μF
C_{SS}: 0.1μF
R_{EN}:100kΩ
L: 10μH
R_{BS}:≦22Ω

*As for the circuit diagram of the Demo-Board, please refer to the Demo-Board circuit diagram of the "8.2.2 mounting board pattern example" section.

4. Allowable package power dissipation

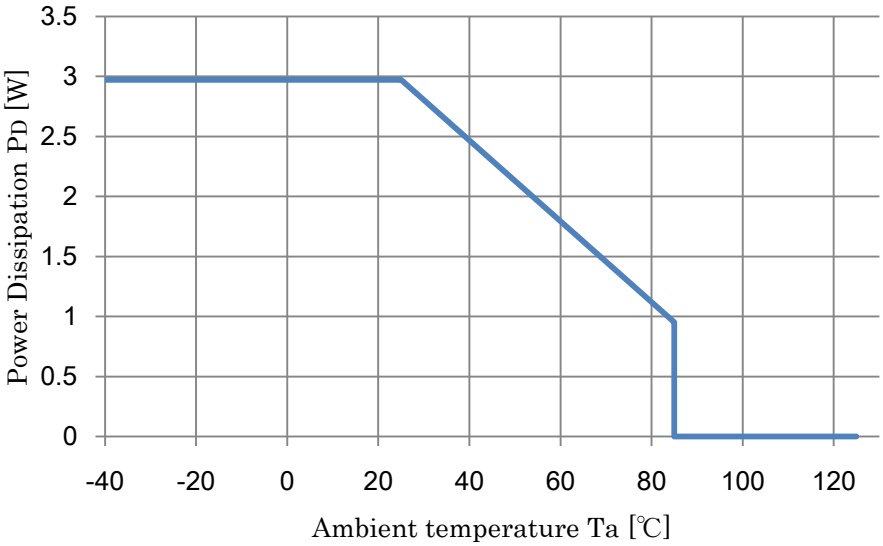


Fig. 4-1 Allowable package powe disspation of NR421A

Notes:

1) Because the Fig4-1 is defined in "PD=2.97[W]" at "Tj=125 [°C]", please keep enough margin when you use.
2) With glass-epoxy PCB: Size=40×40mm, Copper foil area=25×25mm.
3) Losses can be calculated by the following equation. In addition, efficiency ηx will vary depending on the conditions of the input voltage, output current. By measuring the ηx in the actual operation, assigns a numerical value to the equation (1) , as a ηx remain of percent display.

$$P_D = Vo \times Io\left(\frac{100}{\eta x} - 1\right) - \{Io^2 \times L(DCR)\} \quad (1)$$

Main sources of heat generation are an inductor which is flowing the load current , and the IC which has the PowerMOSFET and the control circuit.
By subtracting the steady loss of the inductor from the overall efficiency, the loss of the IC is calculated by equation (1).

If following situations are ...V_O = 5[V], I_O = 3[A] continuous,
the inductor DCR = 40[mΩ],
the Loss of IC when the overall efficiency is 94 percent,
it will be 0.597[W] from the equation (1).

V_O: Output voltage

V_{IN}: Input voltage

I_O: Output current

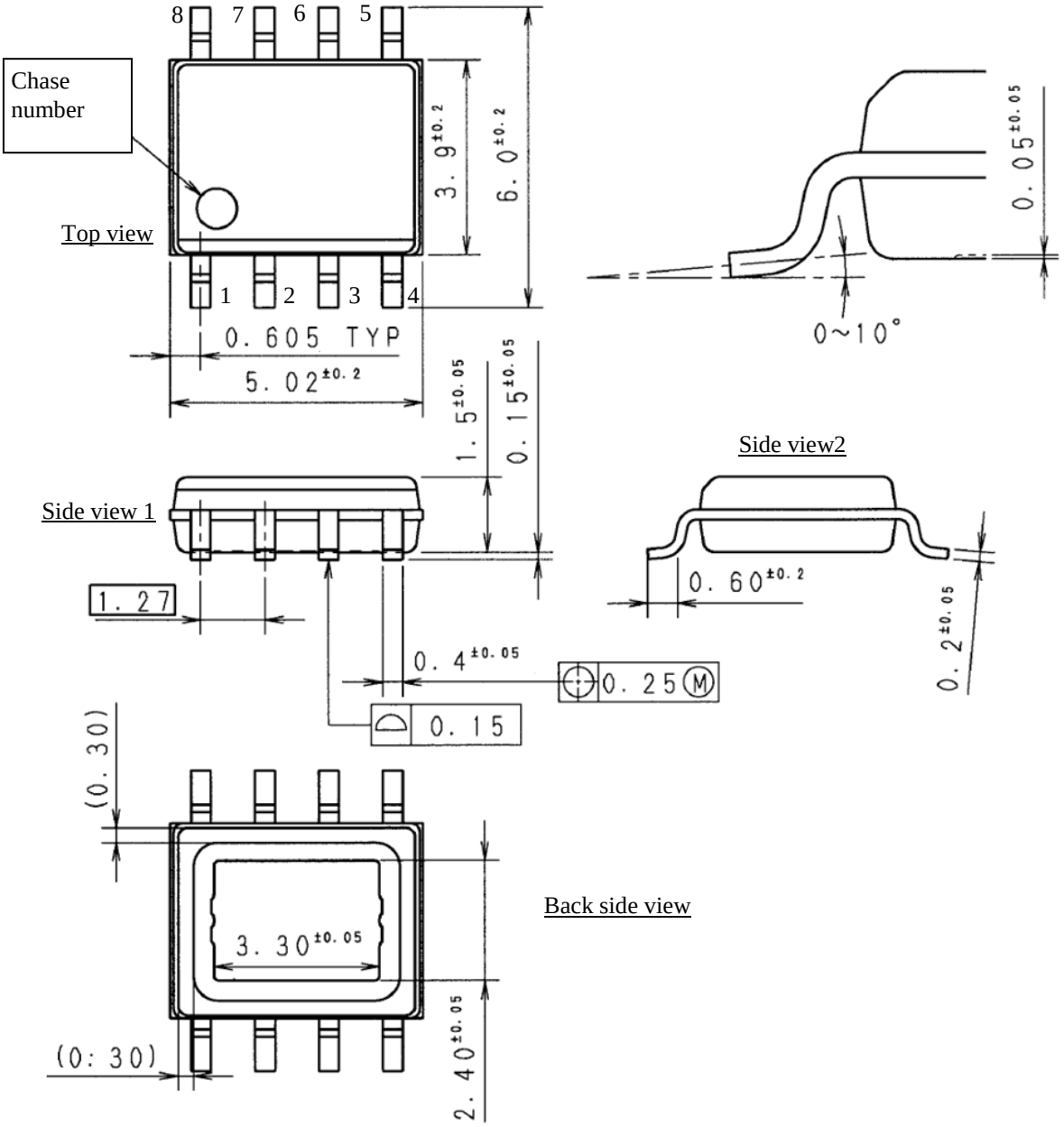
ηx: Efficiency(%)

L(DCR) : DC serial resistance of inductor (Ω)

5. Package Outline

5.1 Outline, Size

- HSOP8 Package



Notes:
1) Dimension is in millimeters (mm)
2) Drawing is not to scale.

Fig. 5-1 HSOP8 Package outline

6. Marking

As for the Marking, the product name and lot number, those are laser marking to mold package surface.

*1. Product name
*2. Lot number (3 digits)
The 1st letter : Last one digit of the year (Y)
The 2nd letter : manufacturing Month (M)
Jan - Sep : 1 – 9
Oct : O
Nov : N
Dec : D
The 3rd letter : manufacturing Week (W)
First week - Fifth week : 1 - 5
*3. Our control number (4 digits)

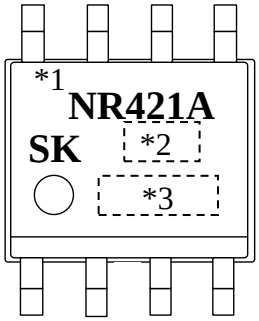


Fig. 6-1 Marking Specification

7. Operational Descriptions

The Characteristic value of, unless otherwise noted, it writes the TYP value in accordance with the NR421A specifications.

7.1 PWM(Pulse Width Modulation) Output Control

The NR421A series consist of three blocks; two feedback loops (voltage control and current control) and one slope compensation. The PWM is controlled with the current mode control by calculating the voltage feedback control, and the current feedback control and the slope compensation signals (Fig7-1). For the voltage feedback control, the output voltage feed back to the PWM control. The error amplifier compares the output voltage divided by resistors with the reference voltage V_{REF} = 0.8V. For the current feedback control, the inductor current feed back to the PWM control. The inductor current divided by Sense-MOSFET is detected with the current sense amplifier. To prevent sub-harmonic oscillations, which is characteristic in current mode control, the slope of current control is compensated.

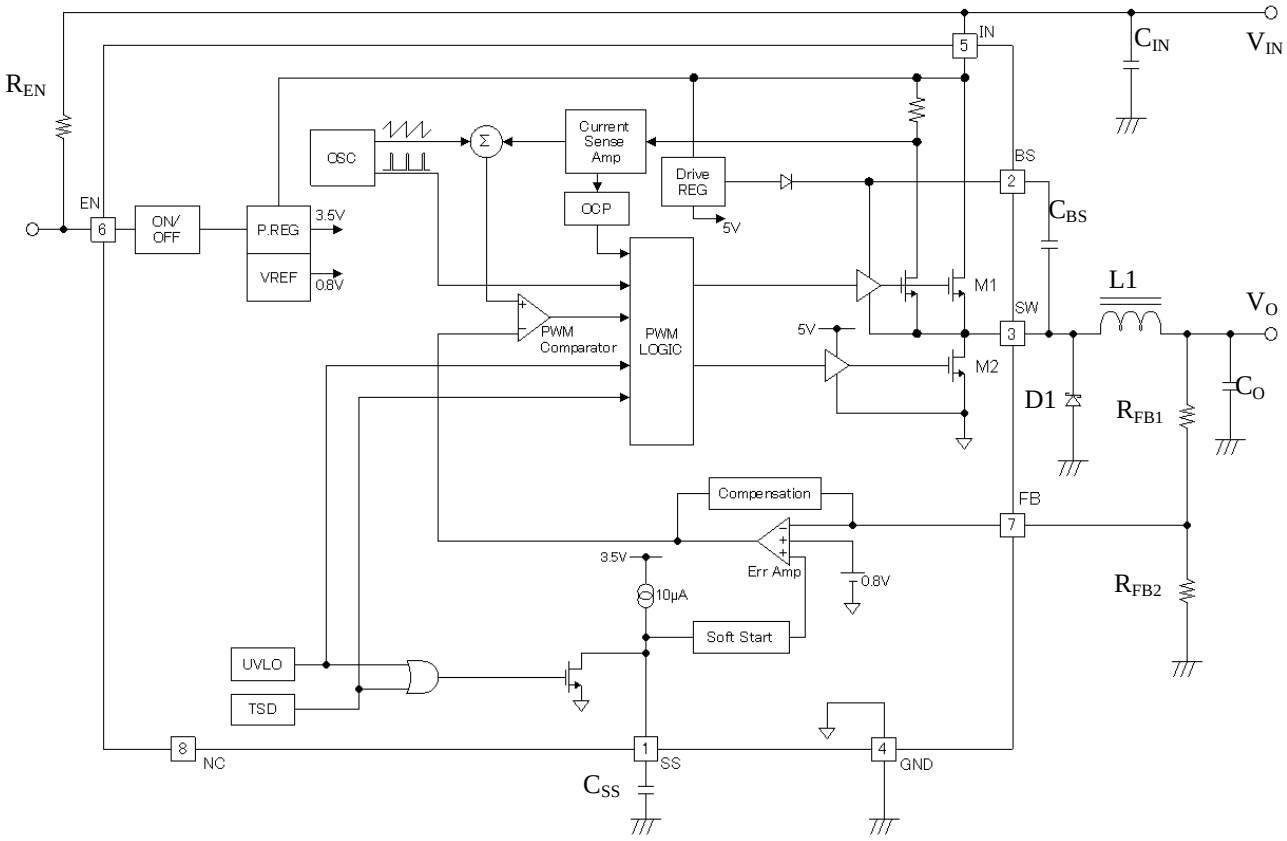


Fig. 7-1 Basic Structure of Chopper Type Regulator with PWM Control by Current Control

The NR421A series start the switching operation when UVLO is released, or EN or SS Pin voltage exceeds the threshold. Initially, it operates switching with minimum ON duty or maximum ON duty. The high-side switch (M1) is the switching MOSFET that supplies output power. At first, the low-side switch (M2) turns ON and charges the boost capacitor C10 that drives M1. When M1 is ON, as the inductor current is increased by applying voltage to SW Pin and the inductor, the output of inductor current sense amplifier is also increased. Sum of the current sense amplifier output and slope compensation signal is compared with the error amplifier output. When the summed signal exceeds the error amplifier (Error Amp.) output voltage, the current comparator output becomes “High” and the RS flip-flop is reset. When M1 turns OFF and M2 turns ON, the regenerative current flows through M2. In the case that an external SBD (D1) is connected, the current also flows through D1.

In NR421A series, the set signal is generated in each cycle and RS flip-flop is set. In the case that the summed signal does not exceed the error amplifier (Error Amp.) output voltage, RS flip-flop is reset without fail by the signal from OFF duty circuit.

7.2 Enable Function (EN:Remote ON / OFF operation of the Regulator)

In the condition that the EN terminal is connected to the IN terminal, when the input voltage V_{IN} is increased beyond 4V(typ.), the UVLO is released and started the switching operation. And, in the condition that the input voltage V_{IN} is applied beyond 6V(typ.), when the EN terminal voltage exceeds 1.4V (typ.), it is started the switching operation.

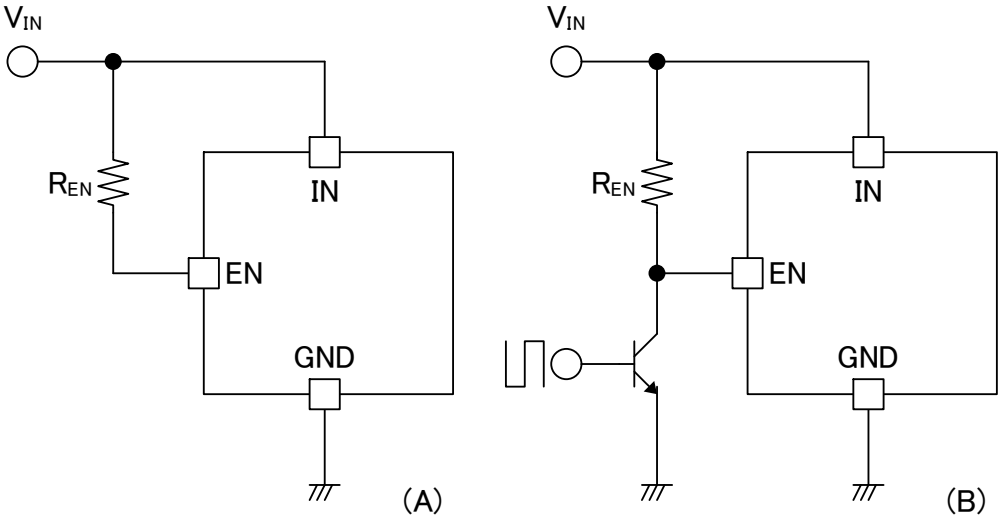


Fig. 7-2 Remote ON/OFF operation by EN terminal

The Fig7-2(B) is the option of the "Remote ON/OFF control" by using the EN terminal. By using switch such as Open-collector and, by removing the EN terminal voltage V_{EN} to GND level (Low), it is possible to turn OFF. In case of without ON / OFF operation by external signal, please use the Fig7-2 (A) connection. It is started by the applying of the V_{IN}, and it is stopped by shut-off of the V_{IN}. R_{EN1} is recommended 100[kΩ].

7.3 Soft-start Function (SS)

By connecting a capacitor between the SS terminal and the GND terminal, when the input voltage is supplied to the IC, the soft-start function will be effective.The output voltage (Vo) is ramped up by the charging voltage level of Css. Because the internal constant current source I_{SS} supplied from the SS terminal is 10 μA, the soft-start period depends on the charging time constant of the C_{SS}. When the charging of C_{SS} is started by the constant current I_{SS}, the SS terminal voltage V_{SS} is linearly increased. The soft-start period is the time that the V_{SS} passes between the "Soft-start start threshold voltage V_{SS1}(=0.9V)" and "Soft-start completion threshold voltage V_{SS2}(=1.79V)". During the Soft-start, the rise-time is controlled by controlling the OFF period of PWM control. The rise time $t_{\_SS}$ and the delay time $t_{\_delay}$ are calculated in the following equations…

$$t_{SS} = C_{SS} \times (V_{SS2} - V_{SS1}) / I_{SS} \quad (2)$$

Note: V_{SS1}(=0.9V) ≦V_{SS}≦ V_{SS2} (=1.79V), I_{SS}=10μA

$$t_{\_delay} = C_{SS} \times V_{SS1} / I_{SS} \quad (3)$$

Note: the period of 0V ≦V_{SS}＜V_{SS1} (0.9V), I_{SS}=10μA

The rise time of the output voltage Vo is " $t_{\_delay}$ + t_{SS} ".

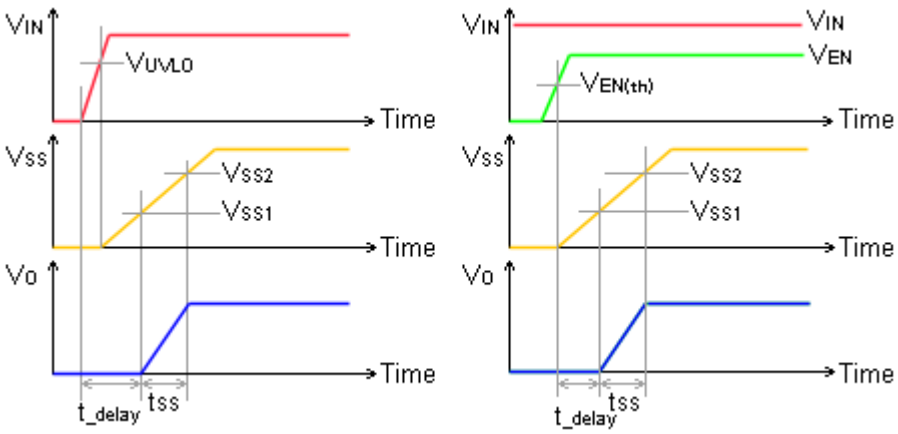


Fig. 7-3 The timing chart of the Soft-start in the normal startup

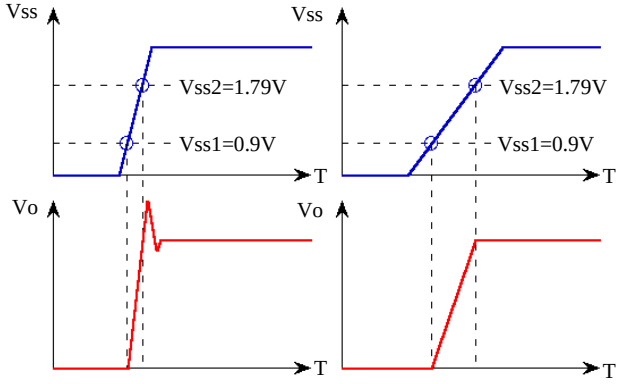


Fig. 7-4 The occurrence of the overshoot on Vo rising waveform

Adjust the capacitance of C_{SS} so that the excessive overshoot may not occur on the Rising-Waveform of the output voltage Vo at the start-up. The overshoot occurs when tss is short.If the soft-start is finished before the constant voltage control follows Vo rising speed,it may become such waveform of Fig7-4. When a capacitance of the C_{SS} is increased, though the overshoot will not occur , please understand that the start-up time is longer. In actual operation, please confirm the Rising-waveform, and adjust the capacitance of the C_{SS}.

Note: About C_{SS} discharge to restart
It is explained about discharging of the C_{SS} capacitor when this IC is restarted such as ON/OFF operation in the EN terminal. When it was restarted, there is a case where the voltage is remaining in the soft-start capacitor C_{SS}. In this IC, it has adopted the forced discharge sequence as shown in the Fig7-5. By the internal impedance, after once discharging the SS terminal voltage to 0.9V or less, and then resume the soft-start.
Discharge of the capacitor Css, it is discharged by the internal impedance 6.1k Ω (typ) in the IC.

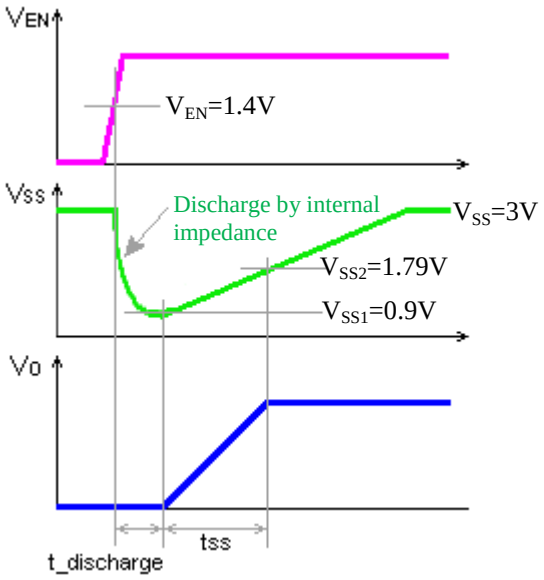


Fig. 7-5 Discharge of the capacitor Css at restart

Under the condition that the voltage is remaining in the Css, after the ON-signal is inputted, it takes the time of "t_discharge+tss" until Vo-waveform rise and stabilize. The soft-start capacitor Css has been charged to the internal regulator voltage 3V.
It considers the discharge from the condition that the soft-start capacitor C_{SS} has been charged up to 3V in the steady condition. The SS terminal voltage V_{SS} at optional time t after the start of discharge will be calculated by the equation (4). For the time t_discharge that the V_{SS} is discharged to 0.9V from 3V, it can be calculated by equation (5).

$$V_{SS}[V] = 3[V] \times EXP\left(\frac{-t[s]}{C_{SS}[F] \times 6.1[k\Omega]}\right) \quad (4)$$

$$t_{\_discharge}[s] = -C_{SS}[F] \times 6.1[k\Omega] \times \ln\left(\frac{0.9[V]}{3[V]}\right) \quad (5)$$

When there is a mode for continuous "ON/OFF" operation, consider delay by discharging of the C_{SS}.

7.4 Over Current Protection (OCP)

The OCP characteristic example is shown in Fig7-6. The NR421A integrates the drooping type over-current protection circuit. The peak current of switching transistor is detected. When the peak current exceeds rated value, the over-current protection limits the current by forcibly shortening the ON time of transistor and decreasing the output voltage. It prevents the current increment at low output voltage by decreasing the switching frequency (F_{DOWN} Mode), if the output voltage drops lower (The FB terminal voltage decreases to 0.57V from 0.8V). When the over-current state is released, the output voltage automatically recovers.

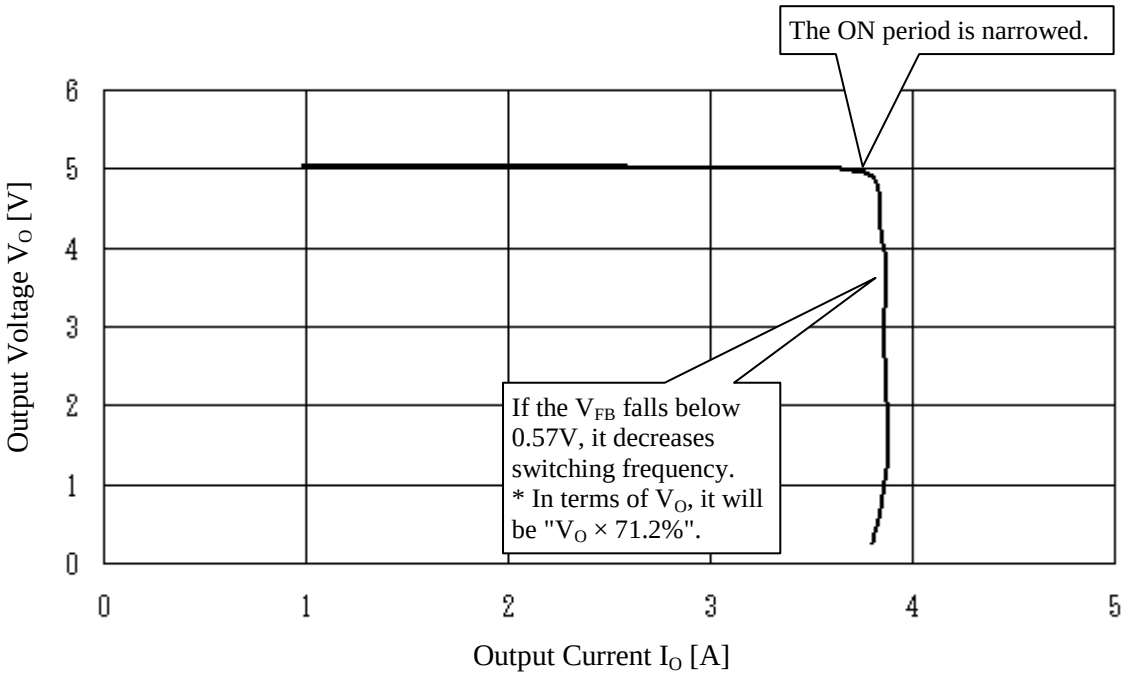


Fig. 7-6 The OCP characteristic example

7.5 Thermal Shutdown (TSD)

The thermal shutdown circuit detects the IC junction temperature. When the junction temperature exceeds the rated value (around 165°C), it shuts-down the output transistor and turns the output OFF. If the junction temperature falls below the thermal shutdown rated value by around 20°C, the operation returns automatically.

* (Thermal Shutdown Characteristics)

Notes

The circuit protects the IC against temporary heat generation. It does not guarantee the operation including reliabilities under the continuous heat generation conditions, such as short circuit for a long time.

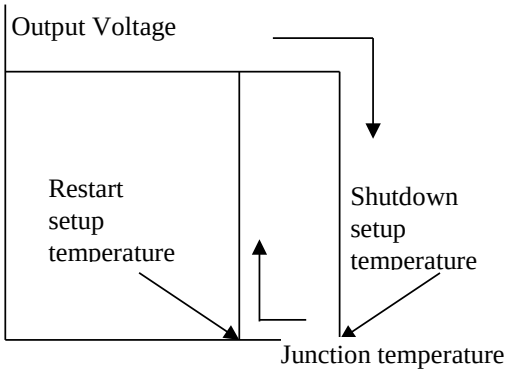


Fig. 7-7 TSD Operation

8. Design Notes

8.1 External Components

All components are required for matching to the condition of use.

8.1.1 Inductor L1

The Inductor is one of the most important components in the Buck regulators. In order to maintain the stabilized regulator operation, the Inductor should be carefully selected so it must not saturate or overheat excessively at any conditions. Please select an inductor with care to 8 items listed below.

- It is for switching regulator use only

  Because the coil for the noise filter (For EMI Countermeasure) has large loss and large heat generation, please do not use.

- Avoidance of sub-harmonic oscillation

  Under the peak detection current control, when the control Duty is more than 0.5 in use conditions, the inductor current may fluctuate at a frequency that is an integer multiple of switching operation frequency. This phenomenon is the known as sub-harmonic oscillation and this phenomenon theoretically occurs in the peak detection current control mode. In order to stabilize the operation, although the inductor current compensation is made internally, the inductance corresponding to the output voltage should be selected as an application. Specifically, for slope compensation amount is fixed in the IC, it is necessary to moderate the slope of the inductor current. The ripple portion of Inductor current ΔI_L and the peak current IL_P are calculated from the following equations:

$$\Delta I_L = \frac{(V_{IN} - V_O) \times V_O}{L \times V_{IN} \times F_{SW}} \quad (6)$$

$$IL_P = \frac{\Delta I_L}{2} + I_O \quad (7)$$

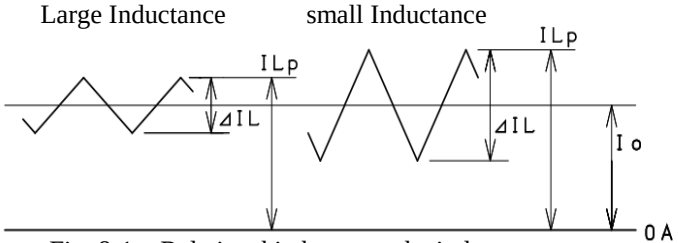


Fig. 8-1 Relationship between the inductance and ripple current ΔI_L

According to the equations, if the inductance of the inductor L is small, both ΔI_L and IL_P is increased. Consequently, the inductor current becomes very steep if inductance is too small, so that the operation of the converter might become unstable. It is necessary to take care of an inductance decrease due to magnetic saturation such as in overload and load shortage. To prevent subharmonic oscillation, specify the condition of the slope of the inductor current by referring to Table8-1.

Table. 8-1 Condition of "D≧0.5"

V_{IN}(V)	Vo(V)	Duty D	$T_{ON(MAX)}$ (μS)	Slope of the inductor current K(A/μS)	ΔI_L(A)	Necessary inductance (μH)Typ
18	14	0.78	2.777	0.178	0.494	22.48
18	12	0.67	2.380	0.311	0.740	19.30
18	10	0.56	1.983	0.498	0.988	16.07
15	12	0.80	2.856	0.156	0.446	19.24
12	9	0.75	2.678	0.207	0.554	14.50
10	7	0.70	2.499	0.267	0.667	11.24
9	6	0.67	2.380	0.311	0.740	9.65
9	5	0.56	1.983	0.498	0.988	8.04
8	5	0.63	2.231	0.373	0.832	8.05

* As for as necessary inductance, select the same value or larger value in Table8-1.

For Table 8-1, K is the specified value. It is recommended to below this value. For any values other than the ones combined in the Table8-1, please consider the values close to those ones. It is the combination under the condition of "VIN≧Vo+3V" in the specification. Table8-1 has been calculated by the following equation.

$$\text{Duty D} = \frac{V_O}{V_{IN}} \quad (8)$$

$$T_{ON(MAX)} = \text{Duty D} \times \left(\frac{1}{F_{SW(MIN)}}\right) \quad (9)$$

※$F_{SW(MIN)}$: This is the lower limit of the switching frequency. Please refer to the electrical characteristics list.

$$\Delta I_L = T_{ON(MAX)} \times K \quad (10)$$

∴ Inductance L of the inductor can be calculated by the following equation.

$$L \geqq \frac{(V_{IN} - V_O) \times V_O}{\Delta I_L \times V_{IN} \times F_{SW}} \quad (11)$$

- Inductance calculation in the normal state

Inductance value of the inductor in the conditions of "Duty <0.5", it will be calculated in the condition of "Duty D≧0.5" similarly to the above equation (11). ΔI_L/Io is the ratio of ΔI_L against the maximum load current Io to use. In case of "ΔIL/Io = 0.2", the necessary inductance is shown as the reference in Table8-2.

Table. 8-2 Condition of "D<0.5" and "ΔI_L/Io=0.2"

V_{IN}(V)	V_O(V)	Duty D	Io(A)	ΔI_L/Io (example)	ΔI_L(A)	Necessary inductance (μH)Typ
18	5	0.28	3	0.2	0.6	21.49
18	3.3	0.18	3	0.2	0.6	16.04
15	5	0.33	3	0.2	0.6	19.84
12	5	0.42	3	0.2	0.6	17.36
12	3.3	0.28	3	0.2	0.6	14.24
8	3.3	0.41	3	0.2	0.6	11.54
7	3.3	0.47	3	0.2	0.6	10.38
5	2	0.40	3	0.2	0.6	7.14
5	1.8	0.36	3	0.2	0.6	6.86
5	1.2	0.24	3	0.2	0.6	5.43

* As for as necessary inductance, select the same value or larger value in Table8-2.

$$\Delta I_L = I_O \times \left(\frac{\Delta I_L}{I_O}\right) \quad (12)$$

※In case of "$\Delta I_L/I_O$=0.3" and "I_O(Max)=3A", the setting of the ΔI_L is calculated at 0.3 × 3A = 0.9A.

- ΔI_L/Io Ratio

  When $\Delta I_L/I_O$ ratio is large, the nescessary inductance decreases. However, there is a matter of trade-off. For example, the output ripple voltage increases. When $\Delta I_L/I_O$ ratio is small, the necessary inductance increases, and the outline of the inductor becomes larger. Conventionally, $\Delta I_L/I_O$ ratio setting of 0.2 to 0.3, it is regarded as a setting for good cost performance .

- Wire diameter of the inductor

  When enlarging inductance, if the outline of the inductor is identical, number of winding increases and winding-wire's diameter becomes narrower. Because the Direct Current Resistance "DCR" increases , so that it becomes impossible to make a large current flow. But,when giving priority to Low-DCR, the core size becomes larger.

- DC superimposition characteristics

  Depending on the material or shape of the core, the inductance of inductor has DC superposition characteristics that decreases gradually by the flowing DC current. Be sure to confirm if the inductance value is significantly lower than the design value when making the maximum load current for practical use flow. Obtain the data of the DC superposition characteristics including graphs from the manufacturer of the coil to understand the characteristics of the Inductor used in advance. In doing so, important parameters are:
  1) Saturation point...At what amperes does magnetic saturation occur?
  2) Inductance fluctuation with the practical load current
  For example, for using it up to 3 A in the actual load Io, it can not use the Inductor which the saturation point is such as 2A. In addition, in spite of having an inductance of 10 μH at the no-load, please pay caution for the thing which has the characteristic that it decreases to such as 5μH by the superposition current of 1A.

- Less noise

  If the core is the open magnetic circuit type shaped like a drum, the magnetic flux passes outside the Inductor, so that the peripheral circuit might be damaged due to noise. Use the Inductor which has a core/structure of the low-leakage magnetic flux type. For details, consult the manufacturer of the Inductor.

- Heat generation

  In actuality, when using the coil for mounting the PCB, heat generation of the coil main body might be influenced by peripheral parts. In most cases, temperature rise of the coil includes the Inductor's own heat generation, and there are temperature limitations such as below:
  1) onboard(Cars) grade product: 150°C
  2) highly-reliable product: 125°C
  3) general product: 85-100°C

  Be sure to evaluate heat generation because temperature rise differs when the PCB on which the Inductor is mounted is designed differently.In general, Inductors with a smaller DCR value on the specification sheet have smaller loss.
  * Select the most appropriate one in consideration of the conditions of use, mounting, heat dissipation, etc.

8.1.2 Input Capacitor C_{IN}

Please use the ceramic capacitor to the input capacitor. It will lower the input impedance and it will contribute to the stable operation of the IC. The input capacitor C_{IN} must be arranged in as much as possible the shortest distance to between IN - GND of the IC. Even if there is a smoothing capacitor C_F in the transformer secondary side rectifying and smoothing circuit, please place the C_{IN} in the immediate vicinity of the IC. As a point of C_{IN} selection, it will include the following:

- Satisfaction of the withstand voltage and, that capacitance change with respect to the applied voltage is low
- The rate of capacity change in the ambient temperature range to be used is small
- Parts temperature which contains the heat-generation is must satisfy the specifications of the maximum operating temperature
- Its impedance Z is sufficiently low in the temperature conditions and using frequency

In the case of C_{IN}, if the source impedance of supplied VIN is infinitely low, the ripple current does not flow to C_{IN}. However, in the actual circuit, the power supply impedance is not that zero.If the power supply to the IC has been assumed that the almost performed from C_{IN}, it can be calculated approximately using equation (13).

$$I_{CINripple}[\text{A rms}] \approx 1.2 \times \frac{V_O[V]}{V_{IN}[V]} \times I_O[A] \qquad (13)$$

* Please query the product information of the capacitor manufacturer.
* Even in the ceramic capacitor, in case of the insertion parts having a lead, its impedance will be higher than surface-mounted type, therefore please be careful.
* In generally, in case of ceramic capacitors, the allowable ripple current is not included in the specification. But,because it has the equivalent series resistance ESR inside, the ceramic capacitor occurs slightly heat-generation by flowing ripple current. Therefore there is a need to comply with the maximum operating temperature containing the heat generation. In this case, also please consider the heat conduction from the heat generating parts of the surrounding.

Select the most suitable parts which has a margin in consideration of the use condition, the mounting condition, the radiation condition, and so on.

8.1.3 Output Capacitor C_O

In the current control mode, the feedback loop which detects the inductor current is added to the voltage control mode. The stable operation is achieved by adding inductor current to the feedback loop without considering the effect of secondary delay factor of LC filter. It is possible to reduce the capacitance of LC filter that is needed to make compensations for the secondary delay, and the stable operation is achieved even by using the low ESR capacitor (ceramic capacitor).

The output capacitor C_O comprises the LC low-pass filter with the Inductor L1 and works as the rectifying capacitor of switching output. The current equal to ripple portion ΔI_L of the Inductor current charges and discharges the output capacitor. The equivalent serial resistance ESR exists in the ceramics capacitor, and the voltage multiplied by ESR and ΔI_L becomes the output ripple voltage and it appears as $V_{Oripple}$.

$$V_{Oripple} = ESR(C_O)[\Omega] \times \Delta I_L[A] \qquad (14)$$

To suppress output ripple voltage $V_{O\ ripple}$ to any value, the required ESR conditions in the ceramic capacitor can be calculated by the following equation (15).

$$ESR(C_O)[\Omega] < \frac{V_{Oripple}[V]}{\Delta I_L[A]} \qquad (15)$$

The ripple current ICOripple of the output capacitor CO is represented by the following equation.

$$I_{COripple} = \frac{\Delta I_L[A]}{2\sqrt{3}} \quad (16)$$

Therefore, if the ripple portion of the inductor current ΔI_L is small, the output ripple voltage V_O ripple will be relatively small. Therefore, if the ripple portion of the inductor current ΔI_L is small, the output ripple voltage V_O ripple will be relatively small. If the ΔI_L is large, it may be necessary to reduce the ESR such as parallel connection of the ceramic capacitor.
In the same way as the input capacitor C_{IN}, as the point of C_O selection, it will include the following:

- Satisfaction of the withstand voltage and, that capacitance change with respect to the applied voltage is low
- The rate of capacity change in the ambient temperature range to be used is small
- Parts temperature which contains the heat-generation is must satisfy the specifications of the maximum operating temperature
- Its impedance Z is sufficiently low in the temperature conditions and using frequency

*Please query the product information of the capacitor manufacturer
*Even in the ceramic capacitor, in case of the insertion parts having a lead, its impedance will be higher than surface-mounted type, therefore please be careful.
*In generally, in case of ceramic capacitors, the allowable ripple current is not included in the specification. But,because it has the equivalent series resistance ESR inside, the ceramic capacitor occurs slightly heat-generation by flowing ripple current. Therefore there is a need to comply with the maximum operating temperature containing the heat generation. In this case, also please consider the heat conduction from the heat generating parts of the surrounding.

Select the most suitable parts which has a margin in consideration of the use condition, the mounting condition, the radiation condition, and so on.

8.1.4 Output Voltage Setup Resistor R_{FB1} & R_{FB2}

The FB terminal is the feedback detection terminal that controls the output voltage. To set the output voltage Vo, please input the divided-voltage by the voltage divider resistor to the FB terminal . Please connect voltage divider resistor R_{FB1} and R_{FB2} for detecting, as shown in the Fig8-2.
For the stable operation of the IC, R_{FB1} and R_{FB2} should be placed to the vicinity of the IC, please do routed between the R_{FB1} and V_O. If the PCB pattern of the FB terminal potential (0.8V) is routed long, please note that problems may occur such as abnormal-oscillation by the superimposition of the noise.

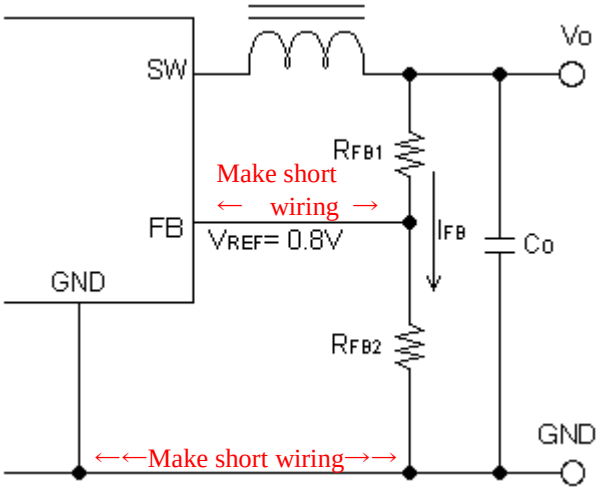


Fig. 8-2 Connection of FB terminal

As a minimum setting of the I_{FB}, it is recommended to about 0.2[mA]. The upper limit of the I_{FB} is not particularly. However, when larger I_{FB} are set up, please note that the power consumption will increase and the efficiency is decreased. R_{FB1}, R_{FB2} and the output voltage V_O can be calculated as following equation:

$$R_{FB2} = \frac{V_{REF}}{I_{FB}} = \frac{0.8[V]}{0.2[mA]} = 4[k\Omega] \qquad (17)$$

∴ Output voltage V_O is represented by equation (18).

$$V_O[V] = V_{REF}[V] \times \left(1 + \frac{R_{FB1}[\Omega]}{R_{FB2}[\Omega]}\right) \qquad (18)$$

Once you have determined the R_{FB2} from equation (17), then, using equation (19) that is obtained by modifiying equation (18), you can calculate the R_{FB1} corresponding to the V_O.

$$R_{FB1}[\Omega] = \frac{R_{FB2}[\Omega] \times (V_O[V] - V_{REF}[V])}{V_{REF}[V]} \quad (19)$$

When the calculation of the above-mentioned the voltage divider resistor, the resistance may not be able to meet the geometric series of E12 and the E24. In this case, such as the R_{FB1} in two series connection, please adjust the combined resistance value. In our Demo Board PCB, It has been designed as R_{FB1} = R4 + R5, R_{FB2} = R6. Please refer to the "Section 8.2.2 Mounting board pattern example".
(Notes)
*R_{FB2} is required to connect for the stable operation when set to V_O = 0.8V.
*Regarding the relation of input / output voltages, it is recommended that setting of the T_{ON} width in the switching waveform is more than 200[nsec].

When the T_{ON} reaches the minimum-ON-time $T_{ON(MIN)}$ in electrical characteristics, it becomes impossible to control narrower than $T_{ON(MIN)}$.Therefore, problems will occur to the stabilization of the output voltage V_O. The following shows the calculation method for confirmation.
One cycle T of the switching is represented by equation (20).

$$T[s] = \frac{1}{F_{SW}[Hz]} \quad (20)$$

In addition, the relationship between the duty cycle D in the switching and the ON-time T_{ON} is expressed in equation (21).

$$\text{Duty } D = \frac{V_O[V]}{V_{IN}[V]} = \frac{T_{ON}}{T} \quad (21)$$

In NR421A, the switching frequency is 350kHz(Typ).But, when the switching frequency is 420kHz as the Fsw(Max), the one cycle of the switching becomes the minimum. The one cycle of 420kHz can be calculated to be 2.38μs by equation (20). The duty D that can secure 200ns T_{ON} will be calculated by the equation (21).

$$\therefore \text{Duty } D = \frac{V_O[V]}{V_{IN}[V]} = \frac{200[ns]}{2.38[\mu s]} = 0.084$$

For example, in case of "V_{IN}=18V", the V_O setting condition that satisfies "D≧0.084" is calculated as follows:

$$\therefore V_O \geqq 18[V] \times 0.084 = 1.51[V]$$

Thus, in the above calculation example, it can not use for the V_O=0.8V. In this case, lower the V_{IN}, please use the setting that has margin for $T_{ON\ (MIN)}$. In the case of "V_O=0.8V", if it is condition of "V_{IN}<9.5V", it will be available.

8.1.5 External Bootstrap Diode for Low Input Voltage

Although the NR421A operates with input voltages lower than 6V, it is recommended to connect a diode between IN Pin and BS Pin in order to enhance the efficiency (Fig8-3). Alternatively an external voltage source can be connected through a diode to the BS Pin (Fig8-4).

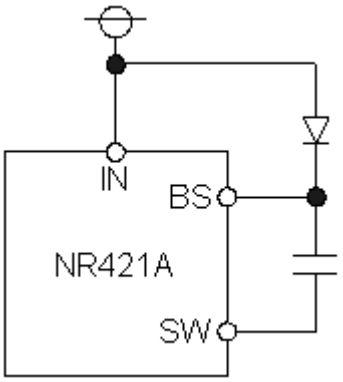


Fig. 8-3 Bootstrap Diode Connection 1

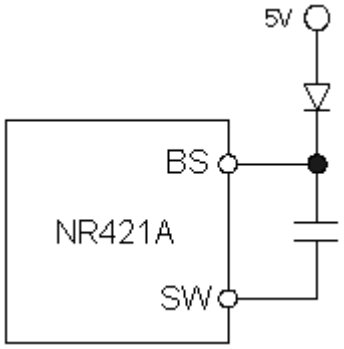


Fig. 8-4 Bootstrap Diode Connection 2

Notes;

1) Externally applied voltage is valid in the case of the conditions of less than 6V. The withstand voltage of the bootstrap diode, please use the SBD which has the same withstand voltage with BS-GND of the IC.
2) In the case of more than input voltage 6V, don't use the external power supply.

8.1.6 Free-wheeling diode D1 (option)

In general, in the case of a synchronous rectification system, the forward voltage drop V_F of the body diode in the low-side MOSFET is slightly larger than the properties of the Schottky Barrier Diode (SBD) single-item. When you insert a SBD which has sufficient low V_F characteristics between SW and GND, there is a possibility that the efficiency is improved. However, through a predetermined dead time, and after the turn-ON of the D-S in the low-side MOSFET, if the on-resistance R_{ON} is sufficiently low, the efficiency improvement effect of additional inserted SBD will be only during the dead time period. In this application, additional the free-wheeling diode D1 is merely option. If you use a D1, please set the V_{RM}(reverse-breakdown-voltage) of the D1 to more than SW-GND breakdown-voltage of the NR421A.

8.2 Pattern Design

High current paths in the circuit are marked as bold lines in the circuit diagram below. These paths are required for wide and short trace as possible. In addition, the pattern trace which is the signal system GND, and the pattern trace which the main circuit current flows, please to so that it does not become common impedance.

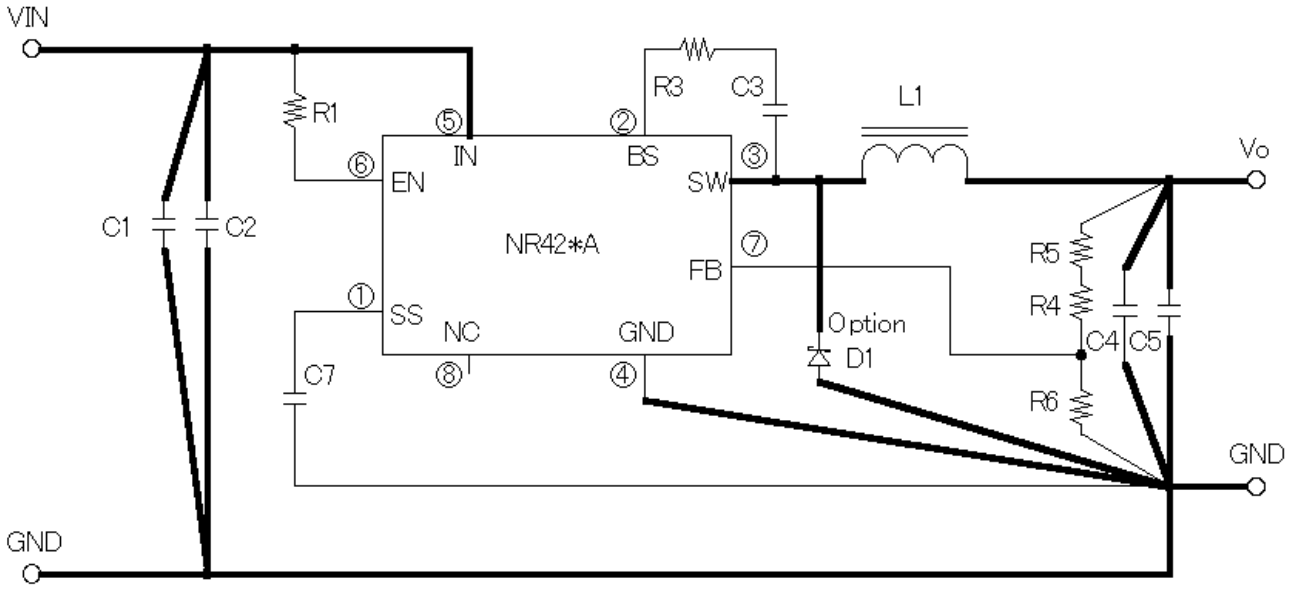
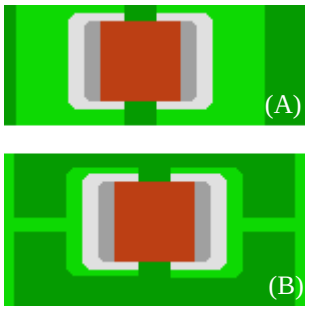


Fig. 8-5 Note points in the wiring pattern

8.2.1 Input / Output Capacitors(C_{IN},C_O)

The input capacitor C_{IN} and the output capacitor C_O are required to connect to the IC as short as possible.
In such cases as the secondary side of the switching power supply, when there is a filter capacitor on the input side in advance, though it is possible that it is included with a input capacitor for NR421A, in case of long distance between filter capacitor and NR421A , it is necessary to connect as “line-bypass-capacitor”,aside from the one for the filter.
The ripple current flows to the capacitor of input and output, you must make Low impedance and ESR.
When you design a circuit board, set to shorter length the pattern of input and output capacitor.
In the same way,consideration is necessary for route of the capacitor pattern.



(A)・・・Recommended Pattern
(B)・・・No good pattern example

Fig. 8-6 C_{IN},C_O pattern example

8.2.2 PCB Layout & Recommended Land Pattern

The pattern example of the printed circuit board for our Demo Board is shown in the following. (Double sided PCB)

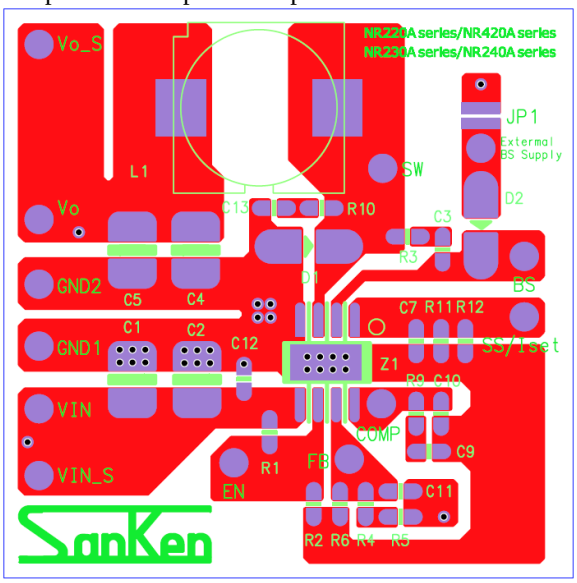


Fig. 8-7 Component mounting side (surface)

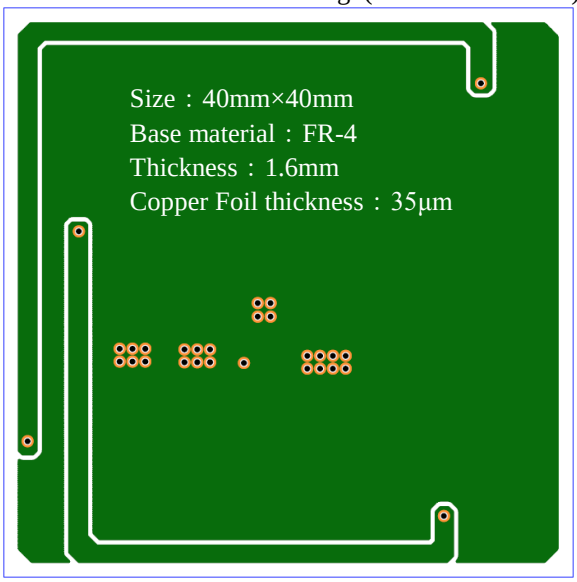


Fig. 8-8 Back side (see from surface)

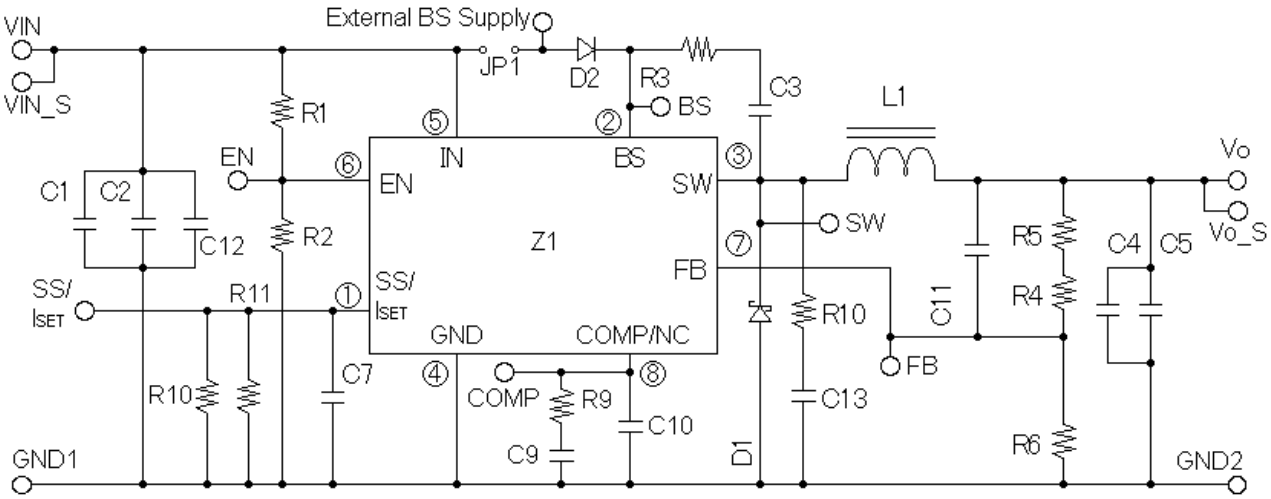


Fig. 8-9 NR220, NR230, NR240, NR420 Series Common Demo-board Circuit Diagram

(Reference)

C1,C2:10μF/50V, C3:0.1μF , C4,C5:22μF/25V, C7:0.1μF, R3≦22Ω, R1:100kΩ, R4:8.2kΩ, R5:4.3kΩ (Settings of R4 & R5, these are for the condition of V_O=3.3V.) R6:3.9kΩ, L1:10μH, JP1:Open

*Part number is in accordance with the silk of the Demo-board.

(Optional parts)

C11：Phase advancing capacitor (External Phase Compensation)･･･Experimental

C12：Bypass Capacitor for IN-GND･･･Experimental

C13：Snubber circuit capacitor･･･Experimental, R10：Snubber circuit resistor･･･Experimental

R2：Open (It is not used in the NR421A)

R3：Adjustment resistor for bootstrap capacitor discharge rate (For the turn-on speed adjustment)

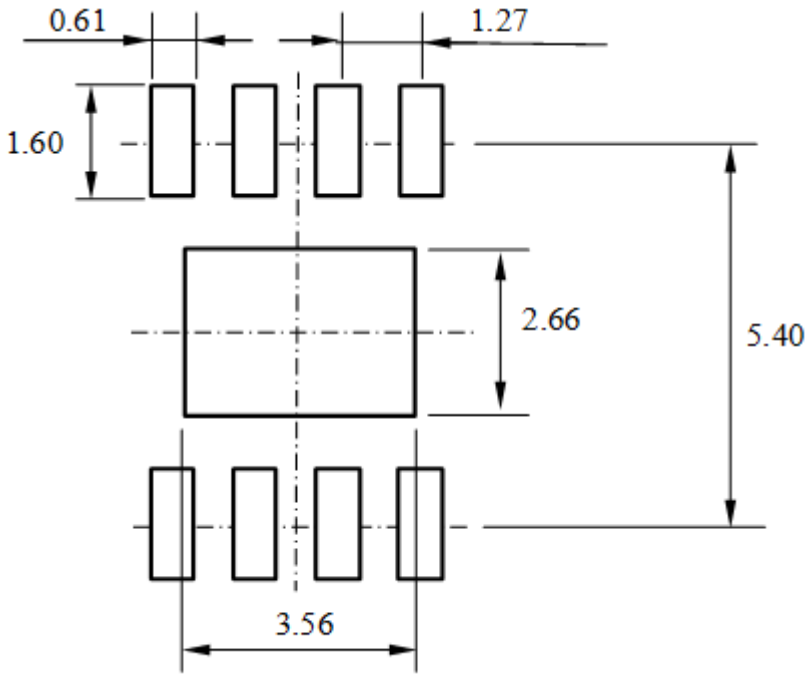
D1：The Schottky barrier diode for efficiency-improvement･･･Experimental

It is recommended the SBD which has smaller V_F than the internal parasitic diode in the Lo-side MOSFET.

D2：It is SBD for external power supply for BS terminal in the low V_{IN} condition･･･Experimental

C9,R9,C10：For External Phase Compensation Circuit (It is not used in the NR421A)

R10,R11：Overcurrent protection activation point adjustment resistor (It is not used in the NR421A)



Notes:
1) Dimension is in millimeters
2) Drawing is not to scale.

Fig. 8-10 Recommended Foot-printing Pattern

8.3 Applied Design

8.3.1 Spike Noise Reduction(1)

The addition of the BS serial resistor

The "turn-on switching speed" of the internal Power-MOSFET can be slowed down by inserting RBS (option) of the Fig8-11.It is tendency that Spike noise becomes small by reducing the switching-speed. Set up 22-ohm as an upper limit when you use R_{BS}.

*Attention

1) When the resistance value of R_{BS} is enlarged by mistake too much, the internal power-MOSFET becomes an under-drive,it may be damaged worst.

2) The "defective starting-up" is caused when the resistance value of R_{BS} is too big.

*The BS serial resistor R_{BS} is R3 in the Demonstration Board.

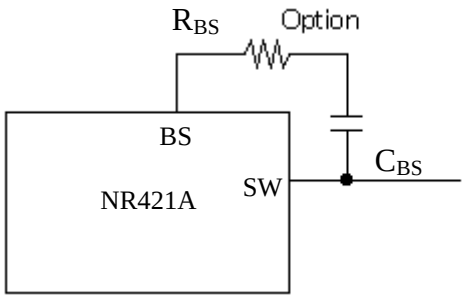


Fig. 8-11 The addition of the BS serial resistor

8.3.2 Spike Noise Reduction(2)

The addition of the Snubber circuit

By adding a resistor and capacitor (RC snubber) to the above countermeasures as shown in Fig8-12, It corrects the output waveform and the recovery time of the diode, it is possible to reduce the further spike noise. However, please note that this method will slightly reduce the efficiency.

* For observing the spike noise with an oscilloscope, the probe lead (GND) should be as short as possible and connected to the root of output capacitor. If the probe GND lead is too long, the lead may act like an antenna and the observed spike noise may be much higher and may not show the real values.

*The snubber circuit parts are C13 and R10.

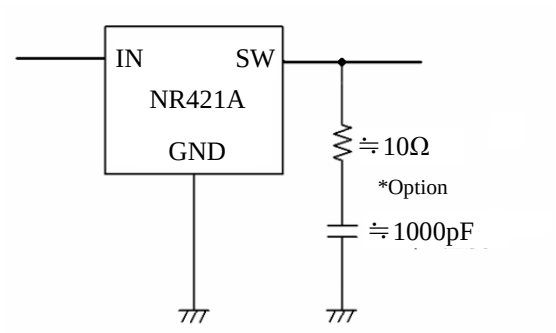


Fig. 8-12 The addition of the Snubber circuit

8.3.3 Attention about the insertion of the bead-core

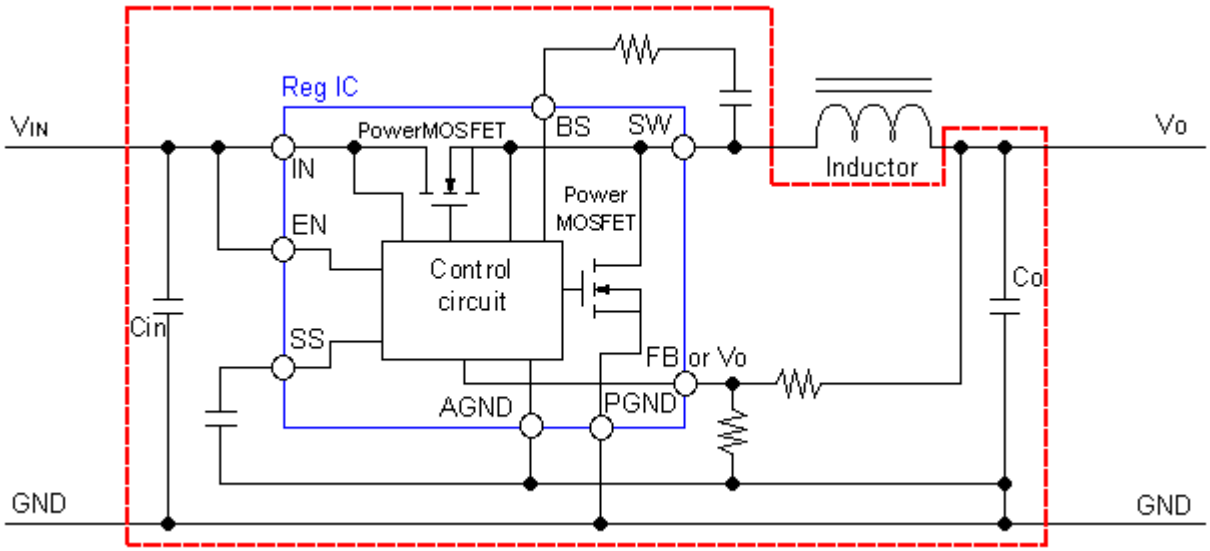


Fig. 8-13 Bead core insertion prohibited area

In the area surrounded by the red dotted line within the Fig8-13, don't insert the bead-core such as Ferrite-bead.
As for the pattern-design of printed-circuit-board, it is recommended that the parasitic-inductance of wiring-pattern is made small for the safety and the stability.
When bead-core was inserted, the inductance of the bead-core is added to parasitic-inductance of the wiring-pattern.
By this influence, the surge-voltage occurs often, or , GND of IC becomes unstable, and also, negative voltage occurs often.
Because of this, faulty operation occurs in the IC. The IC has the possibility of damage in the worst case.
About the Noise-reduction, fundamentally, Cope by "The addition of CR snubber circuit" and "The addition of BS serial resistor".

8.3.4 Reverse Bias Protection

A diode for reverse bias protection may be required between input and output in case the output voltage is expected to be higher than the input Pin voltage (a common case in battery charger applications).

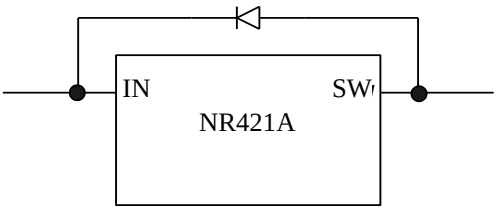


Fig. 8-14 Reverse bias protection diode

9. Typical characteristics (Ta=25°C)

1)Efficiency・Load Regulation

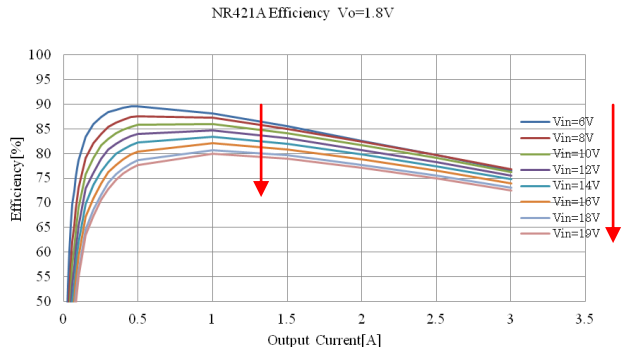


Fig. 9-1

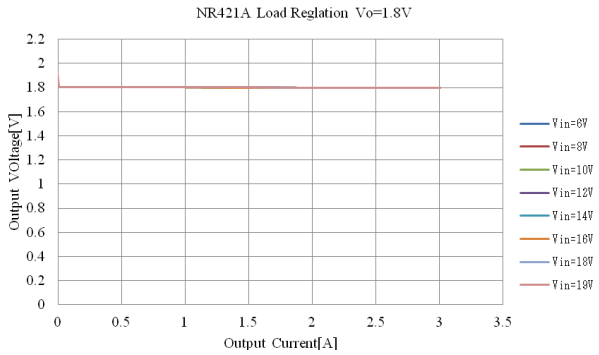


Fig. 9-5

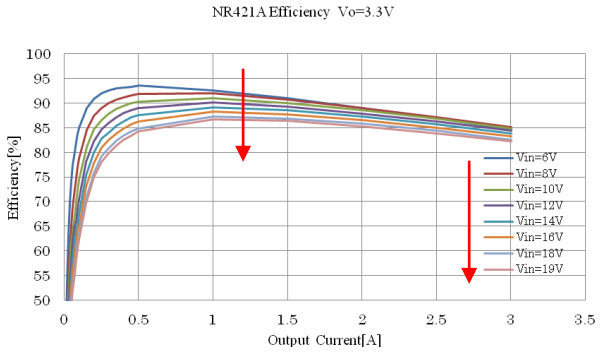


Fig. 9-2

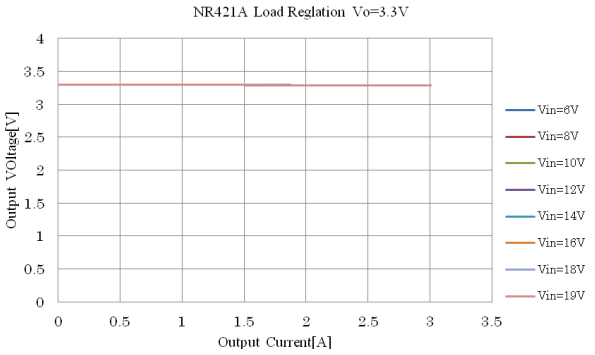


Fig. 9-6

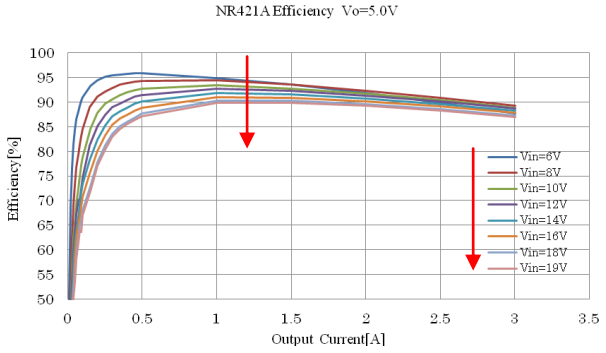


Fig. 9-3

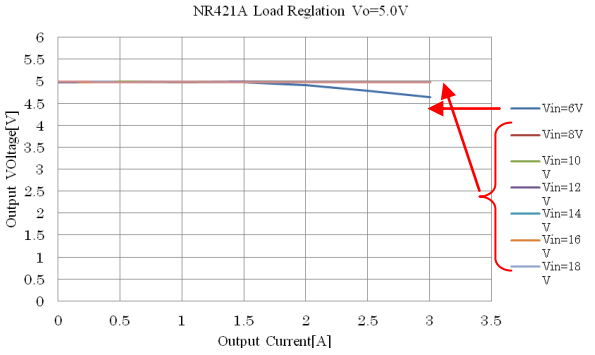


Fig. 9-7

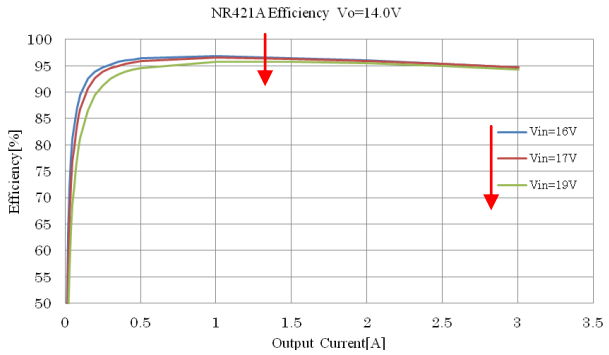


Fig. 9-4

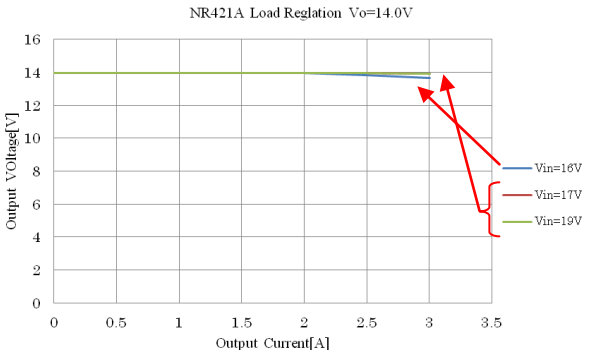


Fig. 9-2

2) UVLO release voltage

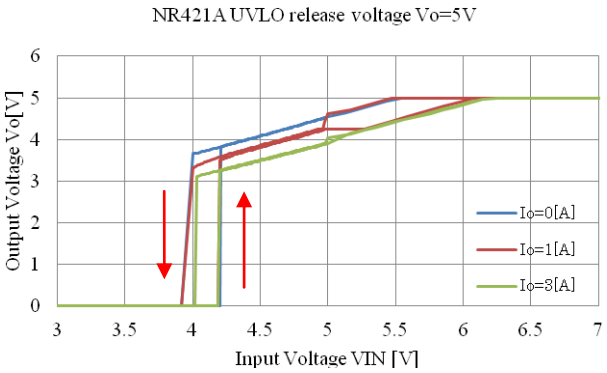


Fig. 9-9

3) OCP characteristic V_O=5V

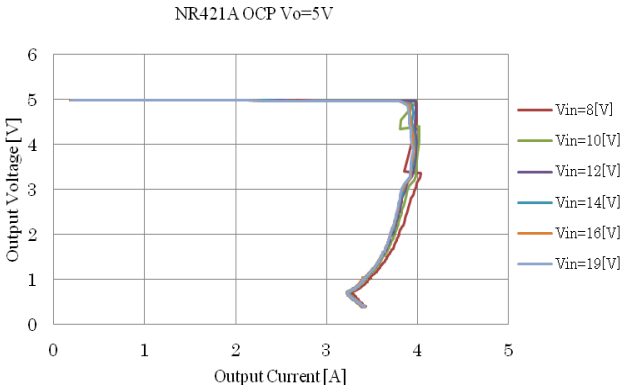


Fig. 9-13

4) OCP characteristic V_O=14V

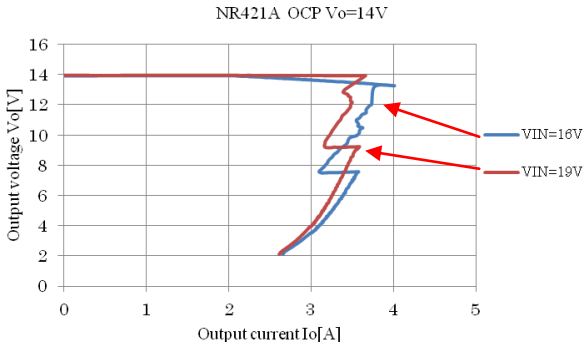


Fig. 9-10

5)Supply Current I_{IN}

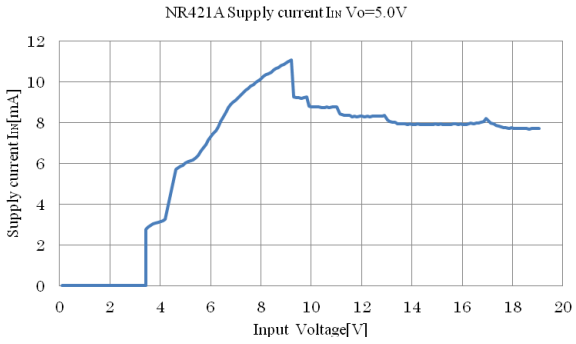


Fig. 9-14

6)Shutdown Supply Current $I_{IN(off)}$

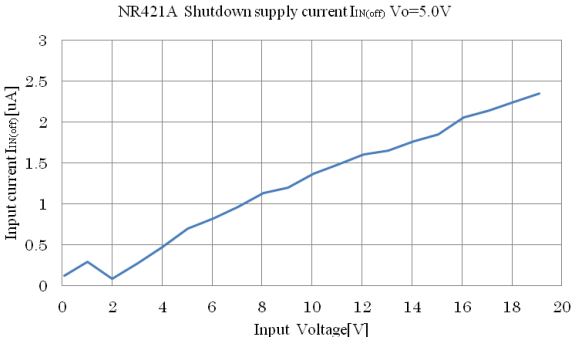


Fig. 9-11

7)Operationg Frequency f_{SW}

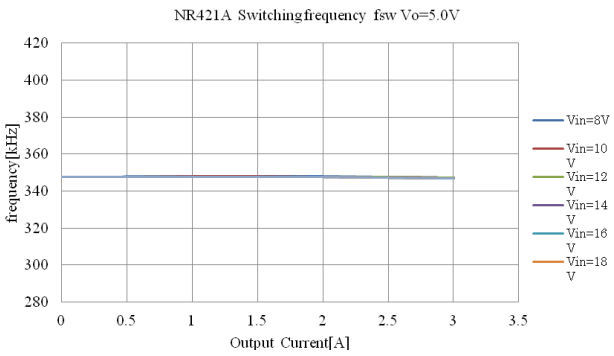


Fig. 9-15

8) EN terminal voltage vs. Output Voltage V_O

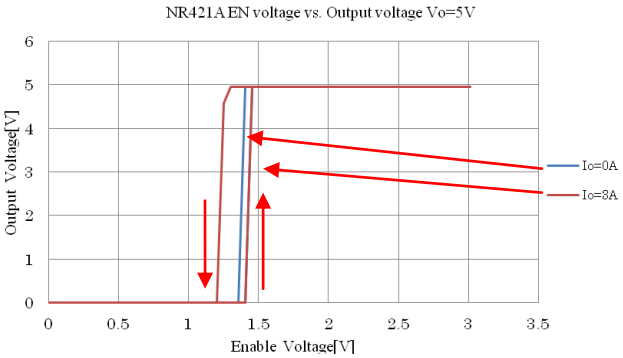


Fig. 9-12

9) TSD operation temperature, Restart temperature

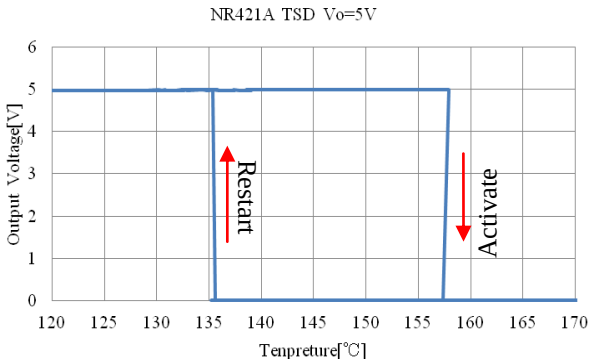


Fig. 9-16

10. Packing specifications

10.1 Taping & Reel outline

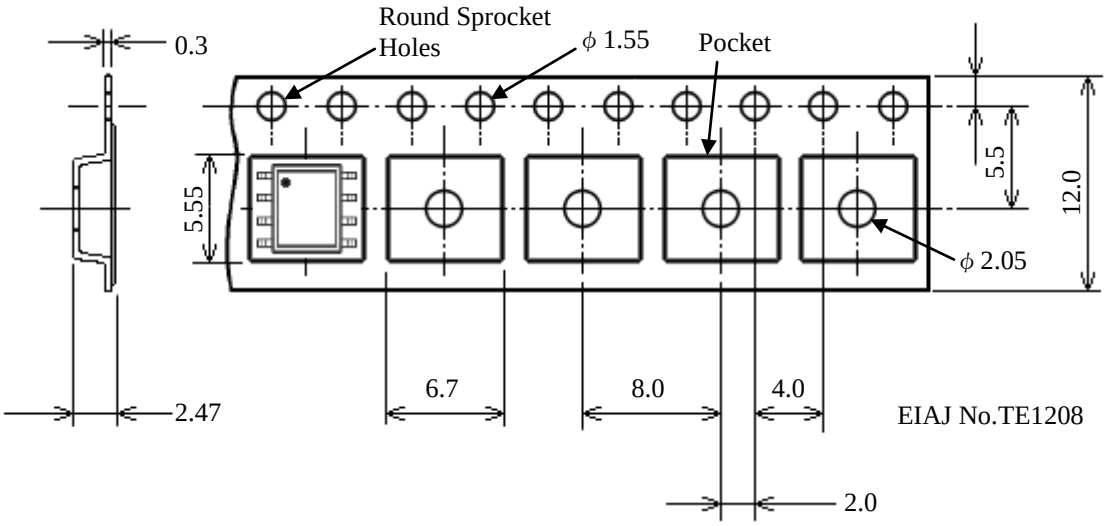


Fig. 10-1 Taping Outline

Notes:
1) All dimensions in millimeters (mm)
2) Surface resistance : under $10^9\Omega$
3)Drawing is not to scale

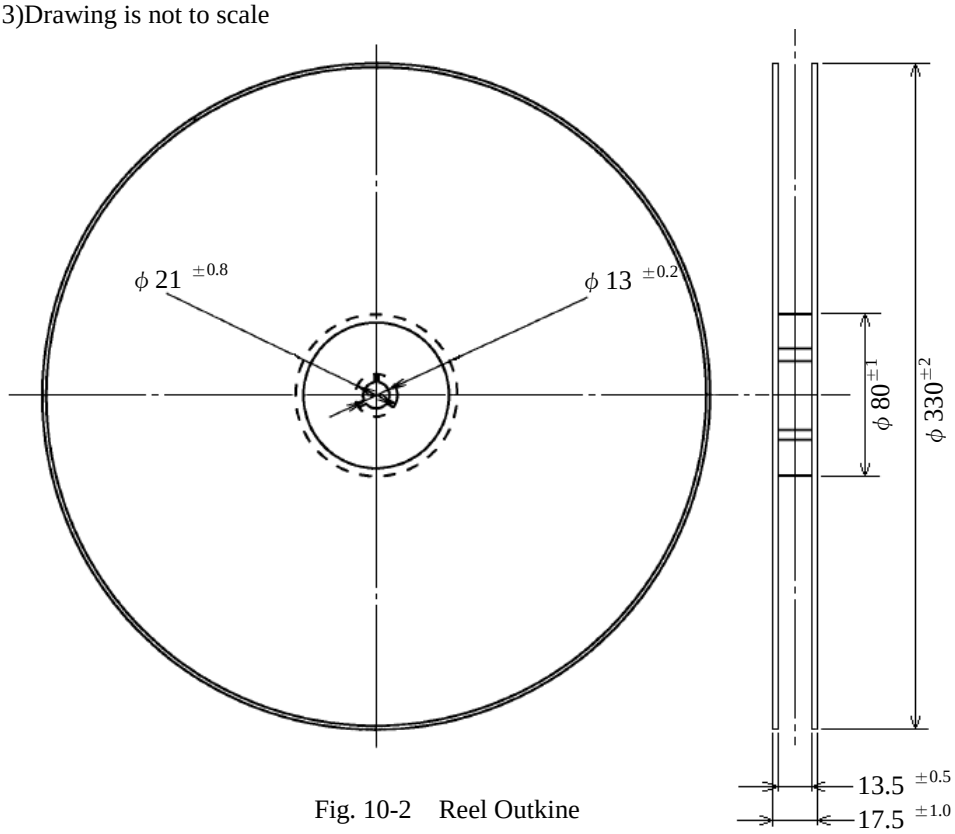


Fig. 10-2 Reel Outkine

Notes:
1) All dimensions in millimeters (mm)
2) Drawing is not to scale

EIAJ No.RRM-12DC

Quantity (TBD)
4000pcs／reel

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