MLX74190

Two-Fold High Power LF Initiator
With integrated Immobilizer

Features

- 2 High power independent drivers (2.5Apeak in square and 1Apeak in sine mode)
- Full bridge drive capabilities
- Built-in protection features (antenna fault detection, over current and T°) for safe operation in all conditions
- Easy-to-use through SPI interface
- Built-in ASK and FSK immobilizers

Application Examples

- Passive Start system
- TPMS Initiator
- LF door opener
- Active RFID initiator

Ordering Information

Part Code	Temperature Code	Package Code	Option Code	Packing Form Code
MLX74190	R (-40°C to 105°C)	PF (Lead free TQFP 7x7 48 leads)	ABA-000	RE

Description

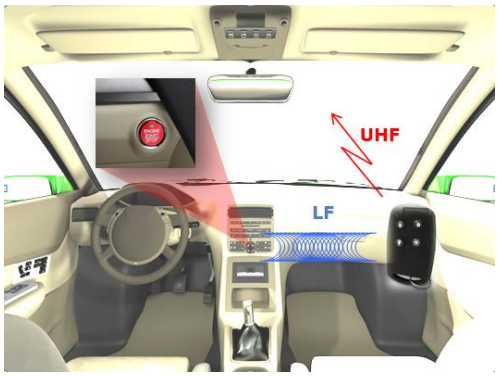


Figure 1: Passive Start Application

The MLX74190 low-frequency (LF) initiator IC consists in two high power LF drivers and built-in immobilizers (IMMO).

The main application for the MLX74190 is automotive remote passive start, where the IC transmits a high power LF telegram to wake-up the key inside the car. The key sends out its identification number to the car via an ultra-high frequency (UHF) signal, enabling the engine to start. The MLX74190 also features two built-in Immobilizers (for ASK and FSK communications), used when the battery of the key is depleted. In this case, the key is placed in a specific zone close to the initiator and a full passive RFID communication is initiated. The load modulation signal returns by the key is received and demodulated by the MLX74190.

The MLX74190 can also serve for a similar purpose with other vehicles such as; motorcycles, scooters, all-terrain vehicle (ATV), jet skis, snowmobiles and motorboats, where the key holder can be detected when approaching the engine and will be able to activate it from a “Start” button, or as a ‘dead man switch’ so that if the driver falls off then the engine is automatically cut. In addition it may be incorporated into building access systems, tire pressure monitoring system (TPMS) initiators and pet identification system.
Both LF drivers are independently programmable to generate sine (max. 1Ap) or square (max. 2.5Ap) waves, with a frequency from 109kHz to 140kHz and an output amplitude from 0.25 to 32Vpp. The two drivers can be used in full or half bridge configuration and are protected against overload (over-current and over-temperature). A built-in diagnosis function allows detecting any wrong connection with the LF antenna (Short to GND, Short to Vbat, open load or wrong resonance frequency).

The MLX74190 is supplied by an external VS voltage from 6-40V and VDD voltage of typically 5V. The VS voltage can be generated by an external DC-DC converter or by DC voltage from vehicle supply.

The MLX74190 is controlled through a standard SPI interface (SDI, SDO, SCK and NCS) and an interrupt pin is generated on-purpose by the IC. The MLX74190 is clocked either with a 2 MHz clock frequency signal coming from the MCU or by an on-chip oscillator connected to an external 4 MHz crystal or ceramic resonator.

Contents

1. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Comment
Driver Supply Voltage	VS		45	V	
5V Supply	VDD		7	V	
Storage Temperature Range	T_S	-55	150	°C	
Junction Temperature	Tj	-40	165	°C	
Static thermal resistance from Junction to Ambient	Rthja		28	K/W	
ESD Sensitivity (HBM global pins)	$V_{ESDglobal}$	+/-3		kV	OUT1, OUT2, VS, ASK_RXi, FSK_RXi
ESD Sensitivity (HBM local pins)	$V_{ESDlocal}$	+/-2		kV	All other pins
ESD Sensitivity (CDM)	V_{CDM_sens} (HBM Global pins)	+/-500		V	

Table 1: Absolute maximum ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2. Range of Functionality

Parameter	Symbol	Min Value	Typical	Max Value	Units
5V Supply	VDD	4.5	5	5.5	V
Driver Supply Voltage – operating	VS	6	-	40	V
Input voltage range on pins: NCS, SCLK, SDI, WUP, CLK_IN and REMOTE_DATA_IN, OSC	Vin_dig	-0.5	VDD	5.5	V
Operating Temperature Range	T_A	-40	-	105	°C

Table 2: Range of functionality

Note:
Every electrical parameter specified in this document, except if specifically indicated, is valid in the complete temperature range: -40 to 105°C.

3. Pin out description

Pin №	Name	Type	Function
1	FSK_RX2	Analog	FSK Immobilizer input pin 2
2	FSK_FB2	Analog	FSK Immobilizer feedback loop 2
3	IP_SENSE	Analog	Current Measurement Output Voltage
4	RBIAS	Analog	Reference Resistor connection for trimming the current reference
5	EXT_CLK	Digital	External clock used in combination with CLK_IN to connect an external resonator
6	CLK_IN	Digital	Input clock coming from MCU or connected to external resonator
7	OSC	Analog	125KHz clock input/output
8	OUT1	Analog	Antenna connection (driver output 1)
9	GND	Ground	Power ground for driver outputs
10	VS	Supply	Supply for driver outputs
11	OUT2	Analog	Antenna connection (driver output 2)
12	CLK_OUT	Digital	2MHz clock output
13	WUP	Digital	Wake up pin
15	SCLK	Digital	Serial clock for SPI
16	NCS	Digital	Not chip select for SPI
17	SDO	Digital	Slave data output for SPI
18	SDI	Digital	Slave data input for SPI
19	IRQ	Digital	Interrupt signal output
20	D_OUT	Digital	Immobilizer data / Digital modulation output signal
21	RDI	Digital	Input signal for direct LF modulation (RDI = REMOTE_DATA_IN)
22	VDDA_CAP	Supply	Analog internal regulator decoupling cap.
23	ASK_RX1	Analog	ASK Immobilizer input 1
24	ASK_RX2	Analog	ASK Immobilizer input 2
25	AGND	Ground	Analog ground
36	VDD	Supply	5V supply
38	DGND	Ground	Digital ground
41	VDDD_CAP	Supply	Digital internal regulator decoupling capacitor
47	FSK_RX1	Analog	FSK Immobilizer input pin 1
48	FSK_FB1	Analog	FSK Immobilizer feedback loop 1
14, 46	Reserved	NA	Must be externally connected to ground
26,27,28,29,30, 31,32, 33, 34, 35, 37,39, 40, 42, 43, 44, 45	NC	NA	Not connected
EXP	EXP	Ground	Exposed PAD, to be connected to ground

Table 3: Pin out description

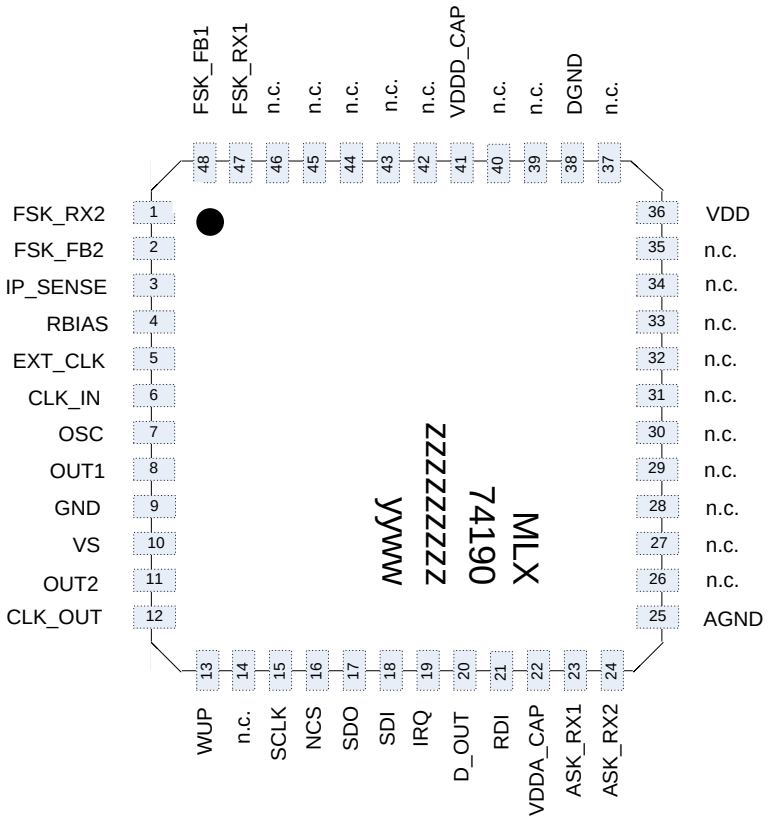


Figure 2: Top view of the package TQFP48

4. High Level Block Diagram

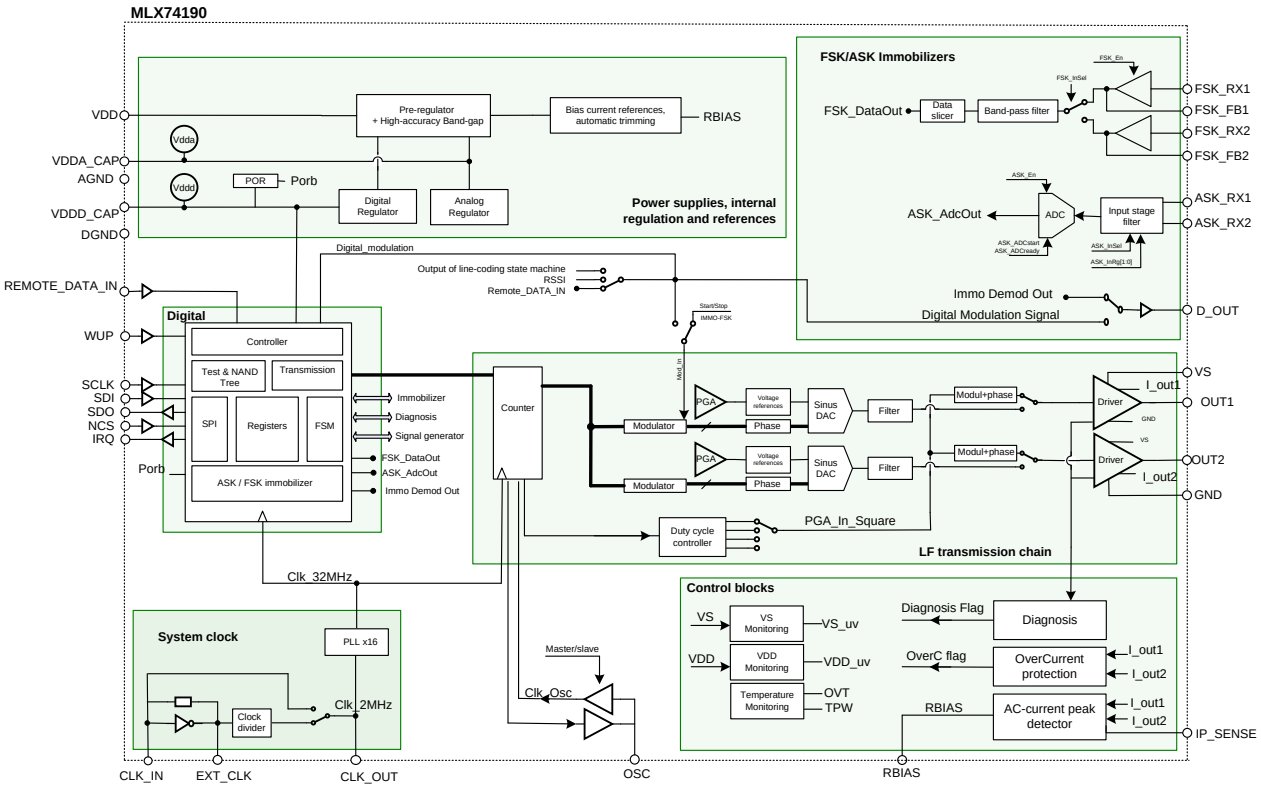


Figure 3: MLX74190 high level block diagram

5. Operating Modes

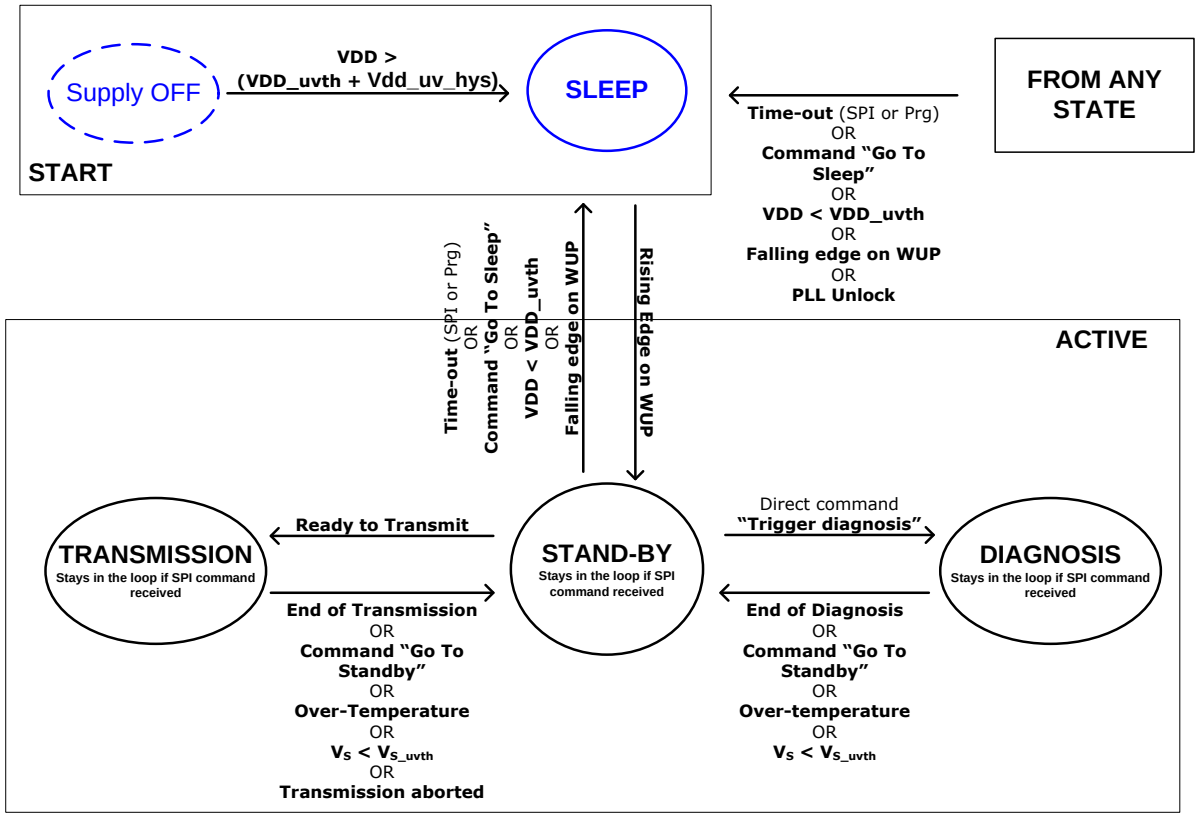


Figure 4: MLX74190 operating modes transition diagram

5.1. Sleep Mode

In SLEEP mode, all internal registers are set to their default values, flags and pointer are reset. All antenna outputs are switched to Hi-Z mode, the PLL is switched OFF and the SPI interface is deactivated. The device exits SLEEP mode when a rising edge is applied on the pin WUP by the external host MCU.

5.2. Standby Mode

In STANDBY mode, all antenna outputs are switched to Hi-Z mode, all digital outputs are switched to their default values and the internal LF transmission chain is deactivated. The SPI interface is activated and the MLX74190 device is able to receive and answer SPI commands from the external host MCU.

5.3. Transmission Mode

In TRANSMISSION mode, the MLX74190 is busy transmitting LF sequence(s). All digital outputs are active; the LF driver outputs are configured according to the active configuration register. The SPI interface is activated and the MLX74190 device is able to receive and answer SPI commands from the external host MCU.

5.4. Diagnosis Mode

In DIAGNOSIS mode, the MLX74190 is busy with diagnosis procedure. All digital outputs are set in default states; the LF driver outputs are activated and ready for diagnosis process. The SPI interface is activated and the MLX74190 device is able to receive SPI command from the external host MCU.

6. Detailed Description

6.1. Power supplies, internal regulation and references

The MLX74190 is supplied with VDD voltage of typically +5V and VS voltage between 6 to 40V, used for the embedded drivers. Both voltages are internally monitored and the MLX74190 device enters the corresponding under-voltage conditions if VDD or VS is going below the VDD_uv or Vs_uv thresholds. For more information about the under-voltage condition, please refer to the chapter

VDD and VS under voltage.

A high accuracy band-gap is implemented, providing the internal reference current for the other built-in blocks of the MLX74190 device. An external high precision **1%** resistor of **5.23 kOhm** has to be connected to the pin **RBIAS**.

Two embedded regulators are included in the MLX74190. An external **220nF** decoupling capacitor will be placed on both pins **VDD_CAP** and **VDDA_CAP**. These two embedded regulators function as follows:

- "Analog regulator" provides a stable supply voltage to analog parts
- "Digital regulator" provides a stable supply voltage to digital parts

For VDD decoupling purposes a 1uF capacitor in parallel to a 100nF capacitor are recommended.

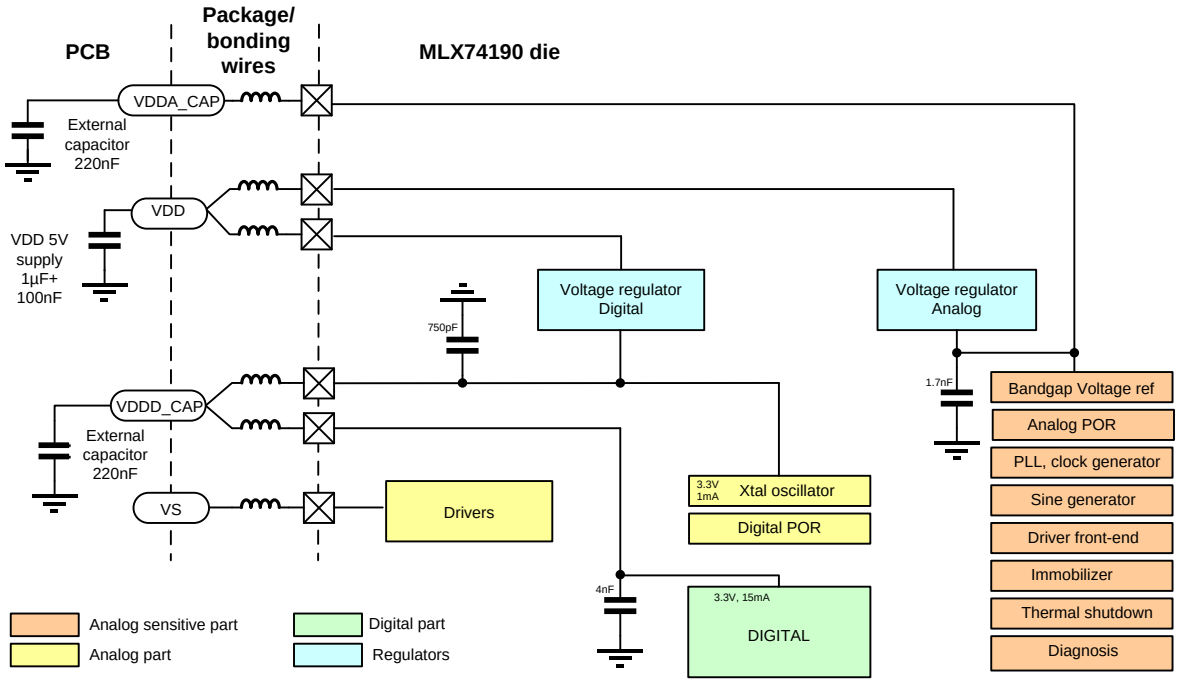


Figure 5: MLX74190 Power supplies, internal regulators and references

6.2. System clock

The 32MHz internal system clock frequency is generated either from an external 2MHz clock signal provided by an external device (usually coming from a microcontroller) or by using an external crystal resonator whose frequency value is 4MHz. The recognition of the input clock source is done automatically during the start-up phase. A 2MHz clock signal is available for external devices on the pin CLK_OUT.

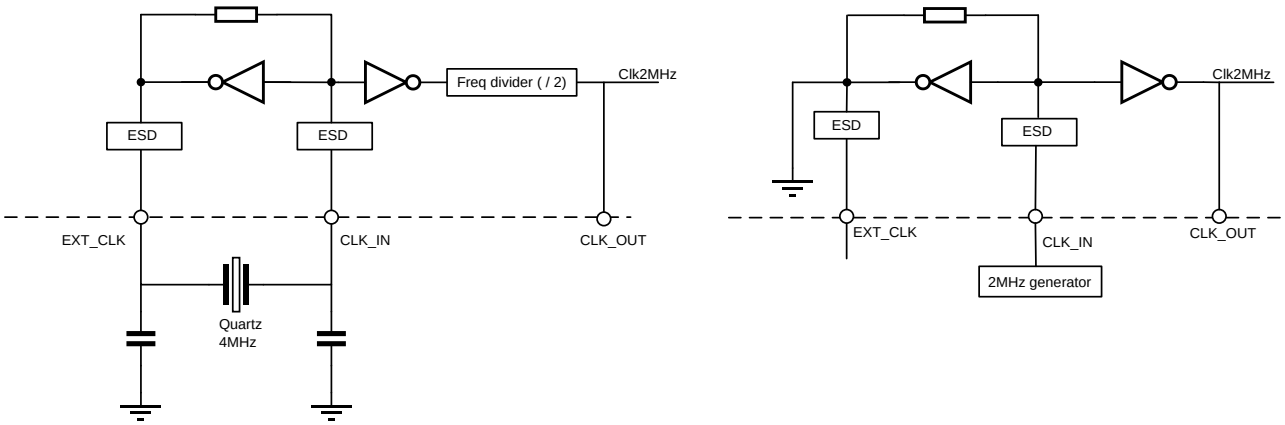


Figure 6: Dual system clock configuration, MCU (2MHz) or Crystal (4MHz)

The signal CLK2MHz is then driven to the built-in PLL, generating the internal system clock of 32MHz used for:

- The control logic
- The sampling of SPI data
- The Generation of the LF driver frequency (sine/square waves)
- The ASK Immobilizer block

6.3. LF transmission chain

The signal is transmitted to the antenna via the LF transmission chain

6.3.1. Frequency generation

The frequency generated by the LF driver can be set to a fixed value of 125 kHz or to a programmable value, according to the configuration register CONF_Byte9. The value of the programmable frequency is defined in the IMMO_Byte0 configuration register. In programmable mode, the programmable frequency is generated from the 32MHz clock with a counter in the range from 225 (**110 kHz**) to 290 (**141.6 kHz**). The following table shows the different frequency steps allowed by the device. 125kHz is the default setting after power-up of the device.

Counter Step (dec.)	Carrier freq. (in Hz)	Counter Step (dec.)	Carrier freq. (in Hz)
225	109863	**258**	125977
226	110352	**259**	126465
227	110840	**260**	126953
228	111328	**261**	127441
229	111816	**262**	127930
230	112305	**263**	128418
231	112793	**264**	128906
232	113281	**265**	129395
233	113770	**266**	129883
234	114258	**267**	130371
235	114746	**268**	130859
236	115234	**269**	131348
237	115723	**270**	131836
238	116211	**271**	132324
239	116699	**272**	132813
240	117188	**273**	133301
241	117676	**274**	133789
242	118164	**275**	134277
243	118652	**276**	134766
244	119141	**277**	135254
245	119629	**278**	135742
246	120117	**279**	136230
247	120605	**280**	136719
248	121094	**281**	137207
249	121582	**282**	137695
250	122070	**283**	138184
251	122559	**284**	138672
252	123047	**285**	139160
253	123535	**286**	139648
254	124023	**287**	140137
255	124512	**288**	140625
256	125000	**289**	141113
257	125488	**290**	141602

Table 4: Programmable frequency step

$$Carrier\_freq[Hz] = \frac{32MHz}{Counter\_Step}$$

6.3.2. Sine wave generation

The sine wave generation mode is selected with the bit *Wave_Mode* in the register CONF_Byte1. In this mode, the generated output is a pure sinus signal, with a **DC** voltage value of **VS/2** and a frequency set according to the frequency generation values described above. The output voltage can also be adjusted from **0.25Vpp** up to **32Vpp** according to the **PGA** gain shown in the table below. This voltage amplitude is selected with the bits *Voltage_Selection[5:0]* in the registers CONF_Byte5 and CONF_Byte6. Special care should be taken to adjust the amplitude output with enough margins in respect to the VS driver supply voltage. This is required to avoid having generated harmonics due to sinus distortion. Please refer to the parameters *Vdrop_sine_LV* and *Vdrop_sine_HV* in **Table 8**.

Configuration bits (dec.)	Output voltage (in Vpp)	Configuration bits (dec.)	Output voltage (in Vpp)
0	0	**23**	11
1	0.25	**24**	12
2	0.5	**25**	13
3	0.75	**26**	14
4	1	**27**	15
5	1.25	**28**	16
6	1.5	**29**	17
7	1.75	**30**	18
8	2	**31**	19
9	2.25	**32**	20
10	2.5	**33**	21
11	2.75	**34**	22
12	3	**35**	23
13	3.5	**36**	24
14	4	**37**	25
15	4.5	**38**	26
16	5	**39**	27
17	5.5	**40**	28
18	6	**41**	29
19	7	**42**	30
20	8	**43**	31
21	9	**44**	32
22	10		

Table 5: Programmable PGA gain

At the start and at the end of the LF transmission, a slope is performed respectively from 0V to VS/2 and from VS/2 to 0V. The slope is based on a fixed slew rate approaching a duration of 20 µs for VS=40V (1V/ µs). This is illustrated in the picture below.

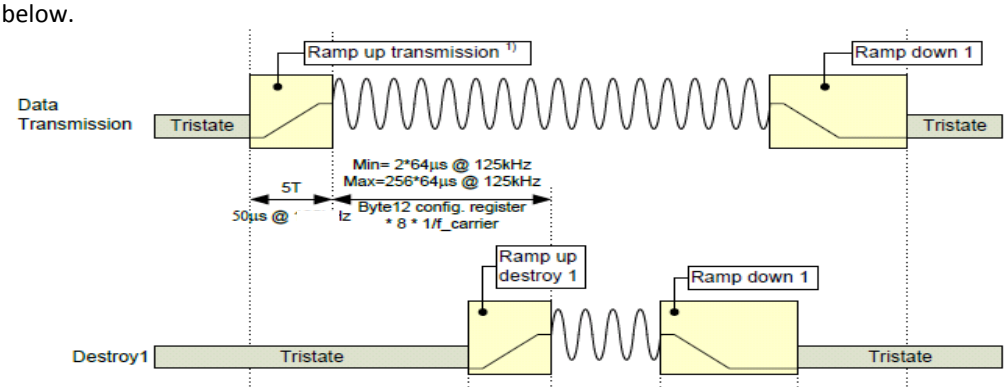


Figure 7: Implementation of slopes at beginning and end of Sine transmission

6.3.3. Square wave generation

The square wave generation mode is selected with the bit *Wave_Mode* in the register CONF_Byte1. In this mode, the generated output is a square wave signal with amplitude fixed to the rail-to-rail value of the driver supply voltage VS.

The duty-cycle of the square wave signal can be configured to 4 values between **6.25%** up to **50%** with the bits *Duty_Cycle[1:0]* in the register CONF_Byte6.

6.3.4. Phase Generation

Each driver stage has an individual phase generation. Phase generation is performed in the digital part of the signal generator and can be selected independently for each output with the bits *Antenna Driver n configuration[1:0]* in the register CONF_Byte1.

- 0°: the output signal is equivalent to the input signal with 0° phase shift.
- 180°: the output signal is equivalent to the input signal with 180° phase shift.

6.3.5. Selection of modulation source

The MLX74190 has a modulation source selector. The 2 bits *LF Mode[1:0]* in the register CONF_Byte9 are used to switch the selector between the different modulation sources:

Digital inputs	Value (MSB.....LSB)	LF mode	Output of the modulations source selector (Digital modulation signal)
LF Mode	00 (0dec)	Normal mode	Line coded data from data register
	01 (1dec)	RSSI	RSSI only (Output is "1" during transmission)
	10 (2dec)	Remote data	REMOTE_DATA_IN (Output corresponds to REMOTE_DATA_IN input)
	11 (3dec)		Default (No function)

Table 6: Modulation source selection

The default mode is no selection (output is "0"). The digital modulation signal will be by default output to the digital pin DOUT. Before starting the transmission, DOUT is equal to "0".

6.3.5.1. Specific case of Modulation through pin REMOTE_DATA_IN, chaining devices.

In case of modulation through the pin REMOTE_DATA_IN pin, i.e. when the IC is in slave mode for transmitting telegram, several hardware prerequisites are needed:

- OSC pin should be set as an input (see bit "Carrier Synchronization "CONF_Byte13) and connected to the master IC which generates the LF frequency, for instance the OSC pin of a second device MLX74190.
- The LF frequency has to be synchronized with the 2MHz input CLK: this means the 4MHz ceramic resonator cannot be used and the 2MHz signal CLK used for master IC is applied on pin CLK_IN.

For example: in case of two chained devices MLX74190: the first one - IC#1 – considered as master, will drive the second one - IC#2 – considered as slave:

- Both pins OSC are connected together
- The pin CLK_OUT of IC#1 (master: a 4MHz ceramic resonator can be used in this case) is connected to the pin CLK_IN of IC#2 (slave: no ceramic resonator needed)
- The pin D_OUT of IC#1 is connected to the pin REMOTE_DATA_IN of IC#2

Once both devices are correctly configured, IC#2 will transmit synchronously on its output(s) the same modulated signal transmitted on the output(s) of IC#1

6.3.6. Modulator

Each driver stage is able to modulate the LF carrier signal in ASK and PSK mode. Selection of the modulation mode is done via the bit *Modulation_mode[1:0]* in the register CONF_Byte11:

- **ASK:** The amplitude of the carrier frequency is modulated from 0 to 100% according to the digital modulation data.
- **PSK:** The phase of the carrier frequency switches between 0° and 180° according to the digital modulation data.

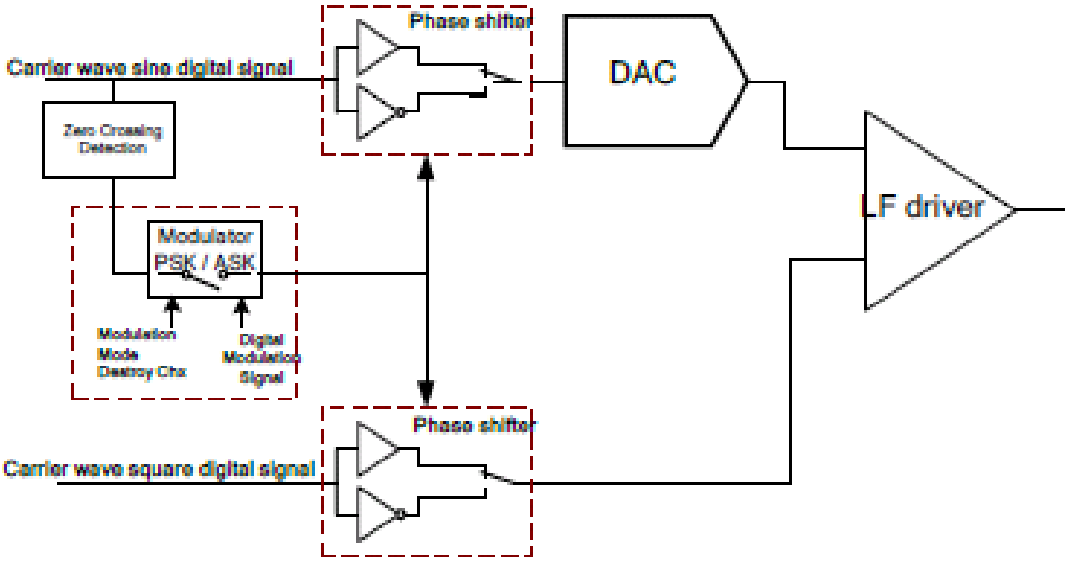


Figure 8: Modulator block diagram

6.3.7. Transmission of destroy bits

The modulator can be configured to transmit DESTROY bits via the bit *Output_Destroy* in the register CONF_Byte7. In this case, two short LF sine bursts will be transmitted on the selected output, with the amplitude corresponding to the PGA gain.

The phase of the two DESTROY bits can be selected independently to 0° or 180°. The two DESTROY bits will be sent without any delay in-between and with a fixed duration time of 16 carrier periods for one DESTROY bit.

Transmitting destroy bits can be used to load the antenna before transmitting a real telegram.

6.3.8. LF Driver outputs

The MLX74190 features two LF drivers to amplify the sine/square wave provided by the LF generation stage.

According to the bits *Antenna Driver n configuration[1:0]* in the register CONF_Byte1, the driver output can be configured as follows:

Output_Configuration[1:0]	Driver output	Output Phase
00	Hi-Z	NA
01	LF transmit	180°
10	LF transmit	0°
11	Pull Down	NA

Table 7: Driver output selection

At the end of any transmission frame or after sending a DESTROY bit, all driver outputs are automatically switched during 7 carrier periods to ground before finally switching to Hi-Z (i.e. 56us at 125kHz carrier). This automatic sequence is implemented to decrease the load current and occurs independently from the transmission mode even if another frame will follow.

6.3.9. Electrical parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
Outputs 1,2 current in sine mode	I_out_sine			1	Ap	
Outputs 1,2 current in square mode	I_out_square			2.5	Ap	
Output high side transistor on-resistance	AD_Rdson_High	0.8		2.27	Ω	Including bonding wire
Output Low side transistor on-resistance	AD_Rdson_Low	0.5		1.65	Ω	Including bonding wire
Output voltage drop in sine mode (VS-Vout), for low voltage (Vout ≤ 16Vpp)	Vdrop_sine_LV	4.1			V	
		2.5			V	Max 15% of distortion
Output voltage drop in sine mode (VS-Vout), for high voltage (Vout > 16Vpp)	Vdrop_sine_HV	8.0			V	
		4.0			V	Max 10% of distortion
Accuracy of output voltage in sine mode	AD_sinus_Low_Error	-0.7		0.4	V	0.25Vpp < Vout < 4,5Vpp
	AD_sinus_Med_Error	-11		11	%	5Vpp < Vout < 7Vpp
	AD_sinus_High_Error	-5		5	%	8Vpp < Vout < 32Vpp
Output peak to peak voltage sine	Vout_sine	0.25		32		See Table 5 (PGA Gain Selection)
Min. output peak to peak voltage square	Vpp_square	32.1		VS	V	For VS = 40V and with I_out_square max
Output switching time from Active to Hi-Z / GND	T_Switch_Hi-Z			1	µs	
Output switching time from Hi-Z / GND to Active	T_Switch_active			2.5	µs	
				0.2	µs	
Total phase shift	Phase_Shift_AD	263	373	525	ns	Sine mode
DC voltage level VS/2 accuracy	AD_Sinus_VS_2	-6.5		6.5	%	Sine mode

Table 8: Antenna driver specifications

6.4. Immobilizer Function

The MLX74190 embeds two ASK and FSK immobilizer blocks. These Immobilizers are used to detect and demodulate data from a transponder via respectively amplitude-shift keying (ASK) or frequency-shift keying (FSK) modulation techniques. The MLX74190 includes 2 input pins for each ASK / FSK demodulators that cannot be activated simultaneously. The demodulated and digitized signal is then transmitted to the MCU via the **D_OUT** output pin.

The immobilizer inputs can be connected to every driver through external hardware and can be enabled / disabled by register settings. They can be fully programmed through a set of registers available in chapter Immobilizer Configuration Register. One channel of either ASK or FSK can be used at a time.

6.4.1. ASK demodulation

The ASK demodulator converts the amplitude-modulated analog signal received on ASK_RXi pins from the transponder into digital data which are accessible by the MCU through the D_OUT output pin.

If the immobilizer is deactivated, the ASK_RXi input pins are connected to GND.
If the immobilizer is activated, the voltage swing at the ASK_RXi inputs is internally clamped to 18Vpp.The ASK_RXi inputs are connected to the LF antenna through an external capacitive divider. This capacitive divider should be calculated regarding the maximum voltage expected on the antenna, to avoid saturating the ASK input (i.e. 18V clamping voltage)

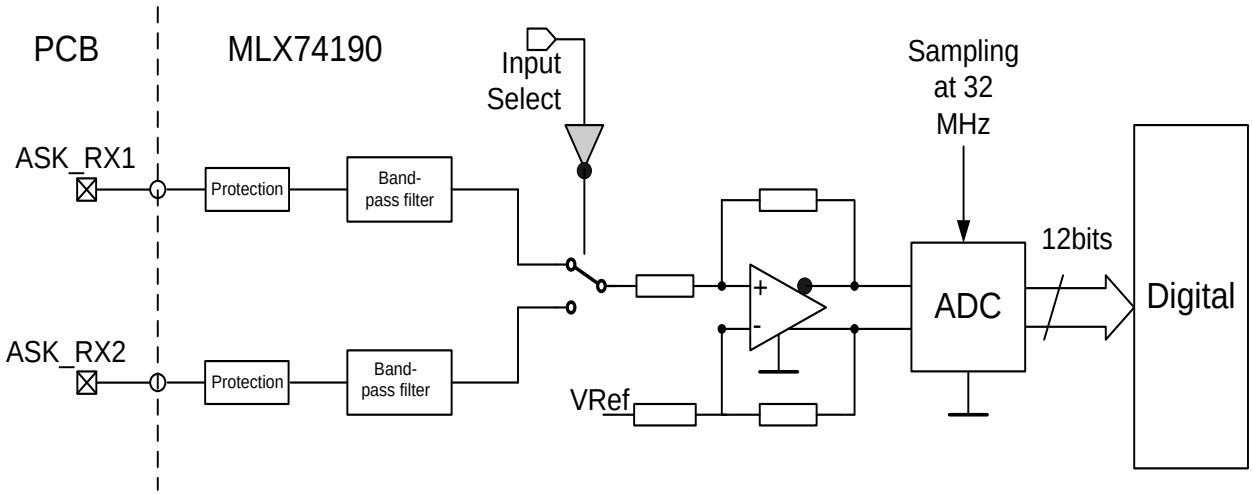


Figure 9: Immobilizer ASK, block diagram

Both ASK_RXi inputs embed a band-pass filter which has to be set according to the incoming data-rate of the TAG. As shown in the table below, the maximum supported data-rate is of 8Kbit/s.

IMMO_Byte1 [6:7]	Data Rate	Min. Modulation Frequency	Max. Modulation Frequency
00	2 Kbit/s	1 KHz	2 KHz
01	4 Kbit/s	2 KHz	4 KHz
10	8 Kbit/s	4 KHz	8 KHz
11	**Reserved**		

Table 9: ASK data rate selection

The time at which the demodulated signal is available at D_OUT can be configured with two timings, available in

Immobilizer Configuration Register (BYTE#2): the *Programmable delay between signal Dig_mod High and ASK demodulator start*, and the *Programmable Early Start time*.

The BPSK delay and the *ASK Glitch filter configuration*, in

Immobilizer Configuration Register, also impact the global timings, as shown in the picture below.

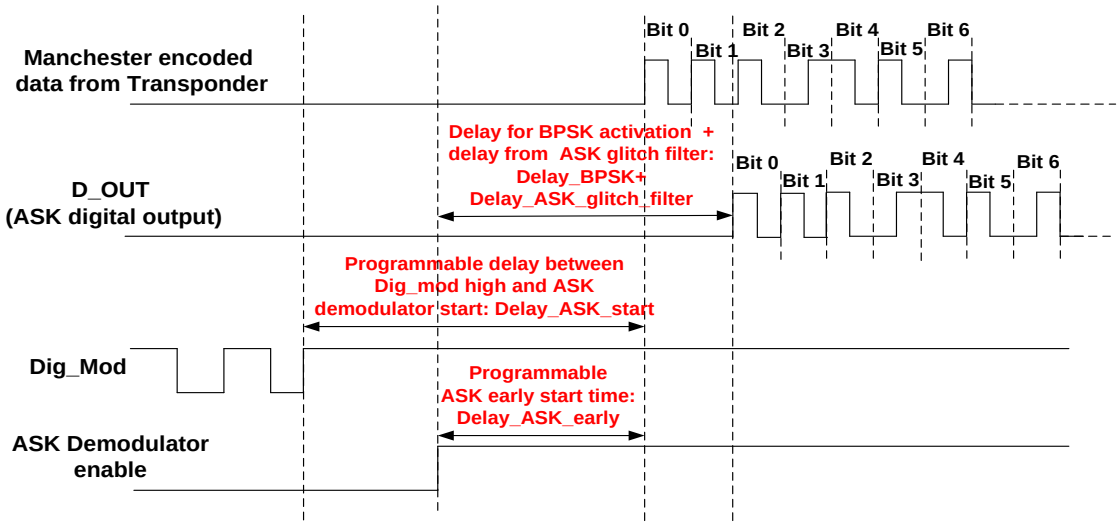


Figure 10: ASK demodulation signals

The formula below can be used to calculate the demodulator's delay:
Demodulator_delay_D_OUT = Delay_ASK_start - Delay_ASK_early + Delay_BPSK + Delay_ASK_glitch_filter

Delays	Unit	DataRate : 2 kbit/s	DataRate : 4 kbit/s	DataRate : 8 kbit/s
Delay glitch filter: off	µs	0	0	0
Delay glitch filter: 01	µs	48	24	12
Delay glitch filter: 10	µs	80	40	20
Delay glitch filter: 11	µs	144	72	36
Delay_BPSK	µs	1616	808	408
Delay_ASK_start and Delay_ASK_early are defined in BYTE#2 of Immobilizer Configuration Register				

Table 10: ASK signal: typical delays

6.4.2. FSK demodulation

The FSK demodulation block is intended to detect and demodulate the response of the transponder compliant with FSK modulation (frequency shift keying). The demodulated data are accessible by the MCU through the D_OUT output pin. The FSK signal is a modulated frequency signal, where high and low bits are coded with two different frequencies.

The frequency of the input signal is measured by counting the oscillation clock for the time period of the input signal. As the high-bit and low-bit frequencies are specified with wide tolerances, the demodulator distinguishes them using the difference between both frequencies and not by their absolute values. After the charge phase, the FSK demodulator measures the time period of its input signal and waits for the transponder resonance-frequency measurement to determine the threshold between high-bit and low-bit frequency.
Then the demodulator waits for the occurrence of the start bit.
The detection of the start bit is effective when the contents of the shift register matches a specific pattern, indicating 8 subsequent periods below the threshold (higher frequency) immediately followed by 4 subsequent periods above the threshold (lower frequency)
The bit stream detected by the digital demodulator passes through a digital filter before being evaluated. After demodulation, the serial bit flow received from the transponder is buffered byte-wise before being sent to the microcontroller.

The two external resistors **Rin** and **Rfb** are typically set to obtain an amplifier gain of 4 and limiting the input current to an absolute maximum of 2mA. These resistors might be adjusted according to the voltage swing on the external antenna.

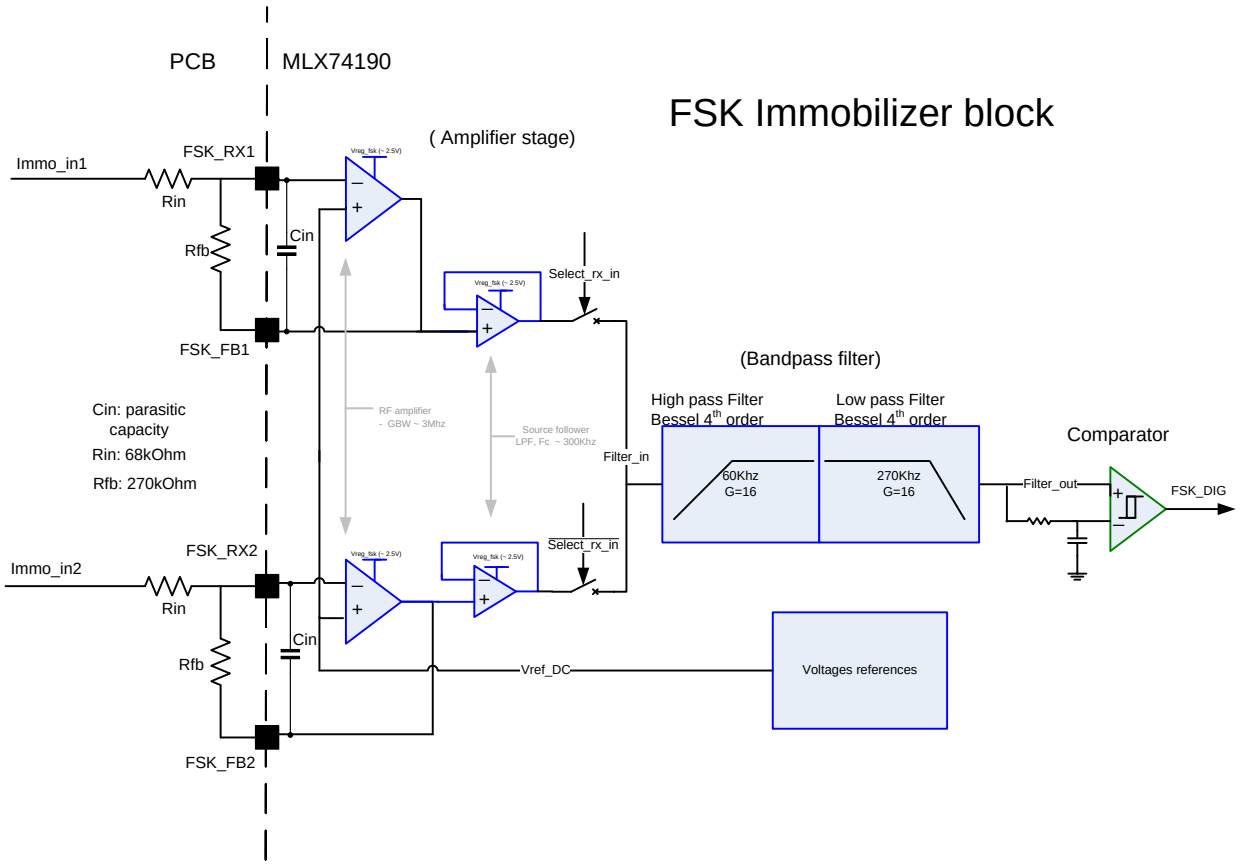


Figure 11: Immobilizer FSK, block diagram

6.4.3. Electrical parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
Input voltage range at ASK_RXi pin	Immo_ASK_range	0		18	Vpp	
ASK_RXi pin input positive current range	Immo_ASK_Ip			20	mA	Vdd = 5V, in the specified input range
ASK_RXi pin input negative current range	Immo_ASK_Im	-20			mA	Vdd = 5V, in the specified input range
ASK_RXi pin positive clamping voltage.	Immo_VClamp_RXp	18	20	22	V	
ASK_RXi pin negative clamping voltage	Immo_VClamp_RXm	-1.50	-0.85	-0.5	V	
ASK_RXi pin input impedance (1)	Immo_ASK_RX_Imp	50			kOhm	Equivalent AC resistor @ 125 KHz
	Immo_ASK_RX_R	100			kOhm	DC resistor
Min. detectable modulation depth at ASK-RXi	Immo_AM_ASK		1.35		mVpp	measured @ BER=0.1% and 4Kbit/s, with amplitude of min 0.9Vpp and max 18Vpp

Table 11: ASK demodulator specifications

(1) In case of deactivated immobilizer, the pin is grounded via a switch with ca. 200Ω series resistance.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
Low bit frequency	Freq_low_bit	130.2	134.7	139.5	KHz	
High bit frequency	Freq_high_bit	118	123	128	KHz	
Input current range at FSK_RXi in charge phase	FSK_I_range	-2		+2	mA	
Phase Shift of RF amplifier (1)	Phase_0			16	°	Meas. @134kHz
Sensitivity / Minimum peak-to-peak input voltage	V_sfb		5		mVpp	
Band Pass Filter	Immo_FSK_Filter	24	60	100	kHz	Low cut off freq.
		160	270	500	kHz	High cut off freq.

Table 12: FSK demodulator specifications

(1) With Rin=68kOhm, Rfb = 270kOhm and input voltage = 20mVpp

6.5. Digital SPI Interface

The MLX74190 is interfaced and configured through a standard Serial Peripheral Interface bus (SPI). The communication is full duplex: the host MCU (microcontroller) receives status information from the MLX74190 while sending configuration settings. Within the communication, the host MCU always acts as a Master and the MLX74190 always acts as a slave.

The microcontroller sends to the MLX74190:

- The configuration of the MLX74190 according to the application requirements
- The data of the telegram to be sent
- The control command

The microcontroller receives from the MLX74190:

- Status register content (default)
- Shift-In register content (after direct command “Set SDO to send SDI”)
- Working register content (after direct command “Read working register”)

The SPI consists of shift-in and shift-out registers controlled with the following signals:

- NCS: Not Chip Select
- SCLK: Serial Clock
- SDI: Serial Data In
- SDO Serial Data Out

Commands:

The MLX74190 understands two types of commands:

- Circular commands: will be understood within the same NCS cycle
- Direct commands: Requiring its own NCS cycle.

The direct commands are executed immediately whereas the circular commands are stored one after the other in the circular buffer and executed successively.

For more information on the implemented commands, please refer to the chapter

SPI Commands below. The length for the command is fixed to 8 bits and it is sent at the beginning of a communication frame.

Data area:

- Variable length from 0 byte till 15 bytes.
- The number of data bytes to be transmitted during one communication frame depends on the command. This is sent at the second position in the SPI communication, just after the command.

6.5.1. SPI signal frames

When NCS is high, the MLX74190 is not selected and any signal at the SCLK and SDI pins is ignored. Moreover, the pin SDO is forced into a high impedance state.
The MLX74190 is selected with the pin NCS set to zero by the master; this pin shall remain to zero during the complete SPI communication cycle. The MLX74190 is able to receive several bytes as one block without delay between the bytes.

SPI data are shifted-in from SDI at each falling edge of the SCK signal (with NCS set to low).
SPI data are shifted-out on SDO at each rising edge of the SCK signal (with NCS set to low).

By default, the MLX74190 returns its status information as follows:

- 1st Byte: general status byte (see

- Status Register)
- 2nd to 7th Byte: status Byte 1 to status byte 6 (see

- Status Register)
- 8th and following bytes: "11111111

The information sent out by SDO will change after the following SPI-direct commands:

- Send general failure flag:

Only the general failure flag (Bit 0 of the general status byte) is returned by the MLX74190. All other bits are set to "1". This is valid until another direct command is sent to change the setting of SDO pin or until the chip enters in sleep mode.

- Set SDO to send SDI:

The data shifted in from SDI will be shifted out on SDO with 1 byte delay.

- Read working register:

The content of the working register of the address defined in the command and the following bytes shall be sent on SDO.

The number of bytes depends on the length of the following frame. A complete frame shall be recognized by a low to high transition on NCS. If the number of bits transferred to SDI during one frame is not divisible by 8 (there is a low to high transition on NCS and the last byte transferred to SDI doesn't consist of 8 bits) a SPI-error flag is generated.

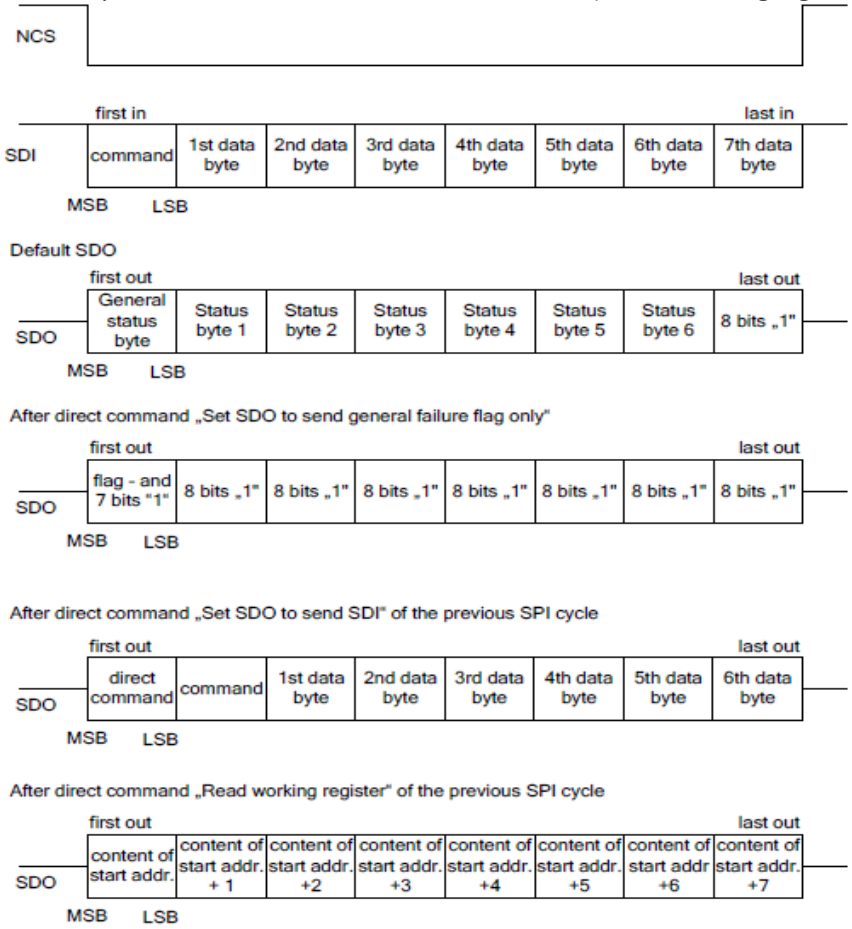


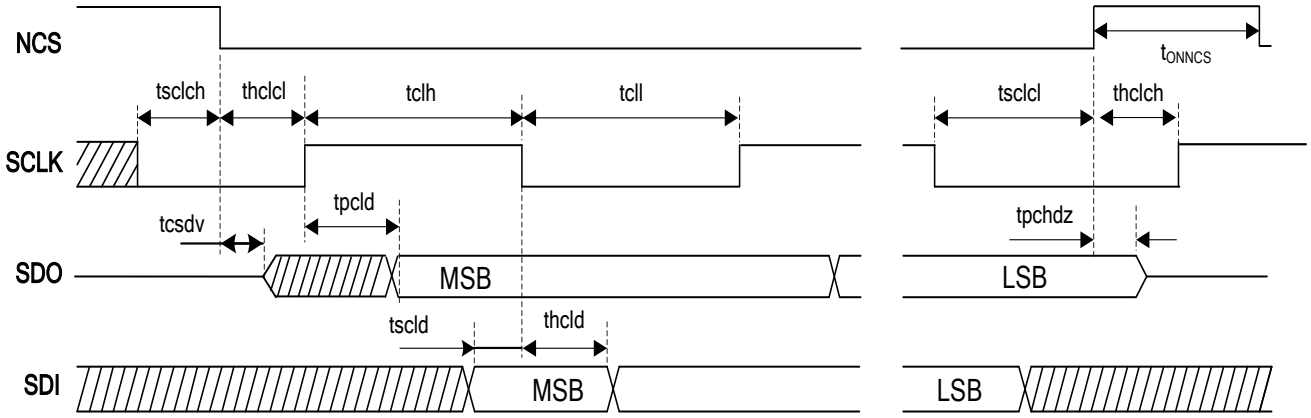
Figure 12: SPI communication frames

6.5.2. SPI Commands

Command BYTE								Hexa code	Command description
7	6	5	4	3	2	1	0		
0: Circular command	1	Number of transmission data bit (max=64, 000000b=1)						-	Program Transmission Data Register
		L	L	L	L	L	L		
	0	0	0	Number of bytes (max 14, 0000b =1)				0X	Program Configuration Register
				L	L	L	L		
	0	0	1	Number of bytes (max 4, 0000b =1)				1X	Program Immobilizer Configuration Register
				L	L	L	L		
	0	1	0	0	Number of bytes (max 4, 000b=1)			2X	Program Transmission Data Format Register without IRQ generation
					L	L	L		
	0	1	0	1	Number of bytes (max 4, 000b=1)			2X	Program Transmission Data Format Register with IRQ generation at start of the first data bit with this format
					L	L	L		
	0	1	1	0	Number of bytes (max 6, 000b=1)			2X	Program Control Register
					L	L	L		
	0	1	1	1	0	0	0	38	Continue with RSSI until next “program transmission data command”
	0	1	1	1	0	0	1	39	RESERVED
	0	1	1	1	0	1	0	3A	RESERVED
	0	1	1	1	0	1	1	3B	Reset read & write pointers of circular buffer
	0	1	1	1	1	0	0	3C	RESERVED
	0	1	1	1	1	0	1	3D	RESERVED
	0	1	1	1	1	1	0	3E	RESERVED
	0	1	1	1	1	1	1	3F	Perform Diagnosis
1:Direct command	0	Address of the working register to be read						-	Reading the specified addressed working register. Content is available on SDO with the next SPI frame (the number of bytes depends on the length of the frame)
		A	A	A	A	A	A		
	1	0	0	0	Number of bytes (max 8, 000 =1)			CX	No operation
					L	L	L		
	1	0	0	1	Number of bytes shifted out at the next SPI sequence (max: 8, 000=1)			CX	Not used
					L	L	L		
	1	1	1	0	0	0	0	F0	Start transmission
	1	1	1	0	0	0	1	F1	Set SDO to Send SDI for the next frame
	1	1	1	0	0	1	0	F2	Set SDO to Send general Status byte and status bytes (depending on the length of the next frame)
	1	1	1	0	0	1	1	F3	Set SDO to send only the general failure flag
	1	1	1	0	1	L	L	F4,F5 F6,F7	RESERVED
	1	1	1	1	0	0	0	F8	Go to Sleep mode
	1	1	1	1	0	0	1	F9	Go to standby mode (**it will abort transmission as well as reset pointers and clearing all failure flags**)
	1	1	1	1	0	1	0	FA	RESERVED
	1	1	1	1	0	1	1	FB	
	1	1	1	1	1	L	L	FC,FDF E,FF	

Table 13: SPI commands

6.5.3. Electrical characteristics and timings



Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
Clock Frequency	Fspi	4			MHz	
SDO transition speed, 20-80%	Tsdotrans	10		30	ns	Vsdo = 5V, Cload = 50 pF
		10		50	ns	Vsdo=5V, Cload = 150 pF
Min. time SCLK=HIGH	Tclh	120			ns	
Min. time SCLK=LOW	Tcll	80			ns	
Propagation delay (SCLK to data valid on SDO output)	Tpcld			75	ns	Including transition time Tsdo_trans
NCS=LOW to data at SDO active	Tcsdv			91	ns	Including filtering time Tfncs
SCLK low before NCS low (setup time SCLK to NCS change H/L)	Tsclch	100			ns	
SCLK change L/H after NCS=low	Thclcl	100			ns	
SDI input setup time (SCLK change H/L after SDI data valid)	Tscld	40			ns	
SDI input hold time (SDI data hold after SCLK change H/L)	Thcld	75			ns	
SCLK low before NCS high	Tsclcl	100			ns	
SCLK high after NCS high	Thclch	100			ns	
NCS L/H to SDO @ high impedance	Tpchdz			75	ns	
NCS min. high time	Ton_ncs	2			µs	
NCS Filter time (Pulses ≤ TfNCS will be ignored)	Tfncs	31		62	ns	NCS Filter time (Pulses ≤ TfNCS will be ignored)
High output level on SDO	sdo_H	Vdd-0,4			V	Isdo = 1,5 mA
Low output level on SDO	sdo_L			0,4	V	Isdo = 2mA
Hi-Z leakage current	Isdo	-5		5	µA	NCS=HIGH,V_{DDIO} = 5V
SPI time-out duration	Tout	88	100	114	ms	Typ value at125kHz, Min at 141kHz, Max at 110kHz =12500 periods of CW at CLK_IN = 2MHz

Table 14: SPI electrical characteristics

6.6. Control blocks

6.6.1. Failure Flags

The following failures / warnings are detected by the MLX74190:

- VS under voltage,
- VDD under voltage (no flag available)
- Temperature pre-warning,
- Over temperature,
- Transmission aborted,
- SPI-error,
- Unspecified SPI command,
- SPI Overflow,
- Over Current.

A general failure flag indicates the detection of at least one specific failure according to the table below.

- The polarity of the general failure flag is inverted: not set = "1", set = "0"
- For all other failure / warning flags: not set = "0" set = "1"

The detected failures are stored in the control and status registers of the MLX74190 (see Status Register).

Failure / warning detection	Storage in control and status register	General failure flag
VS under voltage	1 failure flag	set
VDD under voltage	No failure flag	not set
Temperature pre warning	1 warning flag	not set
Over temperature	1 failure flag	set
Transmission aborted	1 failure flag	set
SPI error	1 failure flag	set
Unspecified SPI command	1 failure flag	set
SPI overflow	1 failure flag	set
Over current (DC or AC)	2 failure flags (1 for each output)	set

Table 15: Failure detection: flags overview

6.6.2. Generating Interruption with IRQ pin

The pin IRQ is used to send interruption to the host MCU. The source of the last generated IRQ pulse is stored in the

Status Register.
A 64us pulse on IRQ is automatically generated in the following cases:

- After a Wake-Up of the device once the PLL is locked, meaning the MLX74190 is able to communicate with SPI (Sleep mode to Standby mode transition)
- At start of LF data transmission (at first bit)
- When data is ready to be transmitting in mode “Wait for trigger via SPI”
- After a diagnosis check
- When the device is ready to transmit data in mode REMOTE_DATA_IN

A 64us pulse on IRQ can be optionally generated in the following case:

- Start of each part of data transmission.(see Circular commands in

- SPI Commands)

6.6.3. Antenna diagnosis

The Diagnosis block is designed to detect any failure related to the antenna connected on the LF driver outputs.

Following potential antenna failures are diagnosed:

- Output Driver short circuited to VS
- Output Driver short circuited to GND
- Disconnected antenna or incorrect Self resonance of the connected Antenna

The following picture illustrates the block diagram of the diagnosis feature.

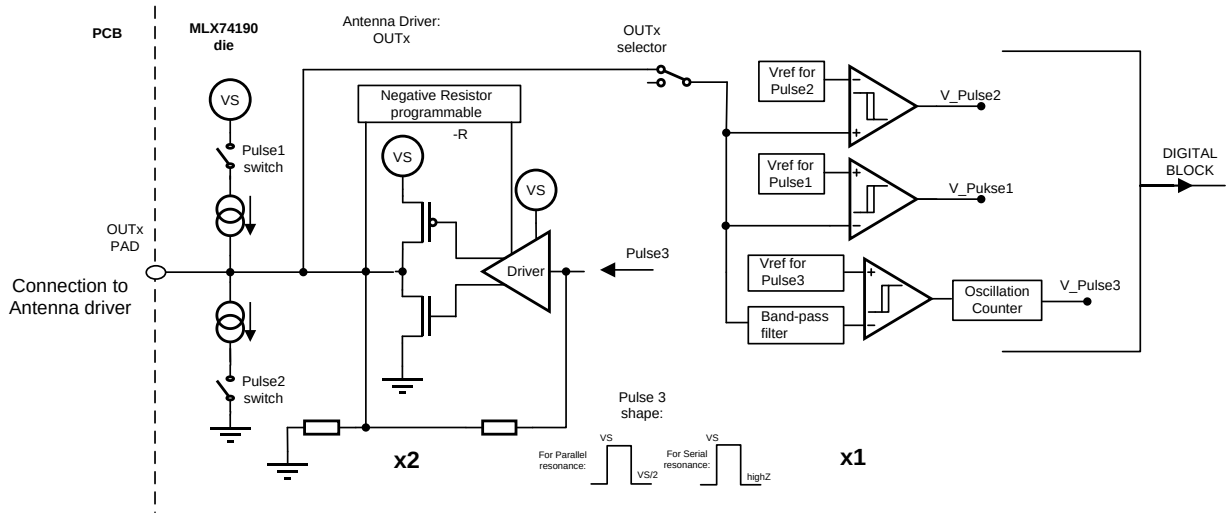


Figure 13: Diagnosis block diagram

The complete diagnosis setup is configured using the Control Register and initiated by sending the SPI-direct command "Perform diagnosis". The results are available in the

Status Register of the MLX74190.

6.6.3.1. Performing diagnosis

After sending the command **Perform Diagnosis** (0x3F) the IC will generate 3 pulses on the selected output.
A high Level pulse to detect any potential short circuit to GND, a Low level pulse to detect any short circuit to VS and a third pulse to detect the presence and the correct tuning of the connected antenna

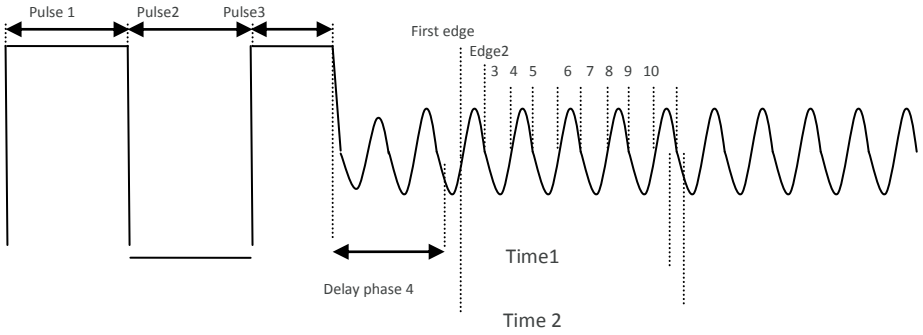


Figure 14: Diagnosis pattern

The output on which to perform diagnosis can be selected in BYTE#2 of Control Register, only diagnosis on one output can be done in the same time.

6.6.3.2. Static check: Pulse 1 and Pulse 2

Pulse 1 and Pulse 2 checks only verify that the output driver is not short circuited to GND or VS level, by applying successively both pulses via internal switches. A feedback line on the selected output, connected to 2 static comparators, verifies that the pulse level is correct.
The durations of Pulse 1 and 2 can be set in BYTE#2 of Control Register, the threshold levels of both comparators can be also adjusted in BYTE#3 and BYTE#4 of Control Register, for respectively high side and low side comparators.

6.6.3.3. Resonance check: Pulse 3

There are two modes for Resonance Check (**Evaluation Mode**, defined in BYTE#4 of Control Register):

- A serial mode in case of serial RLC antenna,
- A parallel mode in case of a filter capacitor is set in parallel to the RLC antenna, to filter harmonics

The main difference is that at the end of the Pulse 3 the device is set to High impedance for serial mode and to VS/2 in parallel mode.

At the end of the pulse 3 a few LF oscillations will be visible on the selected output if all the following conditions are fulfilled:

- An antenna RLC is connected to the selected output
- Its tuning value is in a correct LF range (around 125kHz)
- The internal negative resistance value is set closely to the same value of the resistive value of the RLC antenna.(BYTE#1 of Control Register)

The IC starts to count a defined number of oscillation (**Number of Oscillation to detect**, defined in BYTE#4 of Control Register) if the count does not end between time1 and time2 (defined in BYTE#2 and BYTE#3 of Control Register) the diagnosis test will be considered as failed.
So the choice of **Number of Oscillation to detect**, **TIME1** and **TIME2** should be defined carefully as they depend on the self-oscillation frequency of the Antenna.

Example:

We have an antenna tuned to exactly 126 kHz.
We can set Number of Oscillation to detect =10,
Time_expected (to reach the 10^{th} edges starting from the first one) = 10-1 edges,
So, Time_expected = (9/126kHz) /2 (2 edges per frequency period!) = 35.7us

So that, knowing the resolution of 2us for Time1 and Time2, we can set
Time1 = 34us, i.e. code =0x11
Time2 = 36us, i.e. code = 0x12
Obviously we can set more margins (i.e. in our example Time1_code = 0x10, and Time2_code= 0x13), but the bigger the margin, the less accuracy in the detuning detection

A delay (Delay in Phase 4, BYTE5 of Control Register, max 30us) can be applied at the end of the Pulse 3 to filter the first pulses.
The length of Pulse 3 can be set in BYTE5 of Control Register. Its value depends also on the serial or parallel mode selected.

For more information about Diagnosis, please refer to the application note: **AN_MLX7419x_Diagnosis**

6.6.4. Current Measurement

The current measurement block allows monitoring on time the AC current flowing through the selected Output Antenna Driver.

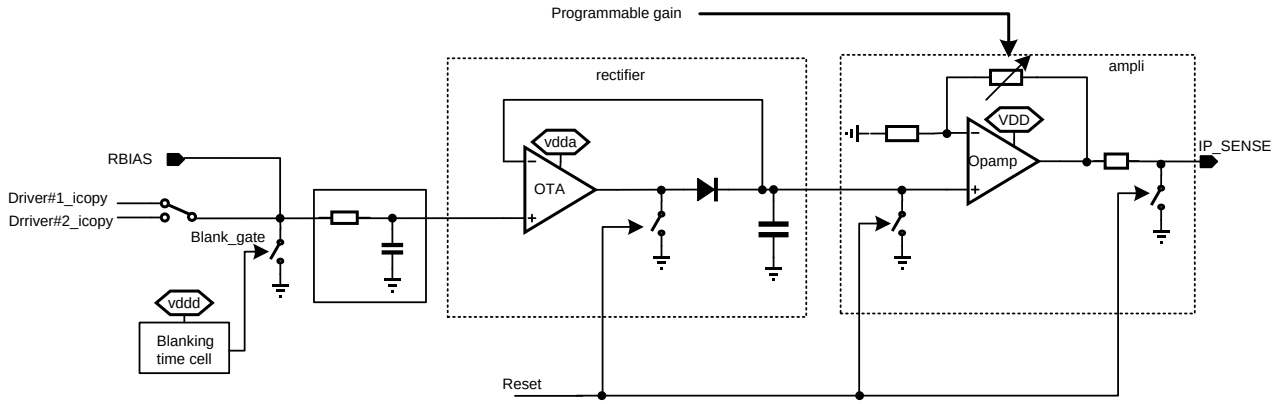


Figure 15: Current measurement, schematics principle

The signals *Driver#n_icopy* corresponds to the selected LF driver output current copied and divided by a factor of 10000. This signal is then rectified by a peak detector circuitry which is reset by each start of a transmission, and amplified by a programmable gain (3 bits) stage. The resulting voltage is available on the pin IP_SENSE which can therefore be sent to the external host MCU.
The current flowing into the LF driver output is expressed with the following formula:

$$I_{Antenna}[Ap] = V_{IPSENSE} \cdot Sensitivity$$

With the *Sensitivity* expressed in [mA/V] and selected in the register CONF_Byte6.

6.6.4.1. Electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
Tolerance of current peak detection	IP_Sense_ADx_err	-10		10	%	Sine transmission For Iout > 300mA pk. Achieved for IP_SENSE voltage equal or higher than 1.1V
		-20		20	%	Sine transmission For 100mA < Iout < 300mA pk. Achieved for IP_SENSE voltage equal or higher than 1.1V
	IP_Sense_SQ_AD_err	-10		10	%	Square transmission For Iout > 800mA pk. Achieved for IP_SENSE voltage equal or higher than 1.1V

		-20		20	%	Square transmission For 500mA < Iout < 800mA pk. Achieved for IP_SENSE voltage equal or higher than 1.1V
Rise time to the peak (after switch off Det-reset)	PeakDet_Trise			32	µs	With condition: Cipsense = 2.2nF
Reset time	PeakDet_Reset		256		µs	
Ripple voltage of IP-sense	PeakDet_Ripple			1	%	At RSSI
Hold time	PeakDet_Thold	5			ms	For less than 1% deviation
Max. output voltage	PeakDet_Vmax			VDD-0.3	V	
Bias resistor value	Rbias		5.23		kΩ	External component, **1% precision**
Capacitor on IP_Sense pin	Cipsense		2.2		nF	External component

Table 16: Current Measurements via IPSENSE pin specifications

6.6.5. AC and DC Over current

The implemented Over Current block performs a constant monitoring of the current flowing through the output drivers. In case of exceeding some fixed limits, it will immediately set the output drivers in Hi-Z and update the Status Register with the corresponding flag(s).

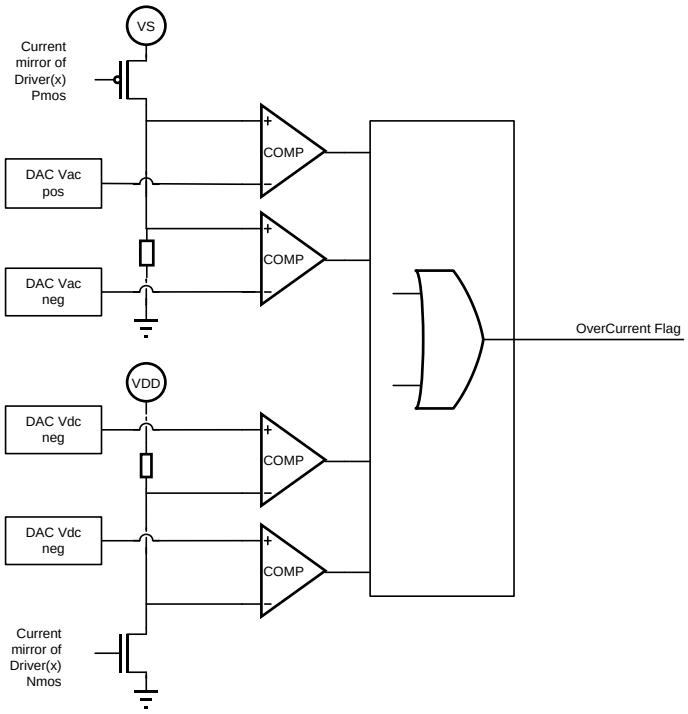


Figure 16: Over Current detection block, schematics principle

A DC output current higher than OverC_I_DCP (resp. lower than OverC_I_DCN for negative side) will trigger an over current detection. In the same way an AC output current higher than OverC_I_ACP (resp. lower than OverC_I_ACN for negative side) will trigger an over current detection.

The channel (activated or not) on which the DC or AC over current condition is detected is put in Hi-Z mode during the rest of the transmission. In case of over-current detection, the general failure flag is also set.

The over-current flags are reset when entering SLEEP mode or by sending “Go To Standby” command.

6.6.5.1. Electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
DC OverCurrent positive side	OverC_I_DCP	0.077		0.316	A	Threshold value
DC OverCurrent negative side	OverC_I_DCN	-0.316		-0.077	A	Threshold value
AC OverCurrent positive side	OverC_I_ACP	2.61		3.44	Ap	Threshold value
AC OverCurrent negative side	OverC_I_ACN	-3.44		-2.61	Ap	Threshold value
DC Overcurrent detection time	T_dc_oc	30	31	32	µs	
AC Overcurrent detection time	T_ac_oc		500		ns	
AC OverCurrent debouncing time	T_ac_deb		500		ns	

Table 17: AD/DC OverCurrent specifications

6.6.6. VDD and VS under voltage

The two Under Voltage comparators allow the monitoring of both voltages VDD and VS and are continuously checking that they do not go below certain defined values which could affect the normal device behavior.

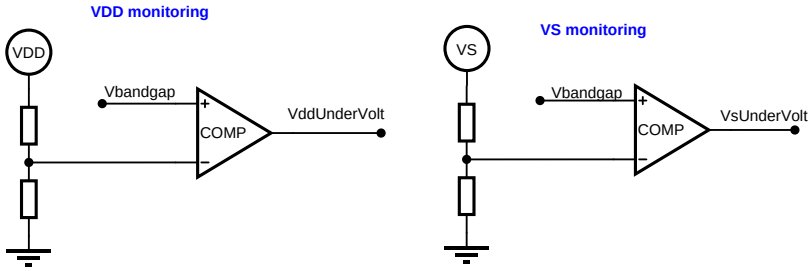


Figure 17: Under voltage detections, schematics principle

When the MLX74190 is set in active mode and the VS voltage is going below the under voltage threshold Vs_uvth, the VS undervoltage and General failure flags are both set (see Status Register). The device is then entering into STAND_BY mode.

When the MLX74190 is set in active mode and the VDD voltage is going below the under voltage threshold VDD_uvth during a time higher than Tuv_Vdd, the MLX74190 is directly entering into SLEEP, without any failure flag set. This is illustrated in the picture below.

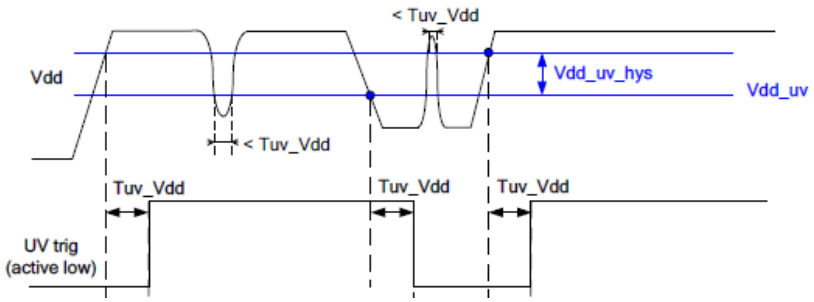


Figure 18: VDD Under voltage: timing diagram

6.6.6.1. Electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit
VS Under Voltage threshold	Vs_uv_th	5		6	V
VS Under Voltage hysteresis	Vs_uv_hys	0.1		0.275	V
VS Under Voltage Filtering time[1)]	Tuv_Vs		50		µs

Table 18: VS under voltage specifications

1) This value is dependent on the decoupling capacitors on VS; the timing will be greater than the specified value.

Parameter	Symbol	Min	Typ	Max	Unit
VDD Under Voltage threshold	Vdd_uv_th	3.97		4.3	V
VDD Under Voltage hysteresis	Vdd_uv_hys	0.075		0.2	V
VDD Under Voltage Filtering time[1), 2)]	Tuv_vdd	1		8.5	µs

Table 19: VDD Under voltage detections: timing specification

1) This value is dependent on the decoupling capacitors on VDD; the timing will be greater than the specified value.
2) Value measured with a decoupling capacitor on V_{DD} of 47nF.

6.6.7. Pre-warning (PWT) and over Temperature (OVT)

The implemented Pre-warning and Over Temperature block does a constant monitoring of the internal temperature of the 2 LF drivers. The Pre-warning flag indicates exceeding the specified temperature limit but without any action impacting the application. This could be seen as warning information. The flag can be read in Status Register. The general failure flag is NOT set if a temperature Pre-warning event occurs.

In case of exceeding the Over Temperature Threshold the corresponding flag is set and the device immediately enters in STANDBY mode. The flag can be read in the Status Register. The general failure flag is set if an Over-temperature event occurs.

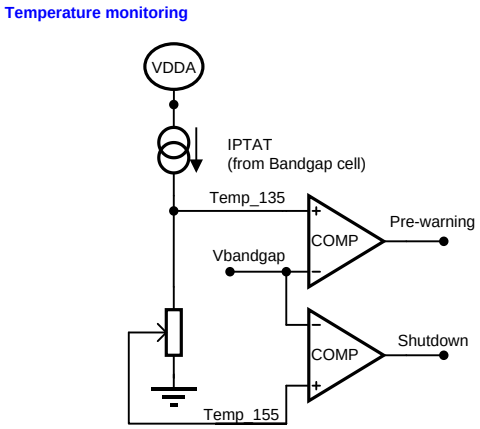


Figure 19: Temperature monitoring: schematics principle

The temperature pre-warning detection threshold is specified between T_pw_th minimum and maximum values. There is a temperature gap between the Pre-warning and Over-temperature thresholds called T_diff.

The Pre-warning and Over-temperature flags are reset when entering the SLEEP mode or when the internal temperature goes below the corresponding threshold (PWT or OVT).
The flag is also reset by sending a “Go to standby” command.

6.6.7.1. Electrical characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Temperature Pre-warning Threshold	T_pw_th	130		145	°C
Temperature Pre-warning Hysteresis	T_pwh_hys	0	0.8	2	°C
Over Temperature Threshold	T_ot_th	150		165	°C
Over Temperature Hysteresis	T_ot_hys	0	0.8	2	°C
Difference between Pre-warning and Over Temperature	T_Diff	15	20	25	°C

Table 20: Temperature monitoring specifications

6.6.8. Transmission aborted

The flag transmission aborted is set when the MLX74190 is in active mode and the working transmission data register is empty (LF data has been transmitted), the shadow register does not contain any more information (in invalid state) and the number of bits or the counter for the end of transmission is not expired. When the transmission is aborted, the device immediately enters in STANDBY with setting the corresponding flag. The general failure flag is also set.
The flag is reset by entering the SLEEP mode or with the command “go to standby”.

6.6.9. SPI error

The flag SPI error is set when the number of bits transferred to SDI during one SPI frame is not a multiple of 8. The general failure flag is also set.

The flag is reset by entering the SLEEP mode or with the command “go to standby”.

6.6.10. Unspecified SPI command

The flag unspecified SPI command is set when the SPI command received could not be identified within the SPI command set of the MLX74190. There is no consequence on the activity of the device. The general failure flag is also set.

The flag is reset by entering the SLEEP mode or with the command “go to standby”.

6.6.11. Overflow

The flag overflow is set when the SPI write pointer overtakes the read pointer. Then the remaining data of the current SPI frame is ignored. The device is entering into STANDBY mode and the general failure flag is set.

The flag is reset by entering the SLEEP mode or with the command “go to standby”.

6.7. Internal Registers

6.7.1. Summary of registers

Type of registers	Name	Byte(s)	Description	type
SPI registers	SPI shift in	1	8 bits SPI communication	R/W
	SPI shift out	1	8 bits SPI communication	R/W
Circular Buffer	Circular Buffer	48	Buffer of the SPI circular commands + data	R/W
Working Registers	Status Register	7	1 byte for general status and 6 bytes for chip status (including diagnosis result)	R
	Configuration register	14	General device configuration	R/W
	Immobilizer Configuration Register	4	Configuration of Immobilizer	R/W
	Control Register	6	Configuration of Diagnosis	R/W
	Transmission Data Format Register	4	Configuration of transmission data	R/W
	Transmission Data Register	1	Transmission data	R/W
Shadow registers	Transmission data format register	4	Transmission data format	W
	Transmission Data register	1	Transmission data	W

Table 21: Registers Summary

6.7.2. Circular Buffer

Each received SPI circular command together with its data bytes, will be stored sequentially at the address of the write pointer. The information will be read sequentially at the address of the read pointer. The data will be transferred to its destination according to the command. The length of the circular buffer = 48 bytes (384 bits).

6.7.2.1. Write operation

The write pointer of the circular buffer defines the current write address. It is controlled by the SPI state machine. Each received SPI command byte or data byte is stored at the address of the write pointer. After the write operation, the write pointer is incremented. At the end of the circular buffer, the write pointer continues with the address "0". The default value of the write pointer is "0".

6.7.2.2. Read operation

The read pointer of the circular buffer defines the current read address. The read pointer is controlled by the memory management. The circular buffer is read at the address of the read pointer. The content of the first address is a command. If the content of the read address is identified as a command, the memory management will wait until it can be executed ("SPI time out"). Then the read pointer is incremented and the following data bytes (according to the command) transferred to their destination sequentially. If the destination register is valid or active, the memory management will wait until the transfer can be executed ("SPI time out"). The content of the address after the last data byte will be the next command. At the end of the circular buffer, the read pointer continues with the address "0".

6.7.3. Status Register

This register gives information about the general status of the MLX74190 (e.g. its mode, the status of working register error flags and the result of last performed Diagnosis). Its length is 7 bytes.

When the MLX74190 is programmed to send the General Status Byte and the following Status bytes via SDO SPI pin the content of the status Register is sent for each SPI communication. If the SPI communication is shorter than 7 bytes only the first corresponding ones are sent and if the SPI communication is longer than 7 bytes the 8th and following are coded with 0xFF.

Byte Number	Bit number	Parameter	Description
0 General Status Byte	0	General Failure Flag	0: flag is set 1: flag is reset
	1 - 6	Position of SPI read register pointer	000000b: SPI write pointer is 0 byte behind the read pointer .. Until max value: 110000b: SPI write pointer is 48 bytes (or more) behind the read pointer
	7	SPI error flag	0: no error 1: error detected
1	0 -2	Mode	000: ready for next transmission 001: busy, transmitting data 010: busy, transmitting RSS1 100: busy, transmitting remote data 110: busy, diagnosis Other codes: RESERVED
	3	Configuration Register	0: invalid 1: valid
	4	Immobilizer Configuration Register	0: invalid 1: valid
	5	Control Register	0: invalid 1: valid
	6	(working)Transmission Data Register Format	0: invalid 1: valid
	7	(working) Data Register	0: invalid 1: valid
2	0	Overflow flag	0: Write pointer does not overtake the Read pointer 1: Write pointer overtakes the Read pointer
	1	Temperature pre-warning flag	0: Temperature is below pre-warning temperature 1: Temperature is above pre-warning temperature
	2	Transmission aborted flag	0: no abort of the last transmission 1: last transmission aborted
	3	Over Temperature flag	0: Temperature is below shutdown temperature 1: Temperature is above shutdown temperature
	4	RESERVED	
	5	Under Voltage at VS	0: normal voltage supply on VS 1: under voltage supply on VS
	6	RESERVED	
	7	Unspecified SPI command	0: no failure 1: Unspecified SPI command

3	0-5	Overcurrent flag	000000: no Over current 010000: Over current on OUT1 100000: Over current on OUT2 110000: Over current on OUT1 and OUT2 Other codes: RESERVED
	6-7	RESERVED	
4	0-7	RESERVED	
5	0	Diagnosis for OUT2: bit3	0: pulse diagnosis: below error threshold and OK 1: pulse diagnosis: above error threshold
	1	Diagnosis for OUT1: bit1	0: static diagnosis High Side: below error threshold and OK 1: static diagnosis High Side: above error threshold
	2	Diagnosis for OUT1: bit2	0: static diagnosis Low Side: below error threshold and OK 1: static diagnosis Low Side: above error threshold
	3	Diagnosis for OUT1: bit3	0: pulse diagnosis: below error threshold and OK 1: pulse diagnosis: above error threshold
	4-7	RESERVED	
6	0-2	RESERVED	
	3-5	Last IRQ - source	000: no IRQ 001: Wake up 010: Ready for transmission 011: start of transmission 100: Diagnosis Other codes: RESERVED
	6	Diagnosis for OUT2: bit1	0: static diagnosis High Side: below error threshold and OK 1: static diagnosis High Side: above error threshold
	7	Diagnosis for OUT2: bit2	0: static diagnosis Low Side: below error threshold and OK 1: static diagnosis Low Side: above error threshold

Table 22: Status Register

6.7.4. Configuration Register

This register allows configuring the transmission mode of the 74190; its length is 14 bytes.

6.7.4.1. Flags

Flag	Description
Valid flag	Set to valid: when the data from the circular buffer are transferred
	Set to invalid: after the end of the transmission (including CONFIG delay) based on the configuration of this register
Active flag	Set to active: when the chip enters transmission state
	Set to inactive: after the end of the transmission (including CONFIG delay) based on the configuration of this register

Table 23: Flags of Configuration Register

6.7.4.2. Write operation

When the memory management unit identifies the command "Program Configuration Register" from the circular buffer, the following data bytes are transferred to the Configuration register sequentially. In this case, the flag of the working configuration register is set to invalid. If the flag of the working Configuration Register is valid the memory management unit waits till it becomes invalid ("SPI timeout").

Byte Number	Bit number	Parameter	Description
0	0-7	RESERVED	
1	0 - 1	Antenna Driver 1 (OUT1) configuration	00: if Destroy1 = 0 then Hi-Z, if Destroy1 = 1 then transmit first destroy bit with180° phase and second destroy bit with 0° phase (default value) 01: if Destroy1 = 0 then transmit data with 180° phase, if Destroy1 = 1 then transmit first and second destroy bits with180° 10: if Destroy1 = 0 then transmit data with 0° phase, if Destroy1 = 1 then transmit first destroy bit with 0° phase and second destroy bit with180° 11: if Destroy1 = 0 then Pull Down OUT1, if Destroy1 = 1 then transmit first and destroy bits with 0° phase
	2-3	Antenna Driver 2 (OUT2) configuration	00: if Destroy2 = 0 then Hi-Z, if Destroy2 = 1 then transmit first destroy bit with180° phase and second destroy bit with 0° phase (default value) 01: if Destroy2 = 0 then transmit data with 180° phase, if Destroy2 = 1 then transmit first and second destroy bits with180° 10: if Destroy2 = 0 then transmit data with 0° phase, if Destroy2 = 1 then transmit first destroy bit with 0° phase and second destroy bit with180° 11: if Destroy2 = 0 then Pull down OUT2, if Destroy2 = 1 then transmit first and destroy bits with 0° phase

	4-6	Current measurement configuration	000: no selection (default value) 101: Select current of Antenna Driver 1 110: Select current of Antenna Driver 2 Other codes: no selection	
	7	Wave mode	0: sinusoidal (default value) 1: rectangular	
2	0-7	RESERVED		
3	0-7	RESERVED		
4	0-7	RESERVED		
5	0-5	Voltage selection for Antenna Driver 1	00001b : 0.25V sine output voltage … Until: 101100b :32V sine output voltage See Table 5: Programmable PGA gain	
	6-7	Voltage selection for Antenna Driver 2: LS bits	00001b : 0.25V sine output voltage … Until: 101100b :32V sine output voltage See Table 5: Programmable PGA gain	
6	0-3	Voltage selection for Antenna Driver 2: MS bits		
	4-5	Duty cycle for square wave	00: 6.25% (default value) 01: 12.5% 10: 25% 11: 50%	
	6-7	Sensitivity for current measurement (LS bits)	For sine wave: 000: 538 mA/V (default value) 001: 405 mA/V 010: 295 mA/V 011: 218 mA/V 100: 162 mA/V 101: 121 mA/V 110: 86 mA/V 111: 64 mA/V	For square wave: 000: 635 mA/V (deflt. value) 001: 478 mA/V 010: 348 mA/V 011: 255 mA/V 100: 198 mA/V 101: 143 mA/V 110: 103 mA/V 111: 79 mA/V
7	0	Sensitivity for current measurement (MS bit)		
	1	Default destroy configuration	0: Pull down 1: Hi-Z (default value)	
	2-5	RESERVED		
	6	Output1 destroy configuration	0: transmit data or inactive (default value) 1: transmit destroy bit	
	7	Output2 destroy configuration	0: transmit data or inactive (default value) 1: transmit destroy bit	
8	0-7	Length of telegram per block (Counter for end of transmission) LS bits	000 0000 0000b: endless until SPI command “go to standby” or “go to Sleep” or time out occurs (100ms). Not valid in normal mode	

9	0-2	Length of telegram per block (Counter for end of transmission) MS bits	000 0000 0001b: 0 bit of the data buffer in LF normal mode. 1*8/frequency_carrier in other LF mode (i.e. 64us at 125kHz) (default value) 000 0000 0010b: 1 bit of the data buffer in LF normal mode. 2*8/frequency_carrier for other LF mode … until: 111 1111 1111b: 2046 bits of the data buffer in LF normal mode. 2047*8/frequency_carrier in other LF mode
	3-4	Sending mode	00: wait for trigger command via SPI 01: Start transmission as soon as working data register is filled with 1 byte. In case of LF mode RSSI, or in Remote data mode: start transmission immediately 10: RESERVED (default value) 11: RESERVED
	5-6	LF mode	00: normal mode (default value) 01: RSSI 10: Remote data 11 : RESERVED
	7	Carrier frequency	0 : 125kHz (default value) 1 : programmed frequency configure in Immobilizer Configuration Register
10	0-7	Delay after end of frame, before starting the next frame (with the next configuration)	0000 0000b: 1*8/frequency_carrier in other LF mode (i.e. 64us at 125kHz) inclusive fixed delay (default value) … until: 1111 1111b: 256*8/frequency_carrier in other LF mode (i.e. 16.384ms at 125kHz) inclusive fixed delay
11	0-6	RESERVED	
	7	Modulation mode	0: ASK (default value) 1: PSK
12	0-7	Counter for start of transmission of destroy bits	0000 0000b =0000 0001b= 2*8/frequency_carrier in other LF mode (i.e. 128us at 125kHz) (default value) 0000 0010b =3*8/frequency_carrier … until: 1111 1111b: 256*8/frequency_carrier in other LF mode (i.e. 16.384ms at 125kHz) inclusive fixed delay
13	0	Carrier Synchronization	0: no external carrier frequency, OSC pin is set as output. Device in master mode. (default value) 1: external carrier frequency (SYNC), OSC pin is switched as an input hi-Z
	1	Output activation in LF-mode Remote data	0: immediately after configuration register is set to valid and LF mode is evaluated (device entered transmission mode) (default value) 1: before start of transmission (first rising edge of REMOTE_DATA_IN

	2	Operating state at end of transmission	0: Once the delay time has expired, stay in Standby mode during around 100ms. If no new transmission is requested, go to sleep mode. (default value) 1: : Once the delay time has expired go to sleep mode
	3-4	Output status for ASK transmission gap	00: set the output at VS/2 for sine wave mode. Pull down for square wave mode (default value) 01: set the output in Hi-Z 10: set the output in Hi-Z during the “modulation Hi-Z periods” configured in IMMO_Byte3, (number of period in Hi-z) then pull it down
	5-7	RESERVED	

Table 24: Configuration Register

6.7.5. Immobilizer Configuration Register

This register allows configuring the immobilizer function of the 74190; its length is 4 bytes.

6.7.5.1. Flags

No active flag for this register

Flag	Description
Valid flag	Set to valid: when the data from the circular buffer are transferred
	Set to invalid: on a Power down, or a command "go to sleep"

Table 25: Flags of Immobilizer Configuration Register

6.7.5.2. Write operation

When the memory management unit identifies the command "Program Immobilizer Configuration Register" from the circular buffer, the following data bytes are transferred to the Immobilizer Configuration Register sequentially.

Byte Number	Bit number	Parameter	Description
0	0-6	FSK Data bits	Set the frequency of the LF driver (see Table 4: Programmable frequency step): 0000000b: Counter steps set to 275 (default value) 0000001b: Counter steps = 225 0000010b: Counter steps = 226 …until: 1000010b: counter steps = 2901111111b: The MCU selects counter step automatically Other codes: RESERVED
	7	Glitch filter configuration, MS bit	00: Off 01: 1/16 bit period 10: 2/16 bit period 11: 4/16 bit period (default value)
1	0 -5	FSK Phase bits	000000b: Phase delay = 60/ freq_osc counts (i.e. 90°) (default value) 000001b: Phase delay = 0° 000010b: Phase delay = 4/ freq_osc 000011b: Phase delay = 8/ freq_osc … 100001b: Phase delay = 128/ freq_osc (i.e. 180°) … 111111b: Phase delay = 248/ freq_osc Note: freq_osc = 32MHz
	6-7	Data Rate	00: 2 kbit/s (default value) 01: 4 kbit/s 10: 8 kbit/s 11: RESERVED
2	0-2	FSK-RX-AFC	000b: Demodulator Threshold automatically set. (default value) 001b: Hysteresis: -1 count, Threshold: -2 counts 010b: Hysteresis: -1 count, Threshold: automatic 011b: Hysteresis: default value, Threshold: -2 counts 100b: Hysteresis: default value, Threshold: +2 counts 101b: Hysteresis: +1 count, Threshold: +2 counts Other codes: RESERVED

	3-5	Programmable delay between signal Dig_mod High and ASK demodulator start. For data rate = 2 or 4 kbit/s	000: 2*T0 (typ. 16us for T0 = 8us) 001: 2*T0 (typ. 16us) 010: 8*T0 (typ. 64us) 011: 8*T0 (typ. 64us) 100: 188*T0 (typ. 1504us) 101: 188*T0 (typ. 1504us) (not allowed for 4kbps if byte2[6-7]=01 or 10) 110: 194*T0 (typ. 1552us) 111: 194*T0 (typ. 1552us) (default value) T0 is defined in BYTE#0 (to get T0 = 8us, 0100000b should be programmed, even if bit#7 of CONF_Byte9 is set to '0')
		Programmable delay between signal Dig_mod High and ASK demodulator start. For data rate =8 kbit/s	000: 4*T0 (typ. 32us for T0 = 8us) 001: 4*T0 (typ. 32us) 010: 16*T0 (typ. 128us) 011: 16*T0 (typ. 128us) 100: 190*T0 (typ. 1520us) 101: 190*T0 (typ. 1520us 110: 202*T0 (typ. 1616us) 111: 202*T0 (typ. 1616us) (default value) T0 is defined in BYTE#0 (to get T0 = 8us, 0100000b should be programmed, even if bit#7 of CONF_Byte9 is set to '0')
	6-7	Programmable ASK Early Start time	00: no delay (default value) 01: at 2kbits: 70*T0 at 4kbits: : 35*T0 not allowed if BYTE2[3,5]=101 at 8kbits: : 18*T0 10: at 2kbits: 105*T0 at 4kbits: : 53*T0 not allowed if BYTE2[3,5]=101 at 8kbits: : 27*T0 11: at 2kbits: 140*T0 at 4kbits: : 70*T0 at 8kbits: : 35*T0 This is only valid for BYTE#2[3,5] = 100,101,110,111. In every other cases, ASK Early Start remains to 0 T0 is defined in BYTE#0 (to get T0 = 8us, 0100000b should be programmed, even if bit#7 of CONF_Byte9 Is set to '0')
3	0	Activation immobilizer	0: Immobilizer deactivated (default value) 1: Immobilizer activated
	1	Select_Demod	0: ASK Demodulation (default value) 1: FSK Demodulation
	2	Input Selection	0: ASK_RX1 or FSK_RX1 (default value) 1: ASK_RX2 or FSK_RX2
	3	Select D_OUT	0: Digital Modulation (default value) 1: Immobilizer demodulator output
	4-6	Modulation Hi-Z Period	000: no Hi-Z after switching off the carrier during modulation (default value) 001: 1 carrier period after switching off the carrier …until 111: 7 carrier periods after switching off the carrier
	7	Glitch filter configuration, LS bit	See Byte0[7]

Table 26: Immobilizer Configuration Register

6.7.6. Control Register

This register allows setup of the diagnosis feature; its length is 6 bytes.

6.7.6.1. Flags

Flag	Description
Valid flag	Set to valid: when the data from the circular buffer are transferred
	Set to invalid: on a Power down, or a command " go to sleep"
Active flag	Set to active: the chips start to perform diagnosis
	Set to inactive: after the end of the diagnosis sequence

Table 27: flags of Control Register

6.7.6.2. Write operation

When the memory management unit identifies the command "Program Control Register" from the circular buffer, the following data bytes are transferred to the Immobilizer Control Register sequentially.

Byte Number	Bit number	Parameter	Description
0	0-3	RESERVED	
	4	Diagnosis Status output1	0: GND (default value) 1: Hi-Z
	5	Diagnosis Status output2	0: GND (default value) 1: Hi-Z
	6	IRQ_mask	0: mask (default value) 1: not masked
	7	RESERVED	
1	0 -2	Perform Diagnosis output selection	100: output 1 101: output 2 111: none (default value) Other codes: RESERVED
	3	RESERVED	
	4	Adjustment of the negative resistance in case of serial resonance mode	0000b: 0 Ω (default value) 0001b: 10 Ω …until 1111b: 150 Ω
2	0-2	Duration time of pulse1 and pulse 2 (for static diagnosis)	000b: 4µs (default value) 001b: 8µs 010b: 16µs … until: 111: 512µs
	3-7	Time1 of oscillation (after first oscillation edge)	00000b: 0 µs (default value) 00001b: 2 µs 00010b: 4 µs … until: 11111b: 62 µs
3	0-1	Pulse 1 Threshold voltage of static diagnosis High side	00: 92% of VS (default value) 01: 84% of VS 10: 68% of VS 11: 36% of VS
	2	RESERVED	

	3-7	Time2 of oscillation (after first oscillation edge)	00000b: 0 µs (default value) 00001b: 2 µs 00010b: 4 µs … until: 11111b: 62 µs
4	0-4	Number of Oscillation to detect (for resonance mode)	00000b: 0 (default value) 00001b: 1 edge or 0 period 00010b: 2 edge or 0.5 period … until: 11111b: 31 edges or 15 periods
	5	Evaluation mode (for resonance mode)	0: serial (default value) 1: parallel
	6-7	Pulse 2 Threshold voltage of static diagnosis Low side	00: 12.5% of VDD (default value) 01: 25% of VDD 10: 50% of VDD 11: 100% of VDD
5	0-2	Length of pulse 3 (for resonance mode)	000 : 4 µs in serial / 0.5 µs in parallel 001 : 8 µs in serial / 1 µs in parallel 010 : 16 µs in serial / 1.5 µs in parallel 011 : 32 µs in serial / 2 µs in parallel 100 : 64 µs in serial / 2.5 µs in parallel (default value) 101 : 128 µs in serial / 3 µs in parallel 110 : 256 µs in serial / 4 µs in parallel 111 : 512 µs in serial / 5 µs in parallel
	3-6	Delay in Phase 4 (for resonance mode)	0000b: 0 µs (default value) 0001b: 2 µs 0010b: 4 µs 0011b: 6 µs …until 1111b: 30 µs
	7	RESERVED	

Table 28: Control Register

6.7.7. Transmission Data Format Register

This register defines the format of the LF data to be transmitted (stored in the Transmission Data Register); its length is 4 bytes.

Flag: for the shadow Transmission Data Format Register	Description
Valid flag	Set to valid: when the data from the circular buffer are transferred
	Set to invalid: after transmitting to the Transmission Data Format Register

Table 29: flag of shadow Transmission Data Format Register

Flag: for the working Transmission Data Format Register	Description
Valid flag	Set to valid: when the data from the Shadow Transmission Data Register have been transferred
	Set to invalid: after having transmitted the number of bits defined in the previous command " Program Transmission Data" and the Shadow Transmission Data Register is valid

Table 30: flag of working Transmission Data Format Register

6.7.7.1. Write operation

When the memory management unit identifies the command "Program Transmission Data Format" from the circular buffer, the following data bytes are transferred to the Shadow Transmission Data Format Register sequentially. For that the flag of the Shadow Transmission Data Format Register should be "invalid", otherwise the memory management will wait until it is invalid (at "SPI time out")

The content of the Shadow Transmission Data Format Register is copied to the working Transmission Data Format Register at a start of a transmission sequence. For that the flag of the working register should be "invalid" and the flag of the shadow register should be "valid"

Byte Number	Bit number	Parameter	Description
0	0	Start level of a bit "0"	0: Low (default value) 1: High
	1-7	Length of T1 (transmission of a "0")	0000000b: 0 (default value) 0000001b: 1/freq_carrier (i.e. 8us for 125kHz) …until: 1111111b: 127/freq_carrier (i.e. 1016us for 125kHz)
1	0 -7	Length of T2 (transmission of a "0")	00000000b: 0 (default value) 00000001b: 1/freq_carrier (i.e. 8us for 125kHz) …until: 11111111b: 255/freq_carrier (i.e. 2040us for 125kHz)
2	0	Start level of a bit "1"	0: Low (default value) 1: High
	1-7	Length of T3 (transmission of a "1")	0000000b: 0 (default value) 0000001b: 1/freq_carrier (i.e. 8us for 125kHz) …until: 1111111b: 127/freq_carrier (i.e. 1016us for 125kHz)
3	0 -7	Length of T4 (transmission of a "1")	00000000b: 0 (default value) 00000001b: 1/freq_carrier (i.e. 8us for 125kHz) …until: 11111111b: 255/freq_carrier (i.e. 2040us for 125kHz)

Table 31: Transmission Data Format Register

6.7.8. Transmission Data Register

This register stores the data to be transmitted in LF normal mode, its length is 1 byte.

One optional shadow register (1 byte) is available, it can be reloaded while the working Transmission Data Format Register is being used. The data are transmitted bit by bit according the format defined in the Transmission Data Format Register. After having sent the LSB of the working register, the content of shadow register is copied and the data telegram will continue with the MSB of the reloaded working data register.

The data to be transmitted is configured using the command “Program transmission data”. The full data to be transmitted are internally stored and sent byte-by-byte through the Transmission data register.

6.7.8.1. Flags

Flag: for the shadow Transmission Data Register	Description
Valid flag	Set to valid: when the data from the circular buffer are transferred
	Set to invalid: after transmitting to the working Transmission Data Register

Table 32: flag of shadow Transmission Data Register

Flag: for the working Transmission Data Register	Description
Valid flag	Set to valid: when the data from the shadow Transmission Data Register are transferred
	Set to invalid: after transmitting of the LSB, or when the number of bits defined in the previous command “ Program Transmission Data” are transmitted
Active flag	Set to active: the chips start to transmit the MSB of the working register
	Set to inactive: after having transmitted the LSB, or when the number of bits defined in the previous command “ Program Transmission Data” are transmitted

Table 33: flag of working Transmission Data Register

6.7.8.2. Write operation

When the memory management unit identifies the command "Program Transmission Data Register" from the circular buffer, the following data bytes are transferred to the shadow Transmission Data Register sequentially. For that, the flag of the shadow register should be “invalid“, otherwise the memory management will wait until it is set to “invalid” (at “SPI time out”)
The content of the Shadow Transmission Data Register is copied to the working Transmission Data Register at a start of a transmission sequence. For that the flag of the shadow register should be “valid”. The content of the shadow register is copied to the working register to reload it once it has expired (LSB has been transmitted). For that the flags of the working register should be both “invalid” and “inactive”, and the flag of the shadow register is “valid”

6.8. Transmission Sequence

Sending mode[1:0] CONF_Byte9	LF mode = normal	LF mode = RSSI	LF mode = REMOTE DATA
00	Wait for direct SPI command 0xF0 “Start transmission” before transmitting LF data		Wait for transition on REMOTE_DATA_IN input
01	Start transmission as soon as working transmission data register is filled-in with the 1st byte	Start transmission immediately	

Table 34: Transmission sequence

7. General electrical characteristics

All the following specifications are valid in the complete temperature range: -40 / 105°C.

7.1. Power On Reset

Parameter	Symbol	Min	Typ	Max	Unit
POR Threshold	Por_Thres	1.6		2.8	**V**
POR Hysteresis	**Por_Hyst**	**0.1**		**0.6**	**V**

Table 35: Power On Reset specifications

7.2. Frequencies specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
Input clock frequency	f_CLK_IN	1.75	2.0	2.25	MHz	External frequency set, for which the PLL is able to lock
Input clock frequency duty cycle	CLK_IN_DC	8		94	%	For time ON of CLK_IN
PLL frequency	f_PLL	31.92	32	32.08	MHz	For f_CLK_IN= 2MHz
PLl jitter	PLL_jit	-200		200	ps	
LF accuracy at 125kHz	LF_acc	-0.1		0.1	kHz	For LF set to 125kHz
LF maximum deviation	LF_maxdev	-200		200	Hz	On the whole programmable range, for f_CLK_IN = 2MHz

Table 36: Frequencies specifications

7.3. Digital input-output specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
Input voltage High	Vdig_High	2.5		VDD+0.3	V	For every digital input pin
Input voltage Low	Vdig_Low	-0.3		0.8	V	For every digital input pin
Input voltage hysteresis	Vdig_Hyst	200		950	mV	For every digital input pin including REMOTE_DATA_IN
Input pins Leakage, for every digital input pins	Leak_H	-		0.1	µA	for Vpin = 5.5V
	Leak_L	-0.1		0.1	µA	Vpin = 0V
Leakage on pin CLK_IN	Leak_H_CLK_IN	0		10	µA	With V_CLK_IN = 5.5V
Leakage on pin OSC, configured as input pin	Leak_H_OSC	-		300	µA	With V_OSC = 5.0V
	Leak_L_OSC	-0.1		0.11	µA	With V_OSC = OV
Wake-up pin filtering time	WUP1_filt	1	3	5	µs	Glitch filter to avoid unwanted sleep mode entries
Output voltage High, for pins SDO, IRQ, D_OUT and CLK_OUT	VOH_drop	0		0.4	V	Max. Voltage drop (loss) versus VDD, with a load of 1mA
Output voltage Low, for pins SDO, IRQ, D_OUT and CLK_OUT	VOL_drop	0		0.4	V	Maximum Voltage drop, with a load of -1mA
Output voltage High, for pin EXT_CLK	VOH_EXT_CLK	0		1.6	V	Maximum Voltage drop (loss) versus VDD, with a load of 1mA
Output voltage low, for pin EXT_CLK	VOL_EXT_CLK	0		1.2	V	Maximum Voltage drop with a load of -1mA
REMOTE_DATA_IN filtering time	RDI_filt	0.5		2.5	µs	With 1nF external capacitor on pin REMOTE_DATA_IN

REMOTE_DATA_IN filtering asymmetry	RDI_filt_asy	-0.9		0.9	µs	
OSC pin propagation delay (input/output)	OSC_delay			62.5	ns	

Table 37: Digital input/output specifications

7.4. Current consumptions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
Sleep mode, VDD= 5V, VS =12V	I_sleep_VS_12V		60	110	µA	Both contributions of VDD and VS supplies
Sleep mode, VDD= 5V, VS = 40V	I_sleep_VS_40V		75	170	µA	Both contributions of VDD and VS supplies
Standby mode, for VDD= 5V	I_VDD_standby			13.5	mA	Contribution of VDD only
Standby mode VS= 40V	I_VS_standby			1.5	mA	Contribution of VS only
Transmission mode, VDD=5V	I_VDD_TX	0		15	mA	Contribution of VDD only, without immobilizer current consumption
Transmission mode, VDD= 5V, with FSK immobilizer	I_Immo_FSK	0		23	mA	Contribution of VDD only
Transmission mode, VDD= 5V, with ASK immobilizer	I_Immo_ASK	0		55	mA	Contribution of VDD only
Consumption per activated output driver, VDD= 5V	I_VDD_AD	1		5	mA	Contribution of VDD only
Consumption per activated output driver, in sine mode, VS =40V	I_active_sine_AD	5		25	mA	Contribution of VS only
Consumption per activated output driver, in square mode, VS =40V	I_active_square_AD	1		7	mA	Contribution of VS only
Consumption in mode LS-ON/ HS-OFF	I_lson	0.4		1.7	mA	Contribution of VS only

Table 38: Current consumption specifications

7.5. Start-up time

Parameter	Symbol	Min.	Typ.	Max.	Unit	Comment
Xtal (external resonator) settling time	T_{XTAL}	40	50	120	µs	With a resonator MuRata CSTCR4M00G55R0
Time after VDD reaches 4,5V and before WUP triggering	T_{WUP}	200			µs	
Time between rising edge on WUP and IRQ generation[1)]	T_{IRQ}	150	428	861	µs	No XTAL / including PLL lock time
		207	478	981	µs	With a resonator Murata CSTR4M00G55R0
IRQ pulse length after Wake-up	$T_{IRQpulse}$	60	64	68	µs	
Time between IRQ after Wake-up and LF signal generator ready for transmission	T_{LF}	0		45	µs	

Table 39: Start-up time specifications

IRQ signal is generated only when the built-in PLL has been stabilized. Consequently, this time is included in the PLL settling time.

8. Application Information

Typical application schematic is shown below:

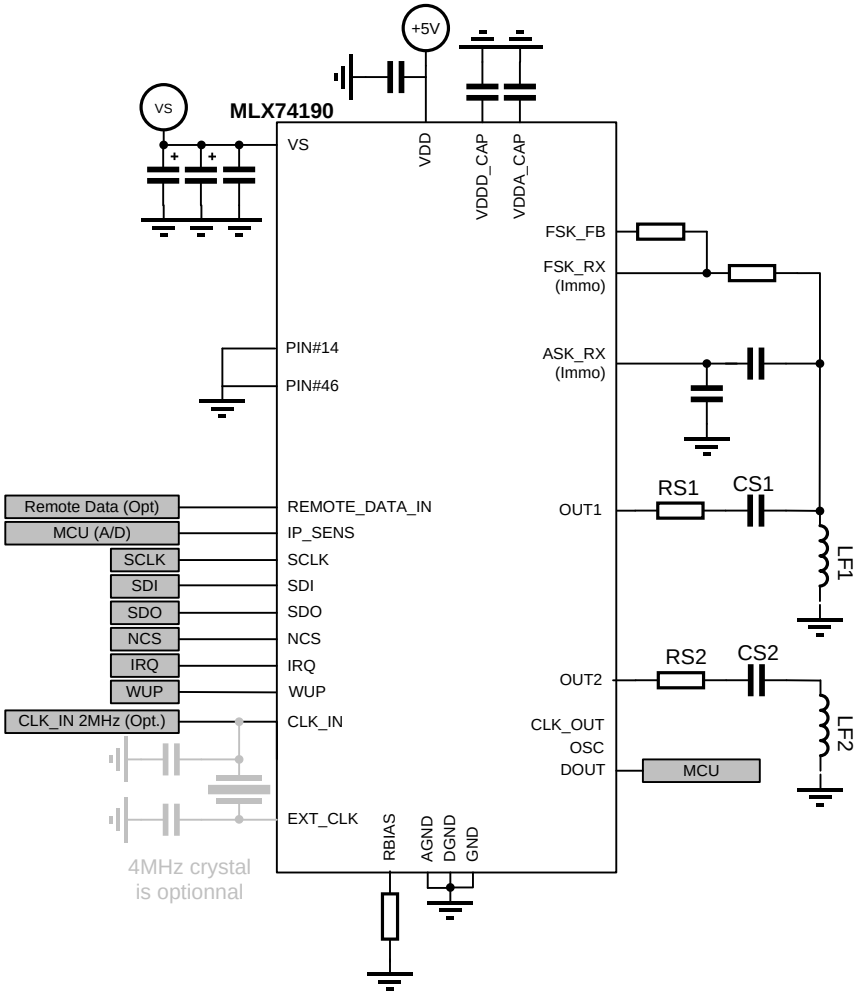


Figure 20: typical application schematic passive start

In order to increase the number of antennas, 2 or more MLX74190 can be connected together in a system of master/slave devices (see chapter "Specific case of Modulation through pin REMOTE_DATA_IN, chaining devices.")
The figure below shows how two MLX74190 can be connected together.
Note that in this case, only the immobilizer function from the slave device can be used (the pin D_OUT of the master IC is already used for transmitting the modulated data to the pin REMOTE_DATA_IN of the slave IC)

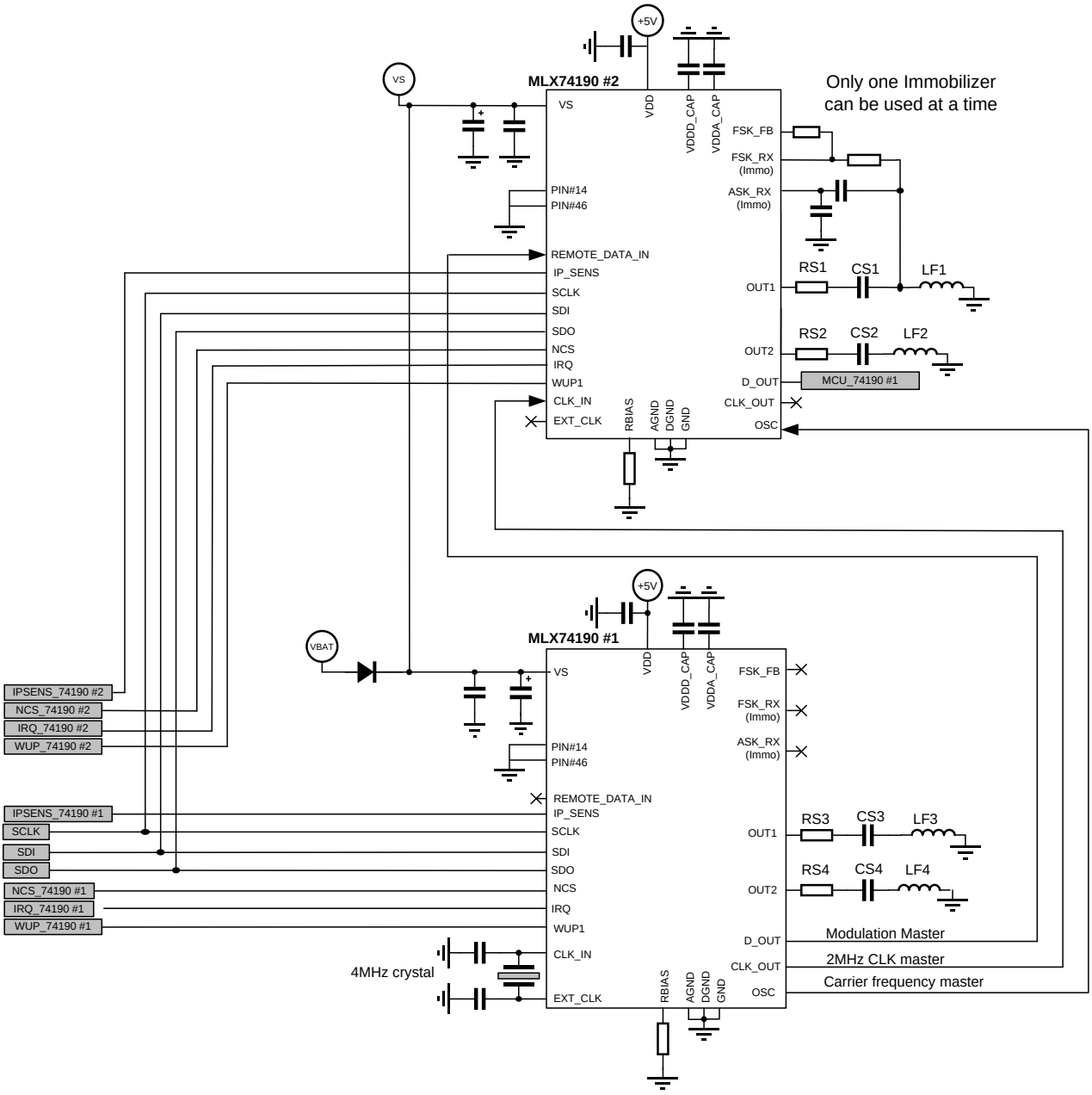


Figure 21: typical application schematic for dual devices in master/slave configuration

9. Package and marking information

9.1. Package data TQFP eP 48L (7x7, 48 leads)

	A	A1	A2	b	b1	D	D1	D2	E	E1	E2	e	L	N	ccc	ddd
Min	-	0.05	0.95	0.17	0.17	9.00	7.00	4.00	9.00	7.00	4.00	0.50	0.45	48	-	-
Nom	-	-	1.00	0.22	0.20								0.60		-	-
Max	1.20	0.15	1.05	0.27	0.23								0.75		0.08	0.08

Notes:

1. All Dimensioning and Tolerances conform to ASME Y14.5M-1994,
Δ2. Datum Plane [-|-|-] located at Mould Parting Line and coincident with Lead, where Lead exists, plastic body at bottom of parting line.
Δ3. Datum [A-B] and [-D-] to be determined at centreline between leads where leads exist, plastic body at datum plane [-|-|-]
Δ4. To be determined at seating plane [-C-]
Δ5. Dimensions D1 and E1 do not include Mould protrusion. Dimensions D1 and E1 do not include mould protrusion. Allowable mould protrusion is 0.254 mm on D1 and E1 dimensions.
6. 'N' is the total number of terminals
Δ7. These dimensions to be determined at datum plane [-|-|-]
8. Package top dimensions are smaller than bottom dimensions and top of package will not overhang bottom of package.
Δ9. Dimension b does not include dam bar protrusion, allowable dam bar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition, dam bar can not be located on the lower radius of the foot.
10. Controlling dimension millimetre.
11. maximum allowable die thickness to be assembled in this package family is 0.38mm
12. This outline conforms to JEDEC publication 95 Registration MS-026, Variation ABA, ABC & ABD.
Δ13. A1 is defined as the distance from the seating plane to the lowest point of the package body.
Δ14. Dimension D2 and E2 represent the size of the exposed pad. The actual dimensions are specified ion the bonding diagram, and are independent from die size.
15. Exposed pad shall be coplanar with bottom of package within 0.05.

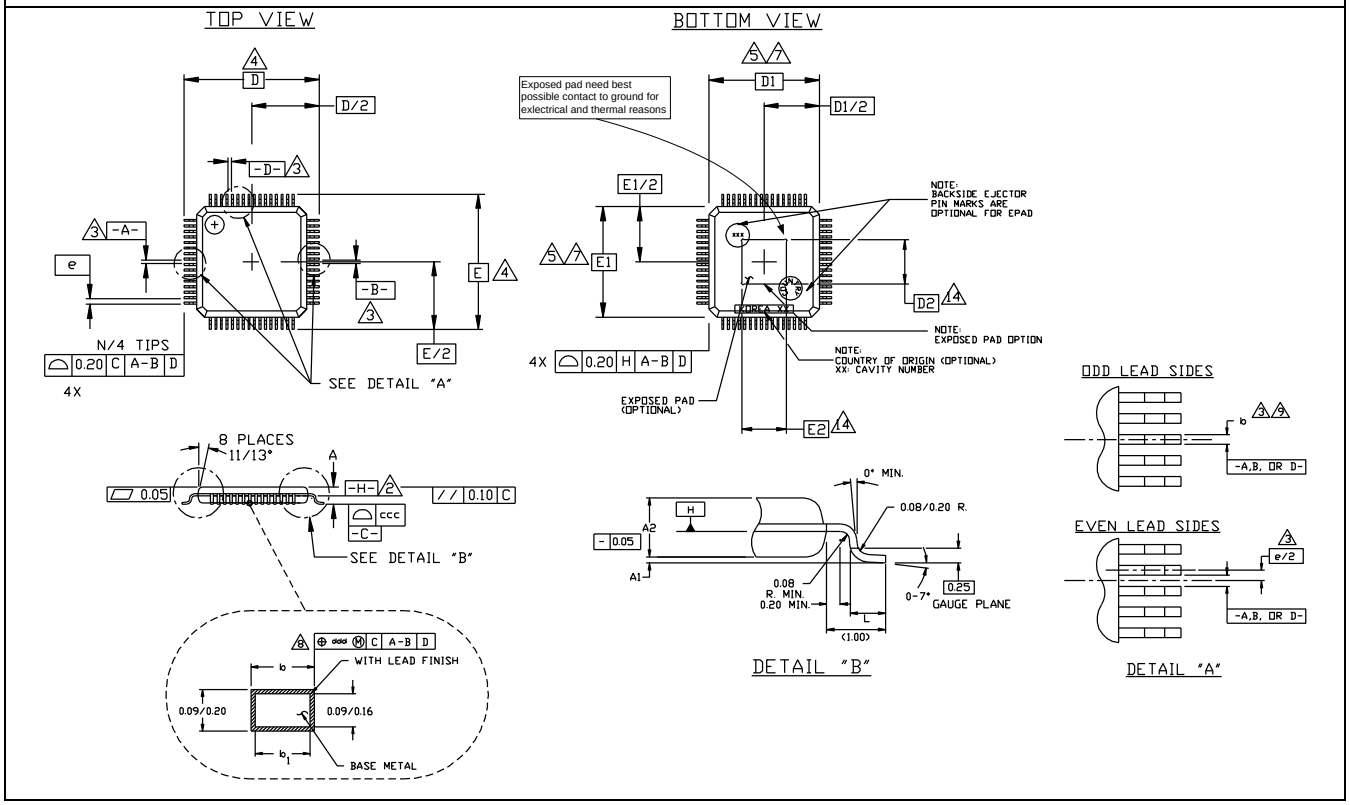


Figure 22: Package Information

9.2. Marking instruction

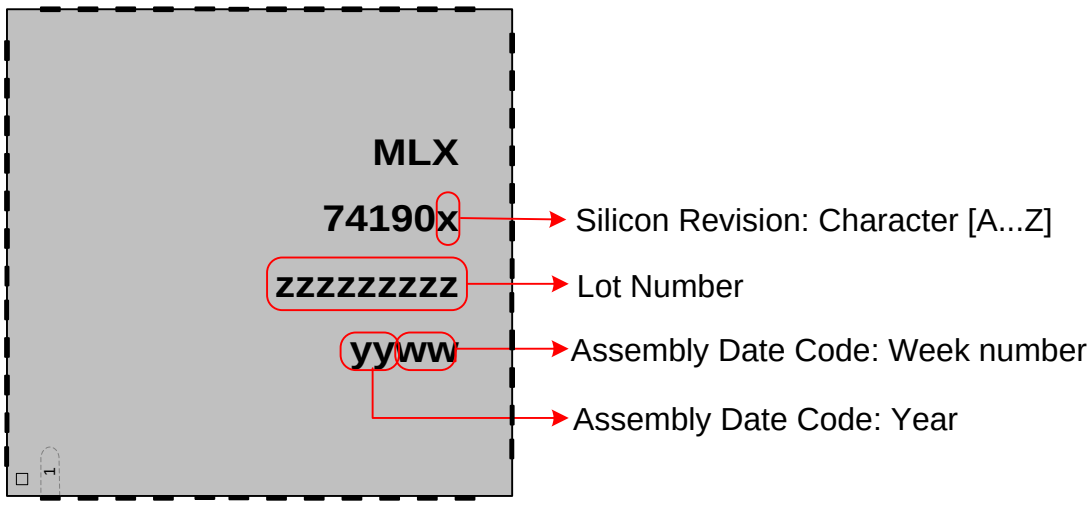


Figure 23: Marking example on IC package TQFP EP 7x7

10. Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc…) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis recommends reviewing on our web site the General Guidelines soldering recommendation (http://www.melexis.com/Quality_soldering.aspx) as well as trim&form recommendations (http://www.melexis.com/Assets/Trim-and-form-recommendations-5565.aspx).

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website: http://www.melexis.com/quality.aspx

11. Contact

For the latest version of this document, go to our website at www.melexis.com.

For additional information, please contact our Direct Sales team and get help for your specific needs:

Europe, Africa	Telephone: +32 13 67 04 95
	Email : sales_europe@melexis.com
Americas	Telephone: +1 603 223 2362
	Email : sales_usa@melexis.com
Asia	Email : sales_asia@melexis.com

12. Disclaimer

The information furnished by Melexis herein ("Information") is believed to be correct and accurate. Melexis disclaims (i) any and all liability in connection with or arising out of the furnishing, performance or use of the technical data or use of the product(s) as described herein ("Product") (ii) any and all liability, including without limitation, special, consequential or incidental damages, and (iii) any and all warranties, express, statutory, implied, or by description, including warranties of fitness for particular purpose, non-infringement and merchantability. No obligation or liability shall arise or flow out of Melexis' rendering of technical or other services.
The Information is provided "as is" and Melexis reserves the right to change the Information at any time and without notice. Therefore, before placing orders and/or prior to designing the Product into a system, users or any third party should obtain the latest version of the relevant information to verify that the information being relied upon is current.
Users or any third party must further determine the suitability of the Product for its application, including the level of reliability required and determine whether it is fit for a particular purpose.
The Information is proprietary and/or confidential information of Melexis and the use thereof or anything described by the Information does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other intellectual property rights.
This document as well as the Product(s) may be subject to export control regulations. Please be aware that export might require a prior authorization from competent authorities.
The Product(s) are intended for use in normal commercial applications. Unless otherwise agreed upon in writing, the Product(s) are not designed, authorized or warranted to be suitable in applications requiring extended temperature range and/or unusual environmental requirements. High reliability applications, such as medical life-support or life-sustaining equipment are specifically not recommended by Melexis.
The Product(s) may not be used for the following applications subject to export control regulations: the development, production, processing, operation, maintenance, storage, recognition or proliferation of 1) chemical, biological or nuclear weapons, or for the development, production, maintenance or storage of missiles for such weapons: 2) civil firearms, including spare parts or ammunition for such arms; 3) defense related products, or other material for military use or for law enforcement; 4) any applications that, alone or in combination with other goods, substances or organisms could cause serious harm to persons or goods and that can be used as a means of violence in an armed conflict or any similar violent situation.
The Products sold by Melexis are subject to the terms and conditions as specified in the Terms of Sale, which can be found at https://www.melexis.com/en/legal/terms-and-conditions.

This document supersedes and replaces all prior information regarding the Product(s) and/or previous versions of this document.

ISO/TS 16949 and ISO14001 Certified