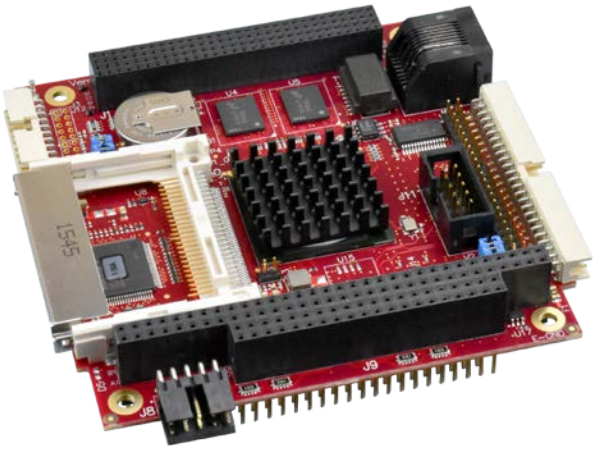
Reference Manual

REV. November 2020



VL-EPM-16 (Tomcat)

DMP Vortex-based SBC with Ethernet, CompactFlash, Serial, and USB

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Notice:

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VersaLogic reserves the right to revise this product and associated documentation at any time without obligation to notify anyone of such changes.

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Product Revision Notes

Revision 4.05 – Updated power supply and adapter information (pages 6,7 and 14)

Revision 4.03 – Updated board size in Technical Specifications

Revision 4.02 – Updated Web links

Revision 4.01 – Updated Web links

Revision 4.00 – Updated ground signal for the null modem. Renamed CBR-5009 pin description. Updated system temperature specification. Update memory address range for PC/104. Updated interrupt control register information.

Revision 3.00 – Updated power requirements, removed CMOS Setup screens (retained reference to KnowledgeBase). Performed grammatical edit.

Revision 2.00 – Minor changes were made to the board and wiring to improve functionality and make the VL-EPM-16 more compatible with the VL-EPM-4.

Revision 1.00 – Commercial release.

Support

The VL-EPM-16 product page contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- Photograph of the circuit board
- BIOS information and upgrades
- Utility routines and benchmark software

This is a private page for VL-EPM-16 users that can be accessed only by entering this address directly. It cannot be reached from the VersaLogic homepage.

Contents

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Introduction 1

Description

Features and Construction

The VL-EPM-16 (Tomcat) is a feature-packed single board computer (SBC) in a compact PC/104-*Plus* format. The VL-EPM-16 is designed for OEM control projects requiring compact size, high reliability, and longevity (product lifespan). Its features include:

- DMP Vortex86DX System-on-Chip (SoC) x86 processor
- 128 or 256 MB DDR2 memory system RAM
- 10BaseT/100BaseTX Ethernet
- PC/104, PC/104-*Plus* expansion interface
- Two USB 1.1/2.0 ports
- Console redirection to COM port or optional video expansion with EPM-VID-3 via PC/104-*Plus* interface
- IDE controller (ATA/66, Ultra ATA/66, ATA-5, UDMA 3-4), one channel, up to two devices
- Four COM ports: two RS-232, two RS-232/422/485
- Parallel port
- CompactFlash socket
- 8254 timer with three independent 16-bit timers; two general purpose timer inputs on user I/O connector
- TVS devices for ESD protection
- Watchdog timer
- PS/2 keyboard and mouse interface
- Field upgradeable BIOS with OEM enhancements
- Battery-backed real time clock
- PC/104 standard 3.55 x 3.775 inch footprint
- Vcc sensing reset circuit
- RoHS-compliant
- Extended temperature options
- Customization available

The VL-EPM-16 is compatible with popular operating systems such as Windows CE, Windows XP Professional/XP Embedded (SP3), Linux, VxWorks, and QNX (see the VersaLogic OS Compatibility Chart). (Windows 7 will not install with less than 512 MB RAM.)

The VL-EPM-16 features high reliability design and construction, including voltage sensing reset circuits and self-resetting fuses on the +5V supplies to the user I/O connectors.

VL-EPM-16 boards are subjected to 100% functional testing and are backed by a limited two-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional SBC.

Technical Specifications

Specifications are typical at 25°C with +5V supply unless otherwise noted.

Board Size:
3.755 x 3.775 inches (PC/104 standard)
Storage Temperature:
-40° to +85°C
Operating Temperature:
VL-EPM-16S, V: 0°C to +70°C, no airflow
VL-EPM-16E, F: -40° to +85°C, no airflow
Power Requirements: *with 128 MB RAM (S, E) or 256 MB RAM (V, F), keyboard, mouse running Windows XP*
VL-EPM-16S, E, F, V:
800 MHz +5V ± 5% @ 0.60 A (3.0 W)
+3.3V or ±12V may be required by some expansion modules
System Reset:
Vcc sensing, resets below 4.70V typ.
Watchdog timeout (warm/cold reset)
DRAM:
Soldered-on 128 MB (S, E) or 256 MB (V, F)
FBGA-60 DDR2
VL-EPM-16S, V – 667 MHz
VL-EPM-16E, F – 600 MHz
Video Interface:
Optional EPM-VID-3 expansion
Console redirection to COM port
IDE Interface:
One channel, 44-pin, 2 mm connector; supports up to and including ATA/66 interface; supports two parallel ATA IDE devices (hard drive, CD-ROM, Disk-on-Module, CF, etc.)
Flash Storage:
CompactFlash socket, shares IDE channel, master or slave, supports DMA
LPT Interface:
Supports one parallel port
Ethernet Interface:
Autodetect 10BaseT / 100BaseT Ethernet controller built in to Vortex86DX, 12K transmit/receive buffer
COM1-2 Interface:
RS-232, 16C550 compatible, 115 Kbps max.
COM3-4 Interface:
RS-232/422/485, 16C550 compatible, 115 Kbps max., 4-wire RS-232 (only CTS and RTS handshaking)
USB:
Two USB 1.1/2.0 ports
Audio:
Speaker output
BIOS:
American Megatrends BIOS with OEM enhancements.
Bus Speed:
PC/104-*Plus* (PCI): 33.33 MHz
PC/104 (ISA): 8.33 MHz
Compatibility:
PC/104 – Full compliance
Weight:
VL-EPM-16S, V – 0.094 kg (0.208 lb)
VL-EPM-16E, F– 0.099 kg (0.218 lb)

Specifications are subject to change without notice.

Block Diagram

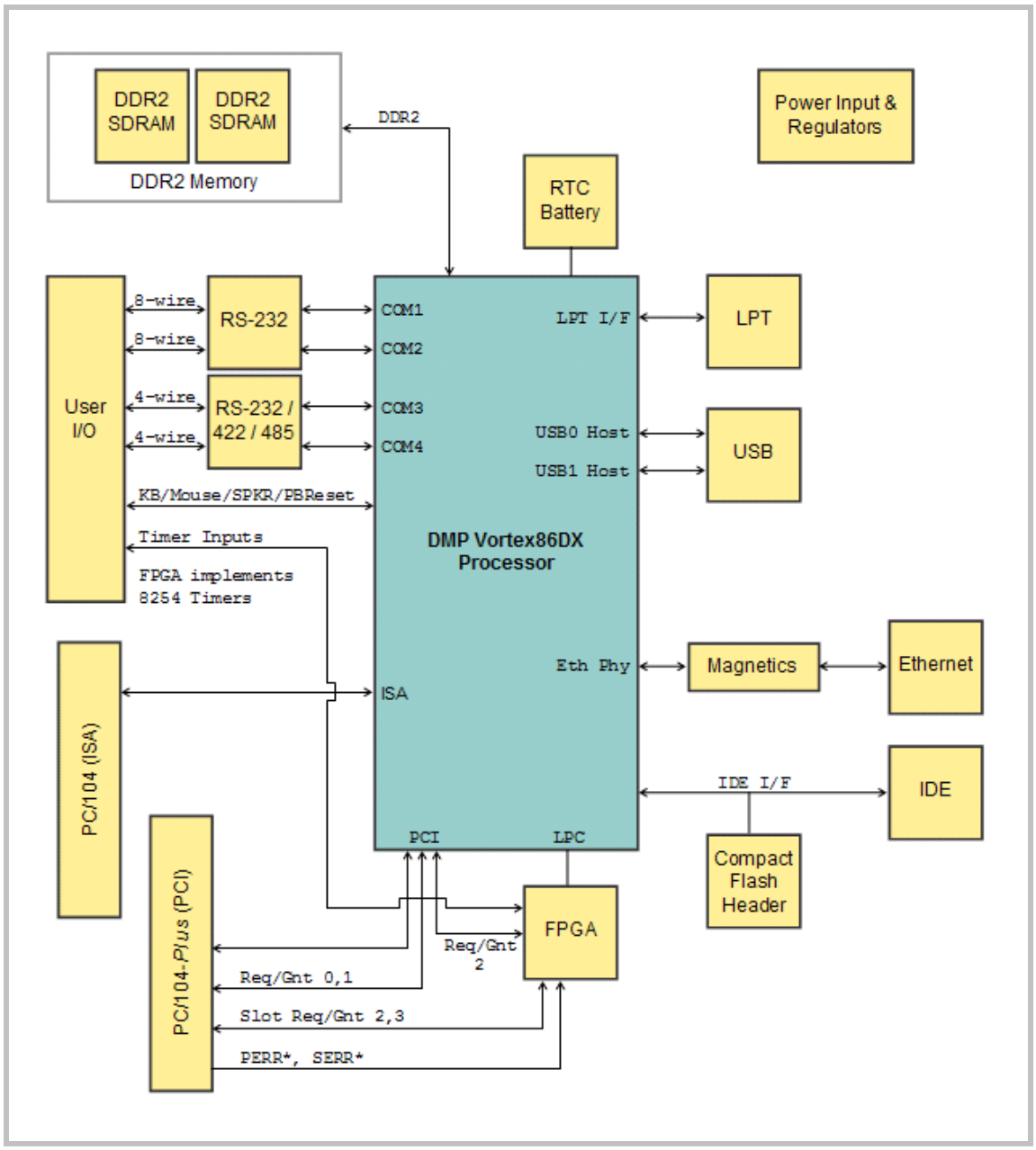

Figure 1. System Block Diagram

RoHS Compliance

The VL-EPM-16 is RoHS-compliant.

About RoHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corp. is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

Electrostatic Discharge

Warning! Electrostatic discharge (ESD) can damage circuit boards, disk drives, and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic antistatic envelope during shipment or storage.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom side of the VL-EPM-16.

Lithium Battery

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly and in an environmentally suitable manner.

HANDLING CARE

Warning! Care must be taken when handling the board not to touch the exposed circuitry with your fingers. Though it will not damage the circuitry, it is possible that small amounts of oil or perspiration on the skin could have enough conductivity to cause the contents of CMOS RAM to become corrupted through careless handling, resulting in CMOS resetting to factory defaults.

Technical Support

If you are unable to solve a problem after reading this manual, visit the VL-EPM-16 product page at the link below. The support page provides links to component datasheets, device drivers, and BIOS and PLD code updates.

VL-EPM-16 Product Page

If you have further questions, contact VersaLogic Technical Support at 503-747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling 503-747-2261.

Please provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges, and return shipping fees. Specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Mark the RMA number clearly on the outside of the box before returning.

Configuration and Setup 2

Initial Configuration

The following components are recommended for a typical development system with the VL-EPM-16 computer:

- ATX power supply
- Standard I/O breakout board (VL-CBR-5009 with adapter cable)
- USB or PS/2 keyboard and mouse
- IDE hard drive
- IDE CD-ROM drive
- EPM-VID-3 for video support

The following VersaLogic cables are recommended:

- VL-CBR-1008 – Power adapter cable - VL-PS-ATX12-300A ATX development power supply (requires VL-CBR-2034)
- VL-CBR-4406 – IDE data cable
- VL-CBR-4405 – IDE adapter board, if you are using drives with 40-pin connectors
- VL-CBR-1013 – Two-port USB adapter board and cables
- VL-CBR-2012 (or Hirose alternative VL-CBR-2010) or VL-CBR-2011 (JAE) LVDS adapter cable; or VL-CBR-1201 SVGA adapter cable

You will also need an operating system installation CD-ROM.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The VL-EPM-16 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the VL-EPM-16 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the VL-EPM-16 and their interface and power cables.

It is recommended that you attach standoffs to the board (see Hardware Assembly) to stabilize the board and make it easier to work with.

Figure 2 shows a typical start-up configuration.

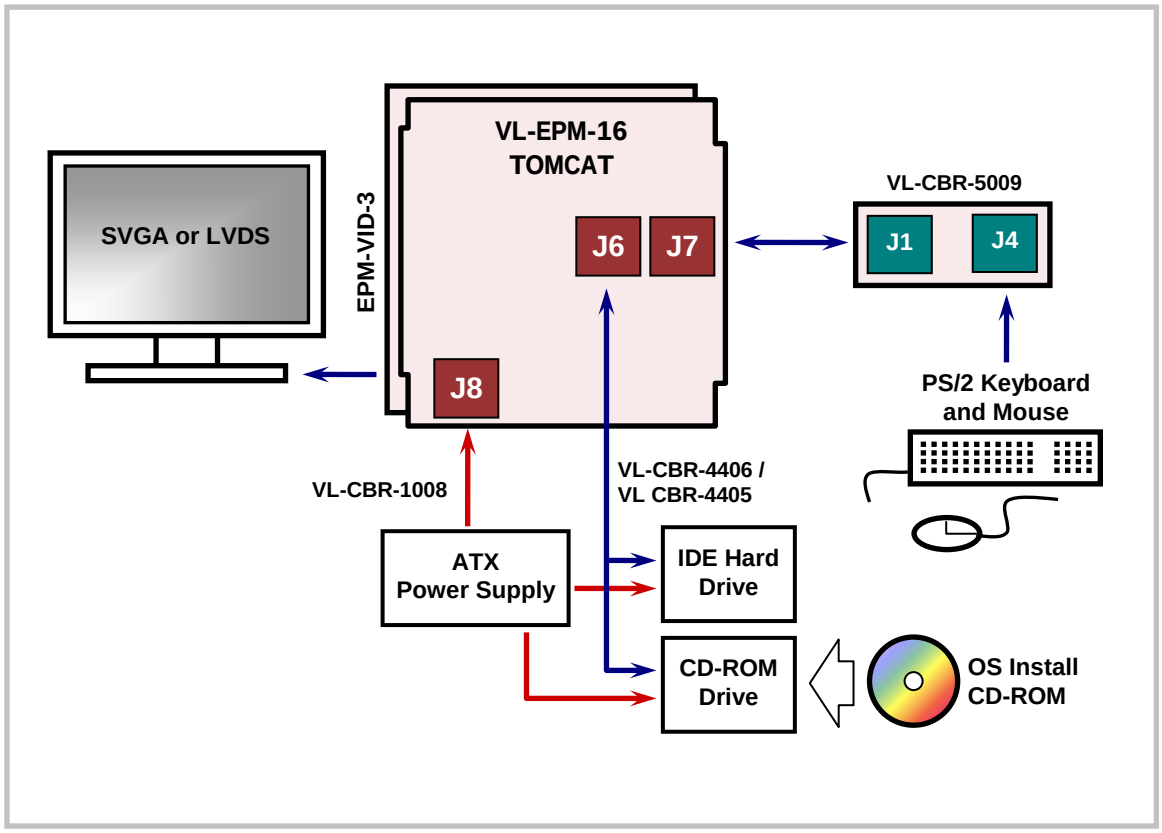

Figure 2. Typical Start-up Configuration

1. Attach Cables and Peripherals

- Install the video card on the bottom of the VL-EPM-16, configured for PC/104-*Plus* Slot 0. (The EPM-VID-3 can also be stacked on top of the VL-EPM-16, but stacking it on the bottom allows greater access to the connectors on the top of the CPU board.)
- Plug the LVDS or SVGA cable into the appropriate EPM-VID-3 connector.
- Plug the breakout board VL-CBR-5009 into socket J7.
- Plug a PS/2 keyboard and mouse into socket J4 of the breakout board. (If using a USB keyboard and mouse, use the VL-CBR-1013 USB adapter cable, attached to header J11.)
- Plug the hard drive data cable VL-CBR-4406 into socket J6. Attach a hard drive and CD-ROM drive to the connectors on the cable. If the hard drive is 3.5-inch, use the 2 mm to 0.1-inch adapter VL-CBR-4405 to attach the IDE cable.
- Attach an ATX power cable to any 3.5-inch drive (hard drive or CD-ROM drive).
- Set the hard drive jumper for master device operation and the CD-ROM drive jumper for slave device operation.

3. Attach Power

- Plug the power adapter cable VL-CBR-1008 into socket J8. Attach the motherboard connector of the ATX power supply to the adapter. VL-PS-ATX12-300A ATX development power supply (requires VL-CBR-2034)

4. Review Configuration

- Before you power up the system, double check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the VL-EPM-16 and peripheral devices.

5. Power On

- Turn on the ATX power supply and the video monitor. If the system is correctly configured, a video signal should be present. (There might be a delay of several seconds before the video signal becomes present.)

6. Install Operating System

- Install the operating system according to the instructions provided by the operating system's manufacturer. (See Operating System Installation.)

  Note: If you intend to operate the VL-EPM-16 under Windows XP or Windows XP Embedded, be sure to use Service Pack 3 (SP3) for full support of the latest device features.

Operating System Installation

The standard PC architecture used on the VL-EPM-16 makes the installation and use of most of the standard x86-based operating systems very simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the operating system. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the VL-EPM-16 Product Page**.**

Dimensions and Mounting

VL-EPM-16 Dimensions

The VL-EPM-16 complies with PC/104-*Plus* dimensional standards. Dimensions are given below to help with pre-production planning and layout.

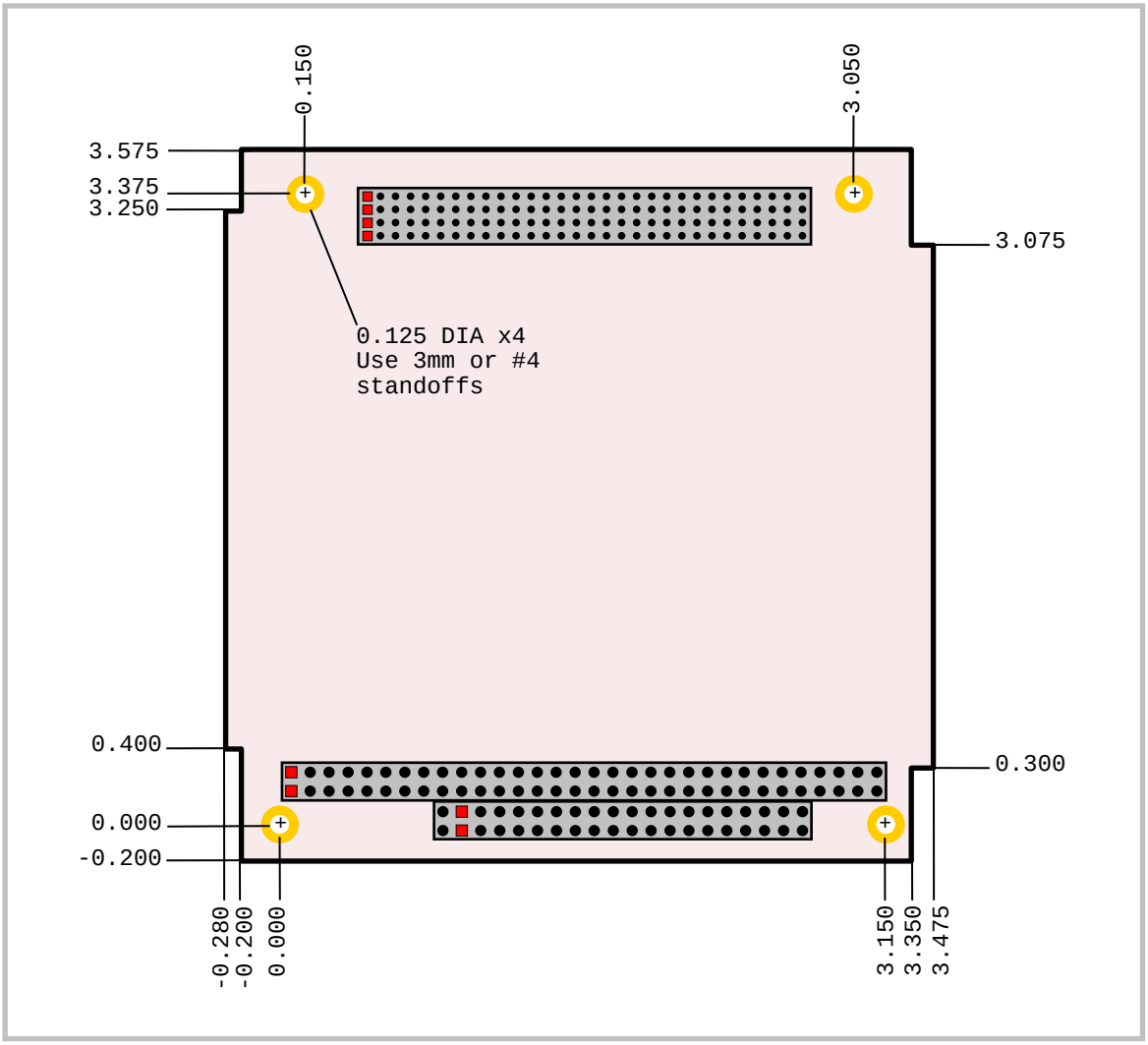

Figure 3. VL-EPM-16 Dimensions and Mounting Holes

(Not to scale. All dimensions in inches.)

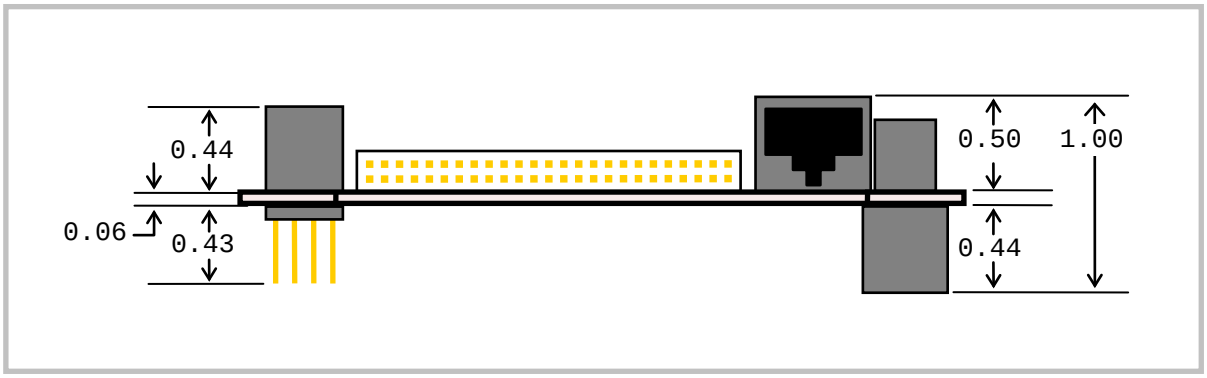

Figure 4. VL-EPM-16 Height Dimensions

(Not to scale. All dimensions in inches.)

VL-CBR-5009 DIMENSIONS

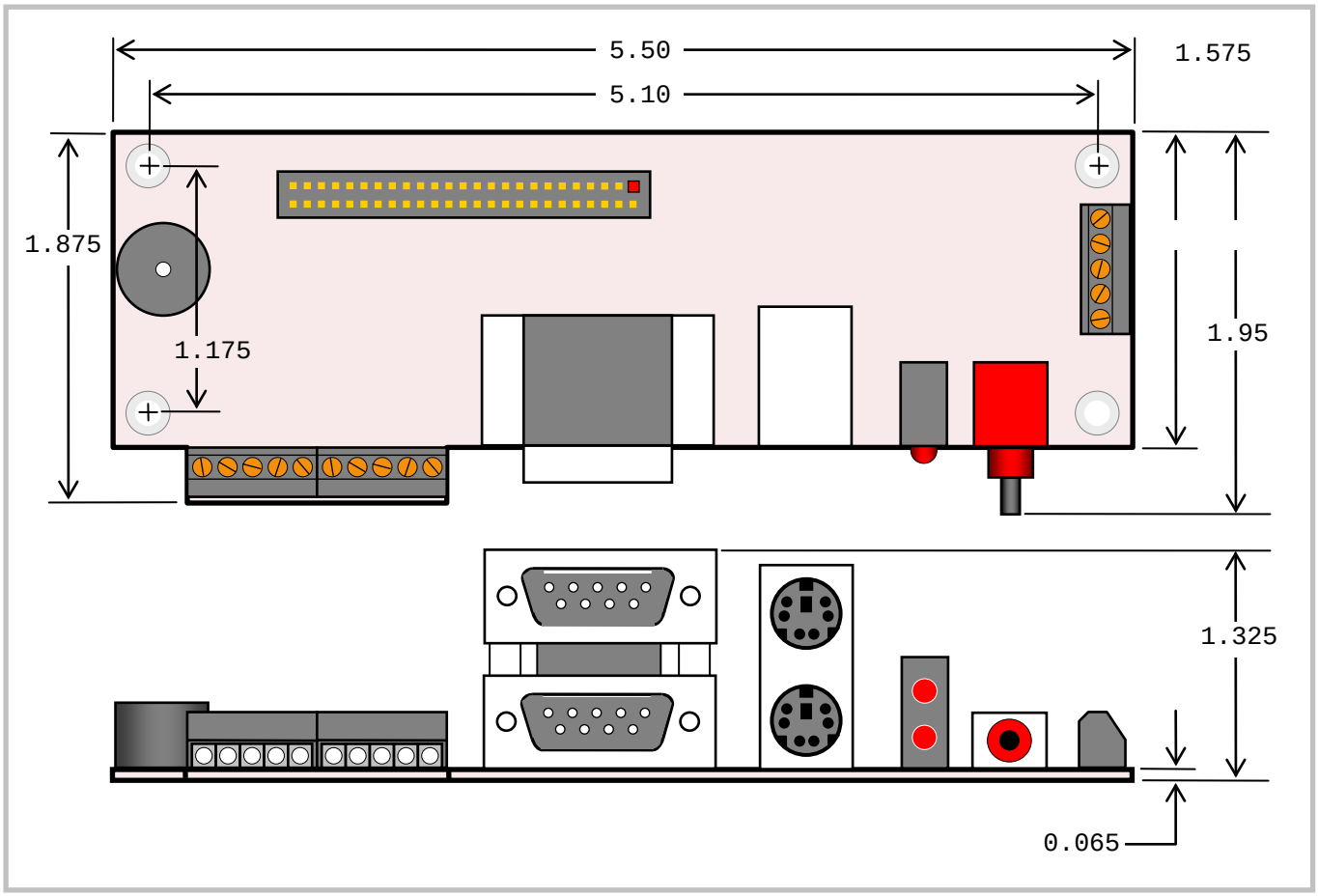

Figure 5. VL-CBR-5009 Dimensions and Mounting Holes

(Not to scale. All dimensions in inches.)

HARDWARE ASSEMBLY

The VL-EPM-16 uses pass-through PC/104 and PC/104-*Plus* connectors so that expansion modules can be added to the top or bottom of the stack. PC/104 (ISA) modules must not be positioned between the VL-EPM-16 and any PC/104-*Plus* (PCI) modules on the stack.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all four standoffs to the mounting surface to prevent circuit board flexing. Standoffs are secured to the top circuit board using four pan head screws. See page 9 for dimensional details. Standoffs and screws are available as part number VL-HDW-105.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack. Use caution when using the extractor tool not to damage any board components.

STACK ARRANGEMENT EXAMPLE

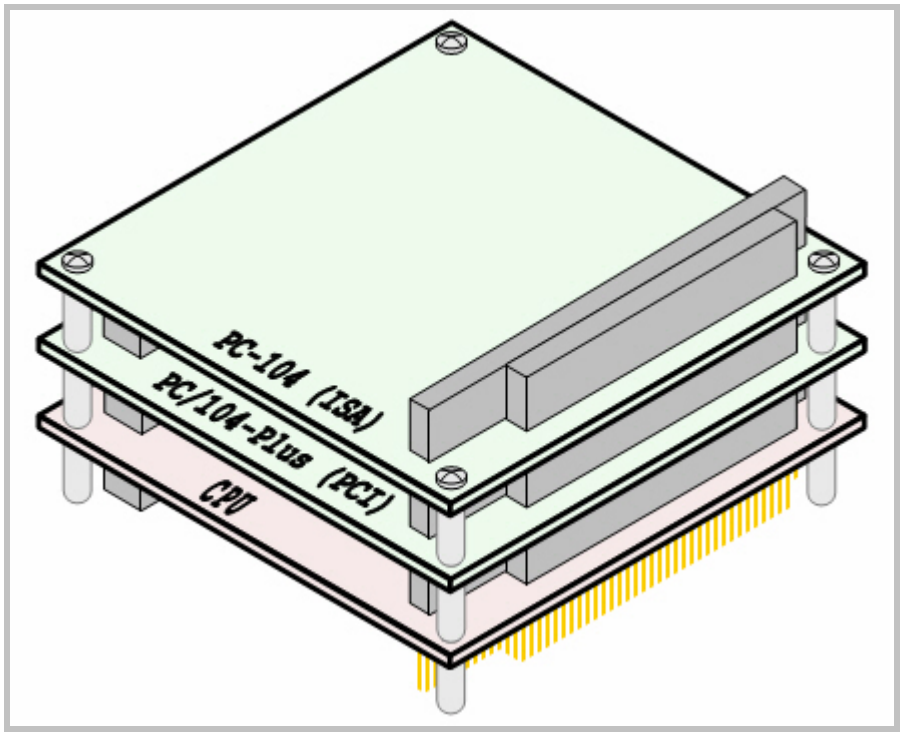

Figure 6. Stack Arrangement Example

External Connectors

VL-EPM-16 Connector Locations – Top

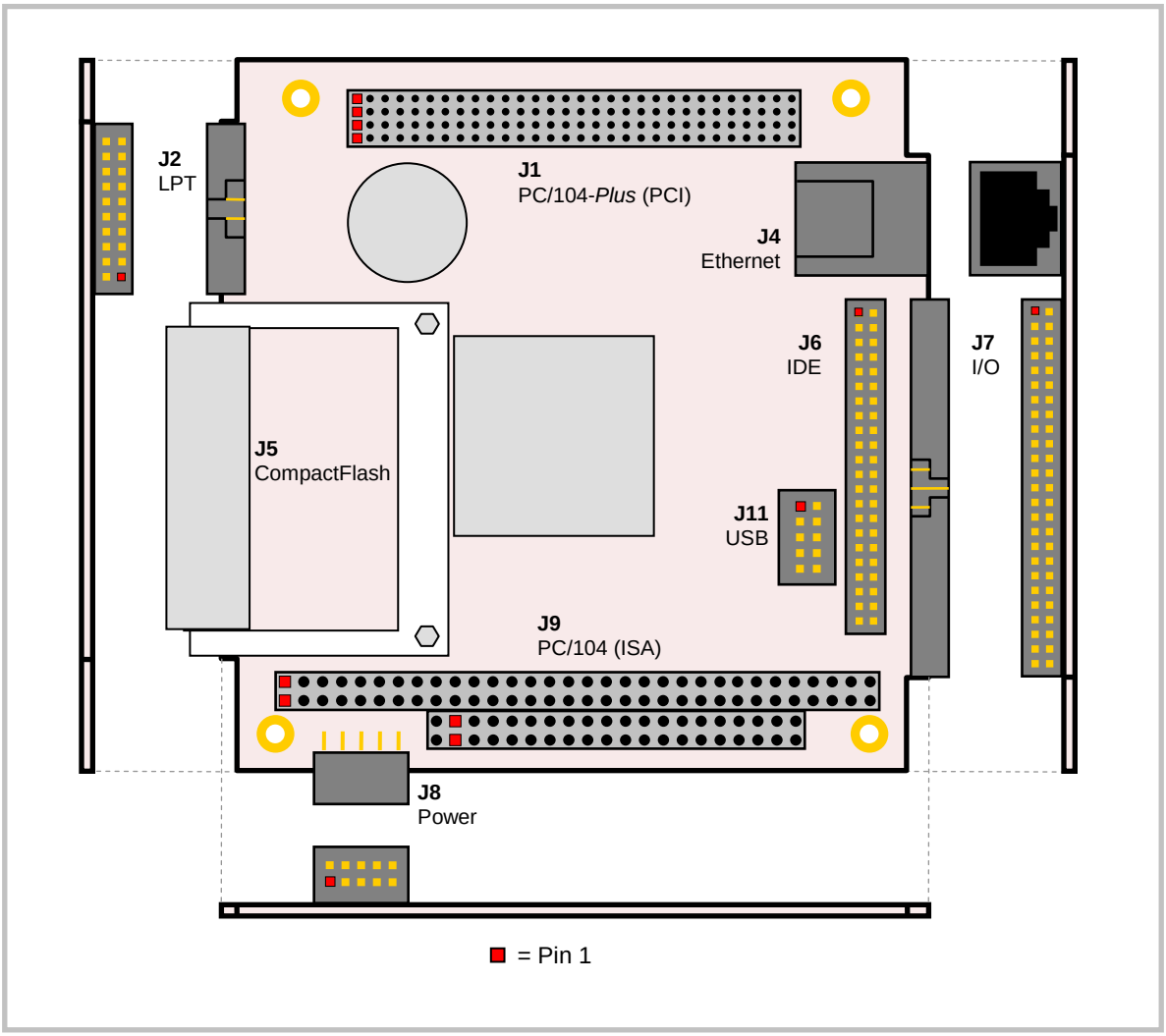

Figure 7. Connector Locations (Top)

VL-EPM-16 CONNECTOR LOCATIONS – BOTTOM

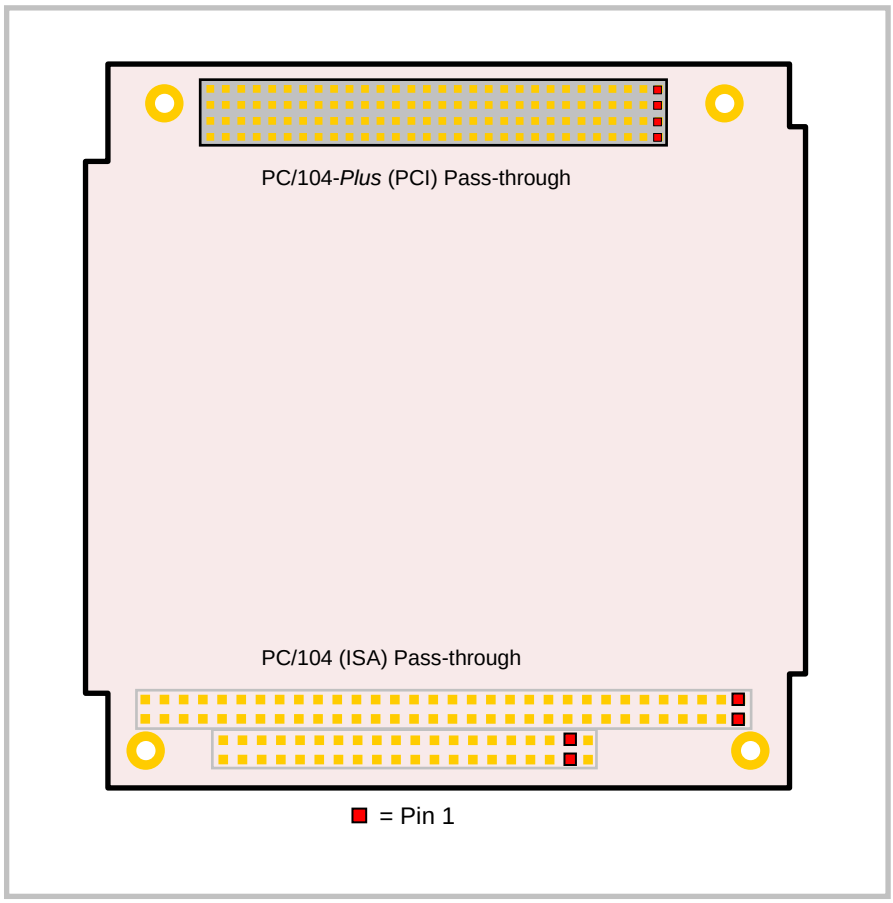

Figure 8. Connector Locations (Bottom)

VL-EPM-16 CONNECTOR FUNCTIONS AND INTERFACE CABLES

Table 1 provides information about the function, mating connectors, and transition cables for VL-EPM-16 connectors. Page numbers indicate where a detailed pinout or further information is available.

Table 1: Connector Functions and Interface Cables

Connector (Note 1)	Function	Mating Connector	Transition Cable	Cable Description	Page	Pin 1 Location X Coord.	Pin 1 Location Y Coord. (Note 2)
J1	PC/104-*Plus* (PCI)	AMP 1375799-1	—	—	22	0.450	3.139
J2	LPT	FCI 89947-720	VL-CBR-2003	12-inch 2mm latching LPT	24	-0.030	2.465
J4	Ethernet	RJ45	—	—	25	2.935	2.545
J5	CompactFlash Type I and II	—	—	—	26	—	—
J6	IDE interface	FCI 89947-144 (IDC)	VL-CBR-4404 VL-CBR-4405	12-inch 2mm IDE cable 2mm to 0.1-inch adapter	27	3.081	2.270
J7	COM ports, keyboard, mouse, GP timer inputs, power LED, push-button reset, PC speaker, LED	FCI 8947-350LF	VL-CBR-5009	12-inch 2mm latching 50-pin to 50-pin with breakout board	28	3.270	2.270
J8	Main power input	Berg 69176-010 (Housing) + Berg 47715-000 (Pins)	VL-CBR-1008 VL-PS-ATX12-300A ATX development power supply (requires VL-CBR-2034)	Interface from industry standard ATX power supply	18	0.025	-0.050
J9	PC/104 (ISA)	AMP 1375795-2	—	—	22	0.050	0.200
J11	USB	FCI 71600-010LF	VL-CBR-1013	Two-port USB adapter and cables	32	2.762	1.409

Notes:

1. Connectors J3, J10, and J12 are not installed.
2. The PCB Origin is the mounting hole to the lower left.

CONNECTOR LOCATIONS – VL-CBR-5009

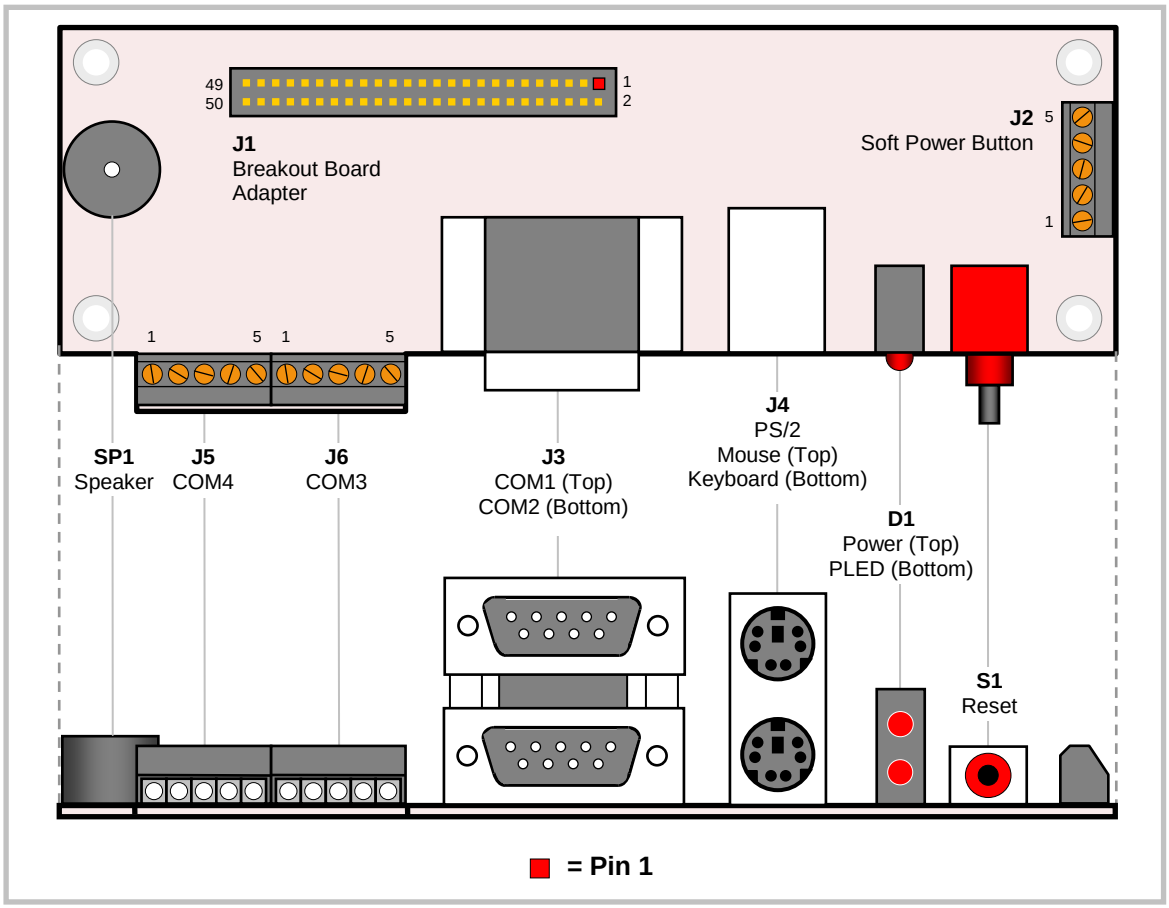

Figure 9. VL-CBR-5009 Connector Locations

VL-CBR-5009 CONNECTOR FUNCTIONS

Table 2: VL-CBR-5009 Connector Functions and Interface Cables

Connector/ Component	Function	Part Number	Description
D1	Power and Programmable LEDs	Dialight 552-0211	LEDx2 T1 3/4 PC Mount Red/Red
J1	High Density Connector	FCI 98414-F06-50U	2mm, 50 pins, keyed, latching header
J2	PB Reset Input	Conta-Clip 10250.4	5 pin screw terminal
J3	COM1, COM2	Kycon K42-E9P/P-A4N	Dual stacked DB-9 male
J4	PS/2 Keyboard and Mouse	Kycon KMDG-6S/6S-S4N	Dual stacked PS/2 female
J5	COM4	Conta-Clip 10250.4	5 pin screw terminal
J6	COM3	Conta-Clip 10250.4	5 pin screw terminal
S1	Reset Button	E-Switch 800SP9B7M6RE	Right angle momentary switch
SP1	Speaker	Challenge Electronics DBX05	Miniature PC speaker

Jumper Blocks

JUMPERS AS-SHIPPED CONFIGURATION

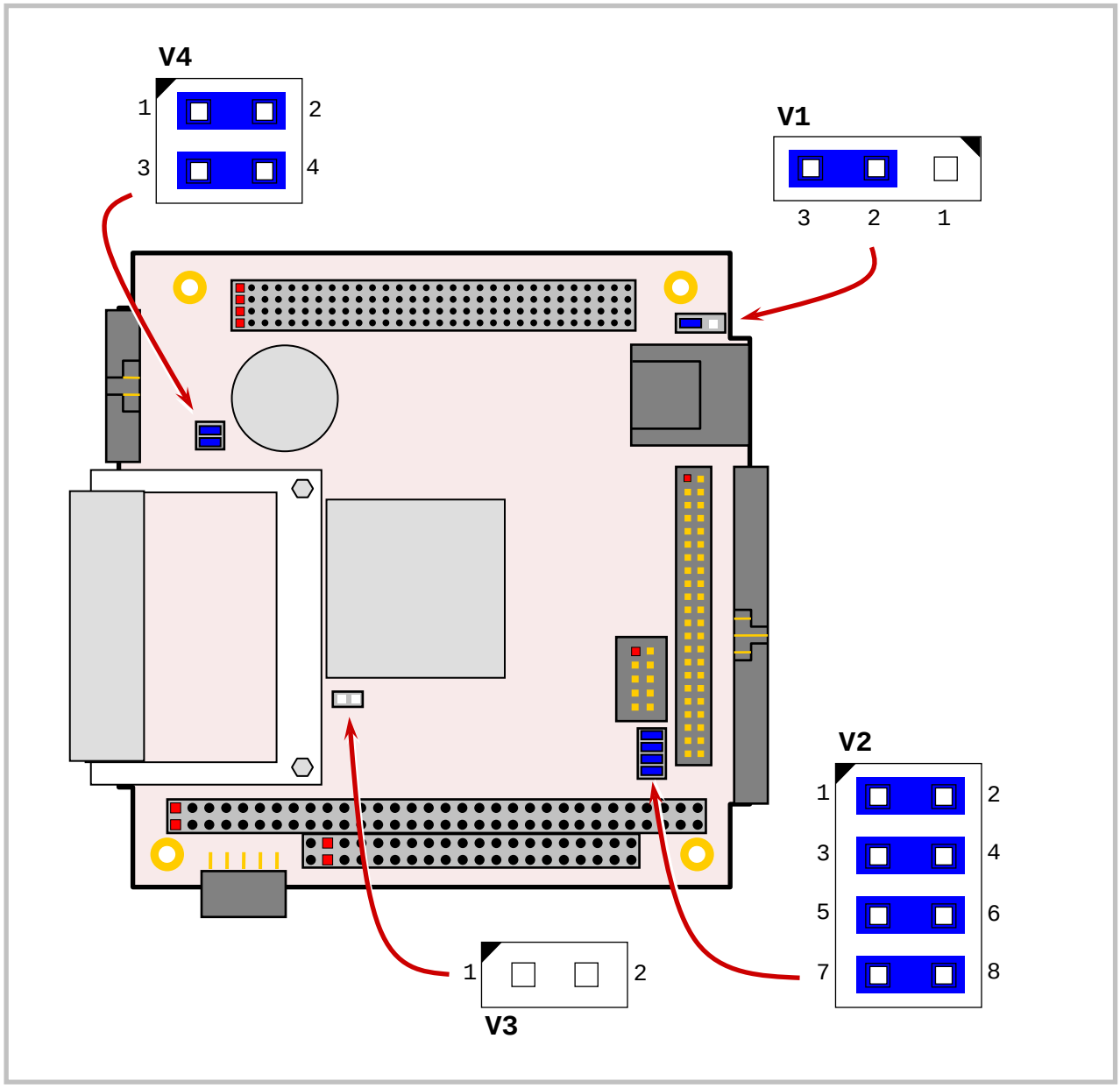

Figure 10. Jumper Block Locations

JUMPER SUMMARY

Table 3: Jumper Summary

Jumper Block	Description	As Shipped	Page
V1	**Battery Power Jumper** [1-2] In – Discharge CMOS Memory [2-3] In – Standard Operation	[2-3] In	19
V2[1-2] V2[3-4]	**COM3 configuration** [1-2] In and [3-4] In – RS-485 Endpoint [1-2] In and [3-4] Out – RS-232 [1-2] Out and [3-4] In – RS-422	[1-2] In [3-4] In	29
V2[5-6] V2[7-8]	**COM4 configuration** [5-6] In and [7-8] In – RS-485 Endpoint [5-6] In and [7-8] Out – RS-232 [5-6] Out and [7-8] In – RS-422	[5-6] In [7-8] In	29
V3	**CompactFlash Master/Slave Section** In — Slave IDE Device Out — Master IDE Device	Out	26
V4[1-2]	**General Purpose Input Bit 1** In — Bit D7 in GPI register reads as 1 Out — Bit D7 in GPI register reads as 0	In	37
V4[3-4]	**General Purpose Input Bit 2** In — Bit D0 in GPI register reads as 1 Out — Bit D0 in GPI register reads as 0	In	37

Power Supply

POWER CONNECTORS

Main power is applied to the VL-EPM-16 through a 10-pin polarized connector (J8), with mating connector Berg 69176-010 (housing) and Berg 47715-000 (pins). See the table below for connector pinout and page 12 for location information.

Warning! To prevent severe and possibly irreparable damage to the system, it is critical that the power connectors are wired correctly. Make sure to use both +5 VDC pins and all ground pins to prevent excess voltage drop. The power connector is not fuse or diode protected. Proper polarity must be followed or damage will occur. Some manufacturers include a pin-1 indicator on the crimp housing that corresponds to pin-10 of the pinout shown in Figure 11.

Table 4: Main Power Connector Pinout

J8 Pin	Signal Name	Description
1	GND	Ground
2	+5 VDC	Power Input
3	GND	Ground
4	+12 VDC	Power Input
5	GND	Ground
6	-12 VDC	Power Input
7	+3.3 VDC	Power Input
8	+5 VDC	Power Input
9	GND	Ground
10	+5 VDC	Power Input

Note: The +3.3 VDC, +12 VDC and -12 VDC inputs are necessary for expansion modules that require these voltages.

Figure 11 shows the VersaLogic standard pin numbering for this type of 10-pin power connector and the corresponding mating connector.

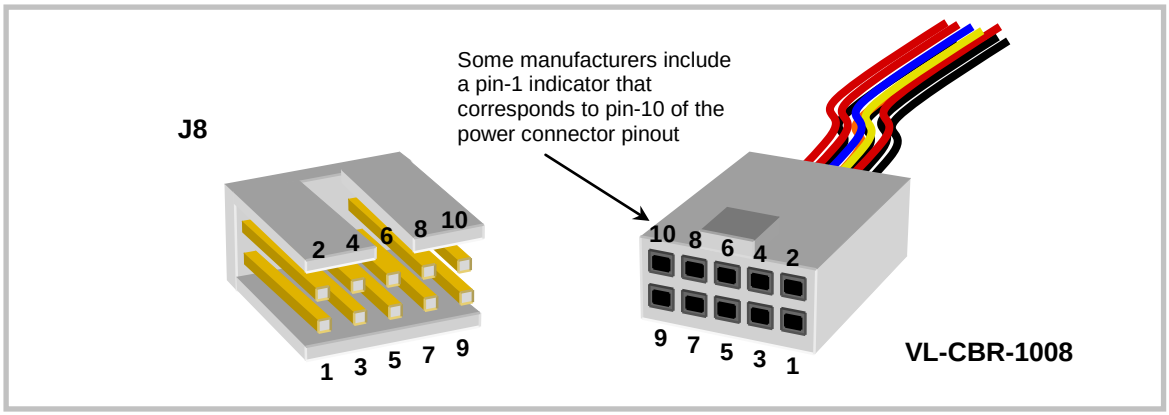

Figure 11. J8 and VL-CBR-1008 Pin Numbering

POWER REQUIREMENTS

The VL-EPM-16 requires only +5V (±5%) for proper operation. The voltage required for the RS-232 ports is generated with an on-board DC/DC converter. Variable low-voltage supply circuits provide power to the CPU and other on-board devices.

The exact power requirement of the VL-EPM-16 depends on several factors, including peripheral connections, and the type and number of expansion modules and attached devices. For example, driving long RS-232 lines at high speed can increase power demand.

LITHIUM BATTERY

Warning! To prevent shorting, premature failure, or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam, or the outside surface of a metalized ESD protective pouch. The lithium battery may explode if mistreated. Do not recharge, disassemble or dispose of in fire. Dispose of used batteries promptly.

Normal battery voltage should be at least +3V. If the voltage drops below +2V, contact the factory for a replacement (part number HB3/0-1). The life expectancy under normal use is approximately 10 years.

CPU

The Vortex86DX processor is an integrated System-on-Chip (SOC) containing an x86 processor. The CPU clock rate is 800 MHz. It integrates 32KB write through 4-way L1 cache, 4-way 256KB L2 cache, PCI rev. 2.1 32-bit bus interface at 33.33 MHz, DDR2, ROM controller, internal peripheral controllers (IPC) with DMA and interrupt timer/counter included, fast Ethernet, UART, USB2.0 host, IDE controller, ISA bus, parallel port, and real-time clock.

System RAM

The VL-EPM-16 has soldered on DDR2 SDRAM with the following characteristics:

- Storage Capacity — VL-EPM-16S, E – 128 MB
  VL-EPM-16V, F – 256 MB
  (custom expansions up to 512 MB)
- Voltage — +1.8V
- Speed — VL-EPM-16S, V – 667 MHz DDR2
  VL-EPM-16E, F – 600 MHz DDR2

CMOS RAM

CLEARING CMOS RAM AND THE REAL-TIME CLOCK

You can move the V1 jumper to position [1-2] for a minimum of three seconds to erase the contents of CMOS RAM the Real-Time Clock (RTC). When clearing the CMOS RAM:

1. Power off the VL-EPM-16.
2. Move the jumper from V1[2-3] to V1[1-2] and leave it for four seconds.
3. Return the jumper to V1[2-3]. (The board will not boot if the jumper is not returned to this position.)
4. Power on the VL-EPM-16.

Default BIOS Settings

The VL-EPM-16 permits you to store user-defined BIOS settings. This allows you to retrieve those settings from cleared or corrupted CMOS RAM, or battery failure. All BIOS defaults can be changed, except the time and date. BIOS defaults can be updated with the BIOS Update Utility.

Warning! If BIOS default settings make the system unbootable and prevent the user from entering CMOS Setup, the VL-EPM-16 needs to be serviced by the factory.

DEFAULT CMOS RAM SETUP VALUES

After CMOS RAM is cleared, the system will load default CMOS RAM parameters the next time the board is powered on. The default CMOS RAM setup values will be used in order to boot the system whenever the main CMOS RAM values are blank, or when the system battery is dead or has been removed from the board.

Real Time Clock

The VL-EPM-16 features a battery-backed real-time clock/calendar chip. Under normal battery conditions, the clock maintains accurate timekeeping functions when the board is powered off.

SETTING THE CLOCK

The CMOS Setup utility (accessed by pressing the Delete key during the early boot cycle, or F4 if operating in terminal mode) can be used to set the time and date of the real-time clock.

Watchdog Timer

The VL-EPM-16 has two watchdog timers, which you can configure in CMOS Setup. The watchdog timers can be set to generate a reset, NMI, or an interrupt when timeout occurs. The expiration time can be set to a maximum of seconds. See the DMP Vortex86 Series Software Programming Reference on the DMP Vortex86DX CPU Support Page for instructions on programming the watchdog timer.

Console Redirection

The VL-EPM-16 can be configured for remote access by redirecting the console to a serial communications port. CMOS Setup and some operating systems such as DOS can use this console for user interaction.

Console redirection settings are configured in the Advanced > Remote Access Configuration menu of CMOS Setup. Console redirection is enabled by default. The decision to redirect the console is made early in BIOS execution and cannot be changed later.

Console redirection can be disabled or redirected to a different COM port. The default settings for the redirected console are 115.2 kbps, 8 data bits, 1 stop bit, no parity, and no flow control.

Null Modem

The following diagram illustrates a typical DB9 to DB9 RS-232 null modem adapter.

```
System 1  <-->  System 2
Name Pin        Pin Name
------------------------
TX    3   <-->   2  RX
RX    2   <-->   3  TX
RTS   7   <-->   1  DCD
CTS   8
DSR   6   <-->   4  DTR
DCD   1   <-->   7  RTS
                 8  CTS
DTR   4   <-->   6  DSR
GND   5   <-->   5  GND
```

Pins 1, 4, and 6 are shorted together on each connector. Unlisted pins have no connection.

Expansion Bus

PC/104-*Plus* PCI (J1)

PC/104-*Plus* modules can be secured directly to the top or bottom of the VL-EPM-16. Make sure to correctly configure the slot position jumpers on each PC/104-*Plus* module appropriately. PC/104 modules must not be positioned between the VL-EPM-16 and any PC/104-*Plus* modules on the stack.

The VL-EPM-16 is compliant with revision 2.0 of the PC/104-*Plus* specification and can support four bus master capable PC/104-*Plus* modules.

The BIOS automatically allocates I/O and memory resources, however, manual PCI Interrupt routing is used.

PC/104 ISA (J9)

The VL-EPM-16 provides full support of the PC/104 bus, with the following exceptions:

- -5.0V power is not supplied on J9 pin B5. This pin is not connected.
- The ISA bus cannot be mastered by an external module. The VL-EPM-16 is always the bus master. The MASTER signal on pin D17 of J9 is not connected.

Most PC/104 cards will work, but be sure to check the requirements of your PC/104 card against the list above.

PC/104 I/O Support

The following I/O ranges will be available on the ISA bus unless there is a device claiming the range on the LPC bus (COM and LPT ports). Be sure to configure the ISA I/O ranges and the onboard serial ports in CMOS Setup to avoid conflicts with one another. (An operating system will not allocate I/O in the legacy ISA range)

- 0x010 – 0x01F
- 0x024 – 0x02D
- 0x030 – 0x03F
- 0x044 – 0x047
- 0x04C – 0x05F
- 0x065
- 0x06E – 0x070
- 0x076 – 0x077
- 0x07D – 0x07F
- 0x090 – 0x091
- 0x093 – 0x097
- 0x09D
- 0x0A2 – 0x0BF
- 0x0E0 – 0x16F
- 0x178 – 0x1DF
- 0x1F8 – 0x375
- 0x377 – 0x3BF
- 0x3CB
- 0x3CD
- 0x3D0 – 0x3D3
- 0x3D6 – 0x3D9
- 0x3DB – 0x3F5
- 0x3F7 – 0x47F
- 0x490 – 0x4CF
- 0x4D2 – 0xCFB
- 0xD00

Available base I/O addresses for COM ports are: 010h, 2E8h, 2F8h, 3E8h, 3F8h.

PC/104 MEMORY SUPPORT

The following memory addresses are available on the ISA bus:

- D0000 – DFFFF

PC/104 IRQ SUPPORT

The following IRQs are available on the PC/104 bus:

- IRQ3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15

Each of the IRQs must be enabled in CMOS Setup before it can be used on the ISA bus. Because ISA IRQ sharing is not supported, make sure that any IRQ channel used for an ISA device is not used elsewhere. For example, if ISA IRQ 4 is enabled, you must use a different IRQ for COM1. IRQs may not be available to the ISA bus due to operating system limitations.

Note Some IRQs may already be assigned to on-board devices. Check the Interrupt Configuration table on page 34 to avoid conflicts.

Parallel Port (J2)

The VL-EPM-16 includes a standard bi-directional/EPP/ECP compatible LPT port (connector J2) that resides at the PC standard address of 378h. The port can be enabled or disabled and interrupt assignments can be made via CMOS Setup. Numerous LPT modes are available for selection via CMOS Setup.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 5: Parallel Port Pinout

J2 Pin	Centronics Signal	Signal Direction
1	Strobe	Out
2	Auto feed	Out
3	Data bit 0	In/Out
4	Printer error	In
5	Data bit 1	In/Out
6	Reset	Out
7	Data bit 2	In/Out
8	Select input	Out
9	Data bit 3	In/Out
10	Data bit 4	In/Out
11	Data bit 5	In/Out
12	Data bit 6	In/Out
13	Data bit 7	In/Out
14	Ground	—
15	Acknowledge	In
16	Ground	—
17	Port busy	In
18	Ground	—
19	Paper end	In
20	Printer select	In

Ethernet Interface (J4)

The Ethernet controller built in to the Vortex86DX processor provides a standard IEEE 802.3 interface for 100Base-TX and 10Base-T applications.

ETHERNET CONNECTOR

A board-mounted RJ45 connector is provided to make connection with a Category 5 or 6 Ethernet cable. The Ethernet controller auto-negotiates connection speed. The interface uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

STATUS LED

Two colored LEDs located next to the RJ-45 connector provide an indication of the Ethernet status as shown in the following table.

Table 6: Ethernet Status LEDs

LED	State	Description
Green (Link/Activity)	On	• Active Ethernet cable plugged into J4 • No Tx/Rx data activity
	Off	• Cable not plugged into J4 • Cable not plugged into an active hub
	Blinking	• Active Ethernet cable plugged into J4 • Tx or Rx data activity detected on the cable
Yellow (Speed)	On	100BaseTX (fast) detected on Ethernet cable
	Off	10BaseT (slow) detected on Ethernet cable

CompactFlash (J5)

Connector J5 provides a socket for a Type I or Type II CompactFlash (CF) module. This IDE based interface operates on the same channel as the IDE interface at connector J6. The CF interface supports operation in DMA mode.

The following CF modules have been tested and qualified as bootable devices by VersaLogic. Part numbers with a suffix of -3500 and -4352 are RoHS-compliant.

Table 7. Qualified Bootable CF Modules

Manufacturer	Density	Mfg Part Number
Hagiwara	1 GB	CF1-1GMDG(H00AA)
Hagiwara	512 MB	CF1-512MDG(H00AA)
Silicon Systems	256 MB	SSD-C25M-3012, -3500, -4352
Silicon Systems	256 MB	SSD-C25MI-3012, -3500, -4352
Silicon Systems	512 MB	SSD-C51M-3012, -3500, -4352
Silicon Systems	512 MB	SSD-C51MI-3012, -3500, -4352
Silicon Systems	1 GB	SSD-C01G-3012, -3500, -4352
Silicon Systems	2 GB	SSD-C02G-3012, -3500, -4352
Silicon Systems	2 GB	SSD-C02GI-3012, -3500, -4352
Silicon Systems	4 GB	SSD-C04GI-3012, -3500, -4352

After installing the operating system, you may configure the CF to be the first boot device, which will reduce boot time.

IDE / PATA Interface (J6)

The IDE interface is available to connect up to two IDE devices, such as hard disks or CD-ROM drives. Connector J6 is the IDE controller with a 44-pin 2 mm connector. Use CMOS Setup to specify the drive parameters of the drive.

Cable length must be 18 inches or less to maintain proper signal integrity.

This interface supplies power to 2.5-inch IDE drives. If you are connecting a 3.5-inch drive to the interface (using the VL-CBR-4405 44-pin to 40-pin IDE adapter), you must supply external power to the drive. The power cable attached to a 3.5-inch drive must be properly grounded so that motor current is not returned via the grounds in the data cable.

Table 8: J6 IDE Hard Drive Connector Pinout

Pin	Signal Name	Function
1	Reset-	Reset signal from CPU
2	Ground	Ground
3	DD7	Data bus bit 7
4	DD8	Data bus bit 8
5	DD6	Data bus bit 6
6	DD9	Data bus bit 9
7	DD5	Data bus bit 5
8	DD10	Data bus bit 10
9	DD4	Data bus bit 4
10	DD11	Data bus bit 11
11	DD3	Data bus bit 3
12	DD12	Data bus bit 12
13	DD2	Data bus bit 2
14	DD13	Data bus bit 13
15	DD1	Data bus bit 1
16	DD14	Data bus bit 14
17	DD0	Data bus bit 0
18	DD15	Data bus bit 15
19	Ground	Ground
20	NC	Key
21	PDMARQ	DMA request
22	Ground	Ground

Pin	Signal Name	Function
23	DIOW	I/O write
24	Ground	Ground
25	DIOR	I/O read
26	Ground	Ground
27	IORDY	I/O ready
28	CSEL	Cable select
29	DMACK-	DMA acknowledge
30	Ground	Ground
31	INTRQ	Interrupt request
32	NC	No connection
33	DA1	Device address bit 1
34	CBLID-	Cable type identifier
35	DA0	Device address bit 0
36	DA2	Device address bit 2
37	CS0	Chip select 0
38	CS1	Chip select 1
39	DASP-	LED
40	Ground	Ground
41	Power	+5.0 V
42	Power	+5.0 V
43	Ground	Ground
44	NC	No connection

Main I/O Connector (J7)

The 50-pin main I/O connector (J7) incorporates the COM ports, PS/2 keyboard and mouse, programmable LED, general purpose timer inputs, pushbutton reset, and speaker interfaces. The table below illustrates the function of each pin.

Table 9: Main I/O Connector Pinout

J7 Pin	CBR-5009 Connector	Pin	Signal	
1	**COM1**	1	Data Carrier Detect	
2	**J3**	6	Data Set Ready	
3	Top DB9	2	Receive Data	
4		7	Request to Send	
5		3	Transmit Data	
6		8	Clear to Send	
7		4	Data Terminal Ready	
8		9	Ring Indicator	
9		5	Ground	
10	**COM2**	1	Data Carrier Detect	
11	**J3**	6	Data Set Ready	
12	Bottom DB9	2	Receive Data	
13		7	Request to Send	
14		3	Transmit Data	
15		8	Clear to Send	
16		4	Data Terminal Ready	
17		9	Ring Indicator	
18		5	Ground	
	COM3		**RS-232**	**RS-422/485**
19	**J6**	1	Ground	Ground
20		5	RTS	TxD+
21		4	TXD	TxD-
22		–	Ground	Ground
23		2	RXD	RxD-
24		3	CTS	RxD+
25		–	Ground	Ground

J7 Pin	CBR-5009 Connector	Pin	Signal	
	COM4		**RS-232**	**RS-422/485**
26	**J5**	1	Ground	Ground
27		5	RTS	TxD+
28		4	TXD	TxD-
29		–	Ground	Ground
30		2	RXD	RxD-
31		3	CTS	RxD+
32		–	Ground	Ground
33	**Mouse**	4	+5.0V (Protected)	
34	**J4**	1	Mouse Data	
35	Top	3	Ground	
36		5	Mouse Clock	
37	**PBRESET**	1	Pushbutton Reset	
38	**S1**	2	Ground	
39	**GP Timer**	3	Ground	
40	**Inputs**	4	GP Timer Input 1*	
41	**J2**	–	Ground	
42		5	GP Timer Input 0*	
43	**Keyboard**	4	+5.0V (Protected)	
44	**J4**	1	Keyboard Data	
45	Bottom	3	Ground	
46		5	Keyboard Clock	
47	**PLED**	1	+5.0V (Protected)	
48	**D1**	2	Programmable LED	
49	**Speaker**	1	+5.0V (Protected)	
50	**SP1**	2	Speaker Drive	

* The GP Timer Input 1 and GP Timer Input 0 signals were reversed on board revision 1.00 and earlier.

Serial Ports

The VL-EPM-16 features four on-board 16550-based serial channels located at standard PC I/O addresses. COM1 and COM2 are RS-232 (115.2 kbps) serial ports. IRQ lines are chosen in CMOS Setup. COM ports can share interrupts with other COM ports, but not with other devices.

COM3 and COM4 can be operated in RS-232 4-wire, RS-422, or RS-485 modes. IRQ lines are chosen in the CMOS Setup.

Each COM port can be independently enabled, disabled, or assigned a different I/O base address in CMOS Setup.

COM PORT CONFIGURATION

There are no configuration jumpers for COM1 and COM2 because they only operate in RS-232 mode. Use CMOS Setup to select between RS-232 and RS-422/485 operating modes for COM3 and COM4.

Jumper block V2 configures COM3 and COM4 for RS-422/485 operation. See “Jumper Summary” for details. The termination resistor should be enabled for RS-422 and the RS-485 endpoint stations. It should be disabled for RS-232 and RS-485 intermediate stations.

If RS-485 mode is used, the differential twisted pair (TxD+/RxD+ and TxD-/RxD-) is formed by connecting both transmit and receive pairs together. For example, on CBR-5009 connectors J6 and J5, the TxD+/RxD+ signal is formed by connecting pins 3 and 5, and the TxD-/RxD- signal is formed by connecting pins 2 and 4.

RS-232 mode for COM3 and COM4 is set in CMOS Setup.

COM3 / COM4 RS-485 MODE LINE DRIVER CONTROL

The TxD+/TxD– differential line driver can be turned on and off by manipulating the RTS handshaking line.

The following code example shows how to turn the line driver for COM3 on and off:

```
mov   dx,03ECh   ; Point to COM3 Modem Control register
in    al,dx      ; Fetch existing value
and   al,FDh     ; Clear bit D1
out   dx,al      ; Set RTS output High (enables line driver)

in    al,dx      ; Fetch existing value
or    al,02h     ; Set bit D1
out   dx,al      ; Set RTS output Low (disables line driver)
```

SERIAL PORT CONNECTORS

See the *Connector Location Diagrams* on pages 12 for connector and cable information. The pinouts of the DB9M connectors apply to the serial connectors on the VersaLogic breakout board CBR-5009.

These connectors use IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 10: COM1-2 Pinout – CBR-5009 Connector J3

COM1	COM2	RS-232
Top DB9 J3 Pin	Bottom DB9 J3 Pin	
1	10	DCD
2	11	RXD*
3	12	TXD*
4	13	DTR
5	14	Ground
6	15	DSR
7	16	RTS
8	17	CTS
9	18	RI

Table 11: COM3/COM4 Pinout – CBR-5009 Connectors J5 and J6

COM3	COM4	RS-232	RS-422	RS-485
J6 Pin	J5 Pin			
1	1	Ground	Ground	Ground
2	2	RXD	RxD-	RxD-
3	3	CTS	RxD+	RxD+
4	4	TXD	TxD-	TxD-
5	5	RTS	TxD+	TxD+

PS/2 Keyboard and Mouse

A standard PS/2 keyboard and mouse interface is accessible through connector J4 of the VersaLogic breakout board, CBR-5009. The breakout board is connected to connector J7 of the VL-EPM-16. The 5V power provided to the keyboard and mouse is protected by a 1 Amp fuse.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Table 12: PS/2 Mouse and Keyboard Pinout

CBR-5009 J4 Top	Signal	Description
1	MSDATA	Mouse Data
2	–	No Connection
3	GND	Ground
4	MKPWR	+5.0V (Protected)
5	MSCLK	Mouse Clock
6	–	No Connection
CBR-5009 J4 Bottom	**Signal**	**Description**
1	KBDATA	Keyboard Data
2	–	No Connection
3	GND	Ground
4	MKPWR	+5.0V (Protected)
5	KBCLK	Keyboard Clock
6	–	No Connection

Push-Button Reset

Connector J7 includes an input for a push-button reset switch. Shorting J7 pin 37 to ground causes the VL-EPM-16 to reboot. This must be a mechanical switch or an open-collector or open-drain active switch with less than a 0.5V low-level input when the current is 1 mA. There must be no pull-up resistor on this signal.

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

A reset button is provided on the CBR-5009 breakout board.

External Speaker

A miniature 8 Ω speaker can be connected between J7 pin 50 (SPKO*) and J7 pin 49. A speaker is provided on the CBR-5009 breakout board.

Programmable LED

Connector J7 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J7 pin 48; connect the anode to +5V. An on-board resistor limits the current to 15 mA when the circuit is turned on. A programmable LED is provided on the CBR-5009 breakout board.

To turn the LED on and off, set or clear bit D7 in I/O port 1E0h. When changing the register, make sure not to alter the values of the other bits. The following code examples show how to turn the LED on and off:

LED On

```
mov   dx,1E0h
in    al,dx
or    al,80h
out   dx,al
```

LED Off

```
mov   dx,1E0h
in    al,dx
and   al,7fh
out   dx,al
```

Note The LED is turned on by the BIOS during system startup (about 10 seconds after power up). This causes the light to function as a "power on" indicator if it is not otherwise controlled by user code.

USB Interface (J11)

Connector J11 includes interfaces for two USB ports (USB0-1). The USB interface on the VL-EPM-16 is UHCI (Universal Host Controller Interface) and EHCI (Enhance Host Controller Interface) compatible. Connector J11 is a 0.1-inch 2x5 IDC header. The VL-CBR-1013 USB adapter cable supplies two USB Type A connectors on a 5.25-inch ribbon cable.

Table 13: USB Connector (J11) Pinout

J11 Pin	Signal Name	USB Channel	Function
1	USBPWR0	USB0	+5.0V (Protected)
2	USBP0R_P		USB0 Data +
3	USBP0R_N		USB0 Data -
4	GND		Ground
5	EARTH_GND		Earth Ground
6	EARTH_GND	USB1	Earth Ground
7	GND		Ground
8	USBP1R_N		USB1 Data -
9	USBP1R_P		USB1 Data -
10	USBPWR1		+5.0V (Protected)

Each USB port power switch (supplying 5V to the USB port) has a low-true status output that when low indicates an over-current, under-voltage, or over-temperature fault condition. This status signal for USB0 goes to bit 0 of GPIO PORT0 on the Vortex processor, and the status signal for USB1 goes to bit 1 of GPIO PORT0. You can read these GPIO ports for the status of these signals. You can also set up interrupts in the Vortex processor that can be routed to an IRQ by setting up the GPIO PORT0 interrupt control registers (see Appendix B).

6 System Resources and Maps

Memory Map

Table 14 shows a map of the lower 1 MB of the VL-EPM-16. Various blocks of memory space between A0000h and FFFFFh are shadowed.

Table 14: Memory Map

Start Address	End Address	Comment
F0000h	FFFFFh	System BIOS Area
E0000h	EFFFFh	Extended System BIOS Area
C0000h	DFFFFh	Expansion Area
A0000h	BFFFFh	Legacy Video Area
00000h	9FFFFh	Legacy System (DOS) Area

I/O Map

Table 15 lists the common I/O devices in the VL-EPM-16 I/O map. User I/O devices should be added using care to avoid the devices already in the map as shown below.

Table 15: On-Board I/O Devices

I/O Device	Standard I/O Addresses
PLED and Product ID Register	1E0h
Revision Indicator Register	1E1h
BIOS and Jumper Status Register	1E2h
Interrupt Control Register	1E3h
Interrupt Mask Register	1E4h
Interrupt Status Register	1E5h
8254 Timer Control	1E6h
Reserved for System Test	1E7h
8254 Timer Address 0	1E8h
8254 Timer Address 1	1E9h
8254 Timer Address 2	1EAh
8254 Timer Address 3	1EBh
Reserved for System Test	1ECh – 1EFh
Primary IDE Controller	1F0h – 1F7h
COM2 Serial Port Default	2F8h – 2FFh
COM1 Serial Port Default	3F8h – 3FFh

Interrupt Configuration

Table 16: Interrupt Configuration

● = default setting ○ = allowed setting

Source	IRQ															
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Timer 0	●															
Keyboard		●														
Slave PIC			●													
COM1				○	●	○	○	○		○	○	○	○		○	○
COM2				●	○	○	○	○		○	○	○	○		○	○
COM3				○	○	○	○	○		○	●	○	○		○	○
COM4				○	○	○	○	○		○	○	●	○		○	○
LPT				○	○	○	○	●		○	○	○	○		○	○
Watchdog*				○	○	○	○	○		○	○	○	○		○	○
RTC									●							
Mouse													●			
Math Chip														●		
Pri. IDE															●	
ISA IRQ3				○												
ISA IRQ4					○											
ISA IRQ5						○										
ISA IRQ6							○									
ISA IRQ7								○								
ISA IRQ9										○						
ISA IRQ10											○					
ISA IRQ11												○				
ISA IRQ12													○			
ISA IRQ15																○
PCI INTA#				○	○	○	○	○		○	○	○	○		○	○
PCI INTB#				○	○	○	○	○		○	○	○	○		○	○
PCI INTC#				○	○	○	○	○		○	○	○	○		○	○
PCI INTD#				○	○	○	○	○		○	○	○	○		○	○

* The watchdog timer can also be set to NMI. The default setting is to reset the CPU board.

PLED and Product Code Register

PLEDPC (Read/Write) 1E0h

D7	D6	D5	D4	D3	D2	D1	D0
PLED	PC6	PC5	PC4	PC3	PC2	PC1	PC0

Table 17: PLED and Product Code Register Bit Assignments

Bit	Mnemonic	Description
D7	PLED	**Light Emitting Diode** — Controls the programmable LED on connector J7. 0 = Turns LED off 1 = Turns LED on
D6-D0	PC	**Product Code** — These bits are hard-coded to represent the product type. The VL-EPM-16 always reads as 0000011. Other codes are reserved for future products. **PC6 PC5 PC4 PC3 PC2 PC1 PC0 Product Code** 0 0 0 0 1 1 0 VL-EPM-16 These bits are read-only.

PLD Revision and Type Register

REVTYP (Read Only) 1E1h

D7	D6	D5	D4	D3	D2	D1	D0
PLD4	PLD3	PLD2	PLD1	PLD0	TEMP	CUSTOM	BETA

This register indicates the revision level of the VL-EPM-16.

Table 18: Revision and Type Register Bit Assignments

Bit	Mnemonic	Description
D7-D3	PLD	**PLD Code Revision Level** — These bits are hard-coded and represent the PLD code revision. **PLD4 PLD3 PLD2 PLD1 PLD0 Revision** 0 0 0 0 1 Rev. 0.1x 0 0 0 1 0 Rev. 1.0x These bits are read-only.
D2	TEMP	**Temperature Rating** — This bit indicates whether the VL-EPM-16 is rated for standard or extended temperature operation. 0 = Standard temperature operation 1 = Extended temperature operation This bit is read-only.
D1	CUSTOM	**PLD Class** — This bit indicates whether the PLD code is standard or customized. 0 = Standard PLD code 1 = Custom PLD code This bit is read-only.
D0	BETA	**Production Level** — This bit indicates if the PLD code is at the beta or production level. 0 = Production level PLD 1 = Beta level PLD This bit is read-only.

GPI Jumper Register

GPI (Read Only) 1E2h

D7	D6	D5	D4	D3	D2	D1	D0
GPI1_JMP	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	GPI2_JMP

Table 19: GPI Register Bit Assignments

Bit	Mnemonic	Description
D7	GPI1_JMP	**General Purpose Input 1 Jumper** — Indicates the status of jumper V4[1-2]. 0 = Jumper out 1 = Jumper in This bit is read-only.
D6-D1	Reserved	These bits have no function.
D0	GPI2_JMP	**General Purpose Input 2 Jumper** — Indicates the status of jumper V4[3-4]. 0 = Jumper out 1 = Jumper in This bit is read-only.

Appendix A – References

PC Chipset	
DMP Vortex86DX Processor	Vortex86DX Support Site
PC/104 Interface	PC/104 Specification
PC/104-*Plus* Interface	PC/104-*Plus* Specification
General PC Documentation	
The Programmer's PC Sourcebook	Amazon.com
General PC Documentation	
The Undocumented PC	Amazon.com

Appendix B – Custom Programming

B

GPIO Registers for PORT1 Interrupts

The PLD interrupt output connects to General Purpose Input/Output (GPIO) bit 6 on PORT1 on the Vortex. This GPIO can generate interrupts in the Vortex. The GPIO is an input by default, so no configuration for direction is necessary, but it must be configured for use as an interrupt. The following registers must be set. See the DMP Vortex86 Series Software Programming Reference on the DMP Vortex86DX CPU Support Page for instructions on programming a GPIO for interrupts.

INTERRUPT CONTROL REGISTER

This register enables interrupts.

IRQCTRL (Read/Write) 1E3h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	IRQEN	INTEN3	INTEN2	INTEN1	INTEN0

Table 20: Interrupt Select Register Bit Assignments

Bit	Mnemonic	Description
D7-D5	Reserved	These bits are reserved and only 0 should be written to them.
D4	IRQEN	IRQ Enable — Enables or disables an interrupt. 0 = Disable interrupt 1 = Enable interrupt
D3-D0	INTEN	These bits default to 0000. Writing any other value to these bits disables interrupts.

Note The PLD interrupt connects to the Vortex processor PORT1 GPIO bit 6. This GPIO can be configured to generate an interrupt on IRQ1, 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15. The interrupt is disabled in the Vortex processor by default. The procedure for setting the interrupt is as follows:

1. Ensure that the Vortex GPIO PORT1 is enabled as an interrupt source by clearing the Port 1 Interrupt Power-Down Control bit, Bit 19 in the Vortex On-Chip Device Control Register (PCI Bus 0, Device 7, Function 0, Register 0xBC).
2. Write an 8-bit value 40h to the GPIO PORT1 Interrupt Mask Register at offset E0h in the PCI configuration space for the ISA Bridge inside the Vortex. This instructs the system to use the GPIO from the PLD.

3. Write an 8-bit value to the following bits in GPIO PORT1 Interrupt Control Register at offset E2h (in the same PCI configuration space):

Bit	Description
D7	0 = Disables the PLD interrupt (default) 1 = Enable the PLD interrupt
D6-D4	Write "000" to this because the PLD interrupt does not need a qualification time (default value).
D3-D0	IRQ Selection: 0 0 0 0 Disable (default) 0 0 0 1 IRQ[9] 0 0 1 0 IRQ[3] 0 0 1 1 IRQ[10] 0 1 0 0 IRQ[4] 0 1 0 1 IRQ[5] 0 1 1 0 IRQ[7] 0 1 1 1 IRQ[6] 1 0 0 0 IRQ[1] 1 0 0 1 IRQ[11] 1 0 1 0 Reserved 1 0 1 1 IRQ[12] 1 1 0 0 Reserved 1 1 0 1 IRQ[14] 1 1 1 0 Reserved 1 1 1 1 IRQ[15]

4. Write an 8-bit value of either 40h (for a level PLD interrupt) or 00h (for an edge triggered interrupt) to GPIO PORT1 Interrupt Mode Control Register at offset E3h (same PCI configuration space).

INTERRUPT MASK REGISTER

This register masks interrupts generated by the PLD. This determines which interrupt status signals can generate a PLD interrupt.

IRQMASK (Read/Write) 1E4h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	IMASK_PERR	IMASK_SERR	IMASK_TC2	IMASK_TC1	IMASK_TCO

Table 21: Interrupt Mask Register Bit Assignments

Bit	Mnemonic	Description
D7-D5	Reserved	These bits are reserved and only 0 should be written to them.
D4	IMASK_PERR	Mask for the PCI Bus PERR Interrupt. 0 = Disable interrupt 1 = Enable interrupt
D3	IMASK_SERR	Mask for the PCI Bus SERR Interrupt. 0 = Disable interrupt 1 = Enable interrupt
D2	IMASK_TC2	Mask for the 8254 Timer #2 output (terminal count) Interrupt. 0 = Disable interrupt 1 = Enable interrupt
D1	IMASK_TC1	Mask for the 8254 Timer #1 output (terminal count) Interrupt. 0 = Disable interrupt 1 = Enable interrupt
D0	IMASK_TC0	Mask for the 8254 Timer #0 output (terminal count) Interrupt. 0 = Disable interrupt 1 = Enable interrupt

INTERRUPT STATUS REGISTER

This register is used for reading the status of interrupts generated by the PLD.

IRQSTAT (Read-Status/Write-Clear) 1E5h

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	Reserved	Reserved	ISTAT_PERR	ISTAT_SERR	ISTAT_TC2	ISTAT_TC1	ISTAT_TCO

Table 22: Interrupt Status Register Bit Assignments

Bit	Mnemonic	Description
D7-D5	Reserved	These bits are reserved and only 0 should be written to them.
D4	ISTAT _PERR	Status for the PCI Bus PERR Interrupt when read. 0 = PERR has not asserted 1 = PERR has asserted This bit is read-status; write-1-to-clear.
D3	ISTAT _SERR	Status for the PCI Bus SERR Interrupt when read. 0 = SERR has not asserted 1 = SERR has asserted This bit is read-status; write-1-to-clear.
D2	ISTAT _TC2	Status for the 8254 Timer #2 output (terminal count) Interrupt when read. 0 = Timer output (terminal count) has not transitioned from 0 to a 1 level 1 = Timer output (terminal count) has transition from a 0 to a 1 level This bit is read-status; write-1-to-clear.
D1	ISTAT _TC1	Status for the 8254 Timer #1 output (terminal count) Interrupt when read. 0 = Timer output (terminal count) has not transitioned from 0 to a 1 level 1 = Timer output (terminal count) has transition from a 0 to a 1 level This bit is read-status; write-1-to-clear.
D0	ISTAT _TC0	Status for the 8254 Timer #0 output (terminal count) Interrupt when read. 0 = Timer output (terminal count) has not transitioned from 0 to a 1 level 1 = Timer output (terminal count) has transition from a 0 to a 1 level This bit is read-status; write-1-to-clear.

The interrupt status register is valid whether or not the interrupt mask is set in the IRQMSK register (that is, it can be used for polling status). An interrupt status is acknowledged (cleared to a 0) by writing a '1' to the status bit.

The processor used on the VL-EPM-16 does not support monitoring of the PERR and SERR error signals on the PC/104-*Plus* (PCI) bus. The PLD will monitor for any assertions on these signals.

The PLD implements an 8254 timer (consisting of three individual timers). The outputs of these timers can generate interrupts when they transition from low-to-high (edge sensitive).

8254 Timer Control Register

This register sets modes related to the inputs on the 8254 Timers.

TIMCNTRL (Read/Write) 1E6h

D7	D6	D5	D4	D3	D2	D1	D0
TIM2GATE	TIM1GATE	TIM0GATE	TM1MODE	TM1SEL	TM0SEL	Reserved	Reserved

Table 23: 8254 Timer Control Register Bit Assignments

Bit	Mnemonic	Description
D7	TIM2GATE	Sets the level on the Gate input for the 8254 Timer #2. 0 = Gate is disabled (set to a logic 0) 1 = Gate is enabled (set to a logic 1)
D6	TIM1GATE	Sets the level on the Gate input for the 8254 Timer #1. 0 = Gate is disabled (set to a logic 0) 1 = Gate is enabled (set to a logic 1)
D5	TIM0GATE	Sets the level on the Gate input for the 8254 Timer #0. 0 = Gate is disabled (set to a logic 0) 1 = Gate is enabled (set to a logic 1)
D4	TM1MODE	Configure how the 8254 Timer #1 and #2 are used. 0 – Timer #1 is cascaded with Timer #2 for a 32-bit timer 1 – Timer #1 operates in normal 16-bit mode
D3	TM1SEL	Configured the clock source for 8254 Timer #1. 0 – Timer #1 input clock is from User I/O connector Input TMRIN1 1 – Timer #1 input clock is 4.16625 MHz internal clock (PCI clock divided by 8)
D2	TM0SEL	Configured the clock source for 8254 Timer #0. 0 – Timer #0 input clock is from User I/O connector Input TMRIN0 1 – Timer #0 input clock is 4.16625MHz internal clock (PCI clock divided by 8)
D1-D0	Reserved	These bits are reserved and only 0 should be written to them.

An 8254 timer is implemented in the PLD. It contains three independent 16-bit timers. It is fully software compatible with the Intel 8254, except that only binary counting modes are implemented (the BCD control bit is implemented but ignored). See the Intel 82C54 Programmable Interval Timer Datasheet for register definitions and programming information.

There is an option to cascade two of the timers together in a 32-bit mode. The timers are identified as Timer 0, 1, and 2. When Timers 1 and 2 are cascaded, Timer 1 is the LS 16-bits and Timer 2 is the MS 16-bits. In this 32-bit cascade mode the timer output of Timer 1 feeds the clock input of Timer 2. In this mode Timer 1 would normally be set so that it generates a clock after counting the full 16-bit range, but there is no requirement to do this.

The 32-bit cascade mode is set in TM1MODE in the Timer Control Register. There are also internal or external clock selections for the timers in this register using the external clocks TMRIN0 and TMRIN1 signals on the user I/O connector at J7. The internal clock is the PCI clock divided by 8 (33.33MHz / 8 = 4.16625MHz). TMRIN0 can only be used with Timer 0. TMRIN1 can only be used with Timer 1. The clock for Timer 2 is always the internal clock except in the 32-bit cascade mode when the output from Timer 1 is the clock for Timer 2.

The timer outputs can generate interrupts. When a timer output transitions from a 0 to a 1 then an interrupt status bit is set which can generate an interrupt. This bit sticks until cleared.