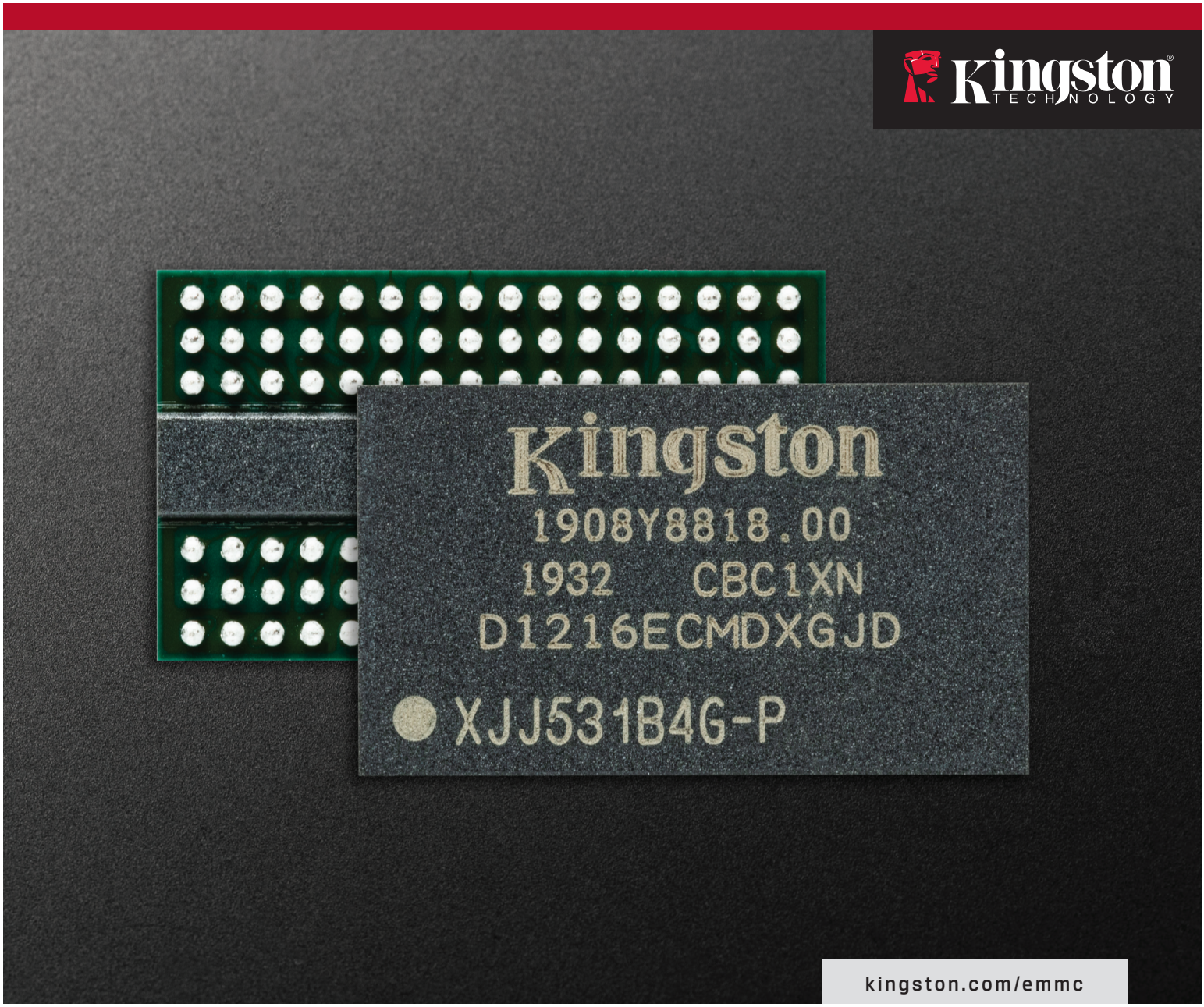


DRAM

Kingston DDR3/3L DRAM for embedded applications

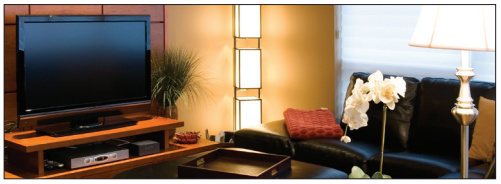
Kingston on-board DRAM is designed to meet the needs of embedded applications and offers a low-voltage option for lower power consumption.

MARKET SEGMENTS

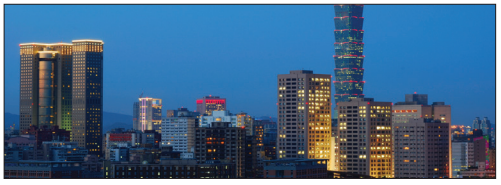
Industrial IoT / Robotics & Factory Automation

5G Networking/Telecommunications Communication Modules (WiFi Routers and Mesh Devices)

Wearables (Smart Watches, Health Monitors, AR & VR)



Smart Home (Sound Bars, Thermostats, Fitness Equipment, Vacuums, Beds, Faucets)



Smart City (HVAC, Lighting, Power Monitoring/ Metering, Parking Meters)

DDR3/3L PART NUMBERS AND SPECIFICATIONS

Part Number	Capacity	Description	Package	Configuration (Words x Bits)	Speed Mbps	VDD, VDDQ	Operating Temperature
D1216ECMDXGJD	2Gb	96 ball FBGA DDR3/3L C-Temp	7.5x13.5x1.2	128Mx16	1866 Mbps	1.35V*	0°C ~ +95°C
D2568ECMDPGJD	2Gb	78 ball FBGA DDR3/3L C-Temp	7.5x10.6x1.2	256Mx8	1866 Mbps	1.35V*	0°C ~ +95°C
D2516ECMDXGJD	4Gb	96 ball FBGA DDR3/3L C-Temp	7.5x13.5x1.2	256Mx16	1866 Mbps	1.35V*	0°C ~ +95°C
D5128ECMDPGJD	4Gb	78 ball FBGA DDR3/3L C-Temp	7.5x10.6x1.2	512Mx8	1866 Mbps	1.35V*	0°C ~ +95°C
D2516ECMDXGME	4Gb	96 ball FBGA DDR3/3L C-Temp	7.5x13.5x1.2	256Mx16	2133 Mbps	1.35V*	0°C ~ +95°C
B5116ECMDXGJD	8Gb	96 ball FBGA DDR3/3L C-Temp	9x13.5x1.2	512Mx16	1866 Mbps	1.35V*	0°C ~ +95°C

*Backward compatible to 1.5V VDD, VDDQ

KEY FEATURES

- Double Data Rate (DDR) architecture: two data transfers per clock cycle
- High-speed data transfer is realized by 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DOS and /DQS) is transmitted/received with data for capturing data at the receiver
- DOS is edge-aligned with data for READS; center-aligned with data for WRITES
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DOS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data Mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODD for better signal quality)
  - o Synchronous ODT
  - o Dynamic CDT
  - o Asynchronous ODT
- Multi-Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DO drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- RESET pin for power-up sequence and reset function
- SRT range: normal/extended
- Programmable output driver impedance control

