

PCN Number:	20190513002	PCN Date:	May 14, 2019
Title:	Datasheet for ADS54J60		
Customer Contact:	PCN Manager	Dept:	Quality Services
Change Type:			
<input type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design
<input type="checkbox"/>	Assembly Process	<input checked="" type="checkbox"/>	Data Sheet
<input type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change
<input type="checkbox"/>	Mechanical Specification	<input type="checkbox"/>	Test Site
<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Material
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Bump Process
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Site
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Materials
<input type="checkbox"/>		<input type="checkbox"/>	Wafer Fab Process

Notification Details

Description of Change:

Texas Instruments Incorporated is announcing an information only notification. The product datasheet(s) is being updated as summarized below. The following change history provides further details.



ADS54J60

SBAS706D – APRIL 2015 – REVISED APRIL 2019

Changes from Revision C (January 2017) to Revision D

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• Changed FFT for 170-MHz Input Signal figure	1
• Changed the description of the CLKINM, CLKINP, SYSREFM, SYSREFP, and PDN pins in <i>Pin Functions</i> table	6
• Changed typical values across parameters in <i>AC Characteristics</i> table	9
• Changed value of A_{IN} from -1 dBFS to -3 dBFS in 470 MHz test condition across all parameters in <i>AC Characteristics</i> table	9
• Added ENOB parameter to <i>AC Characteristics</i> table	11
• Changed the first footnote in <i>Timing Characteristics</i> table	13
• Changed the typical value of FOVR latency from $18 + 4$ ns to 18 ns in <i>Timing Characteristics</i> table	13
• Changed parameter name from t_{PD} to t_{PDI} in <i>Timing Characteristics</i> table	13
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• Changed FFT for 470-MHz Input Signal at -3 dBFS figure, title, and conditions	16
• Changed conditions of FFT for 720-MHz Input Signal at -6 dBFS figure	16
• Changed <i>Spurious-Free Dynamic Range vs Input Frequency</i> figure	17
• Changed <i>DDC Block</i> figure	27
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• Added last sentence to Step 4 in <i>Serial Register Readout: Analog Bank</i> section	36
• Added last sentence to Step 4 in <i>Serial Register Readout: JESD Bank</i> section	37
• Added <i>SDOUT Timing Diagram</i> figure	38
• Deleted unrelated patterns in in <i>JESD204B Test Patterns</i> section	40
• Changed <i>Serial Interface Registers</i> figure	45
• Added register addresses 1h and 2h and their descriptions to <i>GENERAL REGISTERS</i> in <i>Register Map</i> section	46
• Changed the name of <i>MASTER PAGE (80h)</i> to <i>MASTER PAGE (ANALOG BANK PAGE SEL = 80h)</i> in <i>Register Map</i> table	46
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The datasheet number will be changing.

Device Family	Change From:	Change To:
ADS54J60	SBAS706C	SBAS706D

These changes may be reviewed at the datasheet links provided.

<http://www.ti.com/product/ADS54J60>

Reason for Change:

To describe device operation correctly

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

Changes to product identification resulting from this PCN:

None.

Product Affected:

ADS54J60IRMP	ADS54J60IRMPT		
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For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

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