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# System Basis Chip with CAN FD, LDO Regulator and Wake-up Comparator

## NCV7451

The system basis chip (SBC) NCV7451 integrates +5 V / 250 mA LDO regulator with a high-speed CAN FD transceiver and local wake-up comparator, directly controlled by dedicated pins.

### Features

- 5 V  $\pm 2\%$  / 250 mA LDO
  - ◆ Current Limitation with Fold-back
  - ◆ Output Voltage Monitoring
- One High-Speed CAN FD Transceiver
  - ◆ Compliant to ISO11898-2:2016
  - ◆ CAN FD Timing Specified up to 5 Mbps
  - ◆ Current Limitation, Reverse Current Protected
  - ◆ TxDC Timeout
- Local Wake-up Comparator
  - ◆ Integrated Pull-up / Pull-down Current Source
- Very Low Current Quiescent Consumption
- Window Watchdog
- Direct Control
- Thermal Shutdown Protection
- AEC-Q100 Qualified and PPAP Capable
- Wetable Flank Package for Enhanced Optical Inspection
- This is a Pb-Free Device

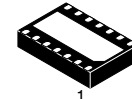
### Typical Applications

- Automotive
- Industrial Networks



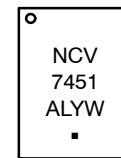
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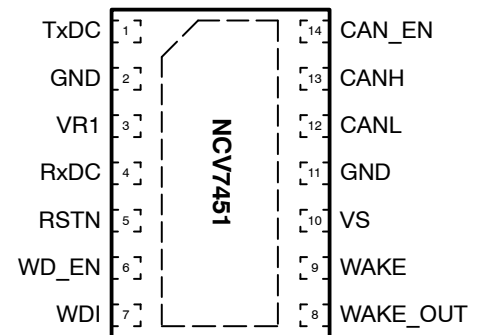
DFNW14 4.5x3, 0.65P  
CASE 507AC

### MARKING DIAGRAM



- NCV7451 = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

### PIN CONNECTIONS



### ORDERING INFORMATION

Device	Package	Shipping†
NCV7451MW0R2G	DFNW14 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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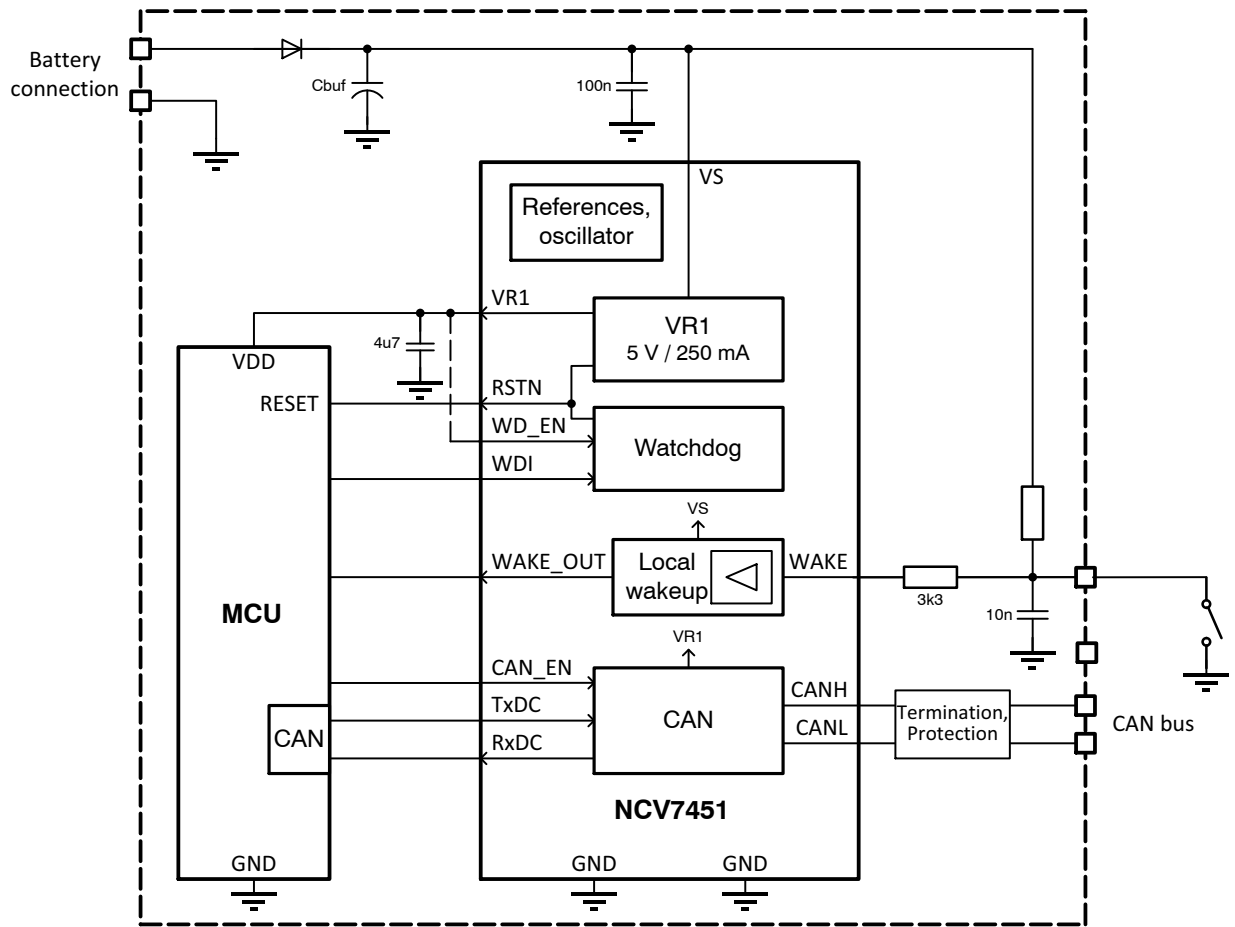


Figure 1. Simplified Application Diagram

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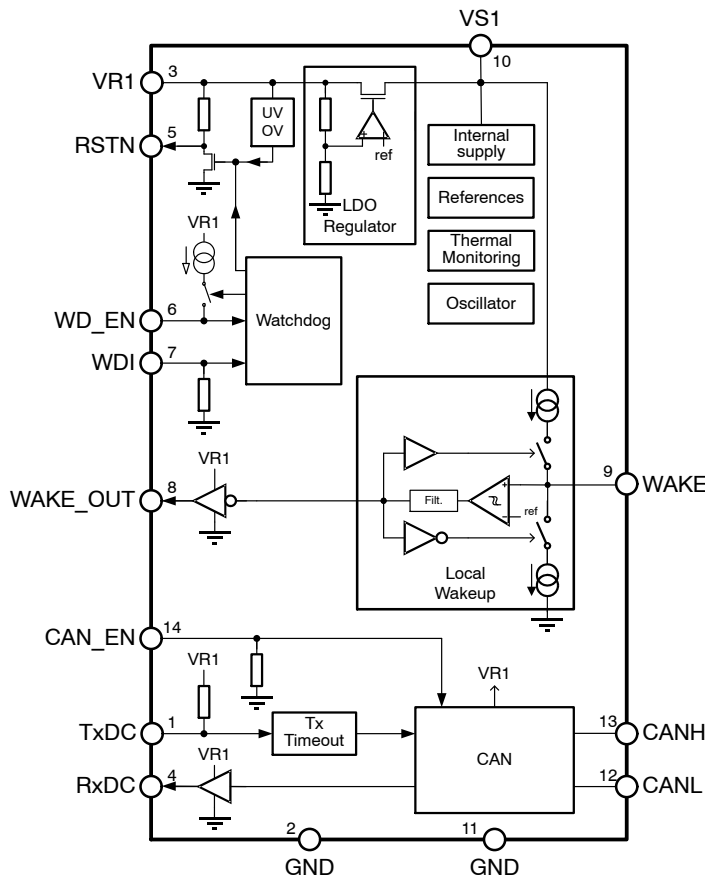


Figure 2. Block Diagram

## PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Pin Type (LV = Low Voltage; HV = High Voltage)	Description
1	TxDC	LV digital input; internal pull-up	CAN transmitter data input
2	GND	Ground connection	Ground supply (all GND pins have to be connected externally)
3	VR1	LV supply output	Output of the 5 V / 250 mA low-drop regulator
4	RxDC	LV digital output; push-pull	CAN receiver data output
5	RSTN	LV digital output; open drain; internal pull-up	Reset signal to the MCU
6	WD_EN	LV digital input; internal pull-up current	Watchdog enable input
7	WDI	LV digital input; internal pull-down	Watchdog trigger input
8	WAKE_OUT	LV digital output	WAKE pin output (inverted WAKE level)
9	WAKE	HV input; pull-up/-down current	WAKE pin
10	VS	HV supply input	Main supply input
11	GND	Ground connection	Ground supply (all GND pins have to be connected externally)
12	CANL	CAN bus interface	CANL line of the CAN bus
13	CANH	CAN bus interface	CANH line of the CAN bus
14	CAN_EN	LV digital input; internal pull-down	CAN transceiver enable input
	EP	Exposed pad	Substrate (has to be connected to all GND pins externally)

**MAXIMUM RATINGS**

Symbol	Rating	Min	Max	Unit	
VS	DC Power Supply Voltage (Note 1)	-0.3	+40	V	
VR1	LDO Supply pin output voltage	-0.3	6 or VS+0.3 (whichever is lower)	V	
VdigIO	DC voltage on digital pins (CAN_EN, WD_EN, WDI, RSTN, RxDC, TxDC, WAKE_OUT)	-0.3	VR1+0.3	V	
WAKE	DC WAKE pin Input Voltage	-40	+40	V	
CANH, CANL	DC voltage on pin CANH and CANL	-40	+40	V	
Vdiff	Differential DC voltage between any two pins (incl. CANH and CANL)	-40	+40	V	
V_ESDHBM	ESD capability, Device HBM, according to AEC-Q100-002 (EIA/JESD22-A114); (Note 2)	Pins VS, CANH, CANL, WAKE	-8	+8	kV
		Other pins	-4	+4	
V_ESDMM	ESD capability; MM, according to AEC-Q100-003 (EIA/JESD22-A115); all pins	-200	+200	V	
V_ESDCDM	ESD capability; CDM, according to AEC-Q100-011 (EIA/JESD22-C101); all pins	-750	+750	V	
V_ESDIEC	ESD capability; System HBM, according to IEC61000-4-2; pins VS, CANH, CANL, WAKE; (Note 3)	-6	+6	kV	
V_SCHAF	Voltage transients, Test pulses According to ISO7637-2, Class D; pins VS, CANH, CANL, WAKE	Test pulse 1	-100	-	V
		Test pulse 2a	-	+75	V
		Test pulse 3a	-150	-	V
		Test pulse 3b	-	+100	V
Tj	Junction Temperature Range	-40	+150	°C	
Tstg	Storage Temperature Range	-55	+150	°C	
Tsld	Peak Soldering Temperature (Note 4)	-	260	°C	
MSL	Moisture Sensitivity Level		1	-	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ resistor
3. Equivalent to discharging a 150 pF capacitor through a 330 Ω resistor; WAKE pin stressed through an external series resistor of 3.3 kΩ and with 10 nF capacitor on the module input, VS pin decoupled with 100 nF.
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

**THERMAL CHARACTERISTICS**

Symbol	Rating	Value	Unit
RθJA	Thermal Characteristics, Thermal Resistance, Junction-to-Air (Note 5) Thermal Reference, Junction-to-Air (Note 6)	77	°C/W
		52	
RψJC	Thermal Characteristics, Thermal Resistance, Junction-to-Case	7	°C/W

5. Value based on test board according to JESD51-3 standard, signal layer with 10% trace coverage.
6. Value based on test board according to JESD51-7 standard, signal layers with 20% trace coverage, inner planes with 90% coverage.

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## RECOMMENDED OPERATING RANGES

Symbol	Rating	Min	Max	Unit
VS	Functional supply voltage	5.0	28	V
	Supply voltage for valid parameter specification	6.0	18	V
VR1	VR1 regulator output voltage	4.9	5.1	V
I(VR1)	VR1 regulator output current (including CAN transceiver consumption)	0	250	mA
VdigIO	Digital inputs/outputs voltage	0	VR1	V
WAKE	WAKE input voltage	0	VS	V
CANH, CANL	CAN bus pins voltage	-40	40	V
T <sub>J</sub>	Junction Temperature	-40	150	°C
T <sub>A</sub>	Ambient Temperature	-40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS

6 V ≤ VS ≤ 18 V; -40°C ≤ T<sub>J</sub> ≤ 150°C; 4.75 V ≤ VR1 ≤ 5.25 V; R<sub>LT</sub> = 60 Ω, C<sub>LT</sub> = 100 pF, C<sub>ST</sub> not used, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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### VS SUPPLY

VS_PORH	VS POR threshold	VS rising	3.4	-	4.1	V
VS_PORL	VS POR threshold	VS falling	2.0	-	3.5	V
I <sub>s_off</sub>	VS consumption, low-power	VS = 14 V, VR1 on (not loaded), WAKE floating, CAN bus recessive, CAN_EN = Low, WD_EN = Low, T <sub>J</sub> ≤ 85°C	-	28	35	μA
I <sub>s_act</sub>	VS consumption, active	VS = 14 V, VR1 on (loaded by 100 mA, not included in I <sub>s_act</sub> ), WAKE floating, CAN bus recessive, CAN_EN = High, WD_EN = High, TxDC = High	-	3.7	5.0	mA

### VR1 VOLTAGE REGULATOR

V <sub>VR1</sub>	Regulator output voltage	0 mA ≤ I(VR1) ≤ 250 mA (including internal CAN consumption), 6 V ≤ VS ≤ 28 V	4.9	5.0	5.1	V
I <sub>lim_VR1</sub>	Regulator current limitation	Maximum VR1 overload current, VR1 > RES_VR1	250	-	650	mA
I <sub>short_VR1</sub>	Regulator short current	Maximum VR1 short current, VR1 < RES_VR1	125	1/2 x I <sub>lim_VR1</sub>	325	mA
V <sub>drop_VR1</sub>	Dropout Voltage	I(VR1) = 100 mA, VS = 5 V	-	0.2	0.4	V
		I(VR1) = 100 mA, VS = 4.5 V	-	0.2	0.5	
		I(VR1) = 50 mA, VS = 4.5 V	-	0.1	0.4	
Loadreg_VR1	Load Regulation	1 mA ≤ I(VR1) ≤ 100 mA	-50	-	50	mV
Linreg_VR1	Line Regulation	I(VR1) ≤ 100 mA	-40	-	40	mV
C <sub>load_VR1</sub>	VR1 load capacity	ESR < 200 mΩ, ceramic capacitor recommended	1.0	4.7	-	μF
RES_VR1	VR1 Reset threshold	VR1 voltage decreasing	4.3	4.5	4.7	V
RES_hyst_VR1	VR1 Reset threshold hysteresis		0.05	0.1	0.2	V
t <sub>filt_RES_VR1</sub>	VR1 undervoltage filter time		-	15	-	μs
OV_VR1	VR1 overvoltage threshold	VR1 voltage increasing / decreasing	5.5	-	6.0	V
OV_hyst_VR1	VR1 overvoltage threshold hysteresis		-	0.06	-	V
t <sub>filt_OV_VR1</sub>	VR1 overvoltage filter time		-	15	-	μs
t <sub>off_VR1</sub>	VR1 off time after TSD		-	1.0	-	s

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## ELECTRICAL CHARACTERISTICS (continued)

6 V ≤ VS ≤ 18 V; -40°C ≤ Tj ≤ 150°C; 4.75 V ≤ VR1 ≤ 5.25 V; RLT = 60 Ω, CLT = 100 pF, CST not used, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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### VR1 VOLTAGE REGULATOR

Is_add_VR1	VS consumption adder of VR1	(Note 7)	-	0.01 x I(VR1)	-	A
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### CAN BUS LINES (Pins CANH and CANL)

I <sub>o(rec)</sub>	Recessive output current at pins CANH and CANL	CAN enabled; -27 V < V <sub>CANH</sub> , V <sub>CANL</sub> < 32 V	-5.0	-	5.0	mA
I <sub>LI</sub>	Input leakage current	0 Ω ≤ R(VR1 to GND) < 1 MΩ; V <sub>CANH</sub> = V <sub>CANL</sub> = 5 V	-5.0	0	5.0	μA
V <sub>o(rec)</sub> (CANH)	Recessive output voltage at pin CANH	CAN enabled; TxDC = High; no load	2.0	2.5	3.0	V
V <sub>o(rec)</sub> (CANL)	Recessive output voltage at pin CANL	CAN enabled; TxDC = High; no load	2.0	2.5	3.0	V
V <sub>o(off)</sub> (CANH)	Recessive output voltage at pin CANH	CAN disabled; no load	-0.1	0	0.1	V
V <sub>o(off)</sub> (CANL)	Recessive output voltage at pin CANL	CAN disabled; no load	-0.1	0	0.1	V
V <sub>o(off)</sub> (diff)	Differential bus output voltage in off mode (V <sub>CANH</sub> - V <sub>CANL</sub> )	CAN disabled; no load	-0.2	0	0.2	V
V <sub>o(dom)</sub> (CANH)	Dominant output voltage at pin CANH	CAN enabled; 50 Ω ≤ R <sub>LT</sub> ≤ 65 Ω; TxDC = Low; t < t <sub>dom</sub> (TxDC)	2.75	3.5	4.5	V
V <sub>o(dom)</sub> (CANL)	Dominant output voltage at pin CANL	CAN enabled; 50 Ω ≤ R <sub>LT</sub> ≤ 65 Ω; TxDC = Low; t < t <sub>dom</sub> (TxDC)	0.5	1.5	2.25	V
V <sub>o(sym)</sub>	Driver output voltage symmetry (V <sub>CANH</sub> + V <sub>CANL</sub> )	CAN enabled; CST = 4.7 nF; TxDC driven by square wave up to 1 MHz	0.9	-	1.1	VR1
V <sub>o(dom)</sub> (diff)	Differential bus output voltage (V <sub>CANH</sub> - V <sub>CANL</sub> )	CAN enabled; 45 Ω ≤ R <sub>LT</sub> ≤ 65 Ω; TxDC = Low; dominant	1.5	2.25	3.0	V
V <sub>o(dom)</sub> (diff)_arb	Differential bus output voltage during arbitration (V <sub>CANH</sub> - V <sub>CANL</sub> )	CAN enabled; R <sub>LT</sub> = 2240 Ω; TxDC = Low; dominant; (Note 7)	1.5	-	5.0	V
V <sub>o(rec)</sub> (diff)	Differential bus output voltage (V <sub>CANH</sub> - V <sub>CANL</sub> )	CAN enabled; no load; V <sub>TxDC</sub> = High; recessive	-50	0	50	mV
I <sub>o(sc)</sub> (CANH)	Short circuit output current at pin CANH	CAN enabled; TxDC = Low; V <sub>CANH</sub> = -3 V -3 V ≤ V <sub>CANH</sub> ≤ 18 V	-100 -100	-70	-40 2.0	mA
I <sub>o(sc)</sub> (CANL)	Short circuit output current at pin CANL	CAN enabled; TxDC = Low; V <sub>CANL</sub> = 36 V -3 V ≤ V <sub>CANL</sub> ≤ 18 V	40 -1.5	70	100 100	mA
V <sub>i(rec)</sub> (diff)_NM	Differential input voltage range recessive state	CAN enabled; no load; -12 V ≤ V <sub>CANH</sub> , V <sub>CANL</sub> ≤ 12 V	3.0	-	0.5	V
V <sub>i(rec)</sub> (diff)_LP		CAN disabled; no load; -12 V ≤ V <sub>CANH</sub> , V <sub>CANL</sub> ≤ 12 V	-3.0	-	0.4	V
V <sub>i(dom)</sub> (diff)_NM	Differential input voltage range dominant state	CAN enabled; no load; -12 V ≤ V <sub>CANH</sub> , V <sub>CANL</sub> ≤ 12 V	0.9	-	8.0	V
V <sub>i(dom)</sub> (diff)_LP		CAN disabled; no load; -12 V ≤ V <sub>CANH</sub> , V <sub>CANL</sub> ≤ 12 V	1.05	-	8.0	V
V <sub>i(diff)</sub> (th)_NM	Differential receiver threshold voltage in normal mode	CAN enabled; -12 V ≤ V <sub>CANH</sub> , V <sub>CANL</sub> ≤ 12 V	0.5	-	0.9	V
V <sub>i(diff)</sub> (th)_LP	Differential receiver threshold voltage in wake-up-detection mode	CAN disabled; -12 V ≤ V <sub>CANH</sub> , V <sub>CANL</sub> ≤ 12 V	0.4	-	1.05	V

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## ELECTRICAL CHARACTERISTICS (continued)

6 V ≤ VS ≤ 18 V; -40°C ≤ Tj ≤ 150°C; 4.75 V ≤ VR1 ≤ 5.25 V; RLT = 60 Ω, CLT = 100 pF, CST not used, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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### CAN BUS LINES (Pins CANH and CANL)

R <sub>i(cm)</sub> (CANH)	Common-mode input resistance at pin CANH	-2 V ≤ V <sub>CANH</sub> , V <sub>CANL</sub> ≤ 7 V	15	25	37	kΩ
R <sub>i(cm)</sub> (CANL)	Common-mode input resistance at pin CANL	-2 V ≤ V <sub>CANH</sub> , V <sub>CANL</sub> ≤ 7 V	15	25	37	kΩ
R <sub>i(cm)</sub> (m)	Matching between pin CANH and pin CANL common mode input resistance	V <sub>CANH</sub> = V <sub>CANL</sub> = 5 V	-1.0	0	1.0	%
R <sub>i(diff)</sub>	Differential input resistance		25	50	75	kΩ
C <sub>i</sub> (CANH)	Input capacitance at pin CANH	TxDC = High; (Note 7)	-	7.5	20	pF
C <sub>i</sub> (CANL)	Input capacitance at pin CANL	TxDC = High; (Note 7)	-	7.5	20	pF
C <sub>i</sub> (diff)	Differential input capacitance	TxDC = High; (Note 7)	-	3.75	10	pF

### TIMING CHARACTERISTICS (see Figure 3, Figure 4 and Figure 5)

t <sub>d</sub> (TxDC-BUSon)	Propagation delay TxDC to bus active	CAN enabled	-	65	-	ns
t <sub>d</sub> (TxDC-BUSoff)	Propagation delay TxDC to bus inactive	CAN enabled	-	90	-	ns
t <sub>d</sub> (BUSon-RxDC)	Propagation delay bus active to RxDC	CAN enabled	-	60	-	ns
t <sub>d</sub> (BUSoff-RxDC)	Propagation delay bus inactive to RxDC	CAN enabled	-	65	-	ns
t <sub>pd_dr</sub>	Propagation delay TxDC to RxDC dominant to recessive transition	CAN enabled	50	100	170	ns
t <sub>pd_rd</sub>	Propagation delay TxDC to RxDC recessive to dominant transition	CAN enabled	50	120	170	ns
t <sub>wake_filt</sub>	Dominant time for wake-up via bus	CAN_EN = Low	0.15	-	1.8	μs
t <sub>dwakerd</sub>	Delay to flag wake event (recessive to dominant transitions)	CAN_EN = Low; Valid bus wake-up event	0.5	-	6.0	μs
t <sub>dwakedr</sub>	Delay to flag wake event (dominant to recessive transitions)	CAN_EN = Low; Valid bus wake-up event	0.5	-	6.0	μs
t <sub>wake_to</sub>	Bus time for wake-up timeout	CAN_EN = Low	1.0	-	10	ms
t <sub>dom</sub> (TxDC)	TxDC dominant time for timeout	CAN_EN = High; TxDC = Low	1.0	-	10	ms
t <sub>Bit</sub> (RxDC)	Bit time on RxDC pin	t <sub>Bit</sub> (TxDC) = 500 ns	400	-	550	ns
		t <sub>Bit</sub> (TxDC) = 200 ns	120	-	220	ns
t <sub>Bit</sub> (Vi(diff))	Bit time on bus pins (CANH - CANL)	t <sub>Bit</sub> (TxDC) = 500 ns	435	-	530	ns
		t <sub>Bit</sub> (TxDC) = 200 ns	155	-	210	ns
Δt <sub>Rec</sub>	Receiver timing symmetry Δt <sub>Rec</sub> = t <sub>Bit</sub> (RxDC) - t <sub>Bit</sub> (Vi(diff))	t <sub>Bit</sub> (TxDC) = 500 ns	-65	-	40	ns
		t <sub>Bit</sub> (TxDC) = 200 ns	-45	-	15	ns



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## ELECTRICAL CHARACTERISTICS (continued)

6 V ≤ VS ≤ 18 V; -40°C ≤ Tj ≤ 150°C; 4.75 V ≤ VR1 ≤ 5.25 V; RLT = 60 Ω, CLT = 100 pF, CST not used, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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### TIMING CHARACTERISTICS (see Figure 3, Figure 4 and Figure 5)

t <sub>d(LP-NM)</sub>	Mode change delay from wake-up detection to normal mode	CAN_EN = Low → High	-	25	47	μs
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### WATCHDOG TIMING

twd_acc	Watchdog timing accuracy		-15	-	15	%
t_wd_TO	Timeout watchdog period	After WD_EN low → high transition or RSTN pulse	56	65	74	ms
t_wd_CW	Window watchdog closed window		5.1	6.0	6.9	ms
t_wd_OW	Window watchdog open window		85	100	115	ms
t_WDI	Minimum WDI pulse width accepted as a watchdog service		6.0	-	-	μs

### WAKE INPUT

Vth_WAKE	WAKE pin threshold		2.0	-	4.0	V
Vhys_WAKE	WAKE pin threshold hysteresis		0.1	-	0.7	V
tfilt_WAKE	WAKE wake-up filter time		10	-	50	μs
Ipu_WAKE	Pull-up current on WAKE pin	V(WAKE) = 4 V	-11	-	-3.0	μA
Ipd_WAKE	Pull-down current on WAKE pin	V(WAKE) = 2 V	3.0	-	11	μA

### DIGITAL OUTPUTS, RxDC, WAKE\_OUT

IoutL_pinx	Low-level output driving current	pinx is logical Low, forced V(pinx) = 0.4 V	1.0	6.0	12	mA
IoutH_pinx	High-level output driving current	pinx is logical High, forced V(pinx) = VR1 - 0.4 V	-8.0	-3.0	-1.0	mA

### DIGITAL OUTPUT RSTN

IoutL_RSTN	Low-level output driving current	RSTN is active (logical Low), forced V(RSTN) = 0.4 V	2.0	5.0	12	mA
VoutL_RSTN	Low-level output voltage, low VR1/VS	VR1 > 4.7 V, I(RSTN) = 0.6 mA	-	0.2	0.4	V
		VR1 > 2 V, VS < VR1, I(RSTN) = 0.1 mA	-	0.2	0.4	
		VR1 = 0 V, VS > 2 V, I(RSTN) = 0.2 mA	-	0.2	0.4	
Rpu_RSTN	Internal pull-up resistor to VR1		5.0	10.0	19	kΩ
t_RSTN	Reset pulse length after VR1 undervoltage or watchdog failure		6.8	8.0	9.2	kΩ

### DIGITAL INPUTS TxDC, CAN\_EN, WD\_EN, WDI

VinL_pinx	Low-level input voltage (logical "Low")		-	-	0.8	V
VinH_pinx	High-level input voltage (logical "High")		2.0	-	-	V
Vin_hys_pinx	Input voltage hysteresis		-	200	-	mV
Rpu_pinx	Internal pull-up resistor to VR1; pin TxDC		55	100	185	kΩ
Rpd_pinx	Internal pull-down resistor to ground; pins CAN_EN, WDI		55	100	185	kΩ
Ipu_WD_EN	Internal pull-up current to VR1, pin WD_EN	V(WD_EN) = 0 V, pull-up current source active	50	100	200	μA
tper_pu_WDEN	WD_EN pull-up current source activation period	WD_EN = CAN_EN = Low	-	610	-	μs

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## ELECTRICAL CHARACTERISTICS (continued)

6 V ≤ VS ≤ 18 V; -40°C ≤ Tj ≤ 150°C; 4.75 V ≤ VR1 ≤ 5.25 V; RLT = 60 Ω, CLT = 100 pF, CST not used, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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### DIGITAL INPUTS TxDC, CAN\_EN, WD\_EN, WDI

ton_pu_WDEN	WD_EN pull-up current source activation on-time	WD_EN = CAN_EN = Low	-	5.0	-	μs
-------------	---	----------------------	---	-----	---	----

### THERMAL PROTECTION

Tsd	Thermal shutdown level	Temperature increasing	155	165	175	°C
Tsd_hys	Thermal shutdown level hysteresis	Temperature decreasing	-	10	-	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Not tested in production, guaranteed by design.

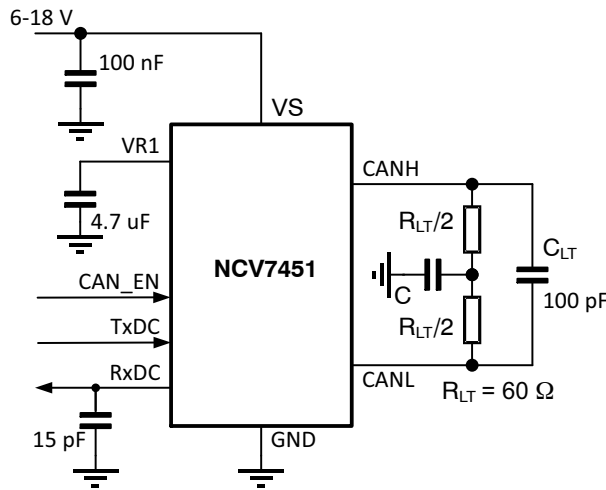


Figure 3. Test Circuit for CAN Timing Characteristics

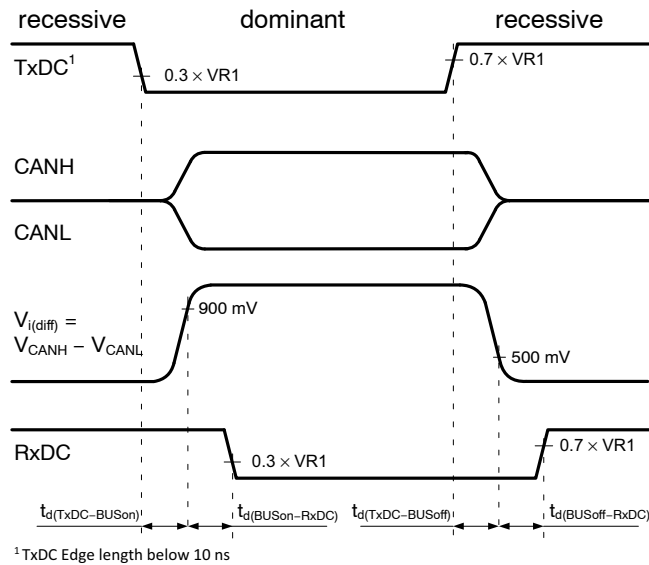


Figure 4. CAN Transceiver Timing Diagram – Propagation Delays

# NCV7451

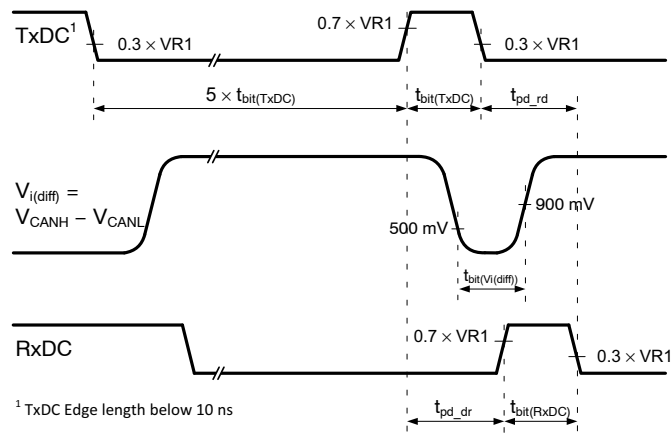


Figure 5. CAN Transceiver Timing Diagram – Loop Delay and Recessive Bit Time

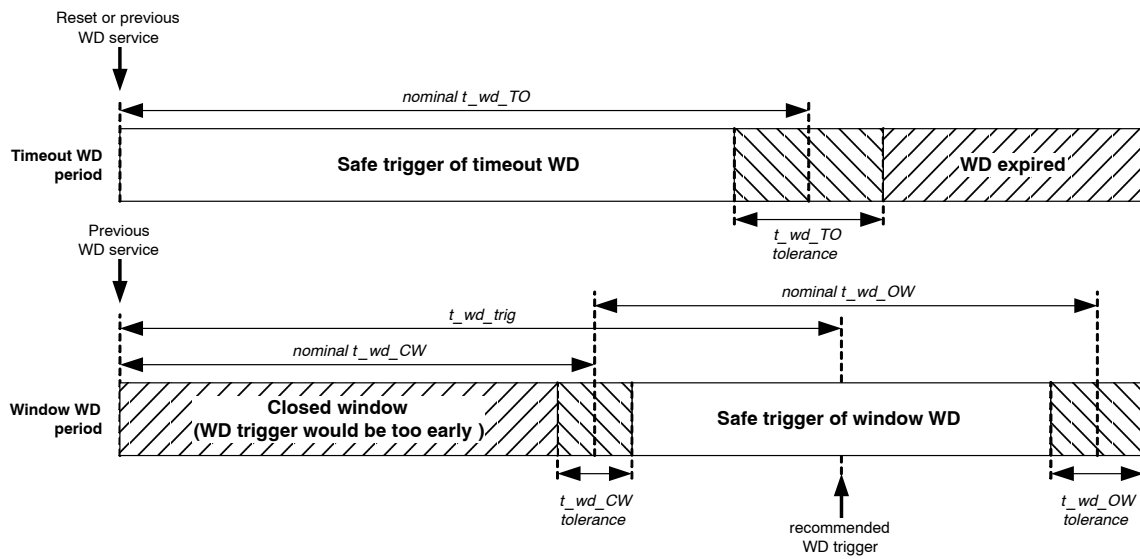


Figure 6. Watchdog Modes Timing

FUNCTIONAL DESCRIPTION

Supply Concept

The device has one battery supply pin VS, supplying the VR1 regulator and logic control. The supply line has to be properly decoupled by filtering capacitors close to the device pin.

VR1 Low-drop Regulator

VR1 is a low-drop output regulator providing 5 V voltage derived from the VS main supply. It is able to deliver up to 250 mA and is primarily intended to supply the on-chip CAN transceiver, the application microcontroller unit (MCU) and related 5 V loads (e.g. its own MCU-related digital inputs/outputs). An external capacitor needs to be connected on VR1 pin in order to ensure the regulator's stability and to filter the disturbances caused by the connected loads.

VR1 voltage supplies all the digital low-voltage input/output pins.

The protection and monitoring of the VR1 regulator consist of the following features:

- ◆ VR1 Current Limitation – the two-level current limitation controlled by VR1 reset comparator to reduce the power dissipation in case of shorts to ground by the current fold-back (see Figure 7)
- ◆ VR1 Reset Comparator – the VR1 regulator output is compared with a reset level RES\_VR1. If the VR1

level drops below this level for longer than  $t_{filt\_RES\_VR1}$ , a reset towards the MCU is generated through the RSTN pin and the CAN transceiver is disabled.

- ◆ VR1 Overvoltage Reset Comparator – the VR1 regulator output is compared with an overvoltage level OV\_VR1. If the VR1 level crosses this threshold for longer than  $t_{filt\_OV\_VR1}$ , a reset towards the MCU is generated through the RSTN pin and the CAN transceiver is disabled.
- ◆ Temperature (see Figure 14)

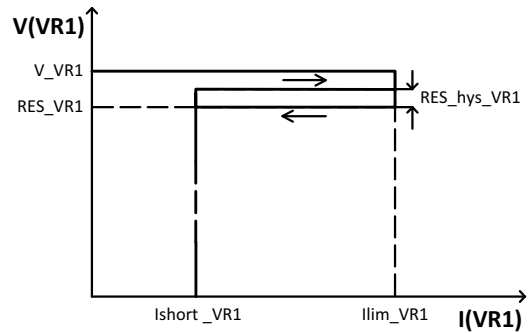


Figure 7. VR1 Current Fold-back

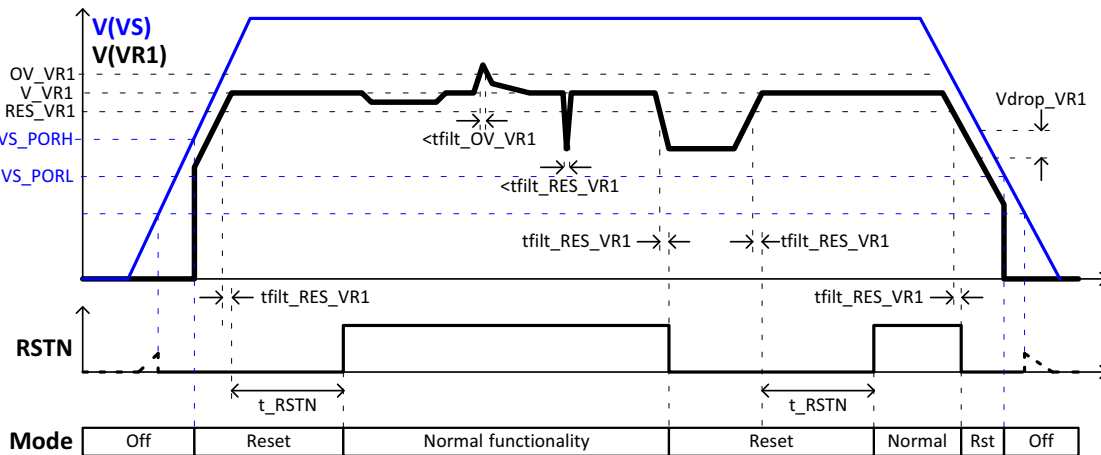


Figure 8. VS1 and VR1 Monitoring

CAN Transceiver

The SBC contains one high-speed CAN transceiver compliant with ISO11898-2:2016. The transceiver consists of the following sub-blocks: transmitter, receiver, and wake-up detector.

If enabled (CAN\_EN = High), the CAN transceiver is ready to provide the full-speed interface between the bus and a CAN controller connected on pins RxDC (received data) and TxDC (data to transmit).

In order to prevent a faulty node from blocking the bus traffic, the maximum length of the transmitted dominant symbol is limited by a time-out counter to  $t_{dom}(TxDC)$ . In case the TxDC Low signal exceeds the timeout value, the transmitter returns automatically to the recessive state. The transmission is again de-blocked when TxDC pin returns to high (recessive) state.

If the CAN block is disabled (CAN\_EN = Low) or RSTN pin active (Low) due to failed watchdog service or VR1

undervoltage / overvoltage, the CAN transceiver is in its wake-up detection state. Logical level on TxDC is ignored and pin RxDC is kept high until a CAN bus wake-up is detected. The CAN bus wake-up corresponds to a pattern consisting of dominant – recessive – dominant symbols of at least  $t_{wake\_filt}$  each. The RxDC starts following the CAN bus afterwards. The pattern must be received within  $t_{wake\_to}$  to be recognized as a valid wake-up event, otherwise internal wake-up logic is reset.

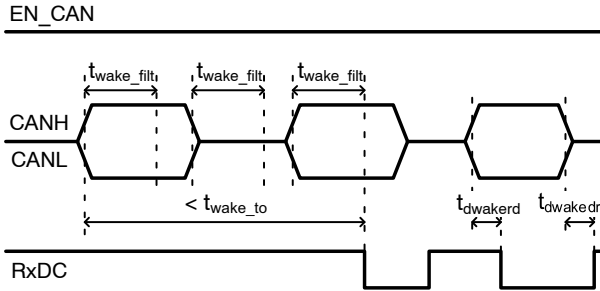


Figure 9. CAN Wake-up Pattern

**WAKE Comparator**

WAKE pin is a high-voltage input typically used to monitor an external contact or switch. The inverted logical level on pin WAKE can be polled via WAKE\_OUT output push-pull pin.

A stable logical level of the WAKE signal is ensured even without an external connection:

- if the WAKE level is High for longer than  $t_{filt\_WAKE}$ , an internal pull-up current source is connected to WAKE pin

- if the WAKE level stays Low for longer than  $t_{filt\_WAKE}$ , an internal pull-down current source is connected to WAKE pin

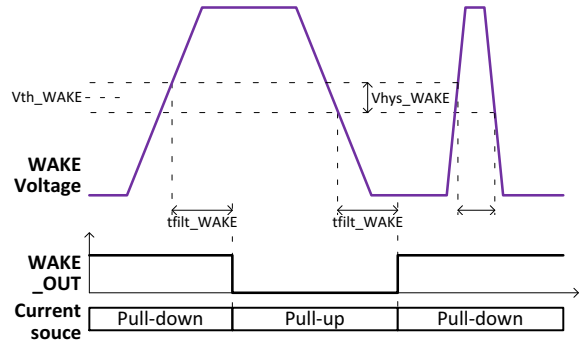


Figure 10. WAKE Pin Functionality

**Watchdog**

The on-chip watchdog requires that the MCU software “triggers” or “services” the watchdog in a specified time frame. A correct watchdog service consists of high-to-low transition on the WDI input. The watchdog timer re-starts immediately after a successful trigger is received.

After any Reset event (power-up, watchdog failure, VR1 under-/overvoltage, thermal shutdown) or watchdog enable (WD\_EN = Low → High), the watchdog always starts in a timeout mode. The MCU software must serve the watchdog any time before the time-out expiration. After the watchdog is triggered for the first time, it starts working in a window mode operation: the watchdog time is split to two distinct parts – a closed window, where the watchdog may not be triggered, is followed by an open window where the MCU must send a valid watchdog trigger (see Figure 12).

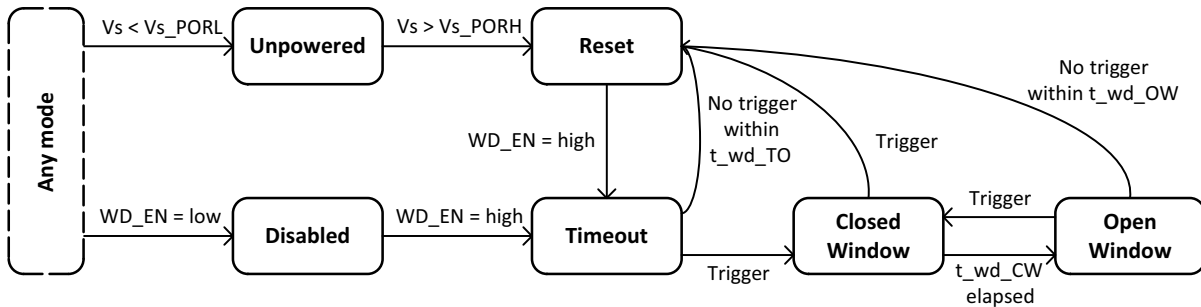


Figure 11. Watchdog Operating Modes

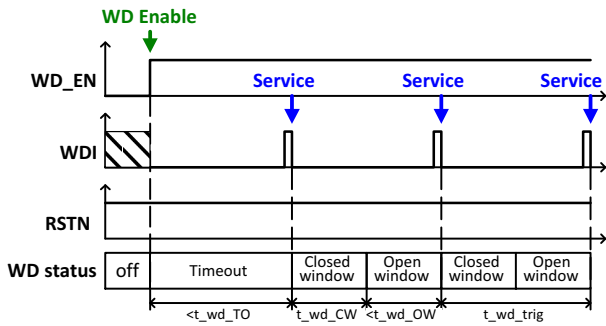


Figure 12. Correct Watchdog Services

In case the watchdog is not triggered before the timeout or open window elapses (Figure 13, Figure 14), or trigger is sent within the closed window (Figure 15), RSTN signal is generated and then watchdog restarted in the timeout mode again.

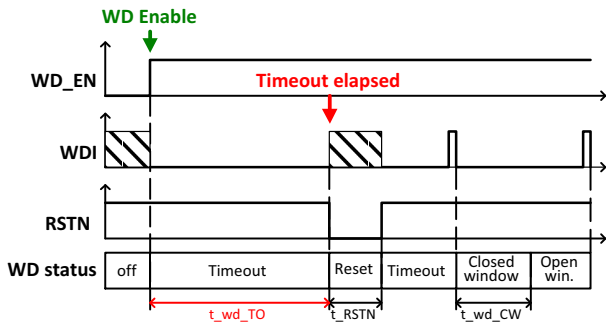


Figure 13. Missed Watchdog in Timeout Mode

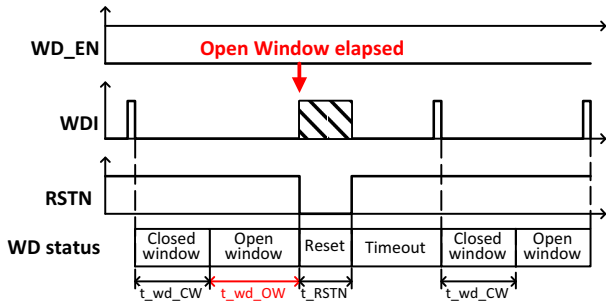


Figure 14. Missed Watchdog in Window Mode

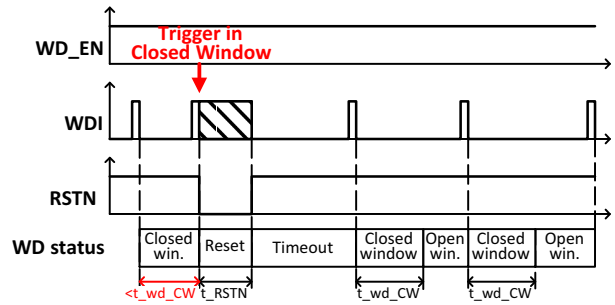


Figure 15. Watchdog Service during Closed Window

The WD\_EN pin has an integrated pull-up source to enable the watchdog in case the pin is disconnected from the application. To reduce the power consumption in the low-power mode (watchdog and CAN disabled), the WD\_EN pull-up current source is switched on for  $t_{on\_pu\_WDEN}$  time with period of  $t_{per\_pu\_WDEN}$ . The pin state is sampled in the end of the current source activation. Once High level is detected on the WD\_EN pin, the current source is activated permanently.

To ensure the High level is correctly detected if the pin becomes floating, external WD\_EN capacitance should stay below 50 pF.

After the rising edge on WD\_EN pin, the MCU should wait  $t_{per\_pu\_WDEN}$  before the first watchdog service.

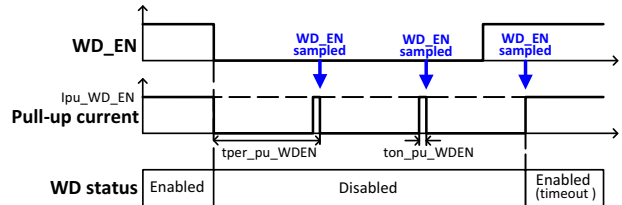


Figure 16. WD\_EN Pull-up Current Source Activation

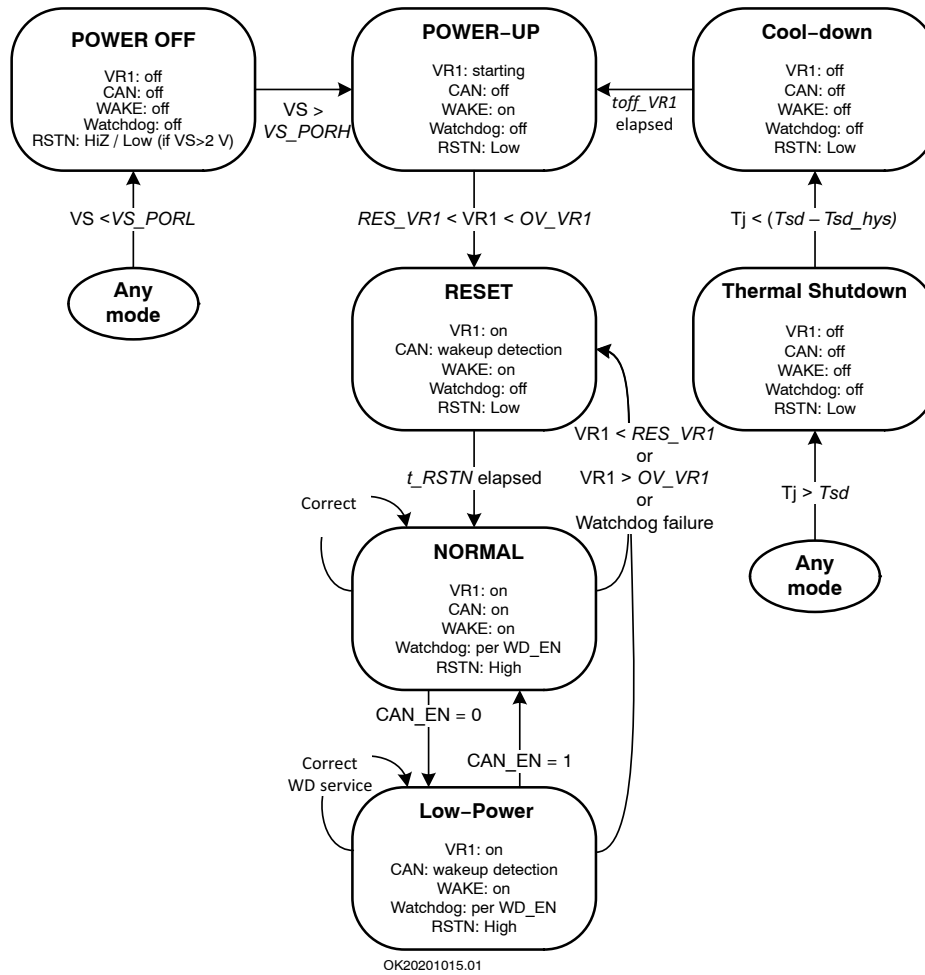
**Thermal Protection**

A thermal protection circuit protects the IC from damage by complete device de-activation if the junction temperature exceeds a value of  $T_{sd}$ .

The device recovers automatically after the junction temperature drops below  $T_{sd}$  level lowered by hysteresis  $T_{sd\_hys}$  and  $t_{off\_VR1}$  (typ. 1 second) expires.

**Operating Modes**

The device operating modes are directly controlled by CAN\_EN input pin and failure events (see Figure 17).



**Figure 17. Operating Modes Diagram**

# NCV7451

## ISO11898-2:2016 PARAMETER CROSS-REFERENCE TABLE

ISO 11898-2:2016 Specification		NCV7451 Datasheet
Parameter	Notation	Symbol
<b>DOMINANT OUTPUT CHARACTERISTICS</b>		
Single ended voltage on CAN_H	$V_{CAN\_H}$	$V_{o(dom)}(CANH)$
Single ended voltage on CAN_L	$V_{CAN\_L}$	$V_{o(dom)}(CANL)$
Differential voltage on normal bus load	$V_{Diff}$	$V_{o(dom)}(diff)$
Differential voltage on effective resistance during arbitration	$V_{Diff}$	$V_{o(dom)}(diff\_arb)$
Differential voltage on extended bus load range (optional)	$V_{Diff}$	NA
<b>DRIVER SYMMETRY</b>		
Driver symmetry	$V_{SYM}$	$V_{o(sym)}$
<b>DRIVER OUTPUT CURRENT</b>		
Absolute current on CAN_H	$I_{CAN\_H}$	$I_{o(SC)}(CANH)$
Absolute current on CAN_L	$I_{CAN\_L}$	$I_{o(SC)}(CANL)$
<b>RECEIVER OUTPUT CHARACTERISTICS, BUS BIASING ACTIVE</b>		
Single ended output voltage on CAN_H	$V_{CAN\_H}$	$V_{o(rec)}(CANH)$
Single ended output voltage on CAN_L	$V_{CAN\_L}$	$V_{o(rec)}(CANL)$
Differential output voltage	$V_{Diff}$	$V_{o(rec)}(diff)$
<b>RECEIVER OUTPUT CHARACTERISTICS, BUS BIASING INACTIVE</b>		
Single ended output voltage on CAN_H	$V_{CAN\_H}$	$V_{o(off)}(CANH)$
Single ended output voltage on CAN_L	$V_{CAN\_L}$	$V_{o(off)}(CANL)$
Differential output voltage	$V_{Diff}$	$V_{o(off)}(dif)$
<b>TRANSMIT DOMINANT TIMEOUT</b>		
Transmit dominant timeout, long	$t_{dom}$	$t_{dom}(TxDC)$
Transmit dominant timeout, short	$t_{dom}$	NA
<b>STATIC RECEIVER INPUT CHARACTERISTICS, BUS BIASING ACTIVE</b>		
Recessive state differential input voltage range	$V_{Diff}$	$V_{i(rec)}(diff)\_NM$
Dominant state differential input voltage range	$V_{Diff}$	$V_{i(dom)}(diff)\_NM$
<b>STATIC RECEIVER INPUT CHARACTERISTICS, BUS BIASING INACTIVE</b>		
Recessive state differential input voltage range	$V_{Diff}$	$V_{i(rec)}(diff)\_LP$
Dominant state differential input voltage range	$V_{Diff}$	$V_{i(dom)}(diff)\_LP$
<b>RECEIVER INPUT RESISTANCE</b>		
Differential internal resistance	$R_{Diff}$	$R_{i(diff)}$
Single ended internal resistance	$R_{CAN\_H}$ $R_{CAN\_L}$	$R_{i(cm)}(CANH)$ $R_{i(cm)}(CANL)$
<b>RECEIVER INPUT RESISTANCE MATCHING</b>		
Matching a of internal resistance	$m_R$	$R_{i(cm)}(m)$
<b>IMPLEMENTATION LOOP DELAY REQUIREMENT</b>		
Loop delay	$t_{Loop}$	$t_{pd\_rd}$ $t_{pd\_dr}$
<b>DATA SIGNAL TIMING REQUIREMENTS for use with bit rates above 1 Mbit/s and up to 2 Mbit/s</b>		
Transmitted recessive bit width @ 2 Mbit/s	$t_{Bit}(Bus)$	$t_{Bit}(Vi(diff))$
Received recessive bit width @ 2 Mbit/s	$t_{Bit}(RXD)$	$t_{Bit}(RxDC)$
Receiver timing symmetry @ 2 Mbit/s	$\Delta t_{Rec}$	$\Delta t_{Rec}$



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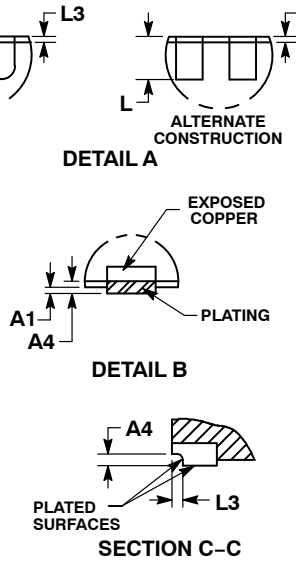
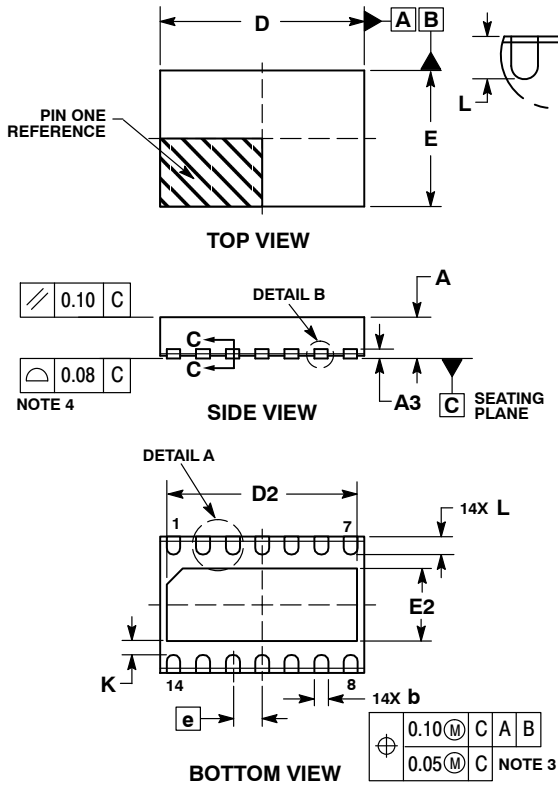
**ISO11898-2:2016 PARAMETER CROSS-REFERENCE TABLE** (continued)

ISO 11898-2:2016 Specification		NCV7451 Datasheet
Parameter	Notation	Symbol
<b>DATA SIGNAL TIMING REQUIREMENTS for use with bit rates above 2 Mbit/s and up to 5 Mbit/s</b>		
Transmitted recessive bit width @ 5 Mbit/s	$t_{\text{Bit(Bus)}}$	$t_{\text{Bit(VI(diff))}}$
Transmitted recessive bit width @ 5 Mbit/s	$t_{\text{Bit(RXD)}}$	$t_{\text{Bit(RxDC)}}$
Received recessive bit width @ 5 Mbit/s	$\Delta t_{\text{Rec}}$	$\Delta t_{\text{Rec}}$
<b>MAXIMUM RATINGS OF <math>V_{\text{CAN\_H}}</math>, <math>V_{\text{CAN\_L}}</math> AND <math>V_{\text{DIFF}}</math></b>		
Maximum rating $V_{\text{Diff}}$	$V_{\text{Diff}}$	$V_{\text{diff}}$
General maximum rating $V_{\text{CAN\_H}}$ and $V_{\text{CAN\_L}}$	$V_{\text{CAN\_H}}$ $V_{\text{CAN\_L}}$	CANH CANL
Optional: Extended maximum rating $V_{\text{CAN\_H}}$ and $V_{\text{CAN\_L}}$	$V_{\text{CAN\_H}}$ $V_{\text{CAN\_L}}$	NA
<b>MAXIMUM LEAKAGE CURRENTS ON CAN_H AND CAN_L, UNPOWERED</b>		
Leakage current on CAN_H, CAN_L	$I_{\text{CAN\_H}}$ , $I_{\text{CAN\_L}}$	$I_{\text{LI}}$
<b>BUS BIASING CONTROL TIMINGS</b>		
CAN activity filter time, long	$t_{\text{Filter}}$	NA
CAN activity filter time, short	$t_{\text{Filter}}$	$t_{\text{wake\_filt}}$
Optional: Wake-up timeout, short	$t_{\text{Wake}}$	NA
Optional: Wake-up timeout, long	$t_{\text{Wake}}$	$t_{\text{wake\_to}}$
Timeout for bus inactivity (Required for selective wake-up implementation only)	$t_{\text{Silence}}$	NA
Bus Bias reaction time (Required for selective wake-up implementation only)	$t_{\text{Bias}}$	NA

# NCV7451

## PACKAGE DIMENSIONS

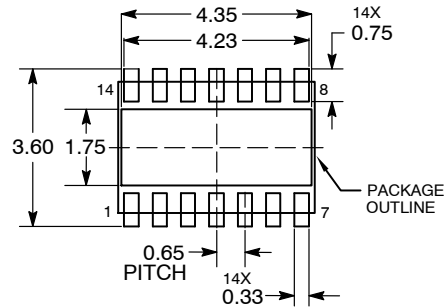
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- NOTES:
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  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
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  5. THIS DEVICE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	---	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.25	0.30	0.35
D	4.40	4.50	4.60
D2	4.13	4.20	4.27
E	2.90	3.00	3.10
E2	1.53	1.60	1.67
e	0.65 BSC		
K	0.30 REF		
L	0.35	0.40	0.45
L3	0.00	0.05	0.10

### RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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