

SITCore System on Chip



Overview

The SITCore SoCs provide a low cost way to add .NET computing power to any embedded product. Available as either a 48 pin QFN, a 100 pin LQFP or a 265 ball BGA, the SITCore SoCs let you design IoT products that are secure, easily integrated with the cloud, and can be easily manage and updated from the cloud for deployments of one to a million or more.

SC20xxx Features

- Low power modes including three independently controllable power domains
- RTC
- Watchdog
- Threading
- TCP/IP with SSL
 - Full .NET socket interface
 - Ethernet
 - PPP
- Graphics
 - Images
 - Fonts
 - Controls
- File System
 - Full .NET file interface
 - SD cards
 - USB drives
- Native extensions
 - Runtime Loadable Procedures
 - Device register access

- Signal controls
 - Generation
 - Capture
 - Pulse measurement

SC13xxx Features

All core OS features, like threading and memory management, are fully supported. Security is still an important part of the offer, with secure assemblies and secure storage. A subset of the crypto libraries is also included. All pin level features are supported, like PWM, ADC and the Signal Generators. SPI, UART, CAN, and I2C are also supported. Full USB Client support, with WebUSB and WinUSB.

There are some missing features that are not typically needed on micro-sized devices, but you still have options.

- Graphics: No native support but BasicGraphics library provides an alternative. In fact, the development board includes a color TFT SPI display.
- File System: No native file system support but ManagedFileSystem library is a full FAT implementation that supports file/directory access on SD cards over SPI bus.
- Networking: SC20 is still the proper way to access networks securely. However, Wiznet W5500 Ethernet chipset and ESP32 WiFi module can be used as an alternative.

Specifications

Spec	SC13048Q	SC20100S/B	SC20260B
Core	ARM Cortex-M4 32 bit	ARM Cortex-M7 32 bit	ARM Cortex-M7 32 bit
Speed	80 MHz	480 MHz	480 MHz
Math Co-processor	Single-precision	Double-precision	Double-precision
Internal RAM	160K	1 MByte	1 MByte
User RAM	128K	512K	512K + 32MB optional external
Internal Flash	512K	2 MByte	2 MByte
User Flash	220K + 8MB optional external	640K + 8MB optional external	640K + 8MB optional external
Instruction Cache	None	16 KByte	16 KByte
Data Cache	None	16 KByte	16 KByte
Package	48-QFN 7 x 7 mm	S/ LQFP100 14 x 14 mm	265-TFBGA 14 x 14 mm
		B/ 100-TFBGA 8 x 8 mm	

Spec	SC13048Q	SC20100S/B	SC20260B
Temperature Range	-40C to +85C	-40C to +85C	-40C to +85C

i NOTE

Resources are shared between your application and the operating system.*

Peripherals

Peripheral	SC13048Q	SC20100S/B	SC20260B
GPIO	37	74	163
SPI	2	3	3
I2C	2	2	3
UART	4 (2 with handshaking)	8 (4 with handshaking)	8 (4 with handshaking)
CAN	1	2	2
PWM	10	16	29
ADC	10	12	21
DAC	1	2	2
SD/SDIP/MMC	0	1	1
Quad SPI	1	1	1
USB Host	0	1	1
USB Client	1	1	1
Ethernet	0	1	1
LCD TFT	0	0	1
Graphics	BasicGraphics via SPI	Full Graphics via SPI	16BPP TFT
Camera	0	0	1

i NOTE

As many pins share peripherals, not all peripherals will be available.*

SC20xxx Power Consumption

	480MHz	240MHz
Running	205mA	110mA
Idle	170mA	97mA
Sleep	6.5mA	6.5mA
Shutdown	40uA	40uA

SC13xxx Power Consumption

	80MHz	40MHz
Running	12.6mA	7.5mA
Idle	6.2mA	4.2mA
Sleep	1.4mA	1.4mA
Shutdown	23uA	23uA

See the Power Management (<http://docs.ghielectronics.com/software/tinyclr/tutorials/power-management.html>) tutorial

Operational Voltage Levels

	Voltage Range
SC13xxx	1.71V ~ 3.6V
SC20xxx	1.62V ~ 3.6V

NOTE

Keep in mind that modules (SOM) may have other components that needs higher voltage, like QSPI and SDRAM. Those need to be accounted for.

Using Interrupts (IRQs)

The microcontrollers we use in our SITCore line of products do not support concurrent interrupts with the same pin number, even if the pins are on different ports (the port is denoted by the second letter of the GPIO pin name -- PA1 is pin 1 on port A). Therefore, interrupts are available on only 16 pins at any given time. For example, pins PA1 and PB1 cannot be used as interrupt pins at the same time, but PA1 and PB2 can. PA1 and PA2 can also be used with interrupts simultaneously.

Pinouts

GPIO pins are rated is 20mA per pin, 140mA total on all pins, and 5 volt tolerant.

SC13048Q Pinout

I/O	Function	I/O	Function	I/O	Function	
1	RTC_VBAT	17	OSPI_I02	33	PA12	USB_DP
2	PC13	18	PB0	34	PA13	
3	PC14	19	PB1	35		VSS
4	PC15	20	PB2	36		VDD_USB
5	PH0	21	PB10	37	PA14	
6	PH1	22	PB11	38	PA15	MOD
7		23		39	PB3	SP1_SCK
8	VSSA/VREF	24		40	PB4	SP1_MISO
9	VDDA/VREF+	25	PB12	41	PB5	SP1_MOSI
10	PA0	26	PB13	42	PB6	CAV1_TX
11	PA1	27	PB14	43	PB7	APP
12	PA2	28	PB15	44	PH3	
13	PA3	29	PA8	45	PB8	
14	PA4	30	PA9	46	PB9	
15	PA5	31	PA10	47		VSS
16	PA6	32	PA11	48		VDD

SC20100S/B Pinout

100S	100B	I/O	Function	100S	100B	I/O	Function	100S	100B	I/O	Function
1	A3	PE2	OSPI_I02	26	C2		VSS	51	K8	PB12	CAN2_RX
2	B3	PE3	LDR	27	D2		VDD	52	J8	PB13	CAN2_TX
3	C3	PE4		28	G3	PA4	ADC12.18	53	H10		USBH_N
4	D3	PE5	PWM15.1	29	H3	PA5	SPIS_SCK	54	G10		USBH_P
5	E3	PE6	PWM15.2	30	J3	PA6	SPIS_MISO	55	K9	PD8	UART3_TX
6	B2		VBAT	31	K3	PA7	SPIS_MOSI	56	J9	PD9	UART3_RX
7	A2	PC13	TAMPER	32	G4	PC4		57	H9	PD10	
8	A1	PC15	OSC32_IN	33	H4	PC5		58	G9	PD11	OSPI_I00
9	B1	PC14	OSC32_OUT	34	J4	PB0	UART4_CTS	59	K10	PD12	OSPI_I01
10	J1		VSS	35	K4	PB1	PWM3.4	60	J10	PD13	OSPI_I03
11	K1		VDD	36	G5	PB2	OSPI_CLK	61	H8	PD14	
12	C1		OSC_IN	37	H5	PE7	UART7_RX	62	G8	PD15	
13	D1		OSC_OUT	38	J5	PE8	UART7_TX	63	F10	PC5	UART6_TX
14	E1		NRST	39	K5	PE9	UART7_RTS	64	E10	PC7	UART6_RX
15	F1	PD0	ADC123.10	40	G6	PE10	UART7_CTS	65	F9	PC8	SDMMC1_D0
16	F2	PC1	ADC123.11	41	H6	PE11	ETH_MDC	66	E9	PC9	SDMMC1_D1
17	E2	PC2	ADC3.0	42	J6	PE12	SPH_SCK	67	D9	PA8	
18	F3	PC3	ADC3.1	43	K6	PE13	SPH_MISO	68	C9	PA9	UART1_TX ¹
19	G1		VSSA	44	G7	PE14	SPH_MOSI	69	D10	PA10	UART1_RX ¹
20	F7		VREF+(SI/PDR_ON(B) ¹)	45	H7	PE15		70	C10		USBC_N
21	H1		VDDA	46	J7	PB10	USBC_P	71	B10		USBC_P
22	G2	PA0	PWM5.1	47	K7	PB11	USBC_N	72	A10	PA13	
23	H2	PA1	ETH_REF_CLK	48	E7		VCAP	73	F8		VCAP
24	J2	PA2	ETH_MDIO	49	E5		VSS	74	E4		VSS
25	K2	PA3	PWM2.4	50	F5		VDD	75	F4		VDD(SI)/VDD(DC(B) ¹)

SC20260B Pinout

Ball	I/O	Function	Ball	I/O	Function	Ball	I/O	Function	Ball	I/O	Function
A1		GND	E6		VDD	J11		VSS	N16		VSS
A2	PI6	PWM8.2	E7		PDR_ON	J12		NC	N17		NC
A3	PI5	PWM8.1	E8		RESERVED pull to GND	J13		VDD	P1		VSSa
A4	PI4	DC D5	E9		VDD	J14		SPIS SCK	P2	PH3	FMC SDNE0
A5	PB5	SPIS MOSI	E10	PI13		J15	PK1	LCD G6	P3	PH4	LCD G5
A6		VDDDDO	E11		VDD	J16		VSS	P4	PH5	FMC SDNWE
A7		VCAP	E12	PD1	FMC D3	J17		VSS	P5	PH15	LCD G2
A8	PK5	LCD B6	E13	PC8	SDMMC1 D0	K1		NRST	P6	PH1	
A9	PG10	DC D2	E14	PC9	SDMMC1 D1	K2	PF6	UART7 RX	P7	PH13	FMC A7
A10	PG9	DC V5	E15	PA8	DC XCLK	K3	PF7	UART7 TX	P8	PH14	FMC A8
A11	PD5	UART2 TX	E16		USBC P	K4	PF8	UART7 RTS	P9	PH9	FMC D6
A12	PD4	UART2 RTS	E17		USBC N	K5		VDD	P10	PH11	FMC D8
A13	PC10	SDMMC1 D2	F1		NC	K6		NC	P11	PB10	DC2 SCL
A14	PA15	PWM2.1	F2		NC	K7		VSS	P12	PB11	DC2 SDA
A15	PI1	SPIS SCK	F3	PI10	ETH RX ER	K8		VSS	P13	PH10	DC D1
A16	PI0	PWM5.4	F4	PI11		K9		VSS	P14	PH11	PWM5.2
A17		VSS	F5		VDD	K10		VSS	P15	PD15	FMC D1
B1		VBAT	F6		NC	K11		VSS	P16	PD14	FMC D0
B2		VSS	F7		NC	K12		NC	P17		VDD
B3	PI7	PWM8.3	F8		NC	K13		VDD	R1	PC2 C1	ADC3.0
B4	PE1	FMC NB1I	F9		NC	K14	PI11	SPIS MISO	R2	PC3 C1	ADC3.1
B5	PB6	QSPI NCS	F10		NC	K15		VSS	R3	PA6	DC PWCLK
B6		VSS	F11		NC	K16		NC	R4		VSS
B7	PB4	SPIS MISO	F12		NC	K17		NC	R5	PA7	ETH CRS DV
B8	PK4	LCD B5	F13	PC7	UART6 RX	L1	PC0	VDDA	R6	PB2	QSPI CLK
B9	PG11	ETH TX EN	F14	PC6	UART6 TX	L2	PF10	ADC123.10	R7	PF12	FMC A6
B10	PI15	LCD B3	F15	PG8	FMC SDCLK	L3		ADC3.6	R8		VSS
B11	PD6	UART2 RX	F16	PG7		L4	PF9	UART7 CTS	R9	PF15	FMC A9
B12	PD3	UART2 CTS	F17		VDD3USB	L5		VDD	R10	PE12	FMC D9
B13	PC11	SDMMC1 D3	G1	PF2	FMC A2	L6		NC	R11	PE15	FMC D12
B14	PA14		G2		NC	L7		VSS	R12	PJ5	LCD B6
B15	PI2	SPIS MISO	G3	PF1	FMC A1	L8		VSS	R13	PH9	DC D0
B16	PH15	LCD B4	G4	PF0	FMC A0	L9		VSS	R14	PH12	DC D3
B17	PH14	CAN1 RX	G5		VDD	L10		VSS	R15	PD11	QSPI IO0
C1	PC15	OSC32 OUT	G6		NC	L11		VSS	R16	PD12	QSPI IO1
C2	PC14	OSC32 IN	G7		VSS	L12		NC	R17	PD13	QSPI IO3
C3	PE2	QSPI IO2	G8		VSS	L13		VDD	T1	PA0 C1	ADC12.0
C4	PE0	FMC NB1O	G9		VSS	L14	PI10	SPIS MOSI	T2	PA1 C1	ADC12.1
C5	PB7	APP	G10		VSS	L15		VSS	T3	PA5	ADC12.19
C6	PB3	SPIS SCK	G11		VSS	L16		NC	T4	PC4	ETH RXD0
C7	PK6	LCD B7	G12		NC	L17		NC	T5	PB1	PWM3.4
C8	PK3	LCD B4	G13		VDD	M1		VREF+	T6	PJ2	LCD B3
C9	PG12		G14	PG5	FMC BA1	M2	PC1	ETH MDC	T7	PH1	FMC SDNRAS
C10		VSS	G15	PG6		M3	PC2	ADC123.12	T8	PG0	FMC A10
C11	PD7	MOD	G16		VSS	M4	PC3	ADC12.13	T9	PE8	FMC D5
C12	PC12	SDMMC1 DE	G17		VDD3USB	M5		VDD	T10	PE13	FMC D10
C13		VSS	H1	PI12	LCD H5VNC	M6		NC	T11	PH6	PWM12.1
C14	PI3	SPIS MOSI	H2	PI13	LCD IOVNC	M7		NC	T12		VSS
C15	PA13		H3	PI14	LCD CLK	M8		NC	T13	PH8	DC3 SDA
C16		VSS	H4	PF3	FMC A3	M9		NC	T14	PB12	CAN2 RX
C17		VDDDDO	H5		VDD	M10		NC	T15		USBH P
D1	PE5	DC D6	H6		NC	M11		NC	T16	PD10	FMC D15
D2	PE4	DC D4	H7		VSS	M12		NC	T17	PD9	FMC D14
D3	PE3	LDR	H8		VSS	M13		VDD	U1		VSS
D4	PB9	DC3 SDA	H9		VSS	M14	PI9	UART8 RX	U2	PA3	PWM2.4
D5	PB8	DC3 SCL	H10		VSS	M15		VSS	U3	PA4	DC H5
D6	PG15	FMC SDNGAS	H11		VSS	M16		NC	U4	PC5	ETH RXD1
D7	PK7	LCD DE	H12		NC	M17		NC	U5	PB3	PWM3.3
D8	PG14	ETH TXD1	H13		VDD	N1		VREF-	U6	PH0	LCD B4
D9	PG13	ETH TXD0	H14	PG4	FMC BA0	N2	PH2	FMC SDCKE0	U7	PJ4	LCD B5
D10	PJ14		H15	PG3		N3	PA2	ETH MDIO	U8	PG1	FMC A11
D11	PJ12	LCD G3	H16	PG2	FMC A12	N4	PA1	ETH REF CLK	U9	PE7	FMC D4
D12	PD2	SDMMC1 CMD	H17	PK2	LCD G7	N5	PA0	PWM5.1	U10	PE14	FMC D11
D13	PD0	FMC D7	J1		OSC OUT	N6	PI0	ADC1.16	U11		VCAP
D14	PA10	UART1 RX	J2		OSC IN	N7		VDD	U12		VDDDDO
D15	PA9	UART1 TX	J3		VSS	N8		VDD	U13	PH7	DC3 SCL
D16	PH13	CAN1 TX	J4	PF5	FMC A5	N9	PE10	FMC D7	U14	PB13	CAN2 TX
D17		Vcap	J5	PF4	FMC A4	N10		VDD	U15		USBH N
E1		NC	J6		NC	N11		VDD	U16	PD6	FMC D13
E2	PI9		J7		VSS	N12		VDD	U17		VSS
E3	PC13	TAMPER	J8		VSS	N13	PI8	UART8 TX			
E4	PI8		J9		VSS	N14	PI7				
E5	PE6	DC D7	J10		VSS	N15	PI6	LCD R7			

Device Startup

The SITCore is held in reset while the RESET pin is low. Releasing RESET will begin the system startup process.

There are three different components of the device firmware:

1. GHI Electronics Bootloader: initializes the system, updates TinyCLR when needed, and executes TinyCLR.
2. TinyCLR: used to load, debug, and execute the managed application.
3. Managed application: the program developed by you or your software developer.

Which components get executed on startup is controlled by manipulating the LDR pin. It is pulled high on startup during normal program execution. When low, the device waits in the GHI Electronics Bootloader. Otherwise, the managed application is executed. The APP pin is used to stop the managed application from running.

Additionally, the communications interface between the host PC and the SITCore is selected on startup through the MOD pin, which is pulled high on startup. The USB interface is selected when MOD is high and UART1 is selected when MOD is low.

The above discussed functions of the LDR, APP, and MOD pins are only available during startup. After startup, the pins return to the default GPIO state and are available as a GPIO (or peripheral pin) in your application. Check out the Special Pins ([../../software/tinyclr/special-pins.html](#)) page for more information.

TinyCLR OS

TinyCLR OS provides a way to program the SITCore in C# from the Microsoft Visual Studio integrated development environment. To get started you must first install the firmware on the SITCore (instructions below) and then go to the TinyCLR Getting Started ([../../software/tinyclr/getting-started.html](#)) page for instructions.

Loading the Firmware

1. Activate the bootloader, hold the LDR signal low while resetting the board.
2. Open TinyCLR Config tool.
3. Select the correct COM port and 'Connect' to the device. If you are not seeing it then the device is not in the loader mode.
4. Download the firmware. Select the downloaded firmware in TinyCLR Config and click 'Update Firmware'.

You can also update the firmware manually. Download the firmware and learn how to use the GHI Electronics Bootloader manually

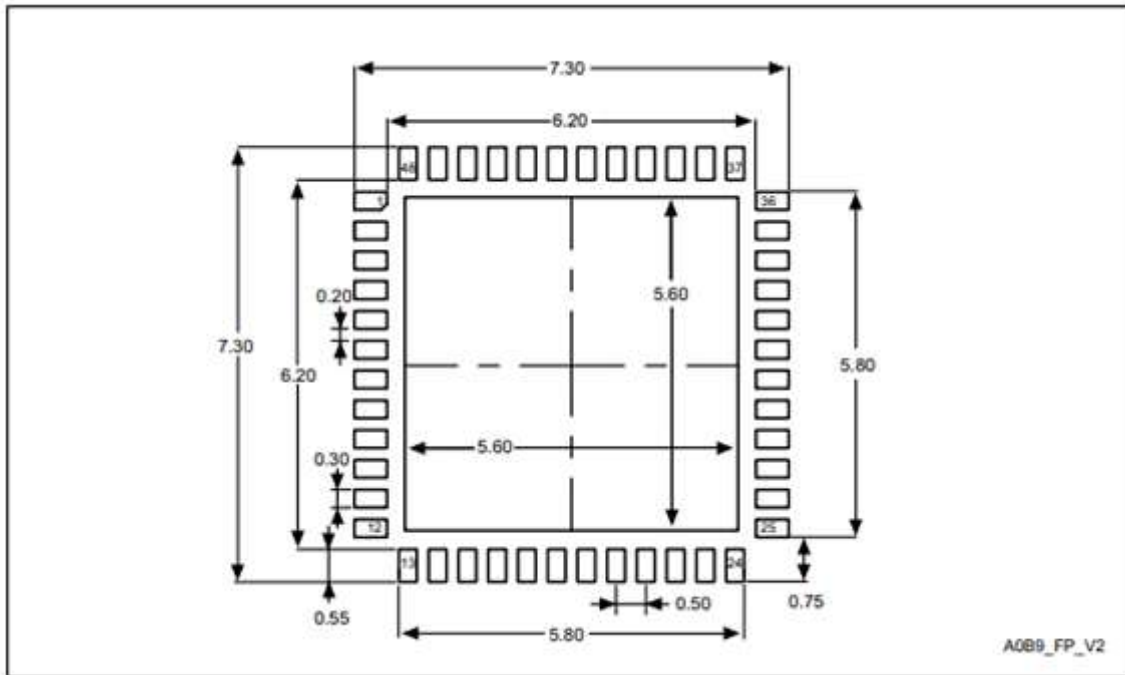
Start Coding

Now that you have installed the bootloader and firmware on the SITCore, you can setup your host computer and start programming. Go to the TinyCLR Getting Started ([../../software/tinyclr/getting-started.html](#)) page for instructions.

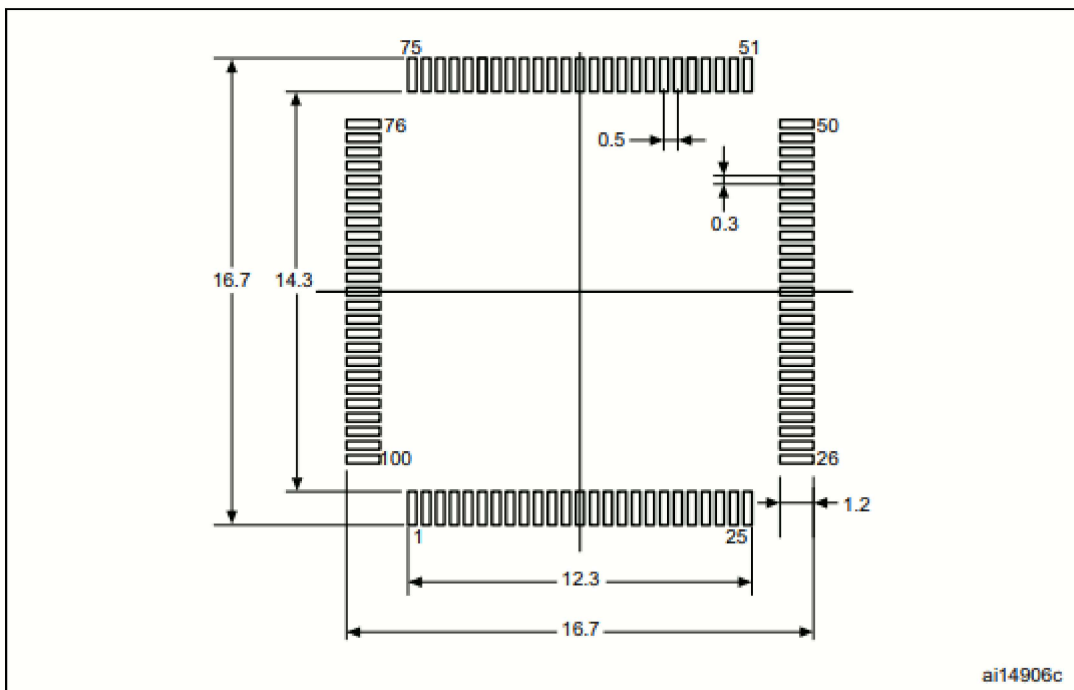
Design Considerations

Footprints

This is the recommended footprint for the SC13048Q:

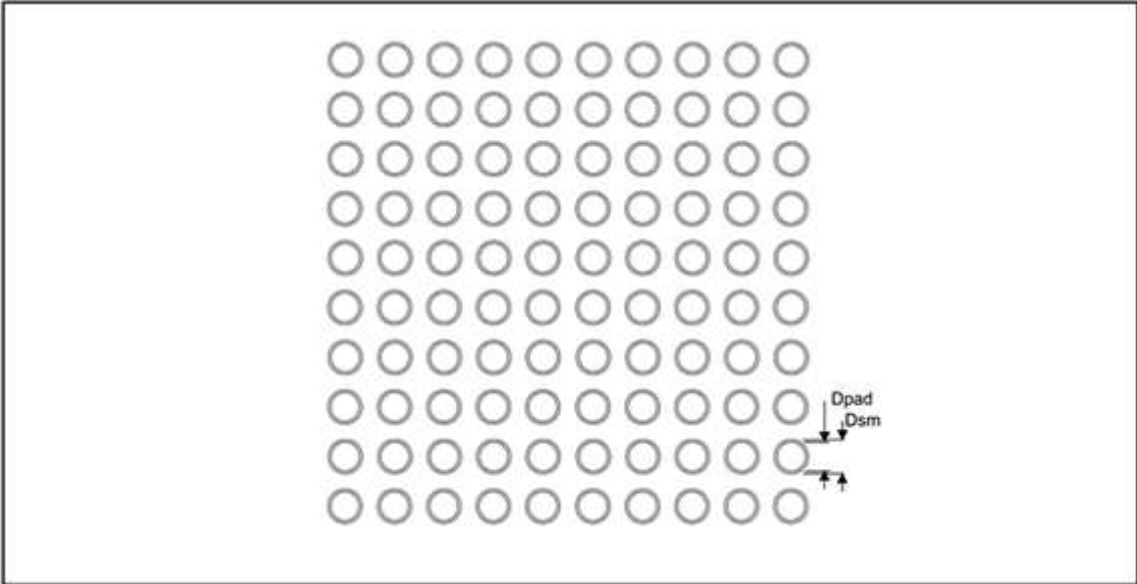


This is the recommended footprint for the SC20100S:



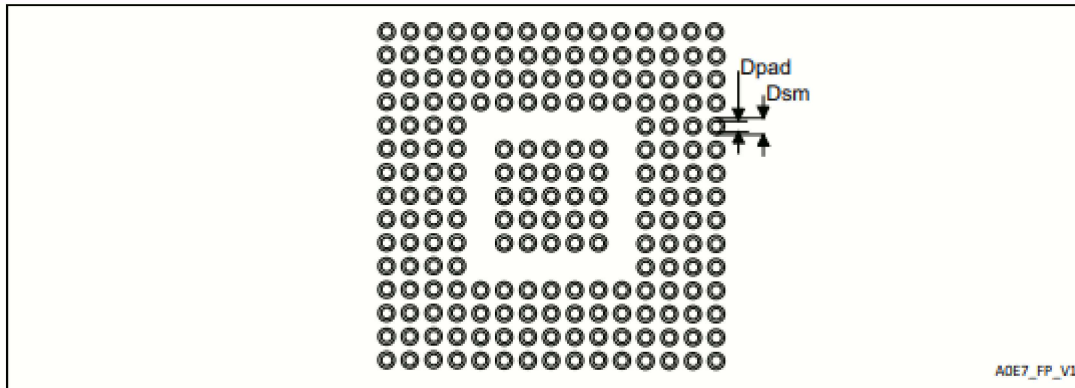
1. Dimensions are expressed in millimeters.

This is the recommended footprint for the SC20100B:



Dimension	Recommended values
Pitch	0.8
Dpad	0.400 mm
Dsm	0.470 mm typ (depends on the soldermask registration tolerance)
Stencil opening	0.400 mm
Stencil thickness	Between 0.100 mm and 0.125 mm
Pad trace width	0.120 mm

This is the recommended footprint and PCB design rules for the SC20260B:



Dimension	Recommended values
Pitch	0.8 mm
Dpad	0.225 mm
Dsm	0.290 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.250 mm
Stencil thickness	0.100 mm

Required Pins

Exposing the following pins is required in every design to enable device programming, updates, and recovery:

- RESET
- LDR
- APP
- MOD (required to select a the debug interface)
- Desired debug interface(s) (see below)

For information on these and other important pins, please refer to the Special Pins page.

Debug Interface

All SITCore products provide two debug and deployment interfaces: USB and serial. Whether USB or serial debugging is selected is determined by the state of the MOD pin during startup and reset. If the MOD pin is held high during startup, the USB debug interface will be selected. If the MOD pin is held low during startup, the serial debug interface will be selected.

When in serial mode, all SITCore products use UART1 except SC20260B chipset/boards use UART5.

Power Supply

A clean power source, suitable for digital circuitry, is needed to power SITCore SoCs. Voltages should be regulated to within 10% or better of the specified voltage. Decoupling capacitors of 0.1 uF are needed near every power pin. Additionally, a large capacitor, typically 47 uF, should be placed near the SoC if the power supply is more than few inches away.

Analog Considerations

It is a good idea to provide a separate filtered supply line for the V_{DDA} , and V_{REF+} pins. Additionally, on the 260 pin devices, you may want to provide a separate filtered ground connection for the V_{SSA} and V_{REF-} pins. While this is not needed for ADC operation, it does help to ensure more accurate ADC readings by reducing analog supply noise.

Crystals

There is a lot to consider when selecting a crystal -- especially the RTC crystal. Please consult AN2867 from STMicroelectronics.

Main Crystal

Most 8 MHz quartz crystals and ceramic resonators from various manufacturer will work with SITCore SoCs. The table below will tell you what to look for based on the crystal's maximum equivalent series resistance (ESR), shunt capacitance (C_0), and load capacitance (CL). Keeping the total capacitance of $C_0 + CL$ well below the recommended maximum will provide more of a safety margin for stable and reliable oscillator operation.

The SITCore SC13048 SoC main clock can also operate using an internal oscillators, with no need for any crystals, even when using USB. If an application requires better accuracy, like when running CAN for example, an external oscillator can be added.

Max crystal ESR (ohms)	Recommended max total of C_0 and CL (pF)
40	49
50	44
60	40
70	37
80	35
100	31
200	22
300	18

RTC Crystal

It can be difficult to select the right RTC crystals, that is due to the RTC oscillator running on an extremely low power. The table below should help. For reliable operation, the total capacitance of C0 (crystal shunt capacitance) and CL (crystal load capacitance) must be less than the recommended max total of C0 and CL.

The SITCore SC13048 SoC built in RTC can also operate using an internal oscillator when a 32.768Khz crystals is not present, however adding an external crystal gives better RTC accuracy.

Max crystal ESR (kilohms)	Recommended max total of C0 and CL (pF)
30	9.9
40	8.5
50	7.6
60	7.0
70	6.5
80	6.0
90	5.7
100	5.4

When laying out your board, it is best to keep the crystal as close as possible to the SoC. The oscillator circuit should also be surrounded by a grounded guard ring or ground plane on the same layer to reduce noise.

RTC Power

The VBAT pin is optionally used to power up the RTC when the system main power is turned off. Also, SITCore chipsets and modules include a built in charging circuit internally, that can be enabled to charge an external supercap. See the RTC tutorial (../software/tinyclr/tutorials/real-time-clock.html) for further details.

QuadSPI External Flash

SITCore supports 16 MByte external QuadSPI flash chips. The options are in the table below.

Manufacture	Part Number
Winbond Electronics	W25Q128JVSIM

Manufacture	Part Number
Winbond Electronics	W25Q128JVSIQ

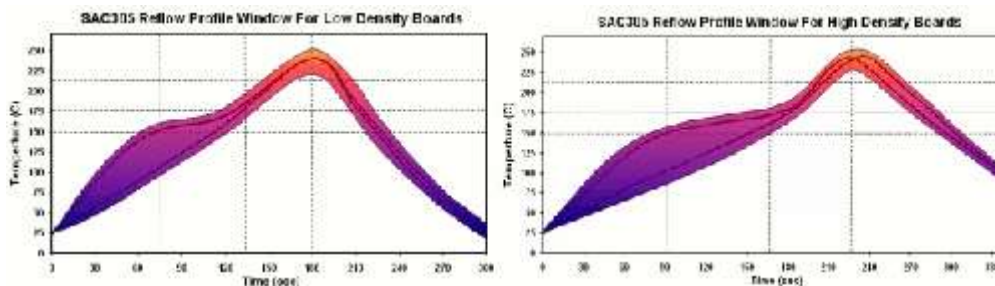
Reset

SITCore processors have a permanent internal pull up resistor that is connected to the RESET (NRST) pin. No external pull up resistor is needed.

Oven Reflow Profile

SITCore SoCs are not sealed for moisture. **Baking SoCs before reflow is recommended and required in a humid environment.** The process of reflow can damage the SoC if the temperature is too high or exposure is too long.

The lead-free reflow profiles used by GHI Electronics are shown below. The profiles are based on AIM SAC 305 solder (3% silver, 0.5% copper). The thermal mass of the assembled board and the sensitivity of the components on it affect the total dwell time. Differences in the two profiles are where they reach their respective peak temperatures as well as the time above liquids (TAL). The shorter profile applies to smaller assemblies, whereas the longer profile applies to larger assemblies such as back-planes or high-density boards. The process window is described by the shaded area. These profiles are only starting-points and general guidance. The particulars of the oven and the assembly will determine the final process.



REFLOW RISE TIME SEC MAX	TEMP TO THROUGH (302°F)	PROGRESS THROUGH (302°F-347°F)	TEMP 230°C-245°C (445°F-475°F)	TEMP ABOVE 217°C (422°F)	Cooling Rate ~4 °C / SEC	COOLING LENGTH AMBIENT TO COOL DOWNS
Short Profiles	≤ 75 Sec	30-60 Sec	45-75 Sec	50-60 Sec	45L 15 Sec	2.75-3.5 Min
Long Profiles	≤ 60 Sec	60-90 Sec	45-75 Sec	60-90 Sec	45L 15 Sec	4.5-5.0 Min

SITCore Dev Boards

The SITCore development boards are ready to get any project started as quickly and easily as possible. Click [here](#) for details.

You can visit our main website at www.ghielectronics.com
 our community forums at forums.ghielectronics.com
 and our documentation at docs.ghielectronics.com