Single 4 x 1 and Dual 2 x 1 Multiplexers

DESCRIPTION

The DG9414, a single 4 to 1 multiplexer, and the DG9415, a dual 2 x 1 multiplexer, are monolithic CMOS analog devices designed for high performance low voltage operation. Combining low power, high speed, low on-resistance and small physical size, the DG9414 and DG9415 are ideal for portable and battery powered applications requiring high performance and efficient use of board space.

Both the DG9414 and DG9415 are built on Vishay Siliconix's low voltage BCD-15 process. Minimum ESD protection, per Method 3015.7, is 2000 V. An epitaxial layer prevents latchup. Break-before-make is guaranteed for DG9415.

FEATURES

- Low voltage operation (+ 2.7 V to + 12 V)
- Low on-resistance - R_{DS}(on): 14 Ω
- Low power consumption
- TTL compatible
- ESD protection > 2000 V (method 3015.7)
- Available in TSSOP-10 (aka MSOP-10)
- **Compliant to RoHS Directive 2002/95/EC**

Pb-free
RoHS
COMPLIANT

BENEFITS

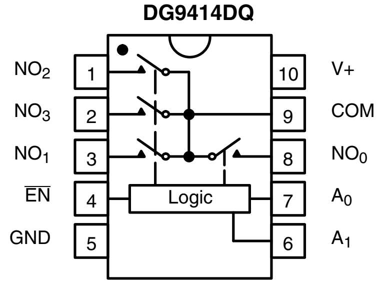
- High accuracy
- Simple logic interface
- Reduce board space

APPLICATIONS

- Battery operated systems
- Portable test equipment
- Sample and hold circuits
- Cellular phones
- Communication systems
- Networking equipment

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

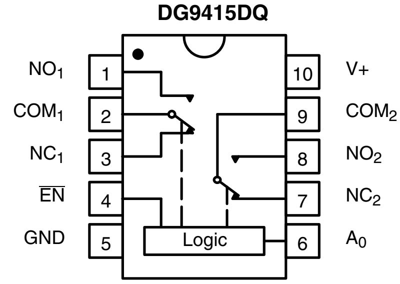
DG9414DQ



$\overline{EN}$	A_1	A_0	On Switch
1	X	X	None
0	0	0	NO_0
0	0	1	NO_1
0	1	0	NO_2
0	1	1	NO_3

X = Do not care

DG9415DQ



$\overline{EN}$	A_0	On Switch
1	X	None
0	0	NC_1 NC_2
0	1	NO_1 NO_2

X = Do not care

ORDERING INFORMATION

Temp Range	Package	Part Number
- 40 °C to 85 °C	MSOP-10	DG9414DQ-T1-E3
		DG9415DQ-T1-E3

ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit
Reference V+ to GND	- 0.3 to + 13	V
IN, COM, NC, NO[a]	- 0.3 to (V+ + 0.3)	V
Continuous Current (Any terminal)	± 20	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)	± 40	mA
ESD (Method 3015.7)	> 2000	V
Storage Temperature (D Suffix)	- 65 to 150	°C

Notes:
a. Signals on S_X, D_X or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.

SPECIFICATIONS (V+ = 3 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 3 V, ± 10 %, V_{IN} = 0.4 V or 2.4 V[e]		Temp.[a]	Limits - 40 °C to 85 °C Min.[c]	Typ.[b]	Max.[c]	Unit
Analog Switch								
Analog Signal Range[d]	V_{ANALOG}			Full	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7 V, V_{COM} = 1 V/1.5 V/2 V I_{NO} or I_{NC} = 5 mA		Room Full		63	97 101	Ω
R_{ON} Match[d]	ΔR_{ON}			Room		3	11	Ω
R_{ON} Flatness[d,f]	R_{ON} Flatness			Room		14	33	Ω
NO or NC Off Leakage Current[g]	$I_{NO/NC(off)}$	V+ = 3.3 , V_{NO} or V_{NC} = 0.3 V/3 V V_{COM} = 3 V/0.3 V		Room Full	- 1 - 10		1 10	nA
COM Off Leakage Current[g]	$I_{COM(off)}$			Room Full	- 1 - 10		1 10	nA
Channel-On Leakage Current[g]	$I_{COM(on)}$	V+ = 3.3 V V_{COM} = V_{NO} or V_{NC} = 0.3 V/3 V		Room Full	- 1 - 10		1 10	nA
Digital Control								
Input Current[g]	I_{INL} or I_{INH}	V_{IN} = 0 or V+		Full	- 1		1	µA
Input High Voltage[d]	V_{INH}			Full	1.6			V
Input Low Voltage[d]	V_{INL}			Full			0.4	V
Dynamic Characteristics								
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 1.5 V		Room Full		102	125 142	ns
Turn-Off Time	t_{OFF}			Room Full		45	68 75	ns
Break-Before-Make Time	t_D			Room	7	78		ns
Transition Time	t_{trans}	V_{NO} = 1.5 V/0 V, V_{NC} = 0 V/1.5 V		Room Full		81	128 144	ns
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω		Room		3		pC
Off-Isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		Room		- 58		dB
Channel-to-Channel Crosstalk (DG9415)	X_{TALK}	R_L = 50 Ω, f = 1 MHz		Room		- 64		dB
NO, NC Off Capacitance	$C_{NO(off)}$, $C_{NC(off)}$	f = 1 MHz	DG9414	Room		11		pF
			DG9415	Room		10		pF
COM Off Capacitance	$C_{COM(off)}$		DG9414	Room		26		pF
			DG9415	Room		13		pF
COM On Capacitance	$C_{COM(on)}$		DG9414	Room		43		pF
			DG9415	Room		25		pF
Power Supply								
Power Supply Range	V+				2.7		3.3	V
Power Supply Current[h]	I+	V+ = 3.3 V, V_{IN} = 0 V or 3.3 V		Full			1	µA

SPECIFICATIONS (V+ = 5 V)

Parameter	Symbol	Test Conditions Otherwise Unless Specified V+ = 5 V, ± 10 %, V_{IN} = 0.8 V or 2.4 V[e]		Temp.[a]	Limits - 40 °C to 85 °C Min.[c]	Typ.[b]	Max.[c]	Unit
Analog Switch								
Analog Signal Range[d]	V_{ANALOG}			Full	0		V+	V
On-Resistance	R_{ON}	V+ = 4.5 V, V_{COM} = 1.5 V/2.5 V/3.5 V I_{NO} or I_{NC} = 10 mA		Room Full		33	56 60	Ω
R_{ON} Match	ΔR_{ON}			Room		2	10	
R_{ON} Flatness[f]	R_{ON} Flatness			Room		10	20	
NO or NC Off Leakage Current[g]	$I_{NO/NC(off)}$	V+ = 5.5 V, V_{NO} or V_{NC} = 1 V/4.5 V V_{COM} = 4.5 V/1 V		Room Full	- 1 - 10		1 10	nA
COM Off Leakage Current[g]	$I_{COM(off)}$			Room Full	- 1 - 10		1 10	
Channel-On Leakage Current[g]	$I_{COM(on)}$	V+ = 5.5 V V_{COM} = V_{NO} or V_{NC} = 1 V/4.5 V		Room Full	- 1 - 10		1 10	
Digital Control								
Input Current[h]	I_{INL} or I_{INH}	V_{IN} = 0 or V+		Full	- 1		1	µA
Input High Voltage[d]	V_{INH}			Full	1.8			V
Input Low Voltage[d]	V_{INL}			Full			0.6	
Dynamic Characteristics								
Turn-On Time[h]	t_{ON}	V_{NO} or V_{NC} = 3 V		Room Full		56	77 86	ns
Turn-Off Time[h]	t_{OFF}			Room Full		25	46 50	
Break-Before-Make Timet[h]	t_D			Room	7	34		
Transition Time	t_{trans}	V_{NO} = 3 V/ 0 V, V_{NC} = 0 V/3 V		Room Full		47	77 84	
Off-Isolation	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz		Room		- 58		dB
Channel-to-Channel Crosstalk (DG9415)	X_{TALK}	R_L = 50 Ω, f = 1 MHz		Room		- 64		
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{gen} = 0 V, R_{gen} = 0 Ω		Room		6		pC
NO, NC Off Capacitance	$C_{NO(off)}$, $C_{NC(off)}$	f = 1 MHz	DG9414	Room		11		pF
			DG9415	Room		10		
COM Off Capacitance	$C_{COM(off)}$		DG9414	Room		25		
			DG9415	Room		13		
COM On Capacitance	$C_{COM(on)}$		DG9414	Room		42		
			DG9415	Room		24		
Power Supply								
Power Supply Range	V+				4.5		5.5	V
Power Supply Current[h]	I+	V+ = 5.5 V, V_{IN} = 0 V or 5.5 V		Full			1	µA

Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min and max values.
g. Guaranteed by 12 V leakage testing, not production tested.
h. Guaranteed by worst case test conditions and not subject to test.

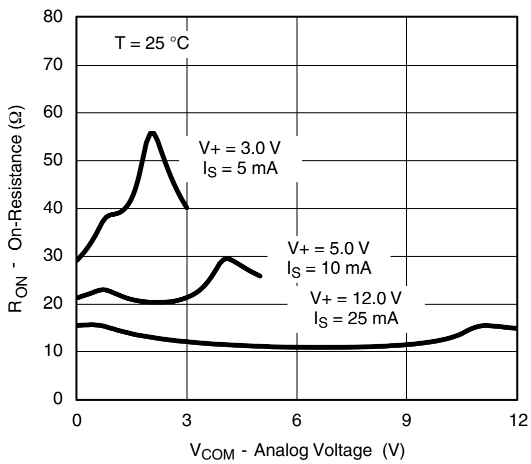
SPECIFICATIONS (V+ = 12 V)

Parameter	Symbol	Test Conditions Unless Specified V+ = 12 V, V_{IN} = 0.8 V or 2.4 V[e]	Temp.[a]	Limits - 40 °C to 85 °C Min.[c]	 Typ.[b]	 Max.[c]	Unit
Analog Switch							
Analog Signal Range[d]	V_{ANALOG}		Full	0		12	V
R_{ON} Match	ΔR_{ON}		Room		1	9	Ω
R_{ON} Flatness[d,f]	R_{ON} Flatness		Room		1	10	Ω
On-Resistance	R_{ON}	V+ = 10.8 V, I_{NO}, I_{NC} = 25 mA V_{COM} = 2/9 V	Room Full		14	17 19	Ω
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V_{COM} = 1/11 V V_{NO}, V_{NC} = 11/1 V	Room Full	- 1 - 10		1 10	nA
	$I_{COM(off)}$		Room Full	- 1 - 10		1 10	nA
Channel On Leakage Current	$I_{COM(on)}$	V_{NO}, V_{NC} = V_{COM} = 11/1 V	Room Full	- 1 - 10		1 10	nA
Digital Control							
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Input High Voltage[d]	V_{INH}		Full	2.4			V
Input Low Voltage[d]	V_{INL}		Full			0.8	V
Dynamic Characteristics							
Turn-On Time[h]	t_{ON}	R_L = 300 Ω, C_L = 35 pF V_{NO}, V_{NC} = 5 V See Figure 2	Room Full		33	55 59	ns
Turn-Off Time[h]	t_{OFF}	R_L = 300 Ω, C_L = 35 pF V_{NO}, V_{NC} = 5 V See Figure 2	Room Full		17	40 41	ns
Break-Before-Make Time Delay[h]	t_D	DG419L Only, V_{NC}, V_{NO} = 5 V R_L = 300 Ω, C_L = 35 pF	Room	2	24		ns
Transition Time	t_{trans}	V_{NO} = 5 V/ 0 V, V_{NC} = 0 V/ 5 V	Room Full		29	56 59	ns
Charge Injection[d]	Q_{INJ}	V_g = 0 V, R_g = 0 Ω, C_L = 1 nF	Room		13		pC
Off Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room		- 58		dB
Channel-to-Channel Crosstalk[d]	X_{TALK}	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	Room		- 64		dB
NO, NC Off Capacitance[d]	$C_{NO(off)}$, $C_{NC(off)}$	V_{IN} = 0 or V+, f = 1 MHz; DG9414	Room		10		pF
		V_{IN} = 0 or V+, f = 1 MHz; DG9415	Room		10		pF
COM Off Capacitance	$C_{COM(off)}$	V_{IN} = 0 or V+, f = 1 MHz; DG9414	Room		24		pF
		V_{IN} = 0 or V+, f = 1 MHz; DG9415	Room		13		pF
COM On Capacitance[d]	$C_{COM(on)}$	V_{IN} = 0 or V+, f = 1 MHz; DG9414	Room		40		pF
		V_{IN} = 0 or V+, f = 1 MHz; DG9415	Room		23		pF
Power Supplies							
Positive Supply Current	I+	V_{IN} = 0 V or 12 V	Full			1	µA

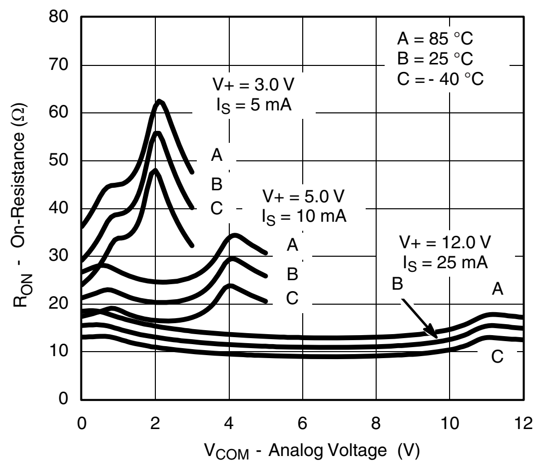
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. Typical values are for design aid only, not guaranteed nor subject to production testing.
c. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this datasheet.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Difference of min and max values.
g. Guaranteed by 12 V leakage testing, not production tested.
h. Guaranteed by worst case test conditions and not subject to test.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

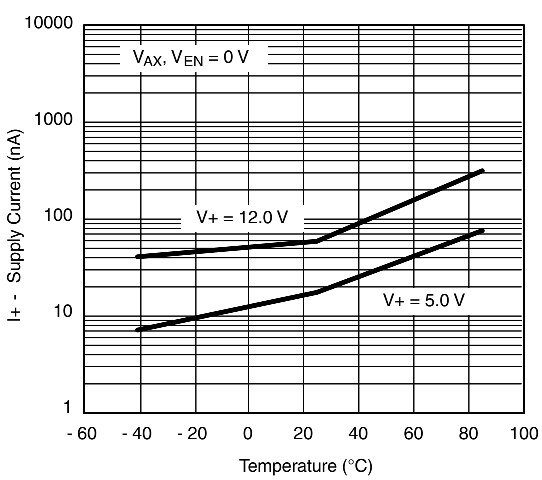
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



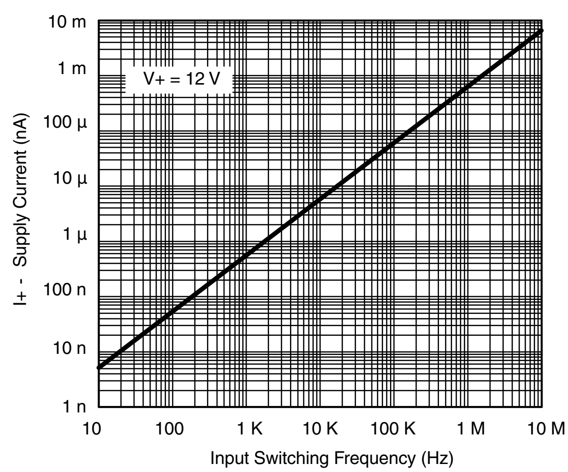
R_{ON} vs. V_{COM} and Supply Voltage



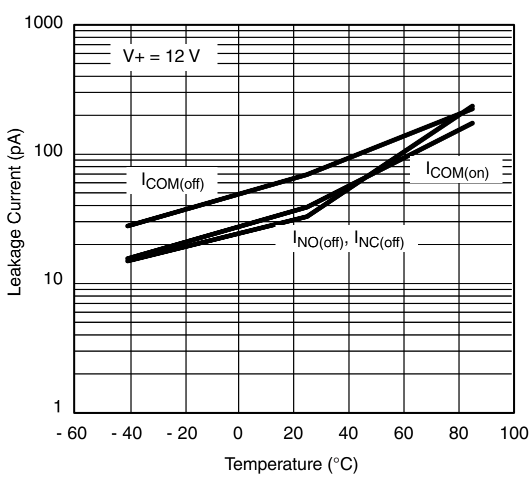
R_{ON} vs. Analog Voltage and Temperature



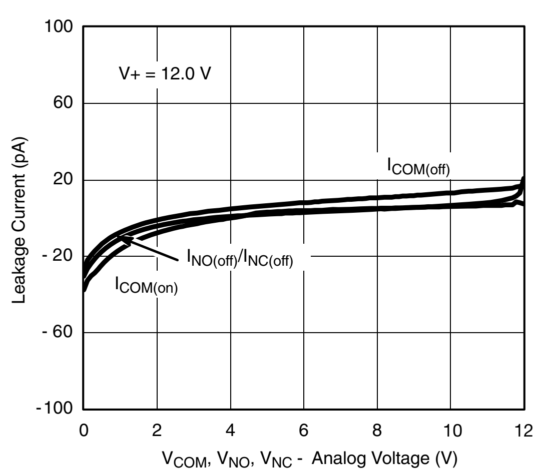
Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency

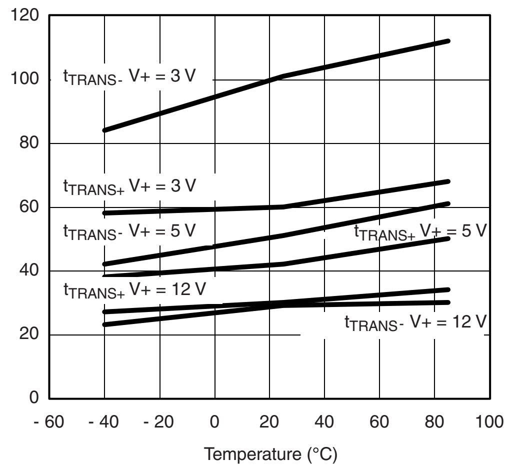


Leakage Current vs. Temperature

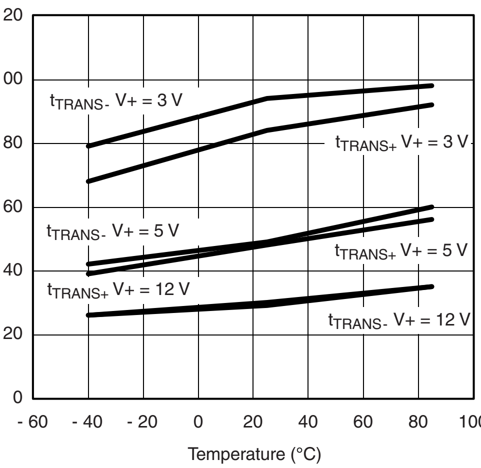


Leakage vs. Analog Voltage

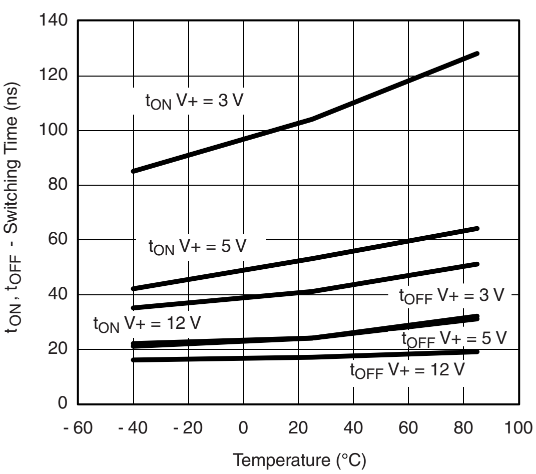
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



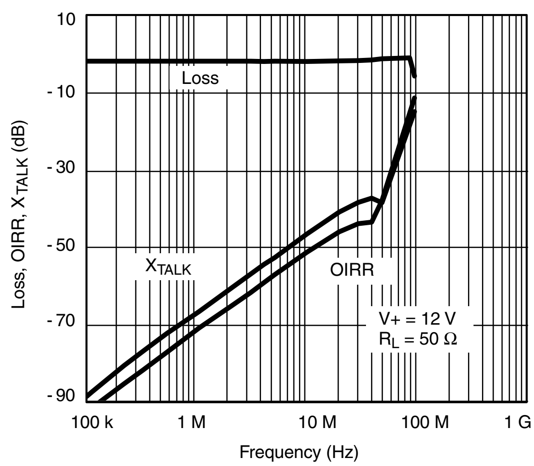
Transistion Time vs. Temperature (DG9414)



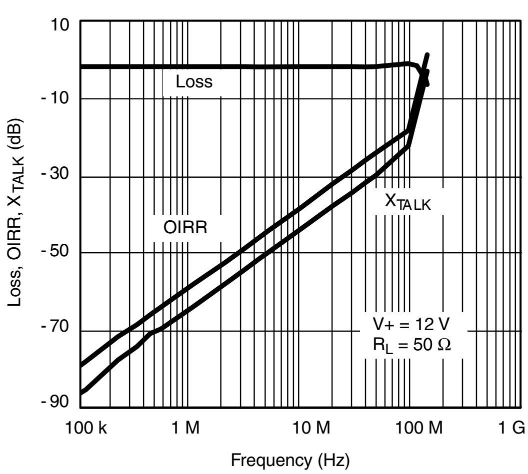
Transistion Time vs. Temperature (DG9415)



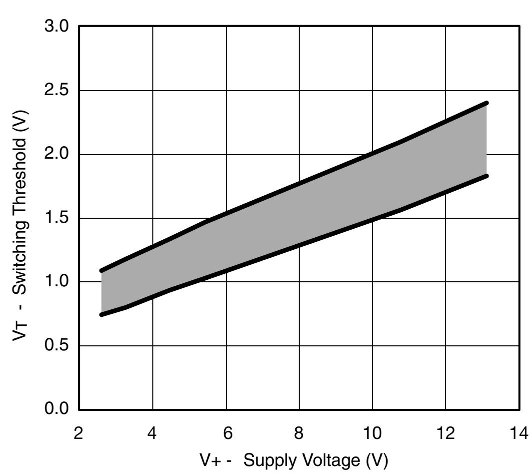
Switching Time vs. Temperature



Insertion Loss, Off-Isolation Crosstalk vs. Frequency (DG9414)

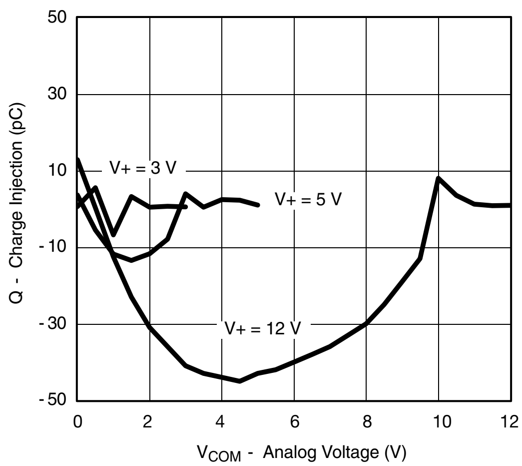


Insertion Loss, Off-Isolation Crosstalk vs. Frequency (DG9415)

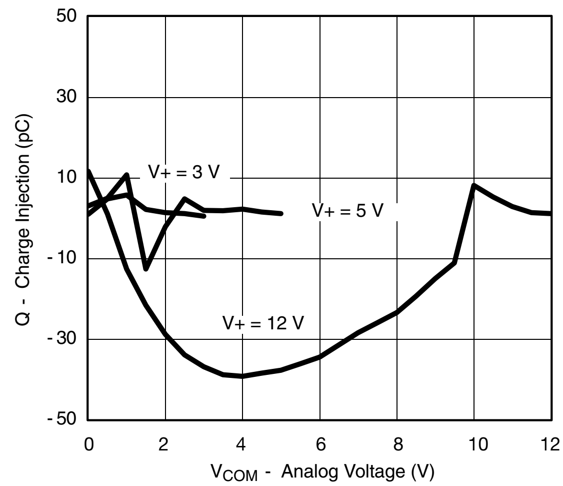


Switching Threshold vs. Supply Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Charge Injection vs. Analog Voltage (DG9414)



Charge Injection vs. Analog Voltage (DG9415)

SCHEMATIC DIAGRAM (Typical Channel)

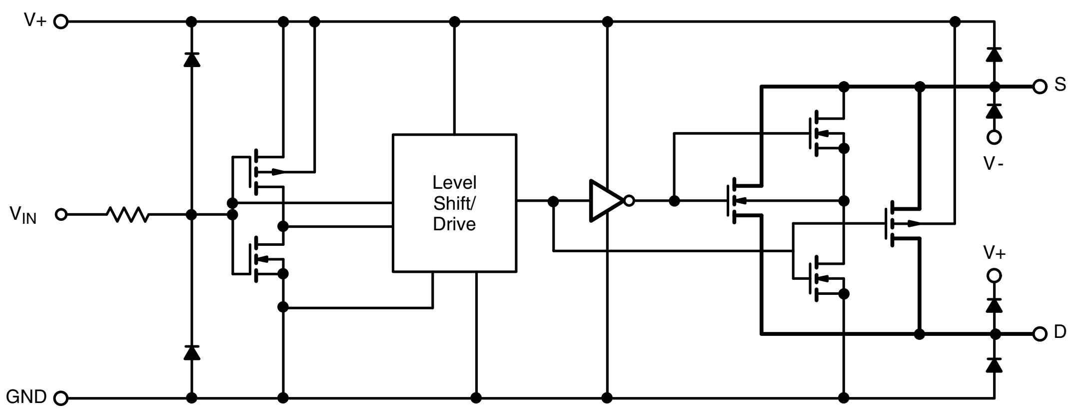
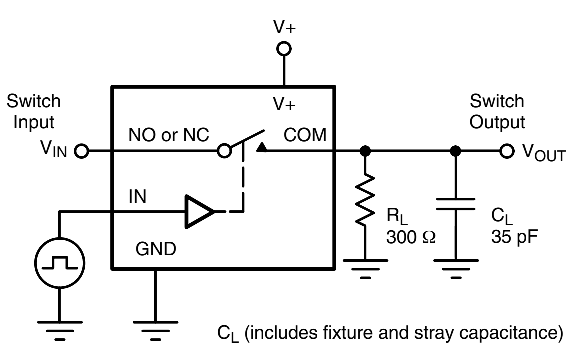


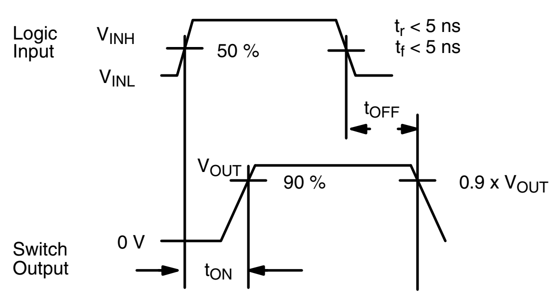
Figure 1.

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{IN} \frac{R_L}{R_L + r_{ON}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time

TEST CIRCUITS

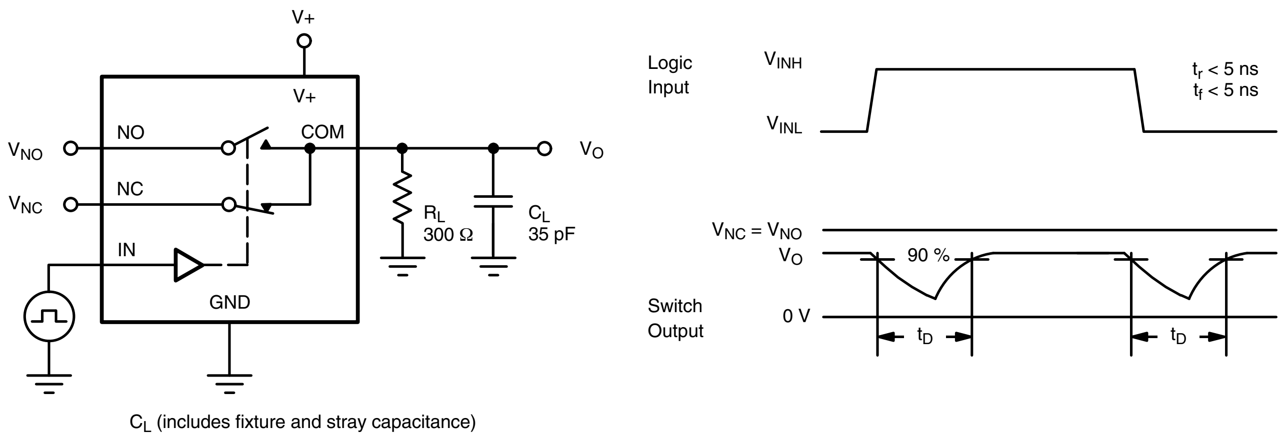


Figure 3. Break-Before-Make

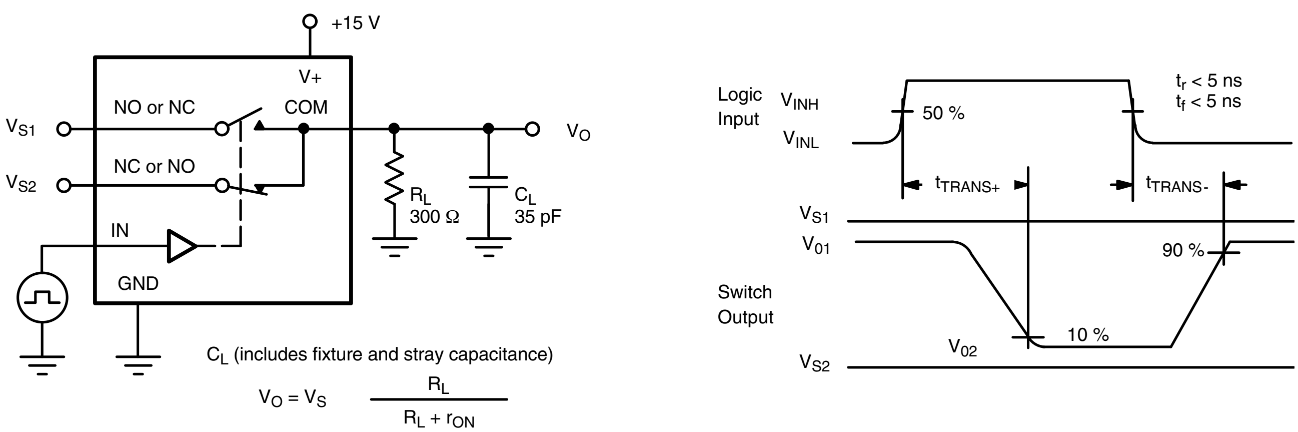


Figure 4. Transition Time

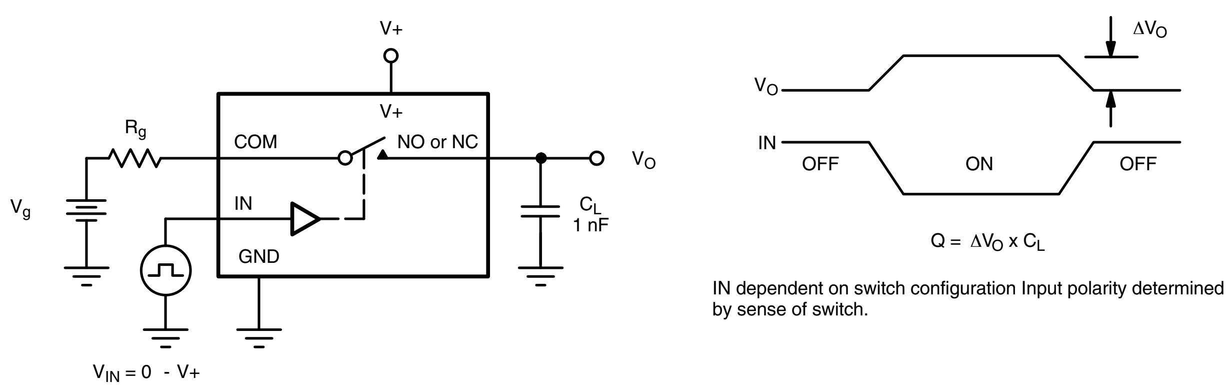
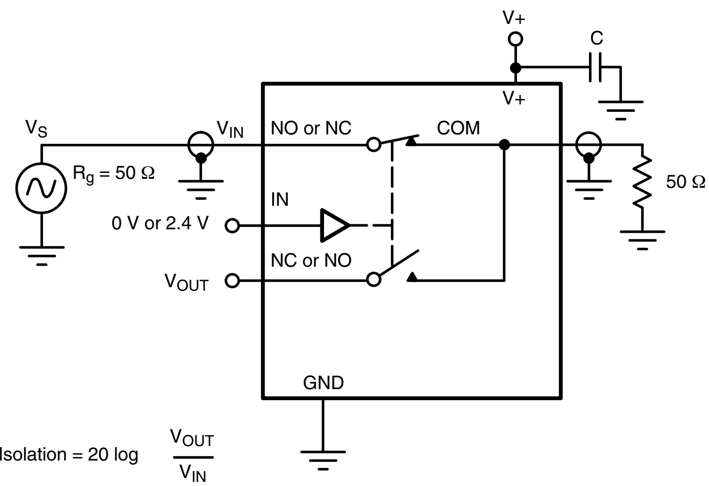


Figure 5. Charge Injection

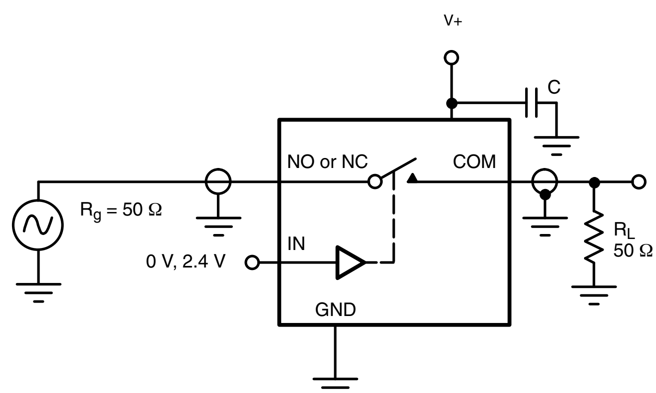
TEST CIRCUITS



$$X_{TALK}\ \text{Isolation} = 20\log\frac{V_{OUT}}{V_{IN}}$$

C = RF bypass

Figure 6. Crosstalk



$$\text{Off Isolation} = 20\log\frac{V_{COM}}{V_{NO/NC}}$$

C = RF Bypass

Figure 7. Off Isolation

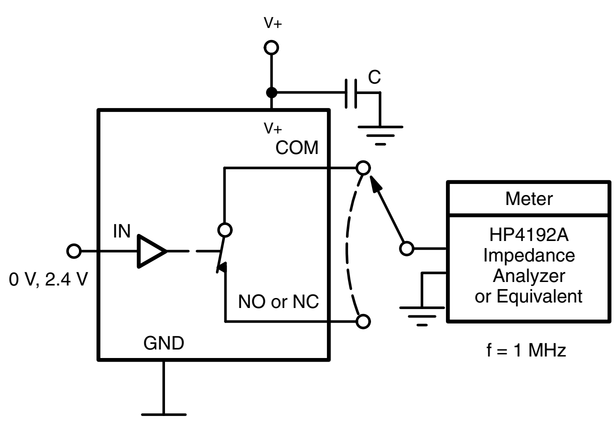
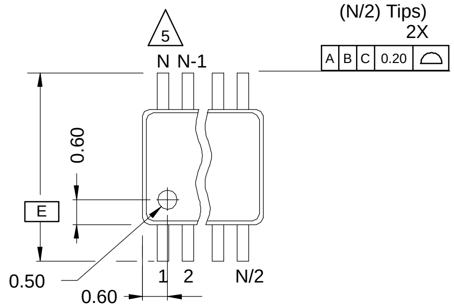


Figure 8. Source/Drain Capacitances

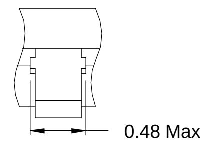
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?71766.

MSOP: 10-LEADS

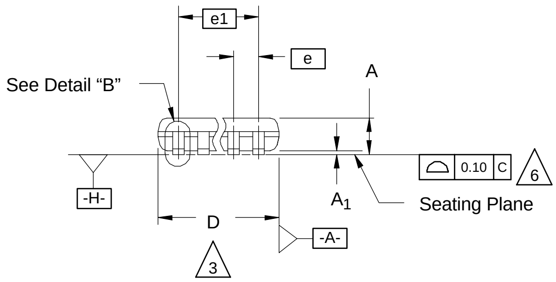
JEDEC Part Number: MO-187, (Variation AA and BA)



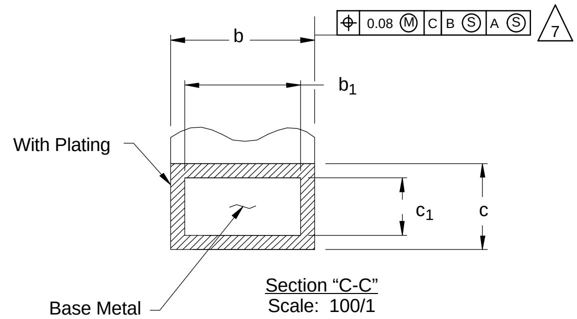
Top View



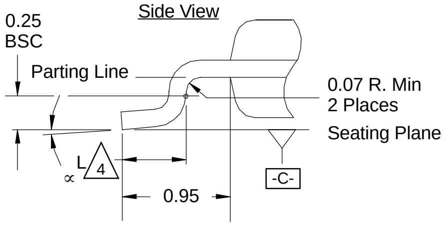
Detail "B"
(Scale: 30/1)
Dambar Protrusion



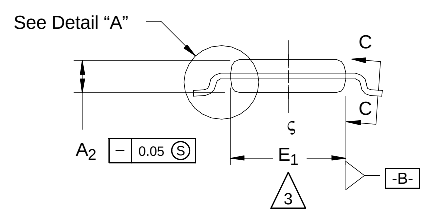
Side View



Section "C-C"
Scale: 100/1
(See Note 8)



Detail "A"
(Scale: 30/1)



End View

NOTES:

1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 10L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.17	-	0.27	8
b_1	0.17	0.20	0.23	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.50 BSC			
e_1	2.00 BSC			
L	0.40	0.55	0.70	4
N	10			5
∝	0°	4°	6°	

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