

TLE4943C

Data Sheet
V 1.2, July 2018



Never stop thinking

Edition July 2018

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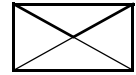
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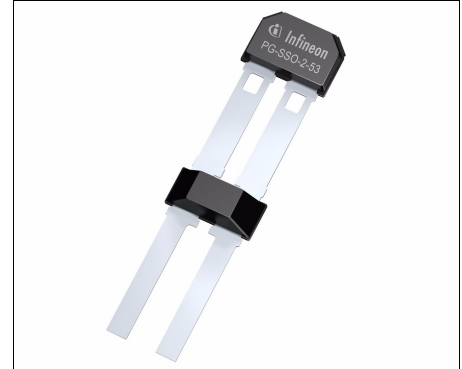


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1 Product Description

1.1 Overview

The TLE4943C is an integrated, active magnetic field sensor for wheel speed applications based on Hall technology. Its basic function is to measure the speed of a pole wheel or a ferromagnetic toothed wheel. It has a two wire-current interface using the AK protocol for communication. This protocol provides beside the speed signal additional information as direction of wheel rotation and air gap information. The sensor combines a fast power-up time with a low cut-off frequency. Excellent sensitivity and accuracy combined with its wide operational temperature range makes the sensor ideally suited for harsh automotive requirements. The TLE4943C is additionally provided with an overmolded 1.8nF capacitor for improved EMC performance.



1.2 Features

- Two wire current interface according AK protocol
- Hall based principle
- Integrated magnetic field sensor for wheel speed measurement
- Detection of rotation direction
- Additional airgap information
- Single chip solution
- High sensitivity
- Large operating air-gaps
- Magnetic pre-induction possible
- Automotive qualified temperature ranges from $T_J = -40^{\circ}\text{C}$ to 150°C
- 1.8nF overmolded capacitor
- Wide operating range from 6.5V to 20V
- Green package with lead-free plating

Product Name	Product Type	Ordering Code	Package
TLE4943C	TLE4943C	SP001963054	PG-SSO-2-53

2 Functional Description

2.1 General

The basic operation of the TLE4943C is to measure the differential magnetic field of ferromagnetic or permanent magnet target wheels and generate an output signal which represents the motion of these objects. Additionally the direction of rotation of a rotating target wheel and the quality (strength) of the magnetic signal are detected. For the applications with ferromagnetic toothed wheels a back bias magnet is required. The magnetic measurement is based on three equally spaced Hall elements, integrated on the IC. The two outer Hall elements have a distance of 2.5mm, the third Hall element is placed in the middle between the outer Hall elements. The outer Hall elements generate a differential signal which corresponds to the speed of the detected object. All three Hall elements are used for the information of direction detection. The IC has a three-level current interface which corresponds to the AK-protocol described below in this data sheet.

Magnetic offsets of up to +/-30mT are cancelled by a self-calibration algorithm. Only a few magnetic edges after start-up (uncalibrated mode) are necessary to finish the self-calibration and providing offset corrected signals in calibrated mode. Independent of the mode every increment of the encoder triggers a signal output. The output signal frequency represents the increment frequency, e.g. 100 increments per second are equal to 100Hz. The frequency of the magnetic signal is half of the output signal frequency.

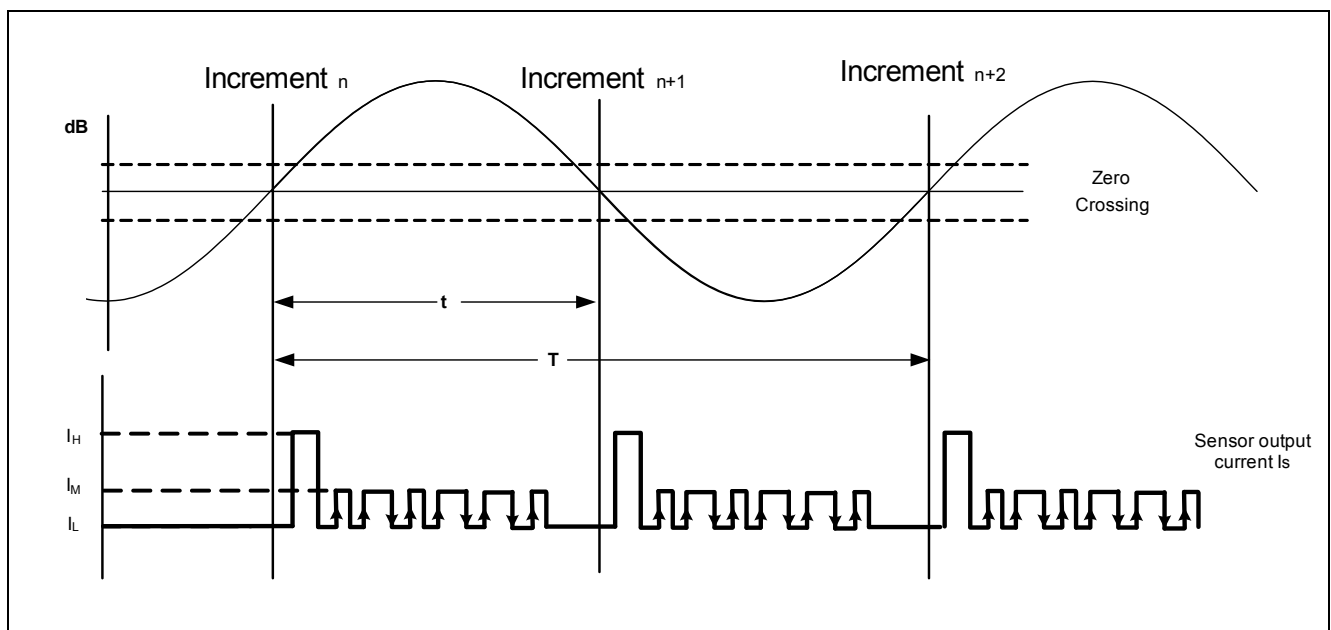


Figure 1 Definition of increment

2.2 Pin Configuration and Sensitive Area

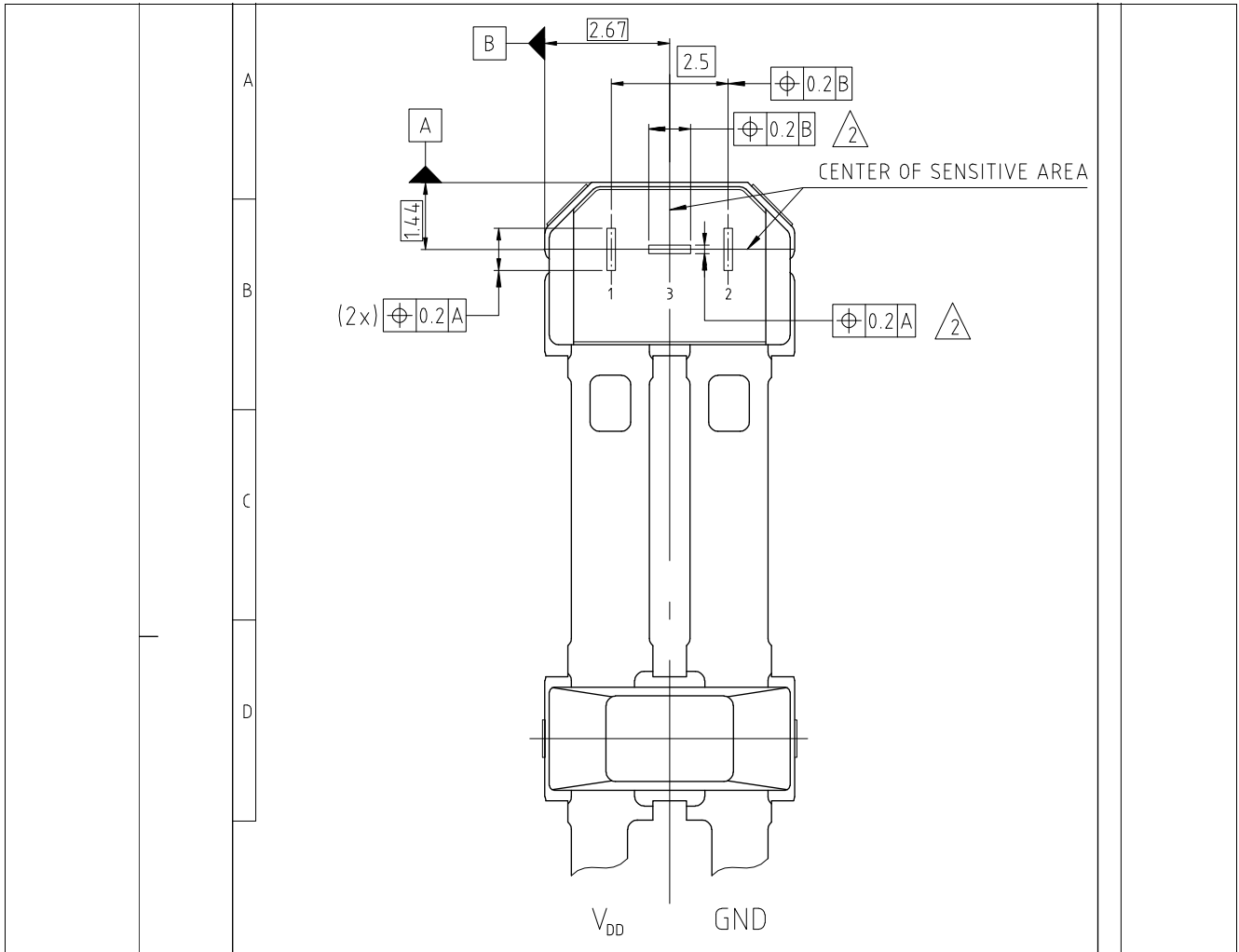


Figure 2 Pin configuration and sensitive area (view on frontside marking of component)

2.3 Marking and Data Matrix Code Description

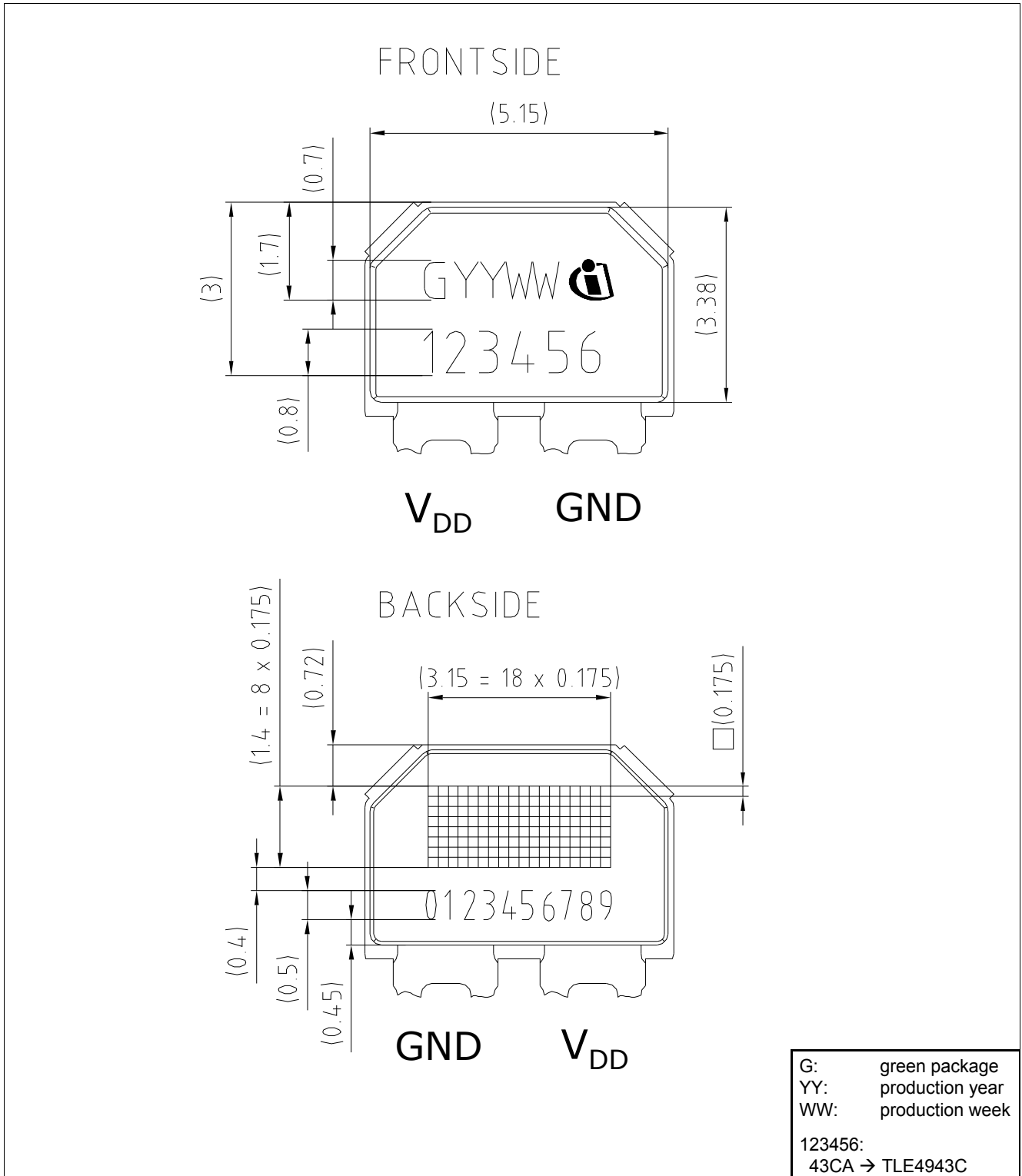


Figure 3 Marking of PG-SSO-2-53

2.4 Block Diagram

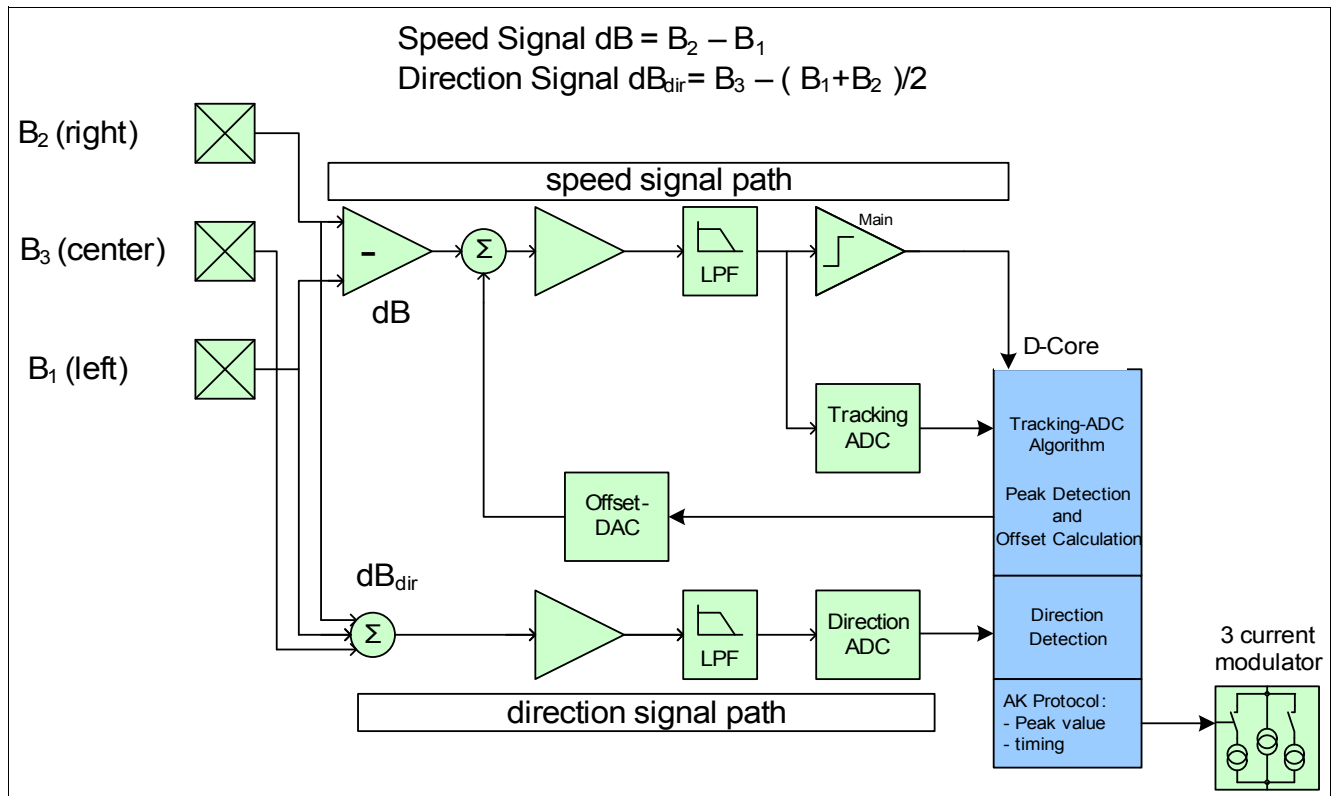


Figure 4 Block Diagram

2.5 Functional Block Description

TLE4943C is composed of the following main blocks:

- Hall elements (B_1 , B_2 , B_3)
- Analog to Digital Converter in the speed signal path (ADC)
- Offset Digital to Analog Converter (Offset DAC)
- Low Pass Filter (LPF)
- Three Current modulator
- Main Comparator (Main)
- Analog to Digital Converter in the direction path (Direction ADC)
- Digital Core (D-core)
- Amplifier for speed and direction path
- Current modulator

The speed signal dB , calculated out of $B_2 - B_1$, is amplified and low pass filtered. Afterwards signal is digitized. Algorithms in the D-Core for peak detection and offset calculation are executed. The offset is calculated out of two detected extrema $(\max + \min) / 2$. This offset is fed back into speed signal path with an Digital to Analog converter to correct any offsets. The main comparator compares the speed signal with zero value. During uncalibrated mode, output of speed pulse is triggered in the D-Core by exceeding a certain threshold $(2 \times dB_{limit})$.

The direction signal is calculated out of all three Hall elements (described in Figure 4). The direction signal is amplified, filtered and digitized. In the D-Core the direction is determined and the data protocol is issued and converted into a current modulated signal. The protocol consists of the speed pulse, issued by zero crossing, and other data bits determined by the D-Core.

2.6 Typical Application Circuit

The circuit below shows the recommended application circuit with reverse bias and overvoltage protection.

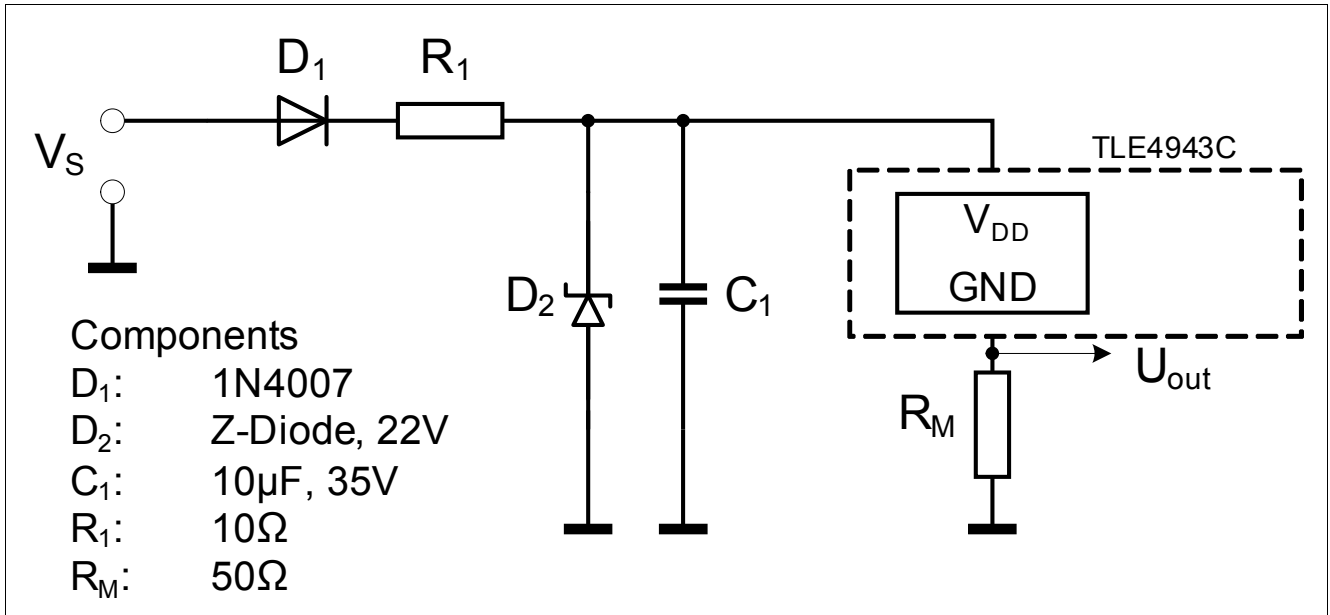


Figure 5 Application circuit

2.7 Protocol Description

The protocol consists of a pre-bit, a speed pulse and a nine data information bits (data protocol). The data protocol is Manchester-coded. This means the value of a bit is coded in a rise- or a fall of the signal between the mid-current value (I_{mid}) and low-current (I_{low}) in a certain time window. "0" is represented by a mid-low transition and "1" is coded by a low-mid transition. Unused bits are output as default values.

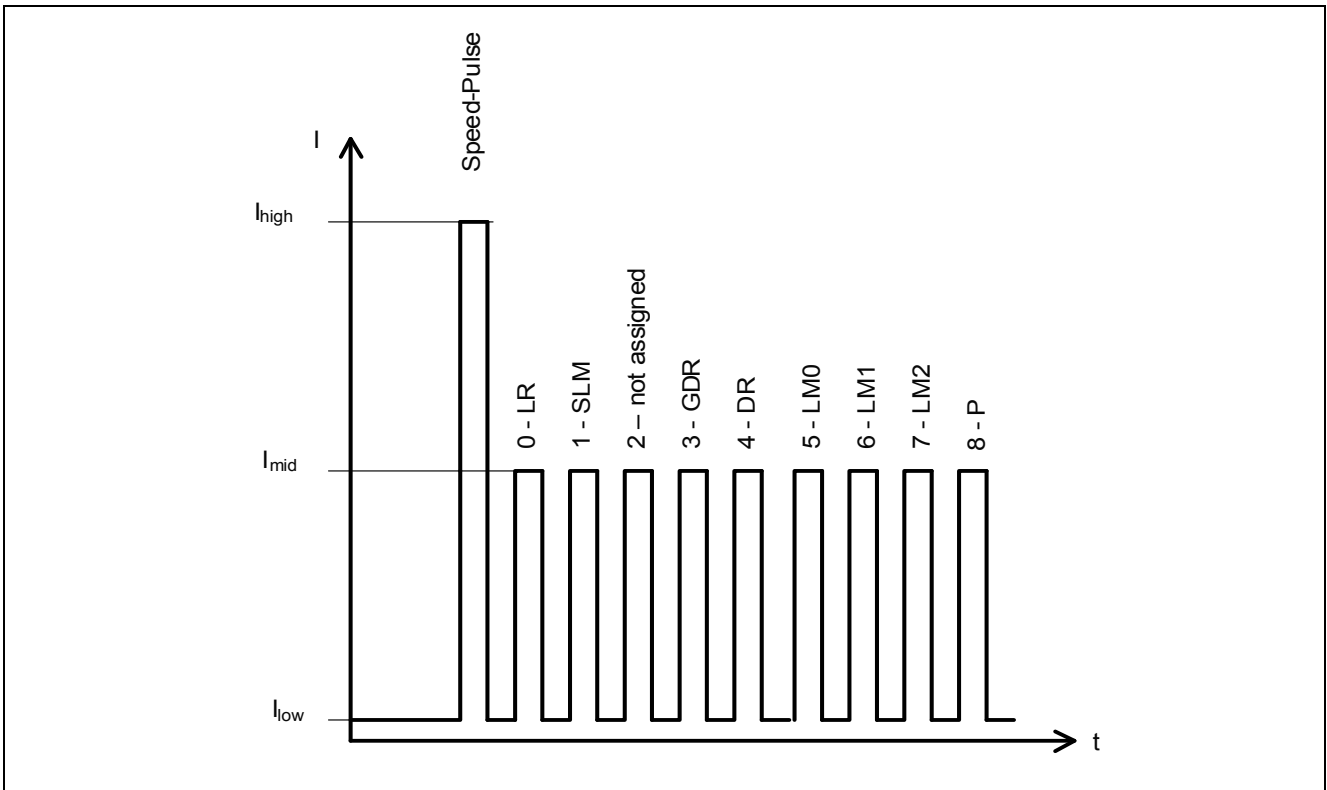


Figure 6 Coding of data bits.

Table 1 Coding of Additional Information

Bit #	Meaning	Name	Value after power up / under voltage	Condition
0	Error bit, Airgap reserve	LR	0	"1" if $dB < dB_{LR}$ (1=error)
1	Validity of signal amplitude measurement	SLM	1	0=measurement of LM0, LM1, LM2 is valid; 1=invalid
2	not assigned		0	
3	Direction validity	GDR	0	"1" = valid, "0" = invalid
4	Direction of rotating information	DR	0	"0" =direction positive

Table 1 Coding of Additional Information (cont'd)

Bit #	Meaning	Name	Value after power up / under voltage	Condition
5	Air gap gauge	LM0	0	LSB of airgap gauge
6		LM1	0	
7		LM2	0	MSB of airgap gauge
8	Parity	P	to be currently calculated	Always set to get even parity (inclusive Parity bit itself)

2.7.1 Definition of Rotation Direction

The direction of rotation is positive if the direction of rotation and the positive Y – axis of the sensor head are pointing in the same direction. This is shown in **Figure 7**. The coordinate system must be regarded as fixed in the sensor head. This must be taken into consideration with assembly variations. In the left representation, frontside of the sensor (=marking) points to multipole ring (=encoder) located behind. For positive direction of rotation the direction of rotation bit (DR) is set to "0".

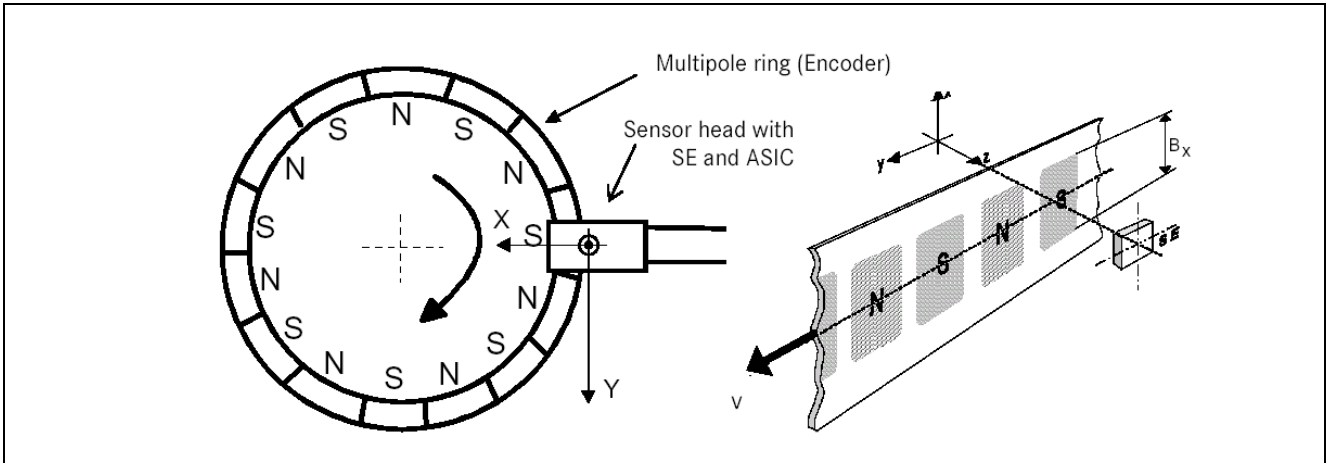


Figure 7 Definition of rotation direction, Sensor Marking (=Frontside) points to encoder

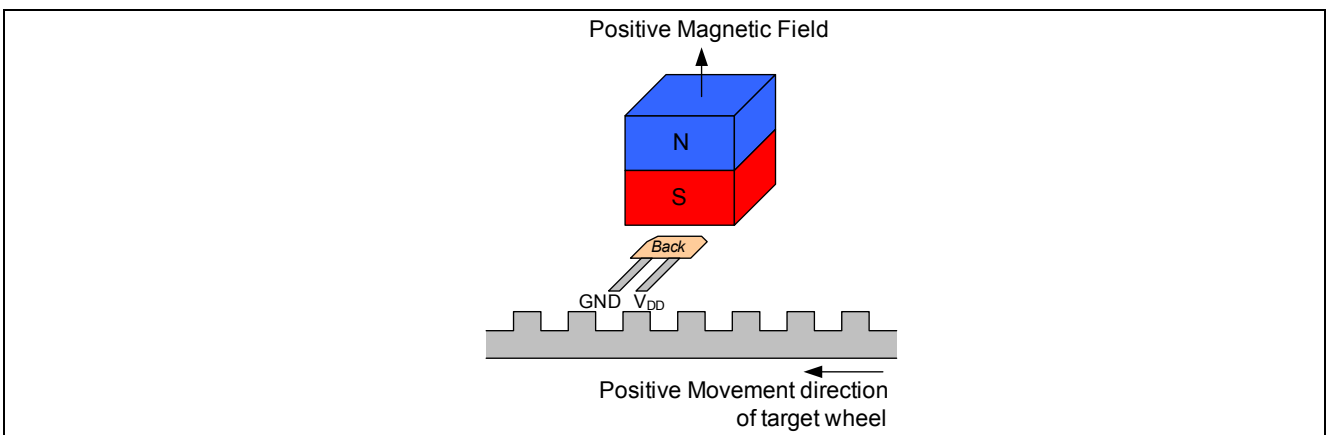


Figure 8 Definition of rotation for back bias application, Sensor Marking (=Frontside) points to encoder

For better understanding three different modes have to be considered: data protocol at normal speed, at high speed and standstill. Explanations will follow on next pages.

2.7.2 Manchester Encoding

The data protocol is Manchester-coded. This means the value of a bit is coded in a rising- or a falling of the signal between the middle-current value (I_{mid}) and low-current (I_{low}) in a certain time window. A transition from low to middle corresponds to "1", a transition from middle to low corresponds to "0". Falling and rising edge of sensor output current starts in the middle of data protocol ($=t_p/2$), see bottom of example in Figure 9.

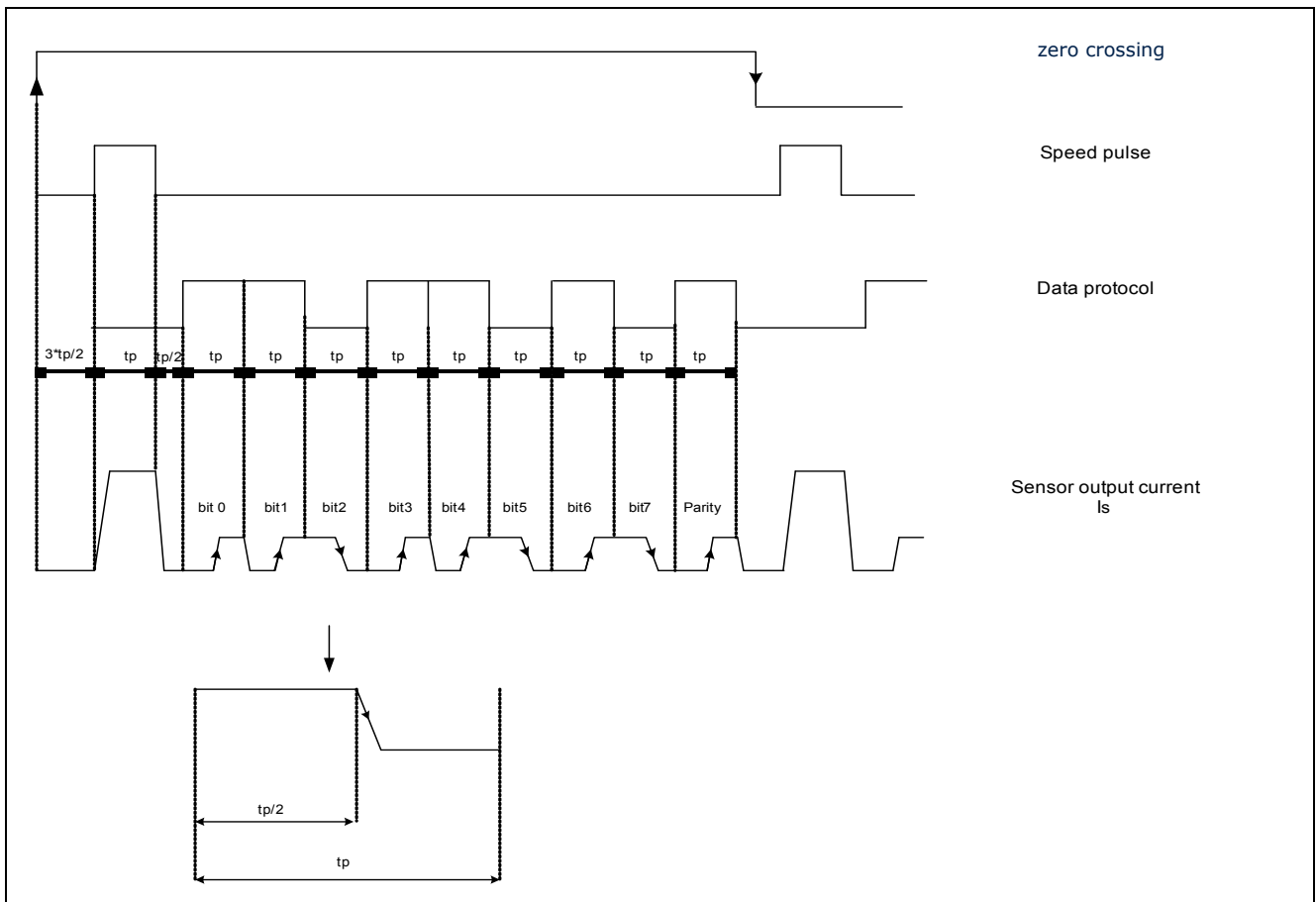


Figure 9 Manchester Encoding

2.7.3 Protocol at Normal Speed

At normal speed (signal frequencies less than 1800Hz) all data bits are transmitted. At the beginning the initial bit (I_{low}) is sent for $t_p/2$. Then the speed pulse with duration t_p is issued which is followed by a current level I_{low} for $t_p/2$. After that the data protocol is sent.

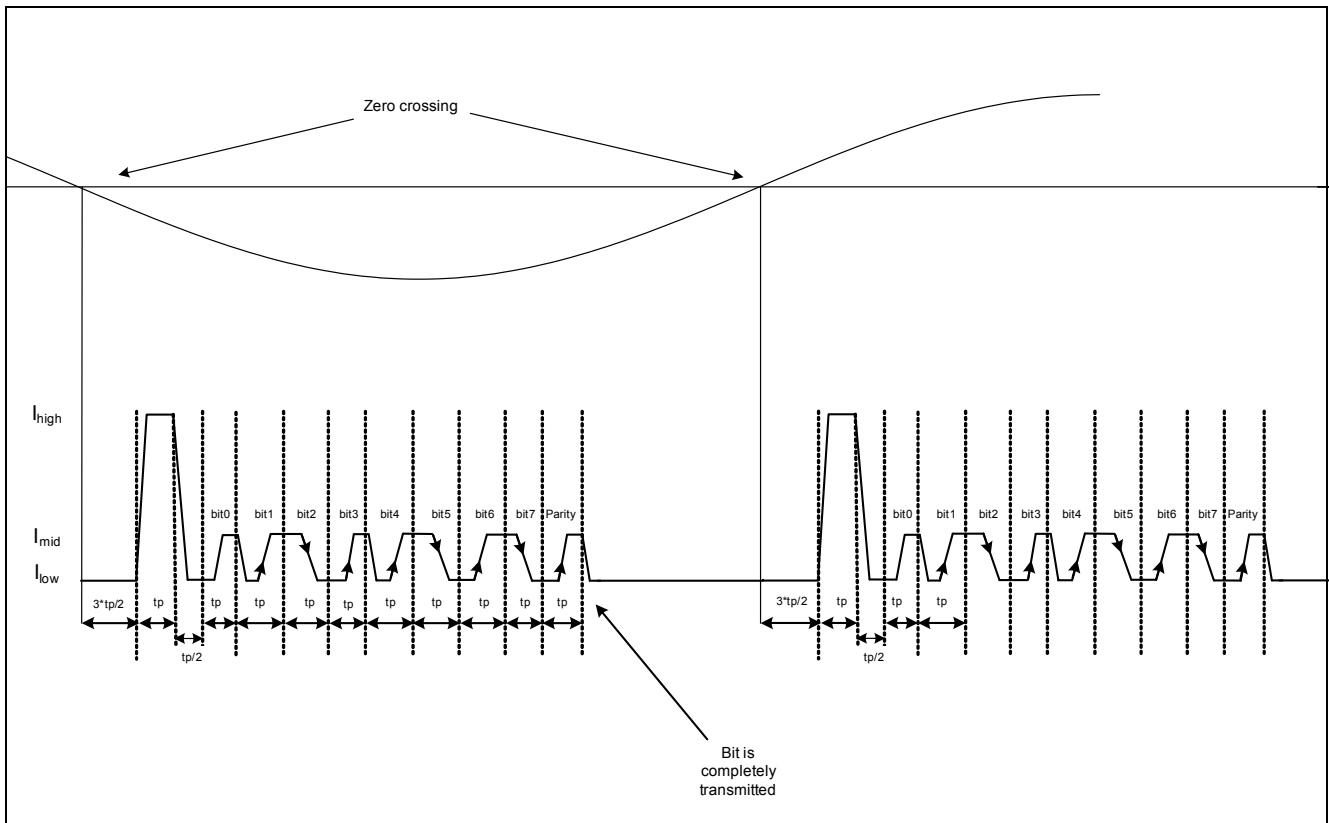


Figure 10 Protocol at normal speed

2.7.4 Protocol for High Speed

For higher speeds the data protocol is shortened (last bits are cut off). The table below shows how many bits are transmitted at different signal frequencies. The serial data protocol is shortened at high speeds, because the time to the next speed pulse is shorter than the protocol cycle. The data bits at the end are therefore "cut off". In each speed range, the maximum possible number of bits of additional information are transferred.

The output of partially transmitted bits called "bit stumps" are suppressed. See also [Chapter 2.7.6](#). The shortening of the protocol does not result in any "bit stumps" (bits which have not been completely transferred). This means that the bits affected by the shortening in any case will be transmitted completely, means, a bit which has been started must also be transferred to the end. Instead of the bits affected by the shortening, the current level I_{low} must be output. The suppression of bit stumps does function reliably in all speed ranges and in all regular operating states of the sensor, i.e. also in the standstill protocol. This ensures that no compatibility problems occur in any regular operating cases caused by e.g. EMC.

Table 2 Transmitted bits at electric signal frequency

Electric Signal frequency ¹⁾	Typical Number of data bits transmitted
< 1818Hz (1800Hz)	9 (bit0 - bit8)
< 2000 Hz (2000Hz)	8 (bit0 - bit7)
< 2222 Hz (2200Hz)	7 (bit0 - bit6)
< 2500 Hz (2400Hz)	6 (bit0 - bit5)
< 2857 Hz (2800Hz)	5 (bit0 - bit4)
< 3333 Hz (3200Hz)	4 (bit0 - bit3)
< 4000 Hz (4000Hz)	3 (bit0 - bit2)
< 5000 Hz (5000Hz)	2 (bit0 - bit1)

1) Note: electric signal frequency is equal to two times of magnetic frequency

Note: Frequencies in brackets are according AK specification

2.7.5 Data Protocol for Standstill

If for a longer time than t_{stop} no increment is recognized, the IC starts to send the standstill-protocol. This protocols is sent every 150ms +/- 20%. In this protocol the current value of the speed-pulse is set to I_{mid} and all the other bits are transmitted like described before. For very slow wheel speeds more than one standstill protocol can be issued between consecutive speed pulses.

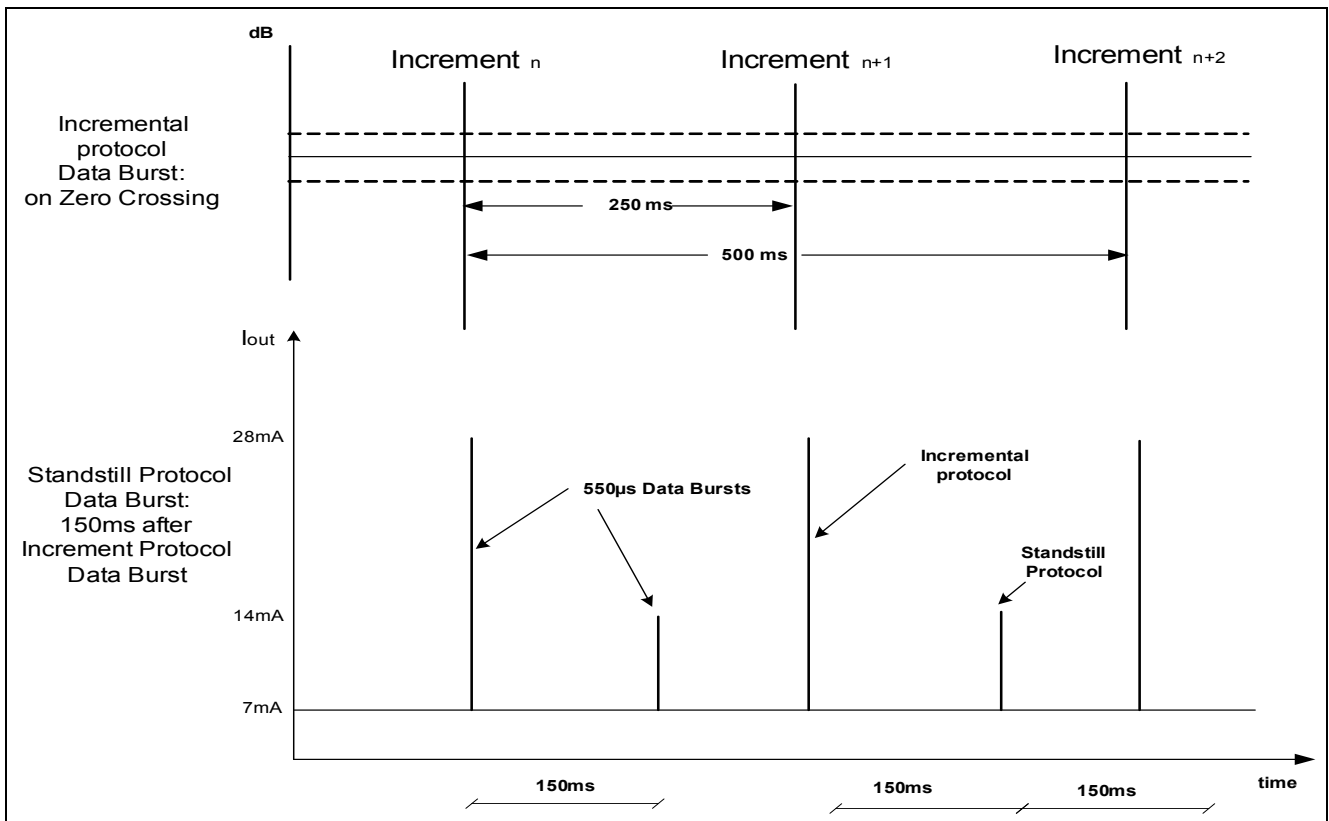


Figure 11 Standstill protocol

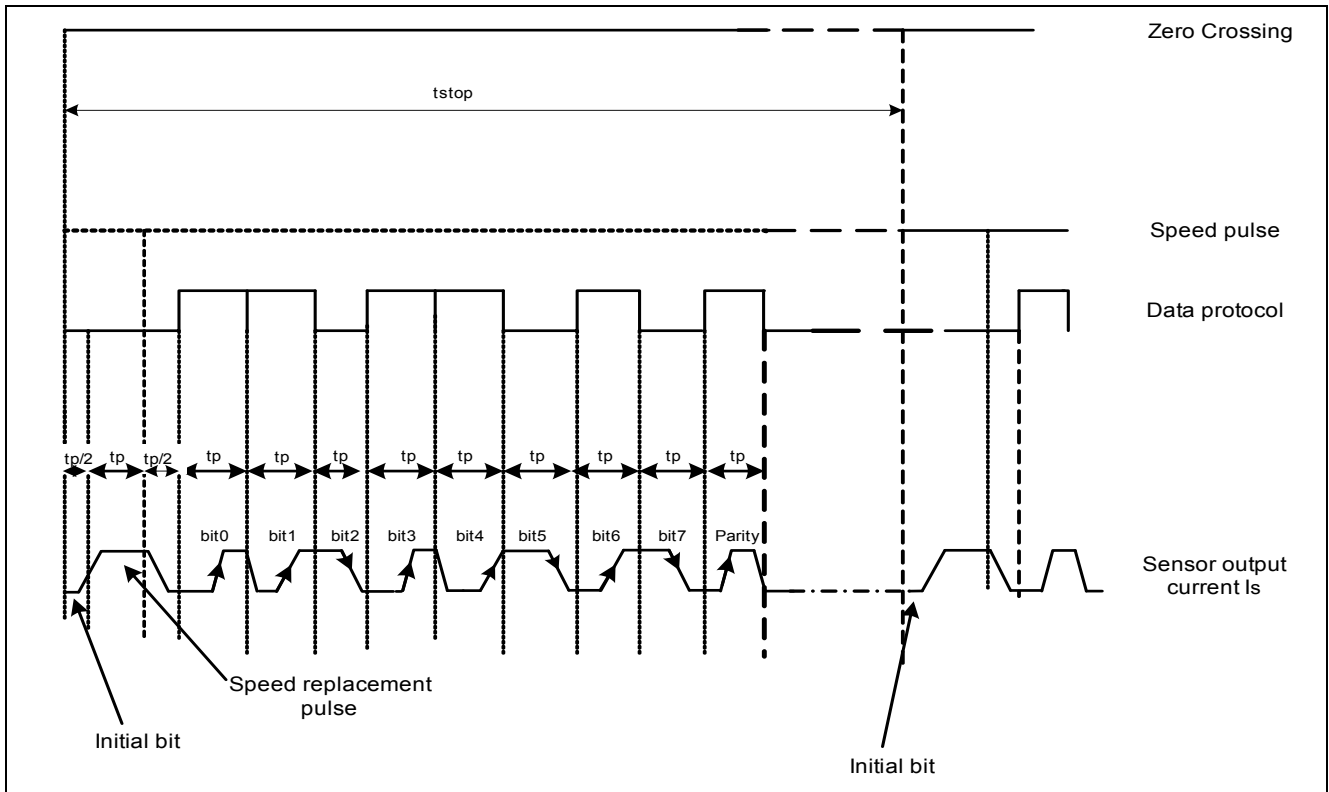


Figure 12 Protocol at standstill

Note on the standstill - travel transition:

If an increment of the magnetic encoder is detected, the standstill protocol will be aborted. The speed pulse I_{high} with the initiating initial bit (with the level I_{low}) has precedence. Due to the suppression of "bit stumps" also required in the standstill protocol, the cutting of the protocol can actually only take place between two data bits, and not during an ongoing bit transmission. The initial bit enables the speed pulse to always be preceded by a current level I_{low} for a duration of at least $t_p/2$. This is helpful for the detection of the speed pulse in the ECU (electronic control unit).

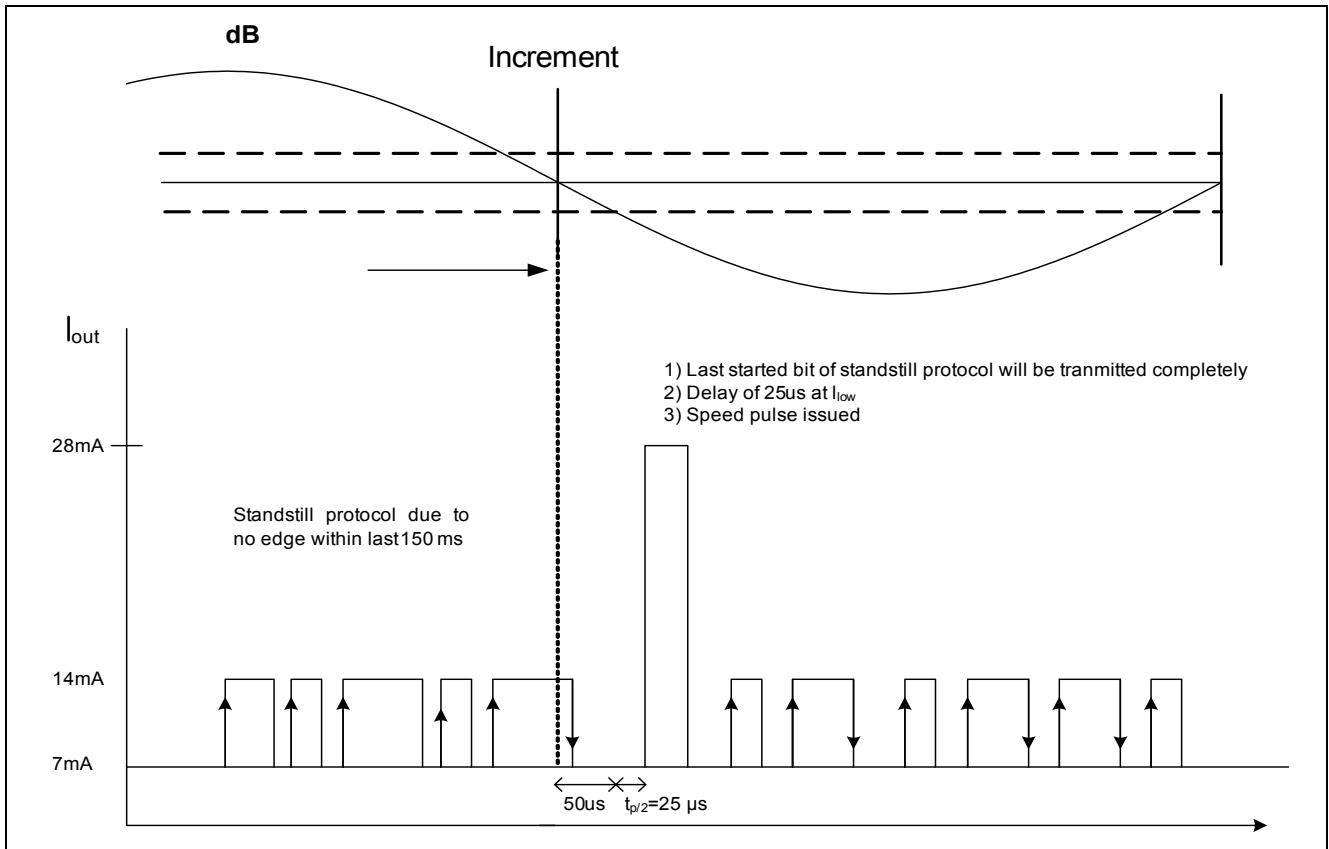


Figure 13 Starting wheel movement during standstill protocol using bit stump suppression

Handling of “Direction Validity” and “Direction” at the standstill protocol:

At any standstill DR is transmitted as zero (default value) and GDR is transmitted as invalid (=0). With the first 5 standstill protocols in a row, the direction algorithm is reset. Therefore at following next three zero crossings (speed pulses) direction detection and change of direction detection takes place (GDR=invalid, DR=default) and GDR is valid and correspondig direction is output at third speed pulse after standstill.

Handling of “Validity of signal amplitude measurement” within standstill protocol:

Validity (SLM) of signal measurement is transmitted as 1 (invalid) and signal amplitude (Level in relation to LR) is transmitted as 0 during standstill protocol. With the first 5 standstill protocols in a row, the SLM/LM is reset to invalid. SLM remains invalid until two new extrema in dB are found. Depending on the amplitude of dB and phase of the standstill protocol, SLM is valid with the second, third or fourth speed protocol after every 5th standstill protocol.

Handling of Error Bit “Air Gap Reserve” (=LR bit) within standstill protocol:

It is transmitted as "0" (no error) in the standstill protocol.

It is reset to 0 with the first 5 standstill protocols in a row. The standstill protocol LR remains “0” (no error) until two new extrema in dB are found.

The initial bit enables the speed pulse to always be preceded by a current level I_{low} for a duration of at least $t_p/2$. This is helpful for the detection of the speed pulse in the ECU.

2.7.6 Bit Stump Suppression

The suppression of bit stumps in the wheel speed sensor (WSS) is implemented and described in this paragraph. Following principle is used to realize a bit stump suppression:

Constant time shift of output of speed pulse and data protocol:

The sensor output is always completely shifted by a bit time t_p when a new protocol starts. This is equivalent to a time output offset, which has the following effect:

The initial bit is not started immediately at the moment in which a new protocol starts, what could occur during an ongoing data protocol at high speed. Instead, t_p is always initially waited for a time offset within which the last ongoing protocol output is monitored. For the case a bit output is still active, this will be completely transferred without being cut off. This will effectively prevent the occurrence of bit stumps. Within this offset time t_p , suppression of the next possible data bit of the last protocol will be introduced. In this way a current bit transfer will be completed and the transfer of any further bits (of the last protocol) will be prevented. At the end of this offset time, the transfer of the initial bit will start. Advantage of this procedure: it is also effective in the standstill protocol, i.e. if a new increment of the encoder is detected during an ongoing standstill protocol, a current ongoing bit transfer are not be ended in any "bit stump". The transmission of additional bits is suppressed. After delay phase, the new transfer begins with the initial bit $t_p/2$, followed by speed pulse and data protocol.

The following figures show the effect of the bit stump suppression according to the method described above using 3 representative cases.

1st case: No cutting off of the preceding protocol. The time between two consecutive protocols is sufficient to transfer all bits. Nevertheless, the new protocol begins at the moment of a new increment of the encoder with the constant-time output offset of the length t_p . This is followed by the initial bitwidth $t_p/2$, then the speed pulse, etc.

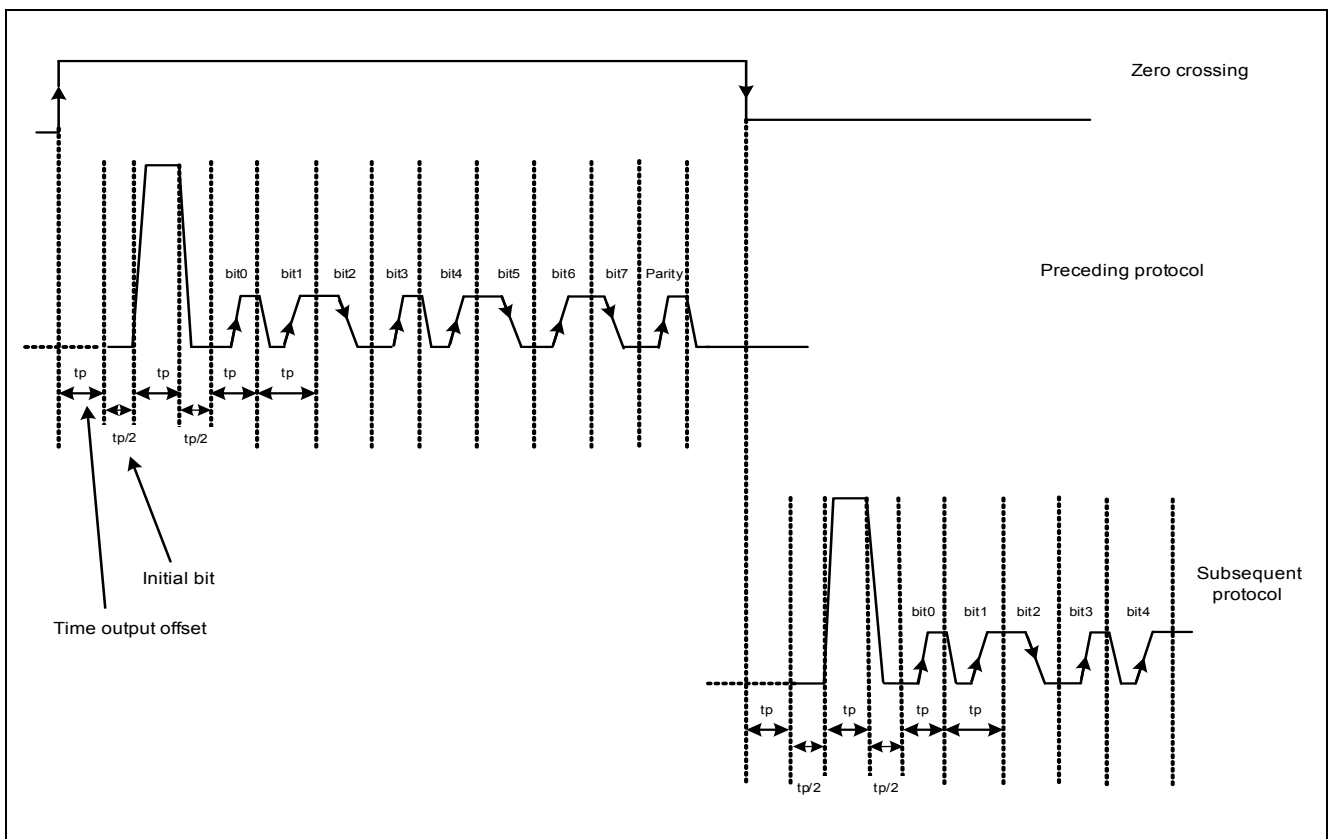


Figure 14 Case 1 - No cutting of the preceding protocol

2nd case: The last bit of the preceding protocol is cut off.

The time between 2 consecutive protocols is no longer sufficient and a new increment of the encoder occurs, while the last bit of the preceding protocol is still being transferred. At this moment the new protocol begins again with the constant-time output offset of the length t_p . However now it is realized in the sensor that a bit transfer is still running. This is completely transmitted within the currently running output offset. After the output offset ends, the initial bit follows with $t_p/2$, then the speed pulse, etc.

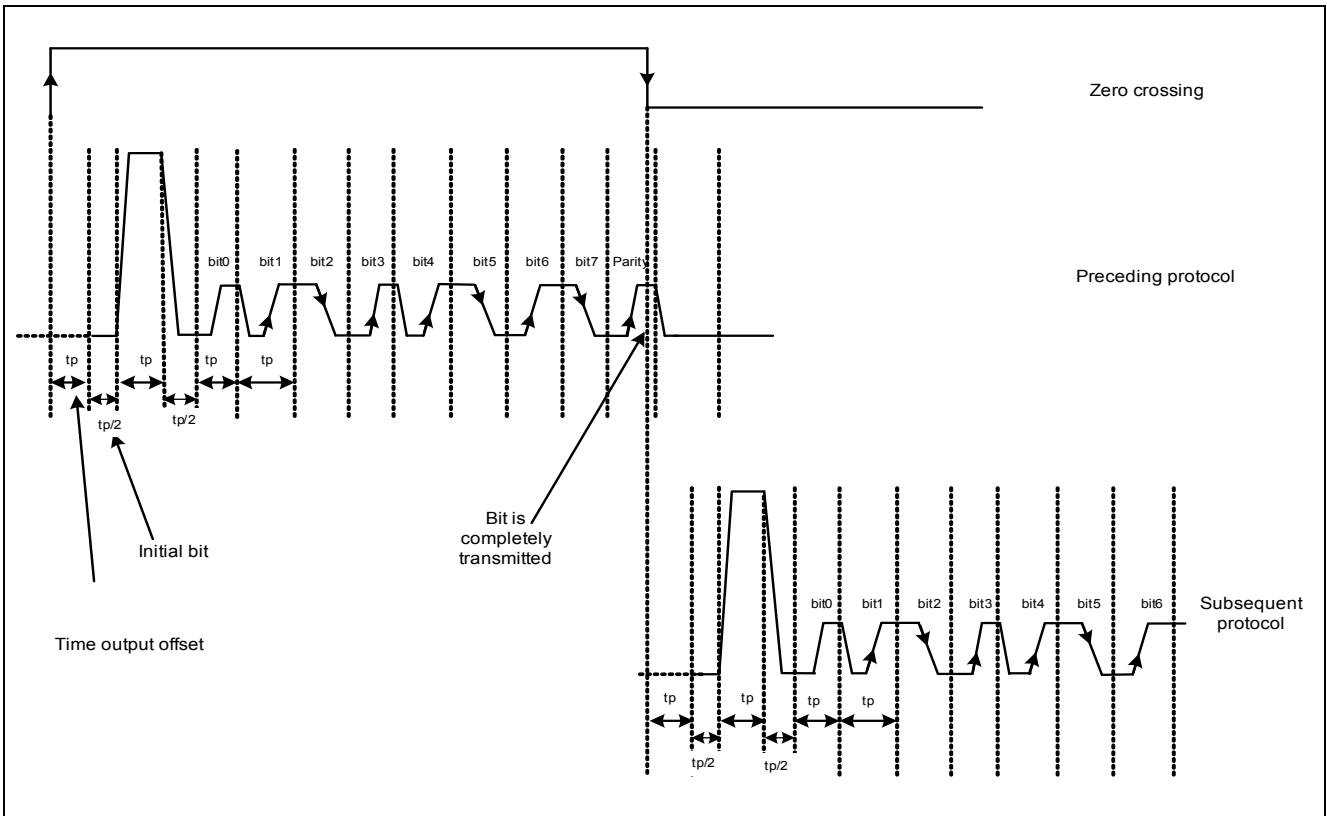


Figure 15 Case 2 - last bit of preceding protocol is cut off

3rd case: several bits of the preceding protocol are cut off

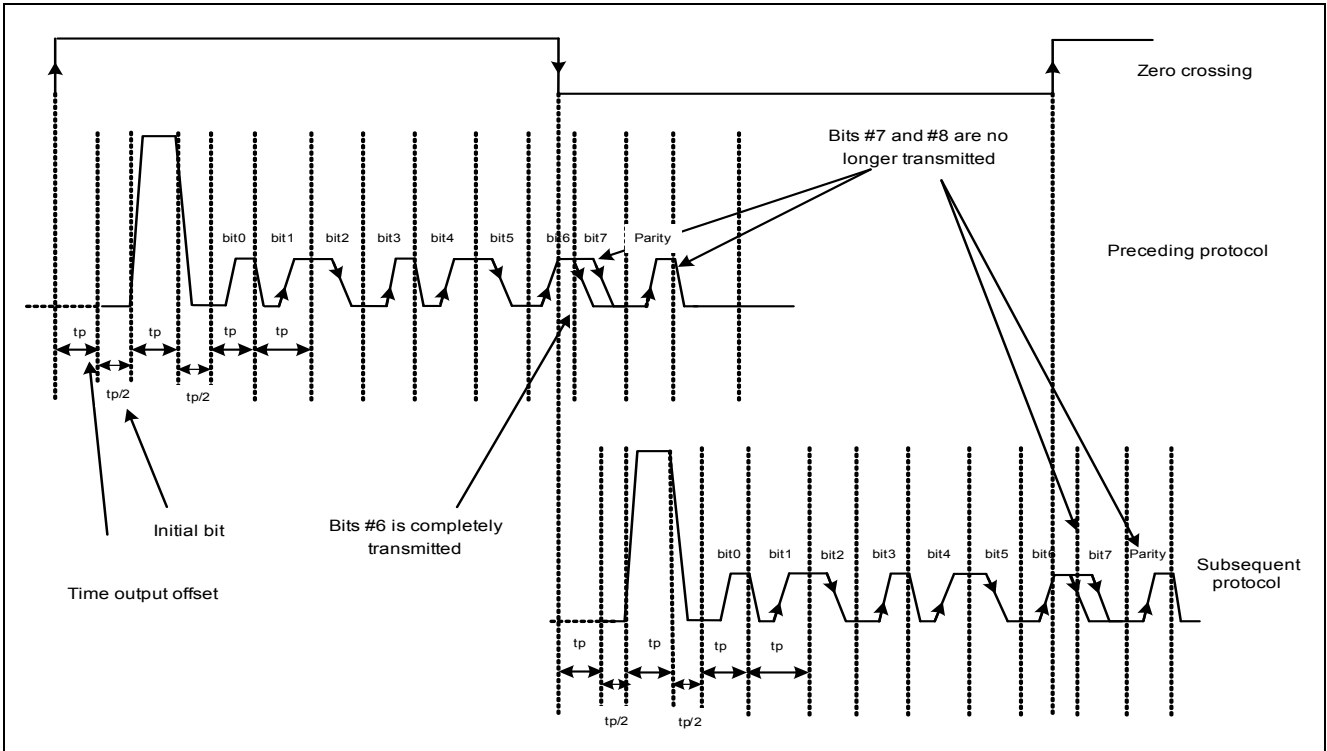


Figure 16 Case 3 - several bits of the preceding protocol are cut off

A new increment of the encoder occurs while, for example, bit #6 of the preceding protocol is still being transferred. At this moment the new protocol begins again with the constant time output offset of the length t_p . It is realized in the sensor that a bit transfer is still running. Bit #6 of the preceding protocol is completely transmitted within the current running output time-offset. In addition, the bits #7 and #8 (parity) still missing are suppressed and no longer transmitted. As a result, the line is clean again and following the end of the output offset the initial bit follows with $t_p/2$, then the speed pulse, etc.

2.8 Operating Modes and States

The basic operation of the TLE4943C is to measure the differential magnetic field of a rotating target wheel and generate an output signal which represents the wheel speed and provides information about rotation direction and signal quality. The IC has a three level current interface. The functionality of the TLE4943C can be distinguished in two different phases: uncalibrated and calibrated mode.

2.8.1 Uncalibrated and Calibrated Mode

After an initial calibration delay time t_{d_input} , the differential magnetic signal dB is tracked by an analog to digital converter (ADC) and monitored within the digital circuit. For detection the signal needs to exceed the internal threshold DNC (digital noise constant). When the signal slope is identified as a falling (or rising) edge and the signal change exceeds the DNC, the first extrema is located and first output pulse is triggered. The digital noise constant value is changed accordingly to magnetic field amplitude, leading to a change in phase shift between magnetic input signal and output signal. This value of the digital noise constant is determined by the signal amplitude. First DNC ($=2 \times dB_{limit}$), indicated as arrows in figure below. A second output is triggered when the signal change exceeds again the value of the new DNC (calculated by $(min1 + max 1)/2$) in the following rising (respectively falling) edge. When a maximum and minimum was found an offset correction will take place. This leads to a phase shift of output signal and the sensor enters the calibrated mode. In calibrated mode switching is triggered by the zero crossing of the differential magnetic signal. The min/max detection is reduced to 1/4 of peak-peak. In calibrated mode minimal DNC is $2 \times dB_{limit}$. Out of this consecutive speed pulses have a nominal delay of about 180° .

Handling of additional information bits in uncalibrated and calibrated mode:

Signal amplitude measurement: SLM is valid if two valid extrema are found (the first extrema after power on is invalid). Latest with fourth protocol SLM is valid.

Startup at high frequencies could lead to shortened protocol. The bit suppression according Chapter "Bit Stump Suppression" is executed.

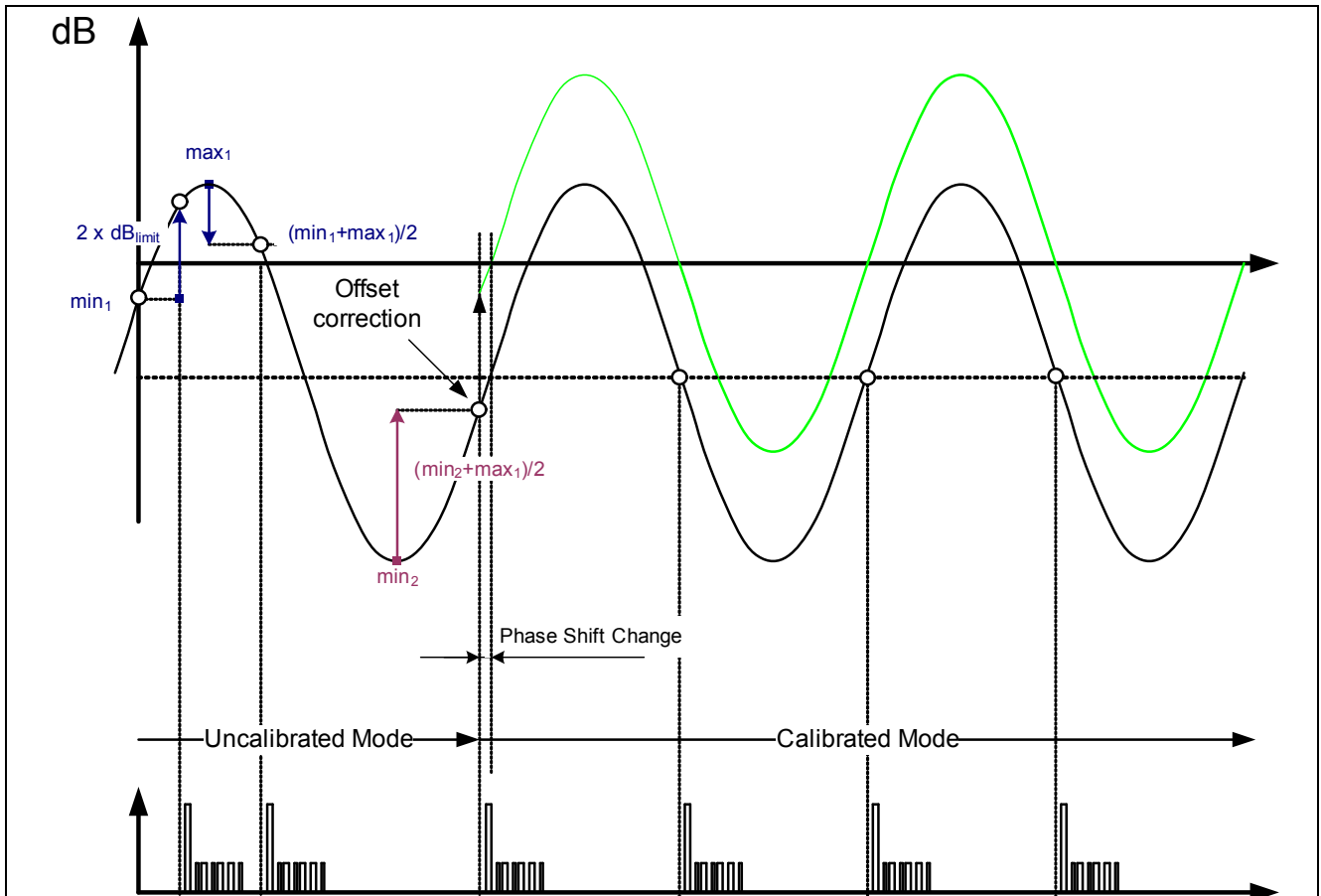


Figure 17 Example for startup behavior and change form uncalibrated into calibrated mode

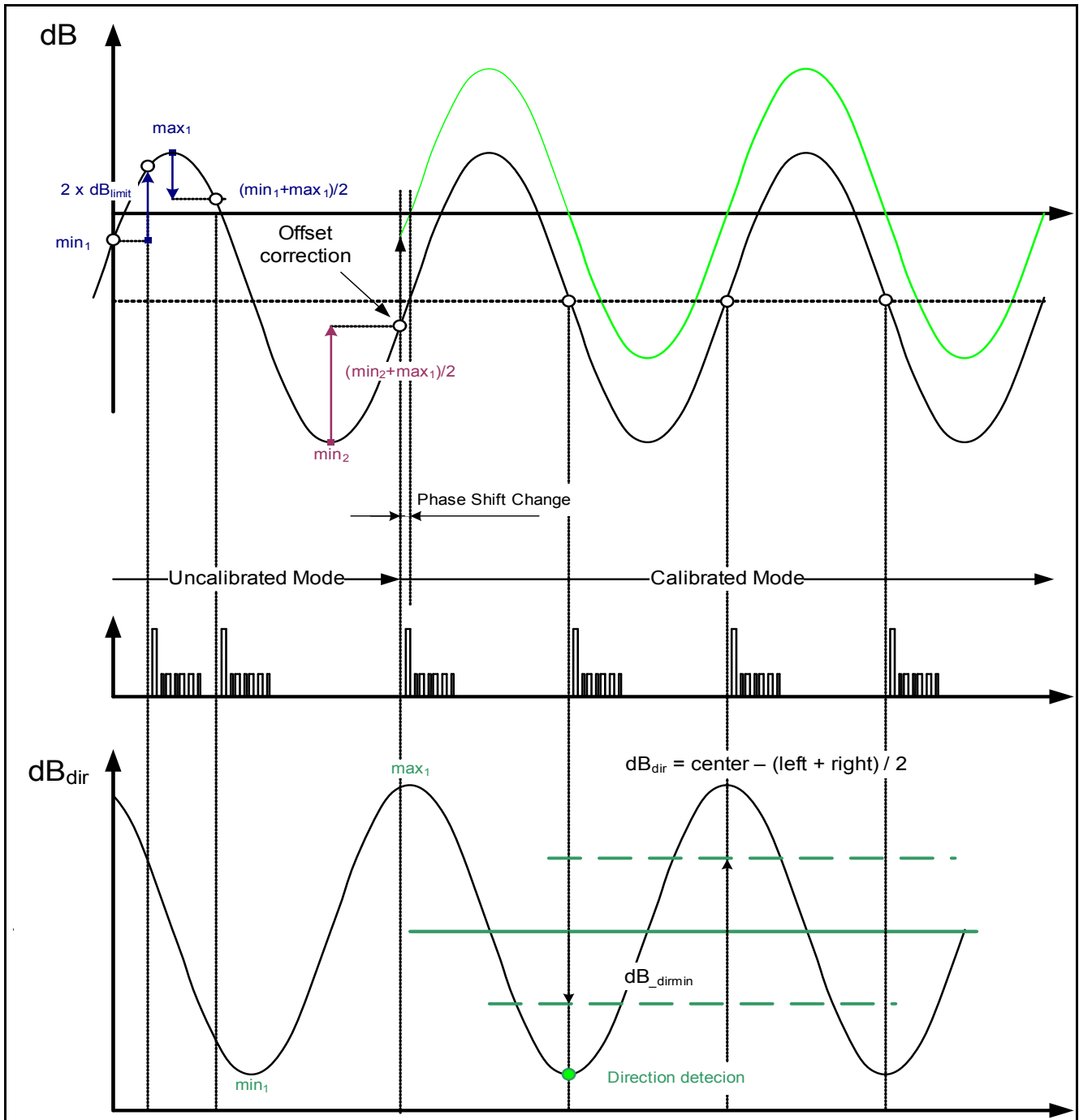


Figure 18 Output triggering in calibrated mode and direction detection

Direction detection

Direction signal is always sampled with the main comparator switching (75us +/-25%) before the sensors output switching (speed protocol). After two consecutive samples of the direction signal, offset of them is calculated and then the third sample is compared with the offset value. The direction is given by the sign of the third sample direction signal and the direction of the edge (rising or falling) of the magnetic speed signal. Using this direction detection method, detected direction is valid latest with the 4th output speed protocol. GDR bit gives the information if the detected direction is valid. On TLE4943C the direction detection is valid if the difference between the two consecutive samples of the direction signal (also used for the calculation of the direction) is greater than two times dB_{dirmin} and speed signal is four times greater than dB_{limit} .

2.9 Under Voltage and Start-up Behavior

The voltage supply comparator has an integrated hysteresis V_{hys} with the maximum value of the release level V_{rel} . This determines the minimum required supply voltage V_{DD} of the chip. A minimum hysteresis V_{hys} is implemented thus avoiding a toggling of the output when the supply voltage V_{DD} is modulated due to the additional voltage drop at R_M when switching from low to high current level at $V_{DD} = 4.5V$ (designed for use with $R_M=50\Omega$). As long as V_{DD} does not exceed V_{rel} sensor stays in low level ($V_{DD} > V_{res}$).

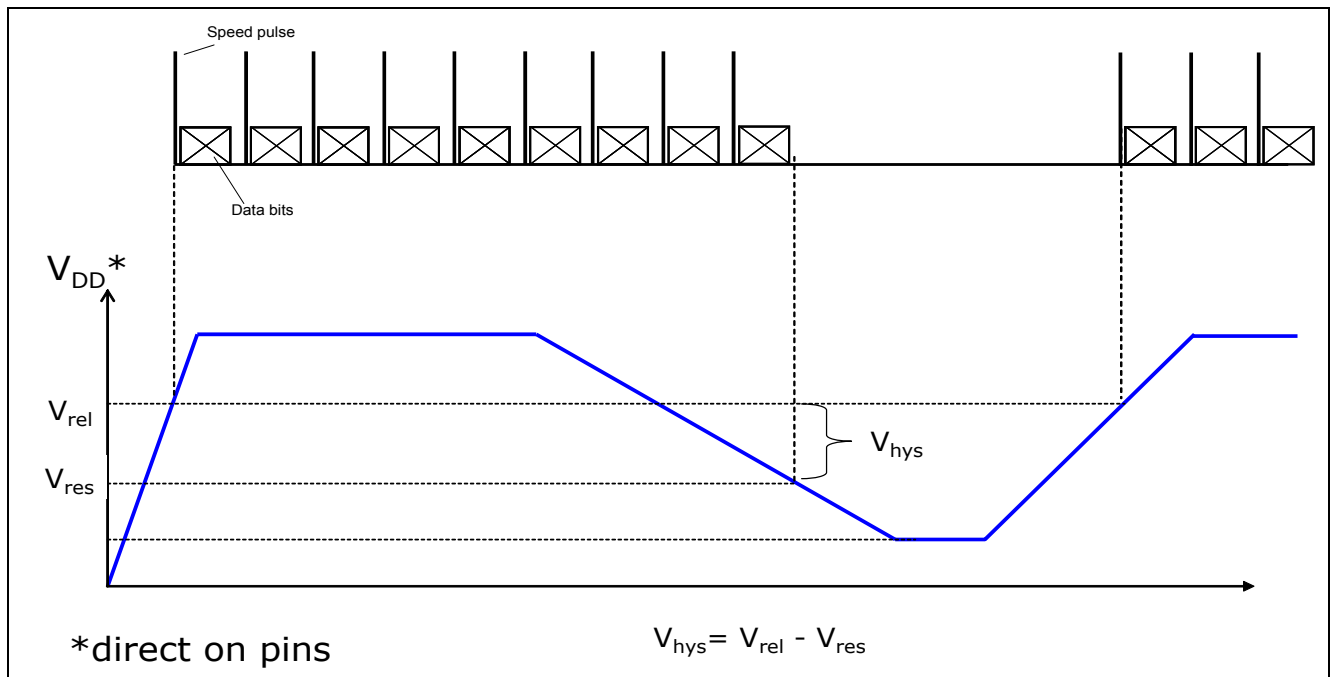


Figure 19 Start-up and under voltage behavior

3 Specification

3.1 Test Circuit

Following test circuit is used for evaluating electrical parameters:

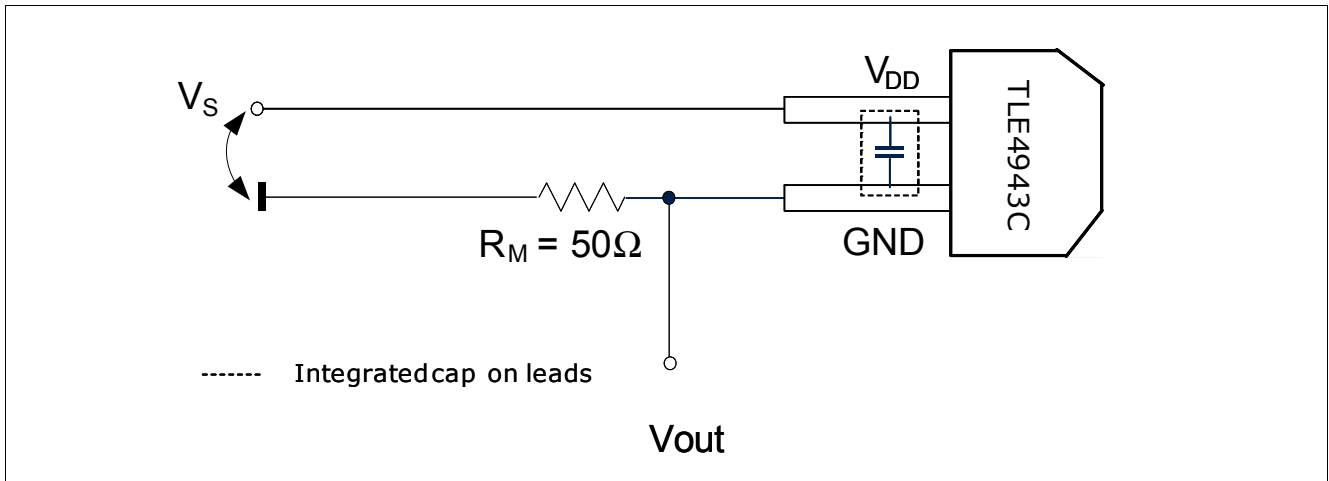


Figure 20 Test circuit

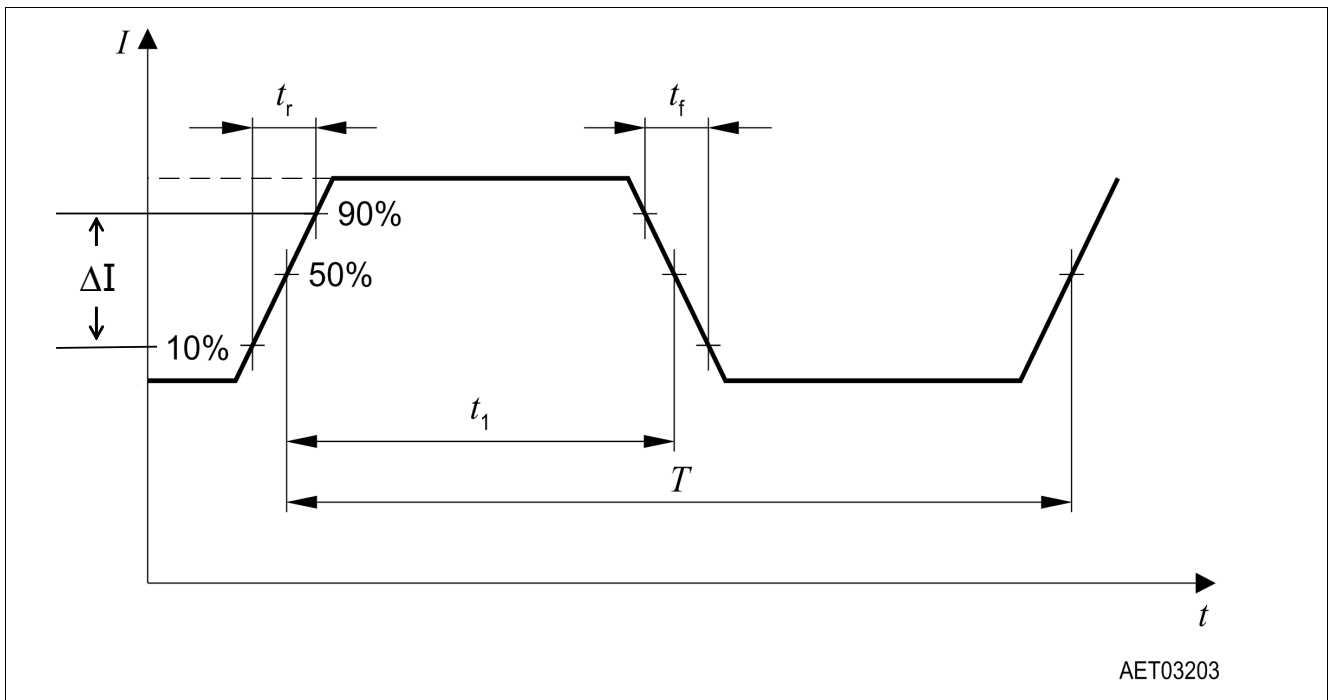


Figure 21 Definition of rise and fall time

ΔI refers to 80% positive and negative edges of I_{low} to I_{mid} and I_{low} to I_{high} and vice versa. Slew rate is calculated by division of $\Delta I/t_r$ (rise time) or $\Delta I/t_f$ (fall time).

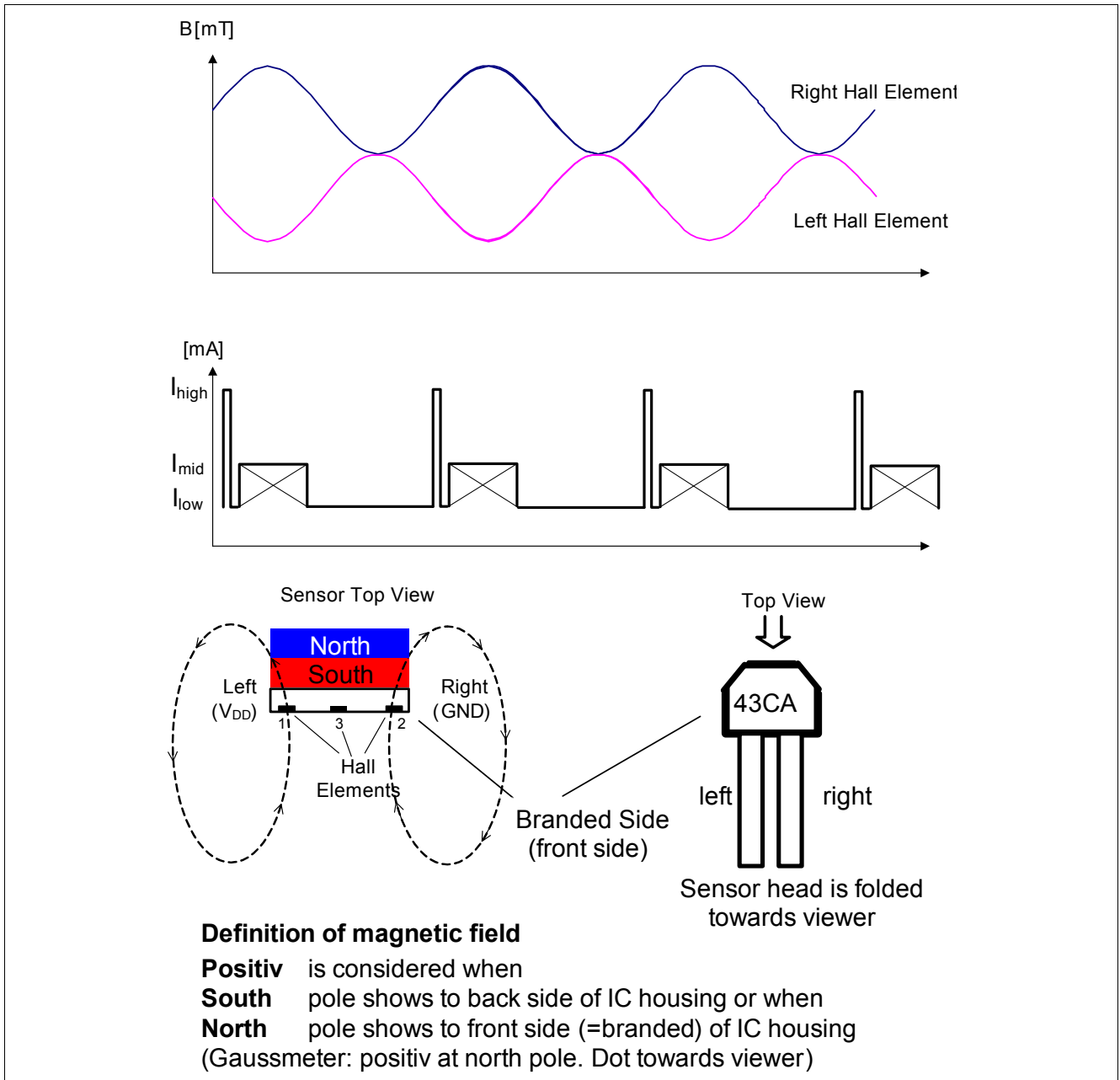


Figure 22 Definition of field direction and sensor switching

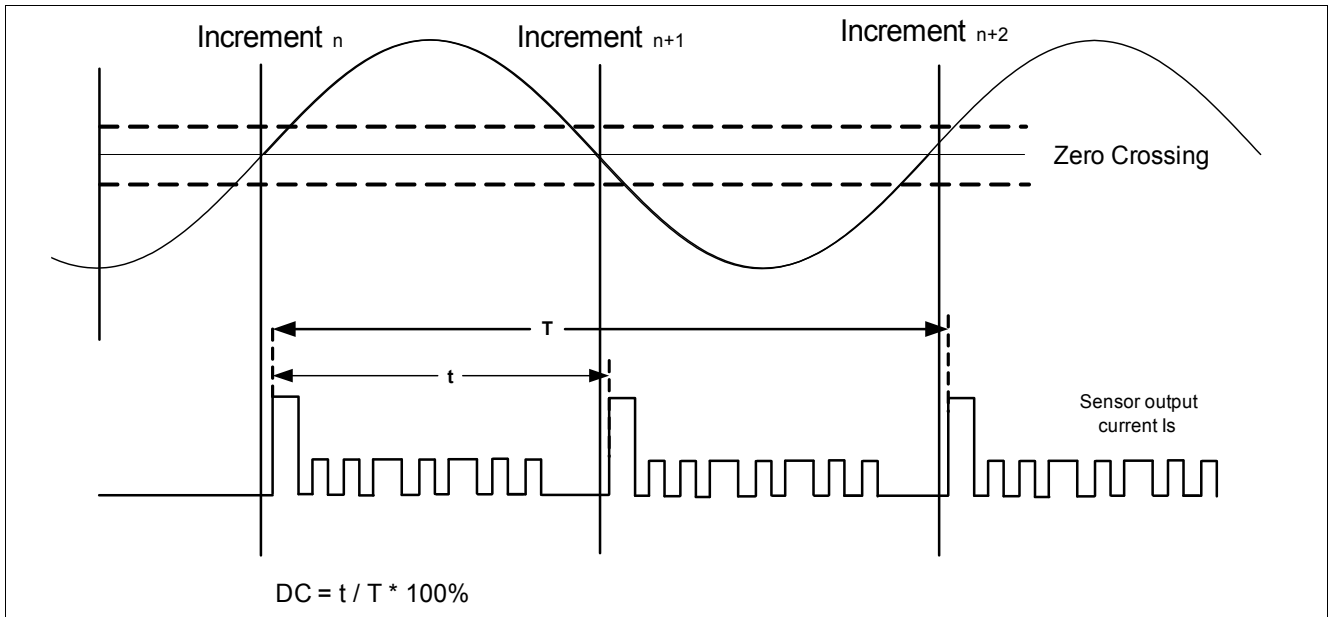


Figure 23 Definition of Duty Cycle

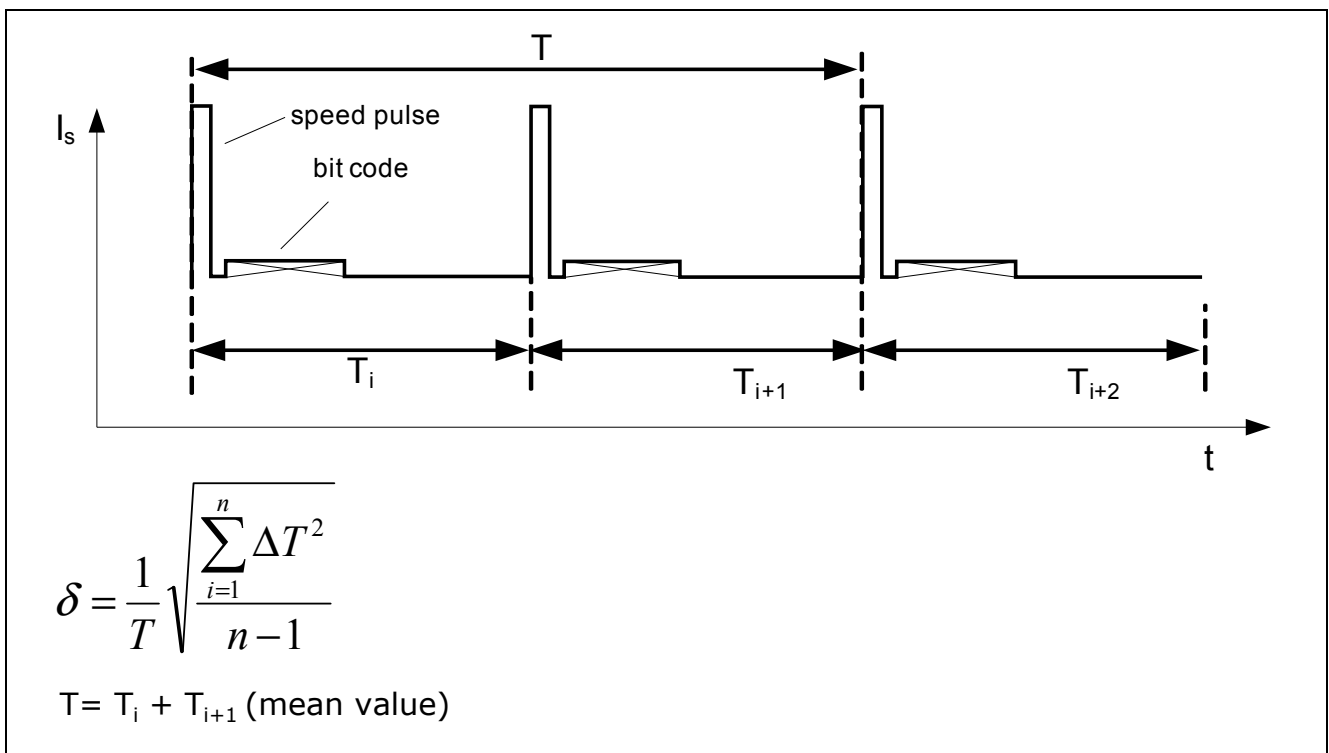


Figure 24 Definition of Jitter

3.2 Absolute Maximum Ratings

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

$T_J = -40^{\circ}\text{C}$ to 150°C , $4.5\text{V} \leq V_{DD} \leq 20\text{V}$ if not indicated otherwise

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	-0.3	-	-	V	$T_J < 80^{\circ}\text{C}$
				16.5		$T_J = 170^{\circ}\text{C}$
				20		$T_J = 150^{\circ}\text{C}$
				22		$t = 10 \times 5 \text{min}$
				24		$t = 2 \text{min}; T_J = -40^{\circ}\text{C}..60^{\circ}\text{C}$
				24		$t = 10 \times 5 \text{min}, R_M \geq 50\Omega$
				26		$t = 400 \text{ms}, R_M \geq 50\Omega$ included in V_{DD}
Junction temperature ¹⁾	T_J ; Either	-40		110	$^{\circ}\text{C}$	12500h
				125		10000h
				150		5000h
				160		2500h
				170		500h
				Additional		190
Reverse polarity voltage		-16			V	$R_M = 50\Omega$ included in V_{DD} $t < 1\text{h}$
Reverse polarity current				200	mA	external current limitation required, $t < 4\text{h}$
				300		external current limitation required, $t < 1\text{h}$
				200		external current limitation required, $t < 10\text{h}, T = 25^{\circ}\text{C}$
Thermal resistance of package	R_{thJA}			190	$\text{K/W}^{2)}$	
Number of power on cycles		500.000			cycles	
Immunity to external fields				2	T	equivalent to 1600kA/m^3 ; $T_J = -40..175^{\circ}\text{C}$
Passive lifetime ¹⁾		15			a	$T_J \leq 50^{\circ}\text{C}, U = 0\text{V}$
Processability		2			a	after Datecode

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

2) Can be significantly improved by further processing like overmolding

3) Conversion: $B = \mu * H$ ($\mu = 4 * \pi * 10^{-7}$)

3.2.1 ESD Robustness

Table 4 ESD Protection

Characterized according to Human Body Model (HBM) tests in compliance with Standard EIA/JESD22-A114-B HBM (covers MIL STD 883D)

Parameter	Symbol	Test Result	Unit	Notes
ESD-Protection	V_{ESD}	± 12	kV	$R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$

or >8000V for TLE4943C (H3B according AEC Q100)

Note: Tested at room temperature

3.3 Operating Range

All parameters specified in the following sections refer to these operating conditions unless otherwise noticed.

Table 5 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	6.5	–	20	V	Directly on IC leads; does not include voltage drop at R_M
V_{DD} Hysteresis	V_{res}	4.0V	4.2	4.5	V	AK: reset voltage
	V_{hys}	1.6	1.8	2.3		
	V_{rel}	5.8		6.5		AK: return voltage
Supply voltage modulation	V_{AC}			6	V_{pp}	$V_{DD}=13V$; $0 < f_{mod} < 150kHz^1$
Junction temperature	T_j					
	Either	-40		110	°C	12500h ²⁾
	OR			125		10000h ²⁾
	OR			150		5000h
	OR			160		2500h
	OR			170		500h
Pre induction	B_o	-500		500		mT
Temperature change per magnetic period for valid DR	dT_{j_Dir}	-7.5		7.5	K	³⁾ valid for $dB_{dir} > 1.9mT$
Temperature change at standsill	dT_{j_Speed}	-150		50	K	⁴⁾ valid for $dB > 3mT$
Pre induction offset between outer probes	$B_{stat\ l/r}$	-30		30	mT	
Differential induction	dB	-120		120	mT	
Pre-induction offset between mean of outer probes and center probe	$B_{stat\ m/o}$	-30		30	mT	
Signal frequency	f	0		5000 ⁵⁾	Hz	
Minimum magn. frequency for direction detection	f_{dir_min}	0.54	0.66	0.83	Hz	

1) sine wave

2) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

3) The permissible change of the temperature is, e.g. 7.5K per one magnetic periode. For example a magnetic signal of 10Hz ($T_{mag} = 0.1s$) results in a max change of temperature = $7.5K / 0.1s = 75K / s$. A wrong direction info may occur if dT_{j_Dir} is exceeded.

4) More than 2 speed protocols might be lost if the temperature change during standstill is exceeded at re-drive.

5) 5000Hz electric signal frequency are equal to 2500Hz magnetic signal frequency (one sin period has two increments).

3.4 Electrical Characteristics

All values specified at constant amplitude and offset of input signal, over operating range, unless otherwise specified. Typical values correspond to $V_{DD}=12V$ and $T_A=25^{\circ}C$

Table 6 Electrical Characteristics¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply current low	I_{low}	5.9	7	8.4	mA	
Supply current mid	I_{mid}	11.8	14	16.8	mA	
Supply current high	I_{high}	23.6	28	33.6	mA	
Supply current ratio middle/low	I_{mid}/I_{low}	1.8	2.0	2.6		
Supply current ratio high/low	I_{high}/I_{low}	3.6	4	5.0		
Supply current @ $V_{DD} \geq V_{res_min}$		1			mA	⁸⁾
Line regulation	dI_x/dV_{DD}			90	uA/V	⁸⁾
Number of pulses suppressed				0		⁸⁾ after power on and internal reset
Magnetic edges required for first output pulse				1	edge	⁸⁾
Number of pulses required for initial offset calibration	n_{start}			4	edges	5th "pulse" is offset corrected ²⁾⁸⁾
Number of pulses required for initial LM measurement		3		4	pulses	⁸⁾
Number of pulses required for initial valid direction detection ³⁾	$n_{DR-start}$			4	pulses	4th pulse has valid direction information, $dB_{dir} \geq 2 * dB_{dirmin}$ ⁴⁾⁸⁾
				7	pulses	7th pulse has valid direction info $2 * dB_{dirmin} > dB_{dir} \geq dB_{dirmin}$ ⁴⁾⁸⁾
Valid direction after change of direction ⁵⁾				3	pulses	3rd pulse has valid direction information, $dB_{dir} \geq 2 * dB_{dirmin}$ ⁴⁾⁸⁾
				6	pulses	6th pulse has valid direction info $2 * dB_{dirmin} > dB_{dir} > 1.8 * dB_{dirmin}$ ⁴⁾⁸⁾
				7	pulses	7th pulse has valid direction info $1.8 * dB_{dirmin} > dB_{dir} > dB_{dirmin}$ ⁴⁾⁸⁾
Frequency limit for direction information availability	$f_{dir-limit}$		2700 ⁶⁾⁸⁾		Hz	due to bit stump suppression
Power up time				1	ms	time for stable current ⁸⁾
Initial calibration delay time	$t_{d,input}$		220	300	us	additive to power up time ⁸⁾
Duty cycle in calibrated mode	DC_{cal}	40	50	60	%	$dB \geq 2mT$ sine wave

Table 6 Electrical Characteristics¹⁾ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Duty cycle in uncalibrated mode	DC _{uncal}	20		80	%	<i>dB</i> >= 2mT sine wave ⁸⁾
Jitter, 1Hz < f < 5000Hz	S _{jitter-close} , T _j ≤ 150°C			±2	%	<i>dB</i> >= 2mT; 1sigma value ⁷⁾⁸⁾
	S _{jitter-close} , T _j ≤ 170°C			±3	%	
Jitter, 1Hz < f < 5000Hz	S _{jitter-far} , T _j ≤ 150°C			±4	%	2mT > <i>dB</i> > dB _{limit} ; 1sigma value ⁸⁾
	S _{jitter-far} , T _j ≤ 170°C			±6	%	
Jitter for speed pulse		0		+0.7	us	rising edge of speed pulse relative to magnetic edge change ⁸⁾
Jitter @ board net ripple f < 5000Hz	S _{jitter-AC} ,			±0.5	%	V _{DD} = 13V ± 6V _{pp} ; 0 < f _{mod} < 150kHz; <i>dB</i> = 15mT ⁸⁾
Current ripple @ ΔV _{DD} = 0V	dI @ dV = 0V					pulse shape: triangular ⁸⁾
	pulse height			1	mA	
	pulse length			400	ns	
Pulse width for speed pulse	t _p	40	50	60	us	Triggerlevel = 10.5mA ⁸⁾
Pulse width for data bits	t _p	40	50	60	us	⁸⁾
Standstill time	t _{stop}	120	150	180	ms	⁸⁾
Pulse width t _p /2 for initial bit	t _{p/2}	20	25	30	us	⁸⁾
Pulse width t _p for time output offset due to bit stump suppression	t _{p_Bit_supp}	40	50	60	us	⁸⁾
Systematic phase error of output edges during start-up and uncalibrated mode		-90		90	°	Systematical phase error of "uncal" edge; n th vs. n + 1 th edge (does not include random phase error) ⁸⁾
Phase shift from uncalibrated to calibrated mode		-10		10	°	⁸⁾
Current slew rate	SR _r , SR _f	8		26	mA/us	10% and 90% value R _M = 50Ω, T _J < 170°C
Signal watchdog reset	n _{swd}	16		16	edges	⁹⁾⁸⁾

1) All parameters refer to described test circuit in this document. See chapter 3.1 Test circuit

2) after power on or chip reset

3) Same direction assumed

4) After power, chip reset or direction reset (after timer watchdog)

- 5) Change of direction of rotation only once assumed
- 6) Direction information is updated at every speed protocol! The direction bit corresponds in any case with the physical reality of the direction of rotation.
- 7) *due to digital quantization jitter can not be below 0.7us. Additional analog jitter*
- 8) *Not subject to production test, verified by design/characterization*
- 9) *If no switching of sensor is detected during 750ms (+/-20%) signal watchdog is activated and direction detection is resetted (GDR=0). After 16 edges (detected with $dB_2 \times dB_{limit}$) sensor resets itself and goes into uncalibrated mode*

3.5 Magnetic Characteristics

Table 7 Magnetic characteristic (amplitude values)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Limit threshold ^{1) 2)}	dB_{limit}	0.3	0.8	1.34	mT	99% criteria (1 of 96) ³⁾
Limit threshold drift	$dB_{limit:Drift}$	-5		+3	%	additional drift over lifetime at 25°C for one and the same sensor
Limit range Bit ¹⁾	dB_{LR}	1.02	1.6	2.18	mT	+/-36%, 99% criteria
		1.28	1.6	1.92	mT	$T_J=10..40^{\circ}C$, 99% criteria
Limit range bit drift	dB_{LR_Drift}	-5		+3	%	additional drift over lifetime at 25°C for one and the same sensor
Ratio dB_{LR} / dB_{limit}		1.7	2.0	2.5		
Minimum signal for direction detection	dB_{dirmin}	0.4	0.8	1.44 ¹⁾	mT	valid for GDR=0; $dB_{dir}=\text{center}-(\text{left}+\text{right})/2$; cal mode, 99% criteria
Validity of signal amplitude measurement	SLM					"0" = valid, invalid after under-voltage and initial value after power up
Signal amplitude (Level in relation to LR)	LM=0	<0.8	<=1	<=1.2		99% criteria, according to AK
	LM=1	>0.8	>1	>1.2		
	LM=2	>1.48	>1.75	>2.1		
	LM=3	>2.5	>2.95	>3.6		
	LM=4	>4.2	>4.95	>6.0		
	LM=5	>7.0	>8.25	>9.9		
	LM=6	>12.0	>14.2	>17.1		
	LM=7	>21.0	>24.7	>29.7		

1) value tested at 0h

2) valid and characterized for $f > 1\text{Hz}$

3) 50% criterion has typ. value of 0.7mT .

Note: All magnetic values are calculated out of measured sensitivity of each single Hall element.

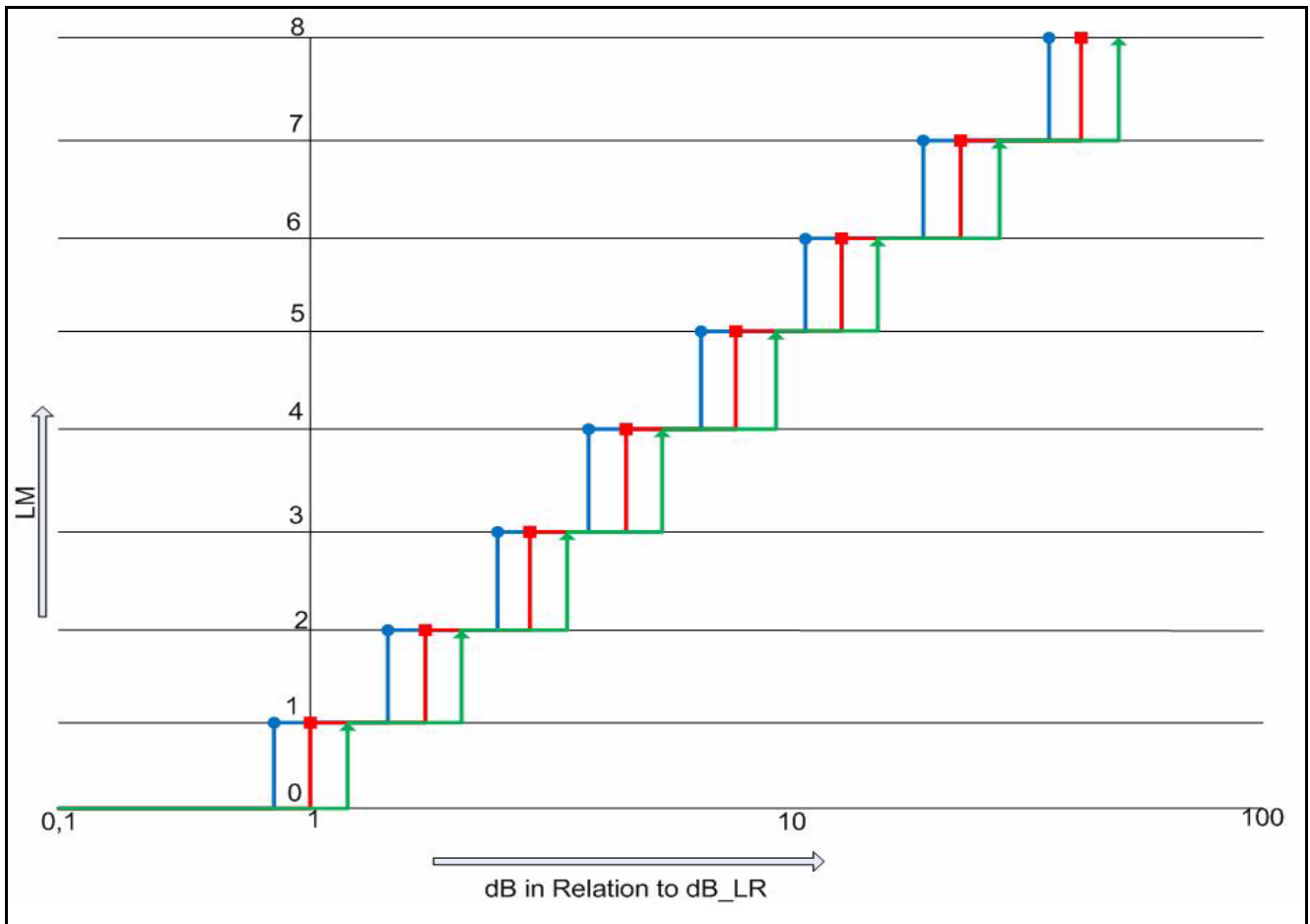


Figure 25 LM bits which are transferred at protocol with increasing magnetic field dB

3.6 Degradation of Direction Signal

Direction signal is calculated as following “dB_direction = center - (left + right) / 2”. The direction detection is optimized for a target wheel pitch of 5 mm. For pitches other than 5 mm the magnetic input signal has to be increased to compensate signal loss accordingly. For an ideal pitch of 5mm the absolute speed signal in mT is two times higher than direction signal due to differential principle. Speed signal in figure below is normalized to magnetic speed signal for a pitch of 5mm. Also direction signal is normalized to speed signal (means degradation factor=0.5) and to an ideal pitch of 5mm. Absolute values in mT are half of speed signal.

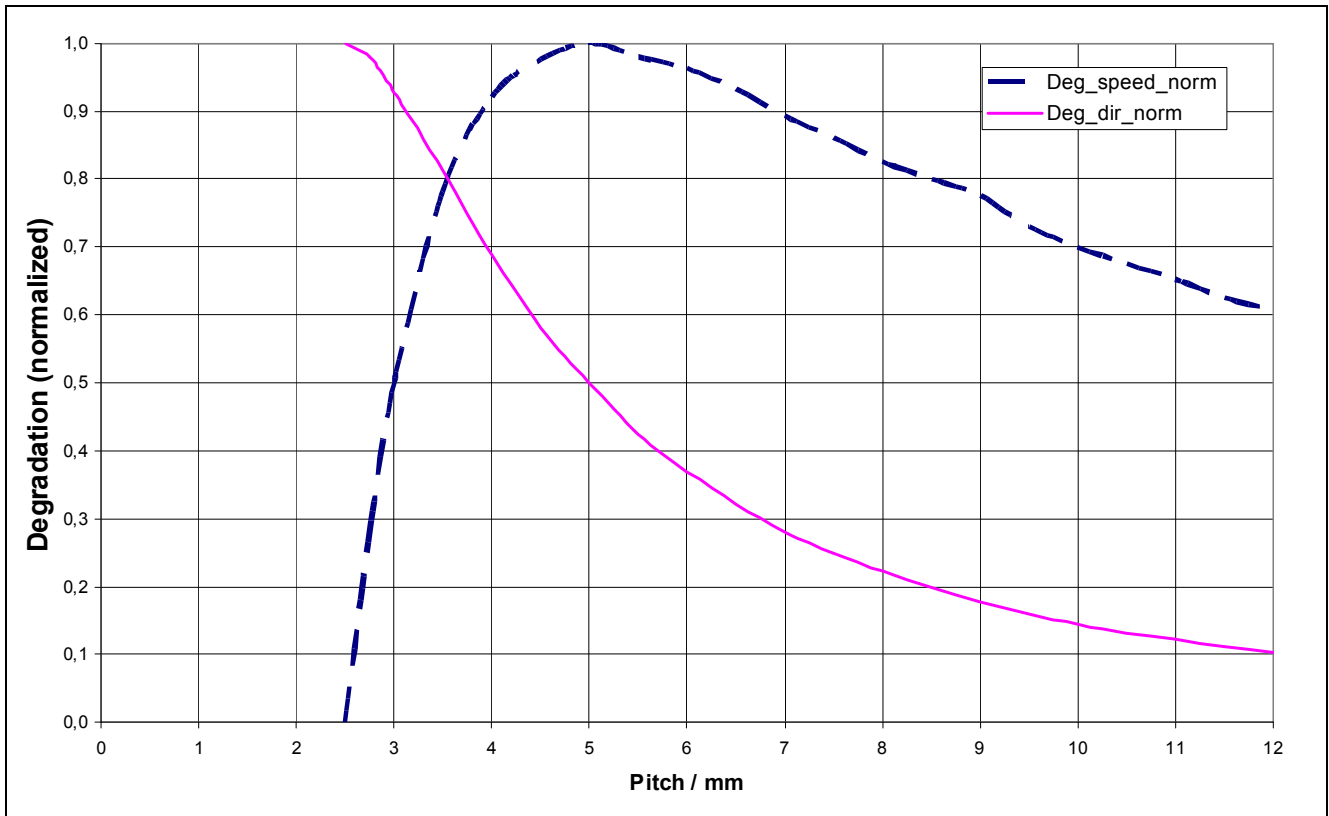


Figure 26 Degradation of speed and direction signal dependent on used target wheel pitch

3.7 Change of Direction of Encoder

A local extremum (maximum or minimum) of the magnetic input signal can be caused during a reversal of rotation direction. In this case the local extremum can be detected by the IC and used for offset calibration. (E.g. the local maximum marked by an arrow in the diagram below.) Obviously the calculated offset value will be incorrect with respect to the following signal. As worst case a duty cycle up to max. 15% to 85% could occur for a few pulses. After a re-calibration, which typically takes place after 2...3 zero-crossings the offset will be correct again and hence the duty cycle. A local extremum is detected when the extremum exceeds the value of half of the difference between the two previous extreme ($\text{dB} > 0.25 \cdot \text{dBpp}$). Smaller extrema are not detected. As a result of "bad" duty cycle after fast direction reversal the sampling points for direction detection are at unusual signal phase angles also.

At a change of rotation direction in calibrated mode two consecutive samples of dB_{dir} have the same sign therefore direction detection is set to invalid. To guarantee a valid direction the next zero crossings after change of direction are used to detect direction. The direction information validity at those two speed pulses is set to invalid and direction of rotation is set to default. Also, the validity of signal amplitude measurement is set to invalid, signal amplitude contains default values and LR is set to 0 (no error). At the latest with the third pulse after direction reversal, direction information is valid and direction is issued again. Signal amplitude validity is set to valid and its according signal amplitude measurement and LR is issued after two new valid extrema are found.

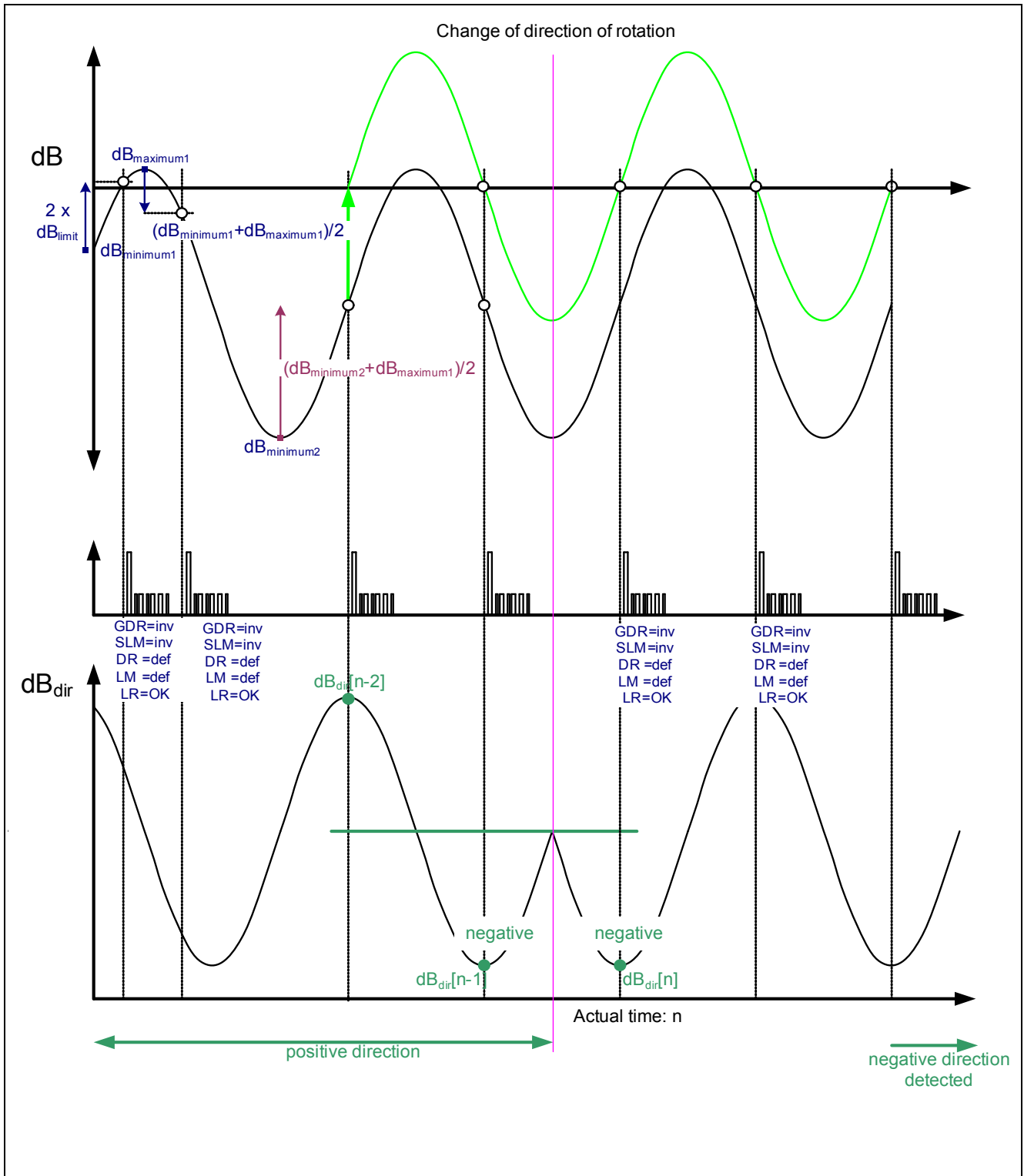


Figure 27 Signal behavior when direction of rotation changes

3.8 Watchdog Reset after Offset Jump

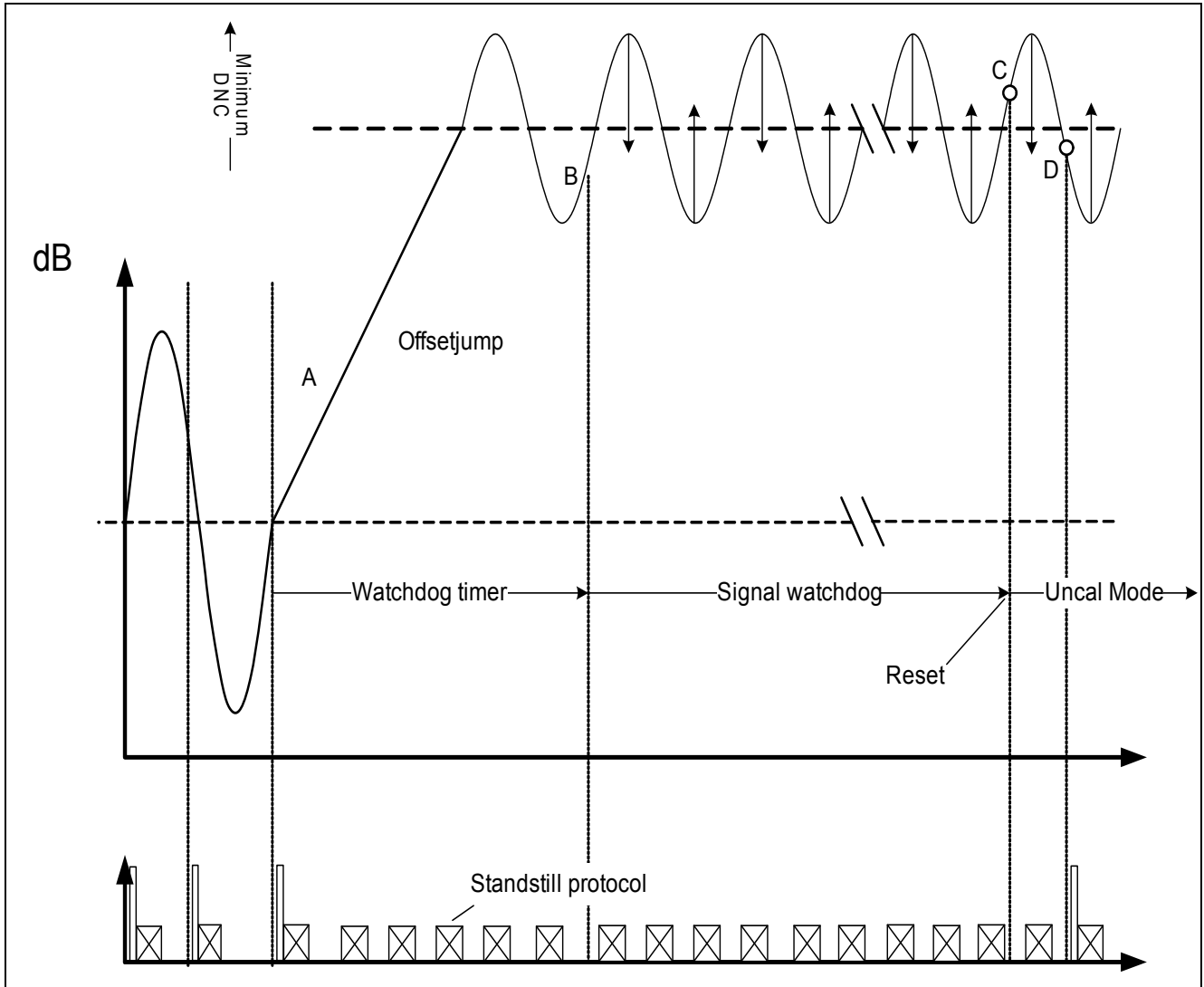


Figure 28 Reset is triggered after watchdog delay time and signal watchdog

When an offset jump, greater than the amplitude of the magnetic speed signal occurs, no zero crossing is passed anymore and therefore sensor outputs no speed pulse. Instead, standstill protocol is issued. After transmitting five standstill protocols (typ. 750ms) the signal watchdog starts. If still no speed pulse is output sensor starts to detect extreme with minimum DNC (digital noise constant). After detecting n_{swd} extreme and still no speed pulse issued, sensor triggers internal reset and enters uncalibrated mode. Therefore validity of direction, direction information, validity of airgap and airgap measurement are set to default values. This represents the same status as after power on. Therefore offset calibration starts again.

4 Electro Magnetic Compatibility

EMC Test Circuit Figure 28 is used.

Additional Information:

Characterization of Electro Magnetic Compatibility are carried out on sample base of one qualification lot. Not all specification parameters have been monitored during EMC exposure. Only key parameters e.g. switching current and duty cycle have been monitored.

Table 8 Ref. ISO 7637-2; 2004; (values depend on R_M); dB=2mT (amplitude of sinus signal); $V_{DD}=13.5V$; $f_B=100Hz$, $T=25^\circ C$, $R_M=30\Omega$

Parameter	Symbol	Level/Typ	Status
Testpulse 1	V_{EMC}	IV / -100V	C/ A (after stress)
Testpulse 2a ¹⁾		IV / 75	A ²⁾
Testpulse 2b		- / 10V	C ³⁾
Testpulse 3a		IV / -150V	A
Testpulse 3b		IV / 100V	A
Testpulse 4		IV / -7V	B
Testpulse 5a		IV / 86.5V	C
Testpulse 5b		$Us^* = 28.5V^{4)}$	C

1) ISO 7637-2 describes internal resistance = 2 Ω (former 10 Ω)

2) Node A (see figure 1) does not exceed 22V clamping voltage of D2 in any case.

3) $R_i = 0.01 \Omega$

4) A central load dump protection of 42V is used. $Us^* = 42V - 13.5V$

Table 9 Ref. ISO 7637-3 Release 1995¹⁾; dB=2mT (amplitude of sinus signal); $V_{DD}=13.5V$; $f_B=100Hz$, $T=25^\circ C$, $R_M=30\Omega$

Parameter	Symbol	Level/Typ	Status
Testpulse 1	V_{EMC}	IV / -30V	A
Testpulse 2		IV / 30V	A
Testpulse 3a		IV / -60V	A
Testpulse 3b		IV / 40V	A

1) Testpulse 1 and 2 are carried out with capacitive coupling clamp even if ISO7637-3 test pulse 1 and 2 is not requesting for capacitive coupling clamp

Table 10 Ref. ISO 11452-3, 2nd edition 2001-03-01 measured in TEM-cell

Parameter	Symbol	Level/Typ	Status
	$E_{TemCell}$	IV / 250V/m	CW; AM=80%, f=1kHz

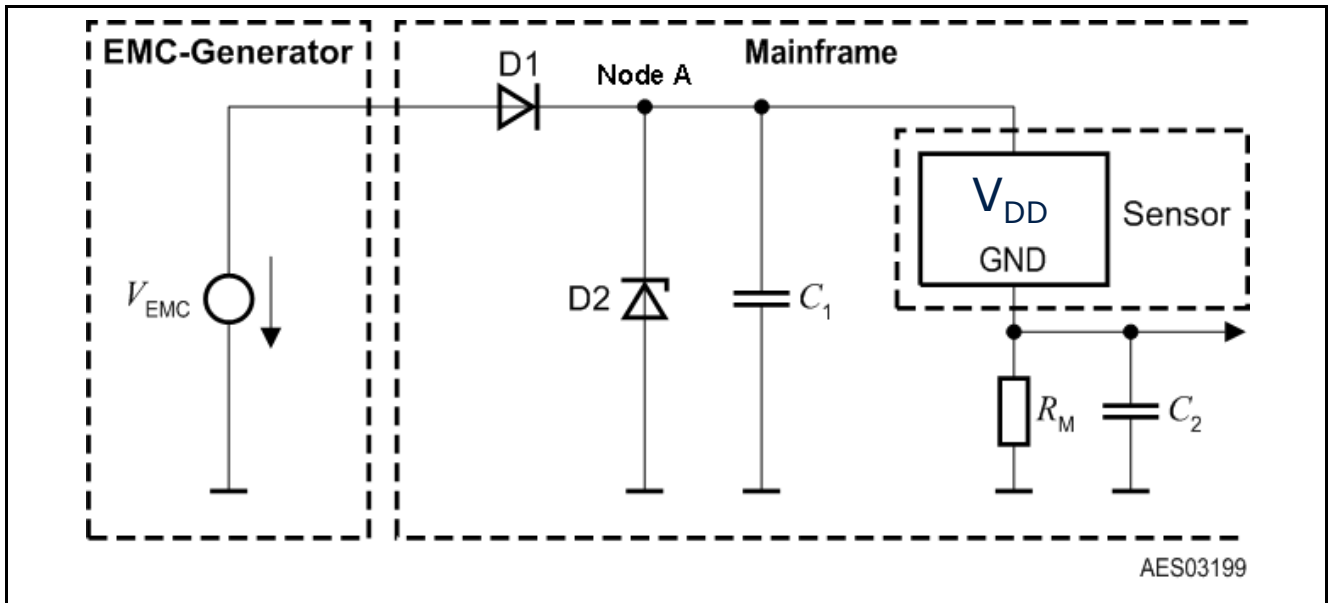


Figure 29 EMC Test Circuit

Components:

D1 = Reverse polarity protection diode, e.g. 1N4007

D2 = 22V

C1 = 10uF

C2 = 1nF

$R_M = 30 \Omega$

5 Package Information

Pure tin covering (green lead plating) is used. Lead frame material is copper based, e.g. K62. Product is RoHS (Restriction of Hazardous Substances) compliant and marked with the letter G in front of the data code marking and contains a data matrix code on the rear side of the package. Please refer to your key account team or regional sales if you need further information.

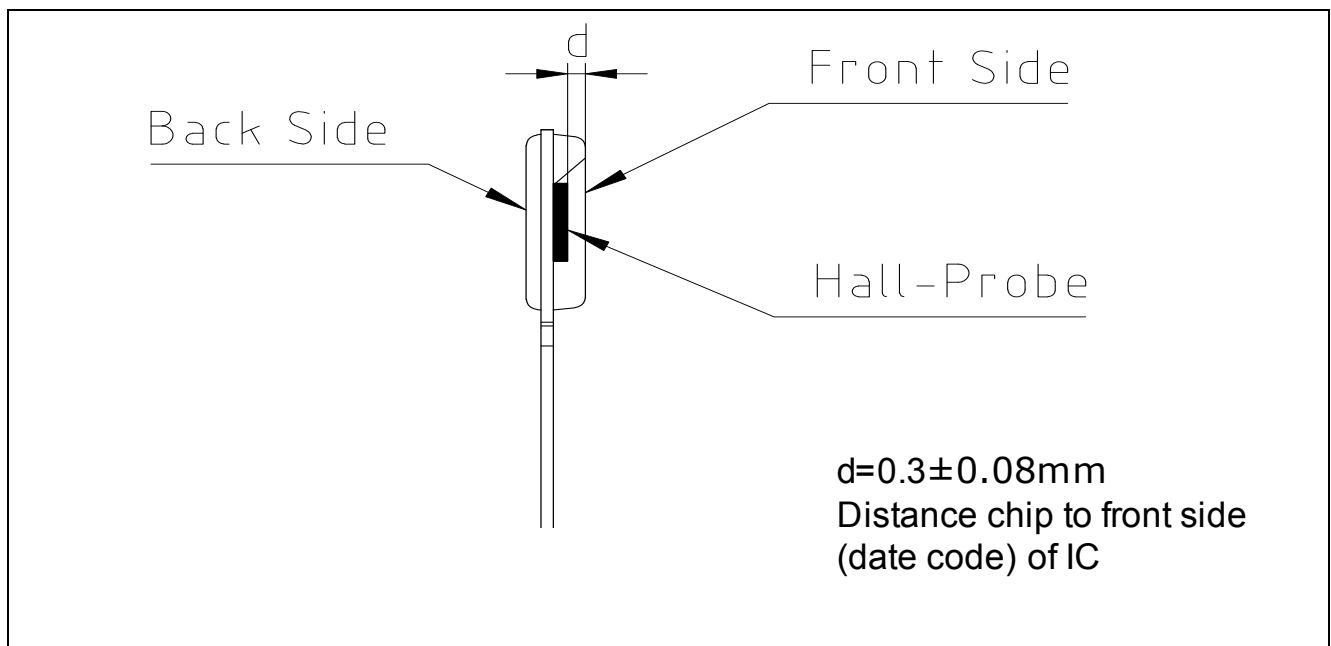


Figure 30 Distance chip to upper side of IC

5.1 Lead Pull Out Force

The lead pull out force according IEC 60068-2-21 (fifth edition 1999-1) is 10N for each lead.

5.2 Glass Transition Temperature (TG)

Typical glass transition temperature is 165°C (minimum 160°C) measured according dynamic-mechanical-analysis (DMA). The glass transition temperature can not be measured in production as separate test vehicle is needed for DMA. Material properties are covered by process parameters and handling instruction for post mold curing.

The typical glass transition temperature is 165°C according DSC method. A TG measurement according DMA on test vehicle for every incoming material batch is carried out.

5.3 Packing and Package Dimensions of PG-SSO2-53

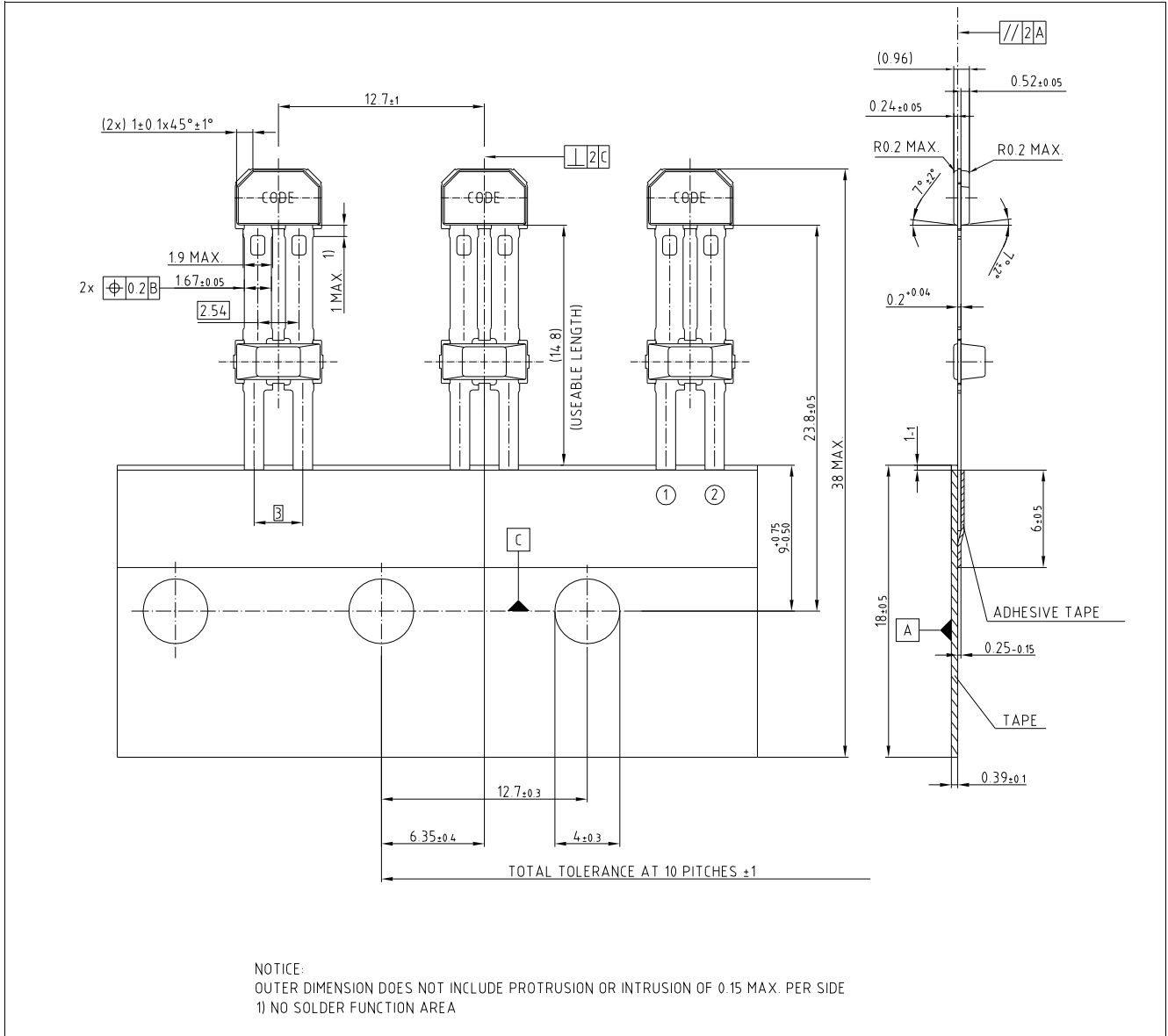


Figure 31 Packing Dimensions in mm of PG-SSO2-53 (Plastik Single Small Outline Package)

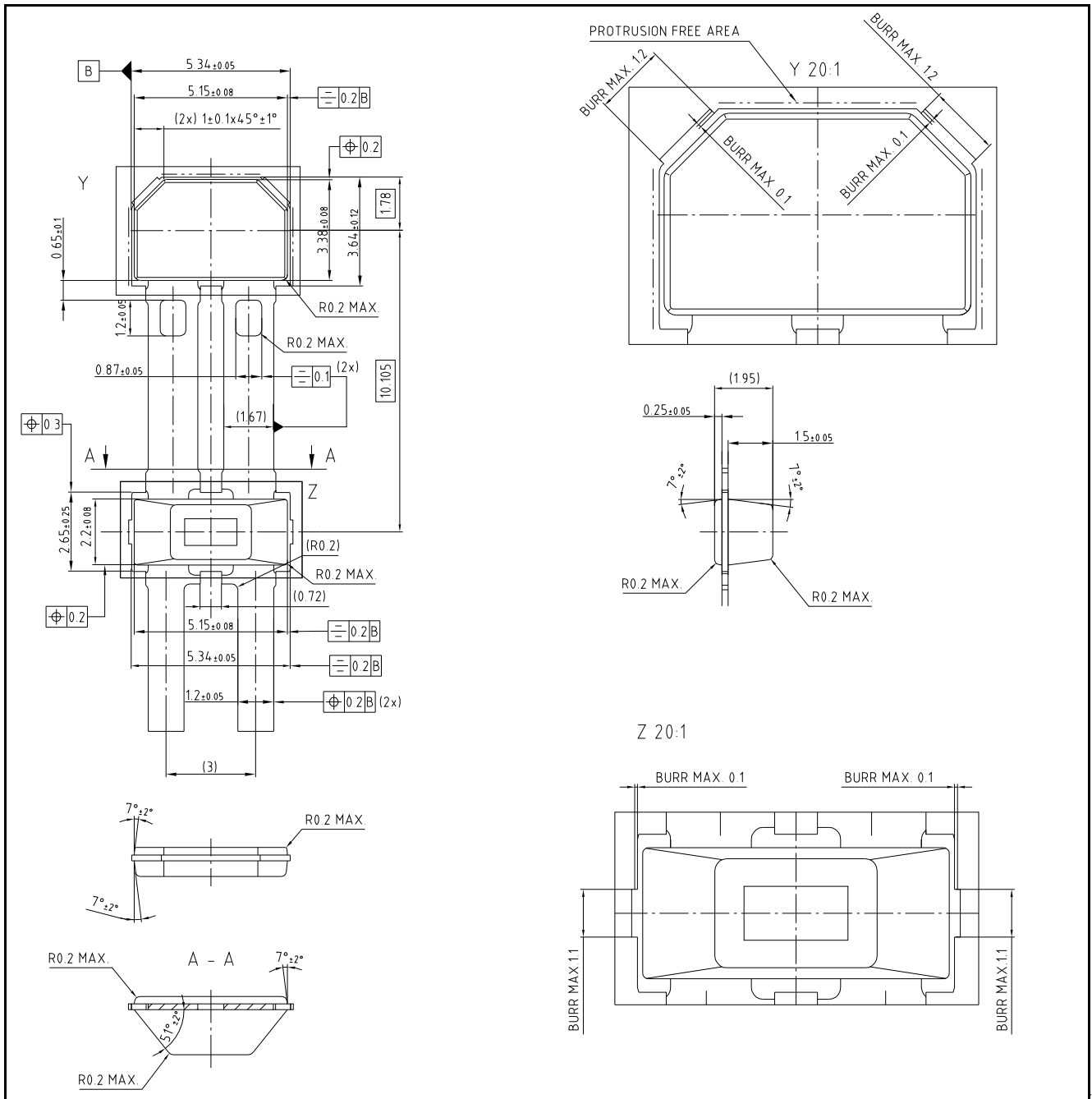


Figure 32 Package Dimensions in mm of PG-SSO-2-53 (Plastic Single Small Outline Package)

5.4 Packing

You can find all of our packages, sort of packing and others on our Infineon Internet Page "Products":
<http://www.infineon.com/products>

www.infineon.com