

# MOSFET – Power, for 1-Cell Lithium-ion Battery Protection, Dual N-Channel 12 V, 18 A, 5.9 mΩ EFC6602R

This Power MOSFET features a low on-state resistance. This device is suitable for applications such as power switches of portable machines. Best suited for 1-cell lithium-ion battery applications.

## Features

- 2.5 V Drive
- 2 kV ESD HBM
- Common-Drain Type
- ESD Diode-Protected Gate
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

## Typical Applications

- 1-Cell Lithium-ion Battery Charging and Discharging Switch

## Specifications

### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

Parameter	Symbol	Value	Unit
Source-to-Source Voltage	V <sub>SSS</sub>	12	V
Gate-to-Source Voltage	V <sub>GSS</sub>	±12	V
Source Current (DC)	I <sub>S</sub>	18	A
Source Current (Pulse) PW ≤ 10 μs, duty cycle ≤ 1%	I <sub>SP</sub>	60	A
Total Dissipation (Note 1)	P <sub>T</sub>	2.0	W
Junction Temperature	T <sub>J</sub>	150	°C
Storage Temperature	T <sub>STG</sub>	- 55 to +150	°C

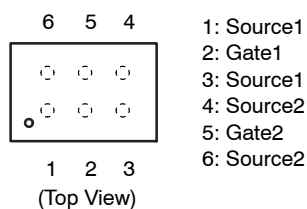
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE RATINGS

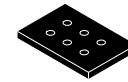
Parameter	Symbol	Value	Unit
Junction to Ambient (Note 1)	R <sub>θJA</sub>	62.5	°C/W

1. Surface mounted on ceramic substrate (5000 mm<sup>2</sup> x 0.8 mm)

### PIN ASSIGNMENT

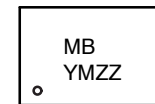


V <sub>SSS</sub>	R <sub>SS(on)</sub> Max	I <sub>S</sub> Max
12 V	5.9 mΩ @ 4.5 V	18 A
	6.3 mΩ @ 4.0 V	
	6.5 mΩ @ 3.8 V	
	8.2 mΩ @ 3.1 V	
	11 mΩ @ 2.5 V	



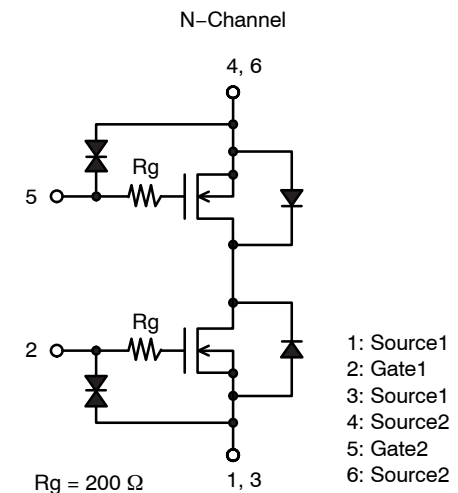
WLCSP6 1.81x2.70 / EFCP2718-6CE-020  
CASE 567HS

## MARKING DIAGRAM



- MB = Specific Device Code  
Y = Year of Production  
M = Assembly Operation Month  
ZZ = Assembly Lot Number

## ELECTRICAL CONNECTION



## ORDERING INFORMATION

Device	Package	Shipping
EFC6602R-TR	WLCSP6 (Pb-Free and Halogen Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Source-to-Source Breakdown Voltage	V <sub>(BR)SSS</sub>	I <sub>S</sub> = 1 mA, V <sub>GS</sub> = 0 V	Test Circuit 1	12	-	-	V
Zero-Gate Voltage Source Current	I <sub>SSS</sub>	V <sub>SS</sub> = 10 V, V <sub>GS</sub> = 0 V	Test Circuit 1	-	-	1	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±8 V, V <sub>SS</sub> = 0 V	Test Circuit 2	-	-	±1	μA
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>SS</sub> = 6 V, I <sub>S</sub> = 1 mA	Test Circuit 3	0.5	-	1.3	V
Forward Transconductance	g <sub>FS</sub>	V <sub>SS</sub> = 6 V, I <sub>S</sub> = 3 A	Test Circuit 4	-	13	-	S
Static Source-to-Source On-State Resistance	R <sub>SS(on)</sub>	I <sub>S</sub> = 3 A, V <sub>GS</sub> = 4.5 V	Test Circuit 5	3.1	4.5	5.9	mΩ
		I <sub>S</sub> = 3 A, V <sub>GS</sub> = 4.0 V	Test Circuit 5	3.3	4.8	6.3	mΩ
		I <sub>S</sub> = 3 A, V <sub>GS</sub> = 3.8 V	Test Circuit 5	3.5	5.0	6.5	mΩ
		I <sub>S</sub> = 3 A, V <sub>GS</sub> = 3.1 V	Test Circuit 5	4.0	5.8	8.2	mΩ
		I <sub>S</sub> = 3 A, V <sub>GS</sub> = 2.5 V	Test Circuit 5	5.2	7.5	11	mΩ
Turn-ON Delay Time	t <sub>d(on)</sub>	V <sub>SS</sub> = 6 V, V <sub>GS</sub> = 4.5 V, I <sub>S</sub> = 3 A	Test Circuit 6	-	530	-	ns
Rise Time	t <sub>r</sub>			-	2100	-	ns
Turn-OFF Delay Time	t <sub>d(off)</sub>			-	6200	-	ns
Fall Time	t <sub>f</sub>			-	5500	-	ns
Total Gate Charge	Q <sub>g</sub>	V <sub>SS</sub> = 6 V, V <sub>GS</sub> = 4.5 V, I <sub>S</sub> = 18 A	Test Circuit 7	-	55	-	nC
Forward Source-to-Source Voltage	V <sub>F(S-S)</sub>	I <sub>S</sub> = 3 A, V <sub>GS</sub> = 0 V	Test Circuit 8	-	0.76	1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Test circuits are example of measuring FET1 side.

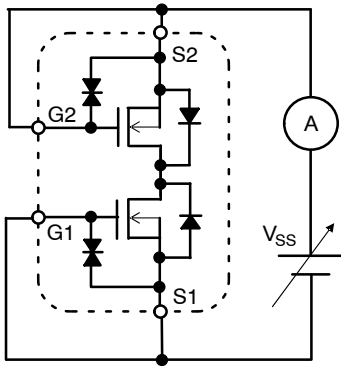


Figure 1. Test Circuit 1 - V<sub>(BR)SSS</sub> / I<sub>SSS</sub>

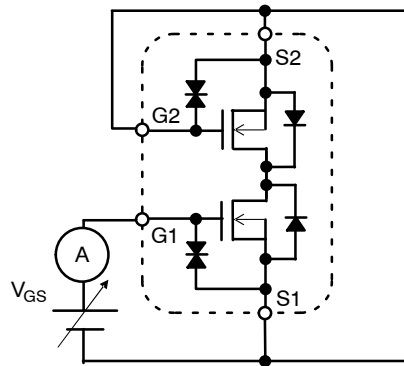


Figure 2. Test Circuit 2 - I<sub>GSS</sub>

When FET1 is measured, Gate and Source of FET2 are short-circuited.

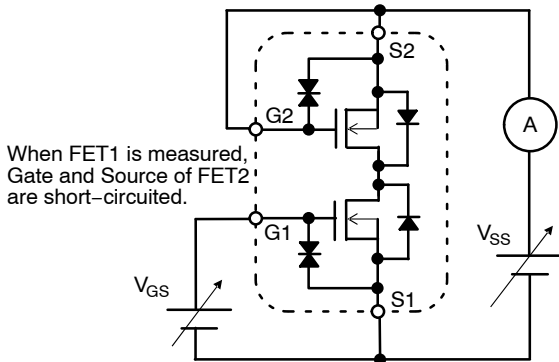


Figure 3. Test Circuit 3 - V<sub>GS(th)</sub>

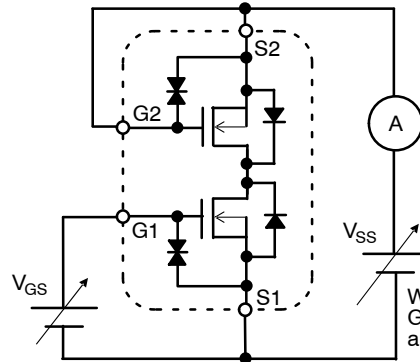


Figure 4. Test Circuit 4 - g<sub>FS</sub>

TEST CIRCUITS (continued)

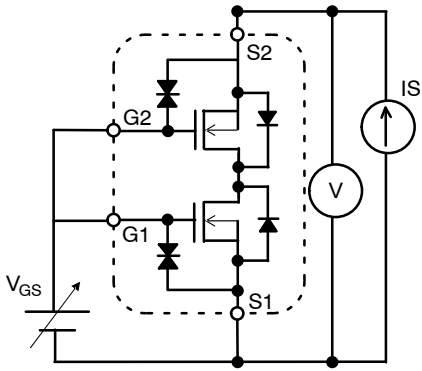


Figure 5. Test Circuit 5 -  $R_{SS(on)}$

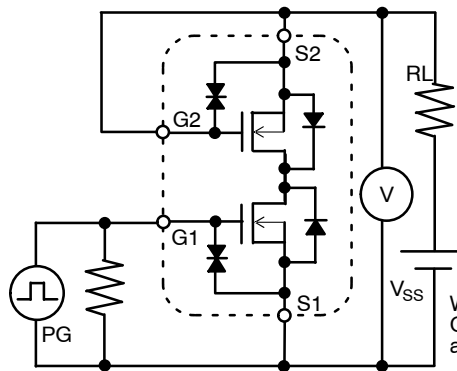


Figure 6. Test Circuit 6 -  $t_d(on)$ ,  $t_r$ ,  $t_d(off)$ ,  $t_f$

When FET1 is measured, Gate and Source of FET2 are short-circuited.

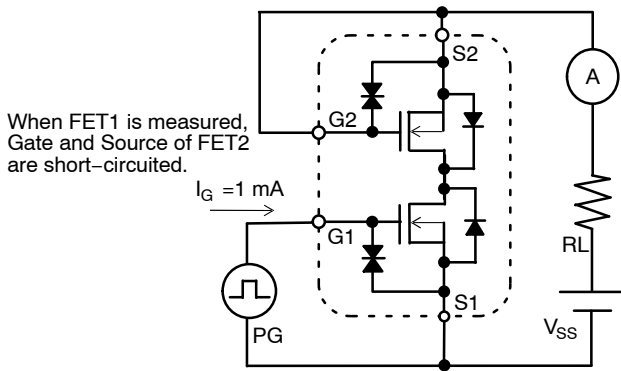


Figure 7. Test Circuit 7 -  $Q_g$

When FET1 is measured, Gate and Source of FET2 are short-circuited.

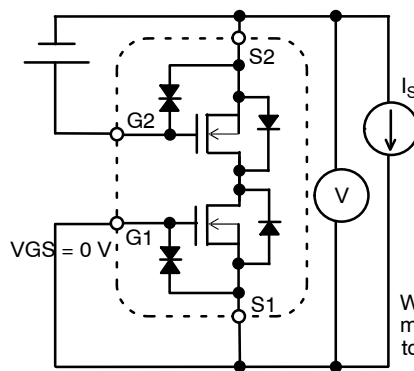


Figure 8. Test Circuit 8 -  $V_{F(S-S)}$

When FET1 is measured, +4.5 V is added to  $V_{GS}$  of FET2.

When FET2 is measured, the position of FET1 and FET2 is switched.

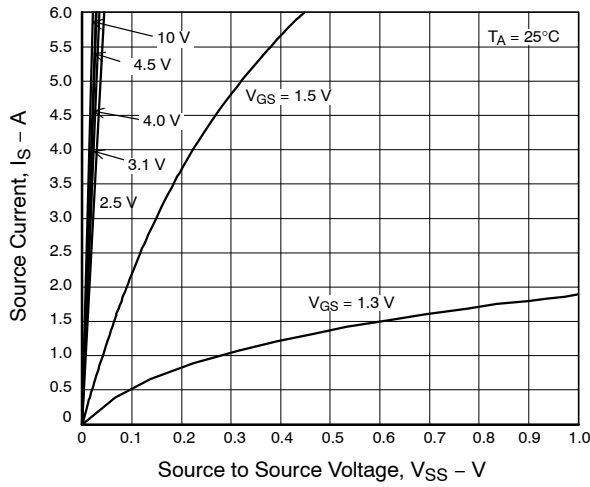


Figure 9.  $I_D - V_{SS}$

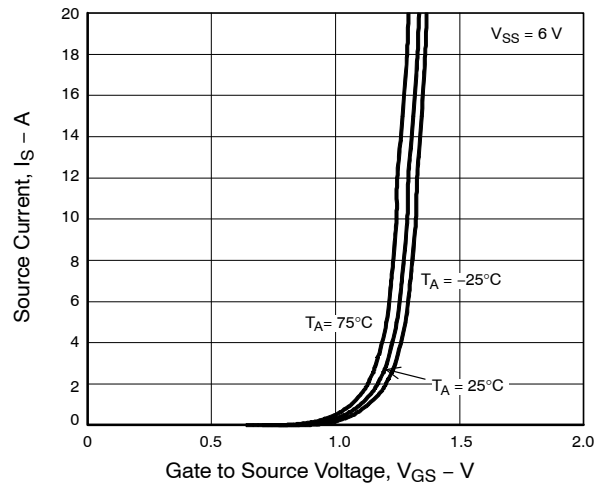


Figure 10.  $I_S - V_{GS}$

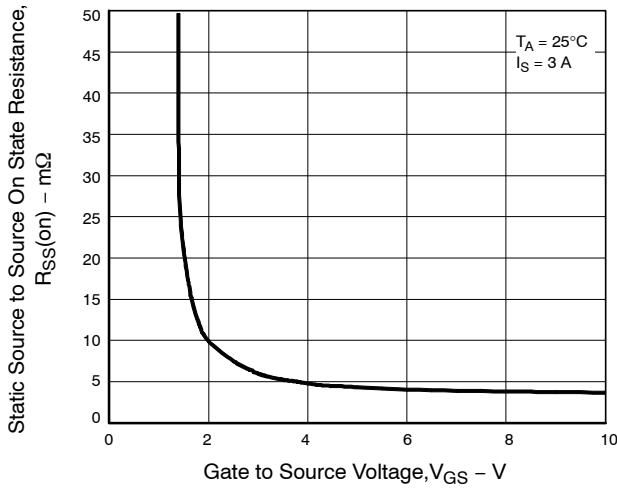


Figure 11.  $R_{SS(on)} - V_{GS}$

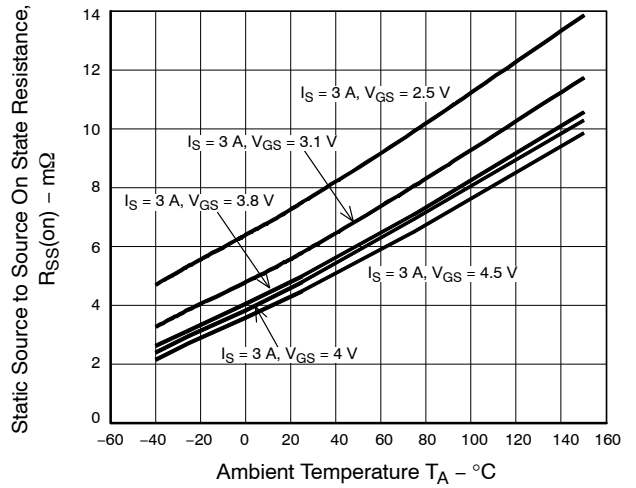


Figure 12.  $R_{SS(on)} - T_A$

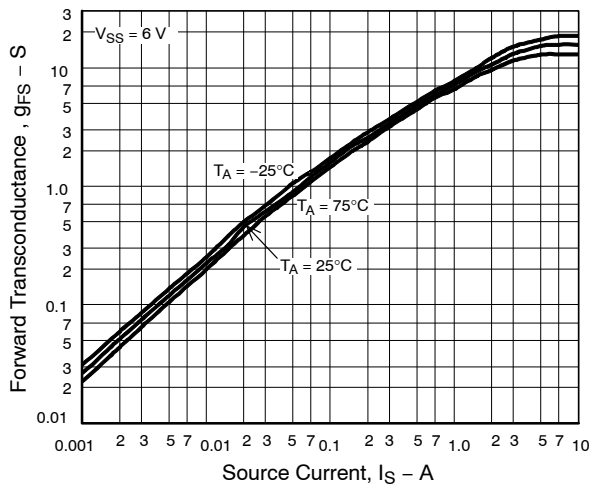


Figure 13.  $g_{FS} - I_S$

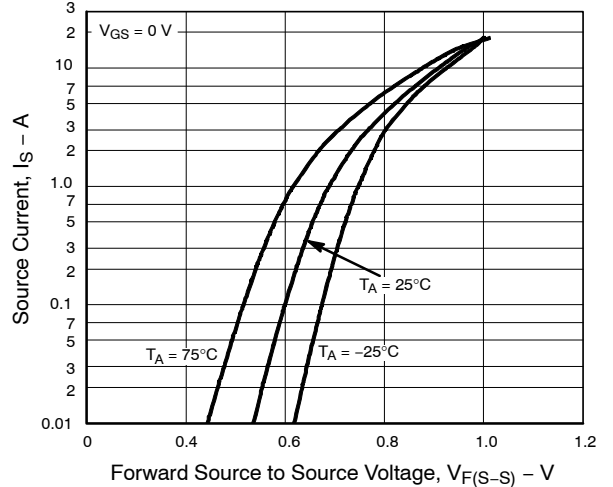


Figure 14.  $I_S - V_{F(S-S)}$

# EFC6602R

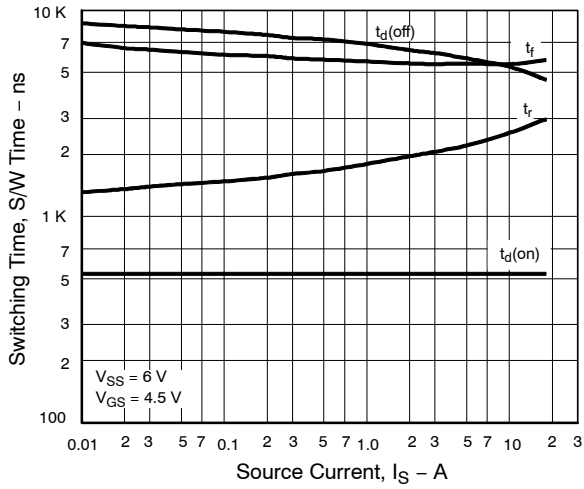


Figure 15. S/W Time -  $I_S$

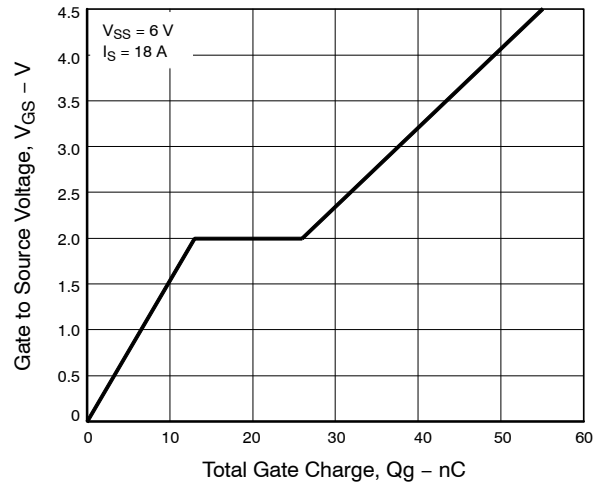


Figure 16.  $V_{GS}$  -  $Q_g$

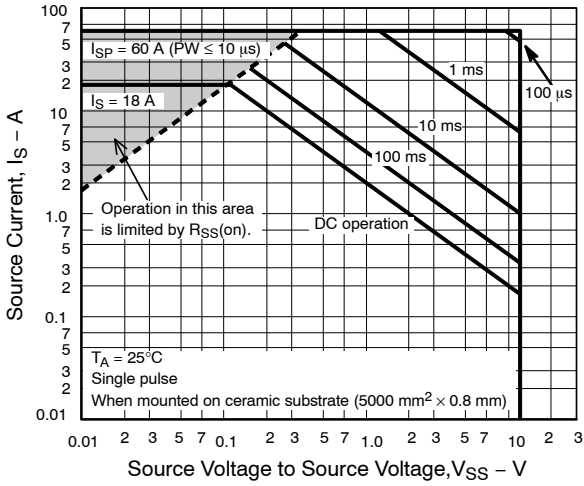


Figure 17. SOA

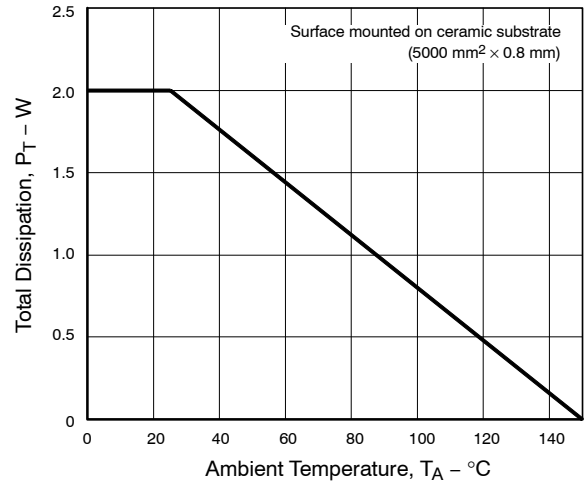


Figure 18.  $P_T$  -  $T_A$

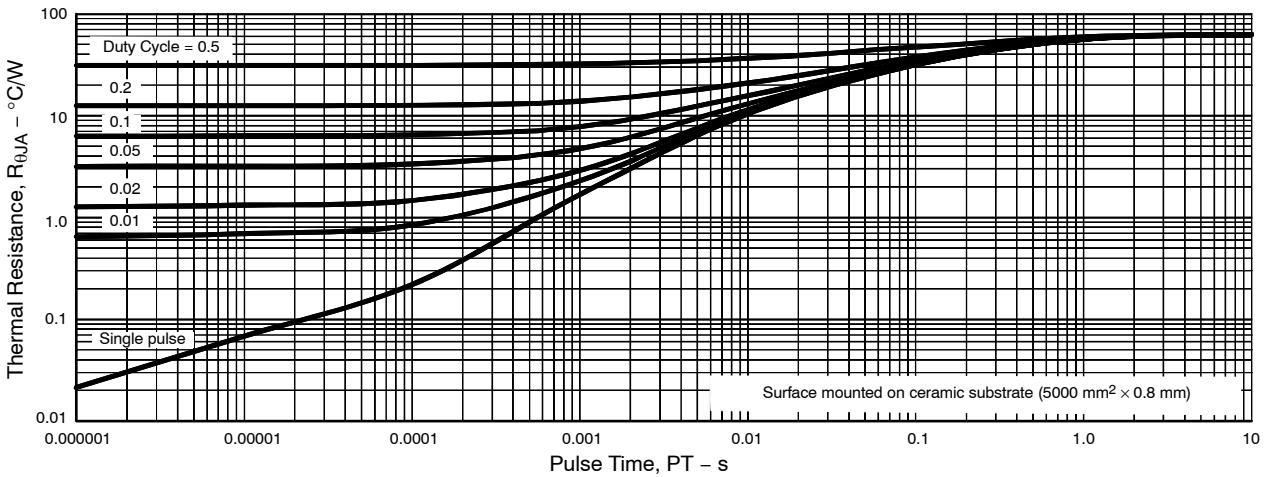


Figure 19.  $R_{\theta JA}$  - Pulse Time

Note on usage: Since the EFC6602R is a MOSFET product, please avoid using this device in the vicinity of highly charged objects. Please contact sales for use except the designated application.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

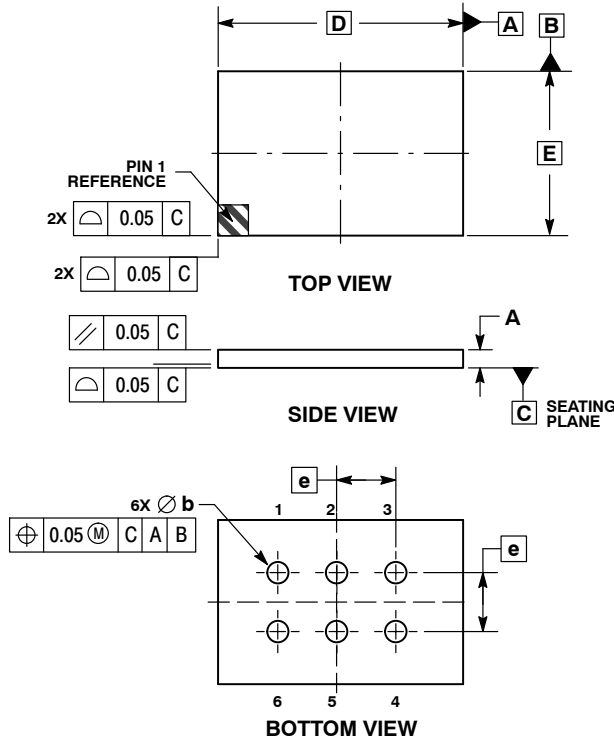
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SCALE 4:1

WLCSP6 1.81x2.70 / EFCP2718-6CE-020  
CASE 567HS  
ISSUE A

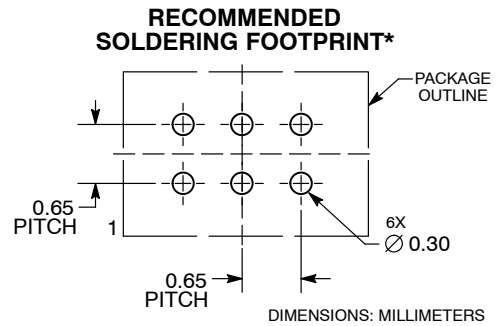
DATE 14 NOV 2014



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.18	0.22
b	0.27	0.33
D	2.70 BSC	
E	1.81 BSC	
e	0.65 BSC	



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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