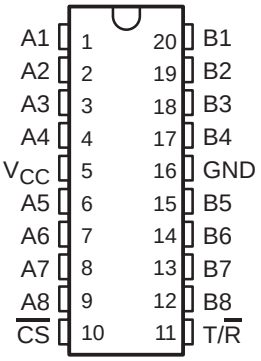
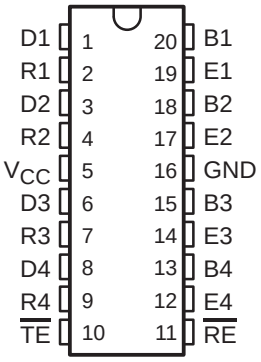
SLLS028G – AUGUST 1987 – REVISED JUNE 1998

- **Suitable for IEEE Standard 896 Applications†**
- **SN75ALS056 is an Octal Transceiver**
- **SN75ALS057 is a Quad Transceiver**
- **High-Speed Advanced Low-Power Schottky (ALS) Circuitry**
- **Low Power Dissipation:**
  52.5 mW/Channel Max
- **High-Impedance pnp Inputs**
- **Logic-Level 1-V Bus Swing Reduces Power Consumption**
- **Trapezoidal Bus Output Waveform Reduces Noise Coupling to Adjacent Lines**
- **Power-Up/Power-Down Protection (Glitch Free)**
- **Open-Collector Driver Outputs Allow Wired-OR Connections**
- **Designed to Be a Faster, Lower-Power Functional Equivalent of National DS3896, DS3897**

SN75ALS056 . . . DW OR N PACKAGE
(TOP VIEW)



SN75ALS057 . . . DW OR N PACKAGE
(TOP VIEW)



description

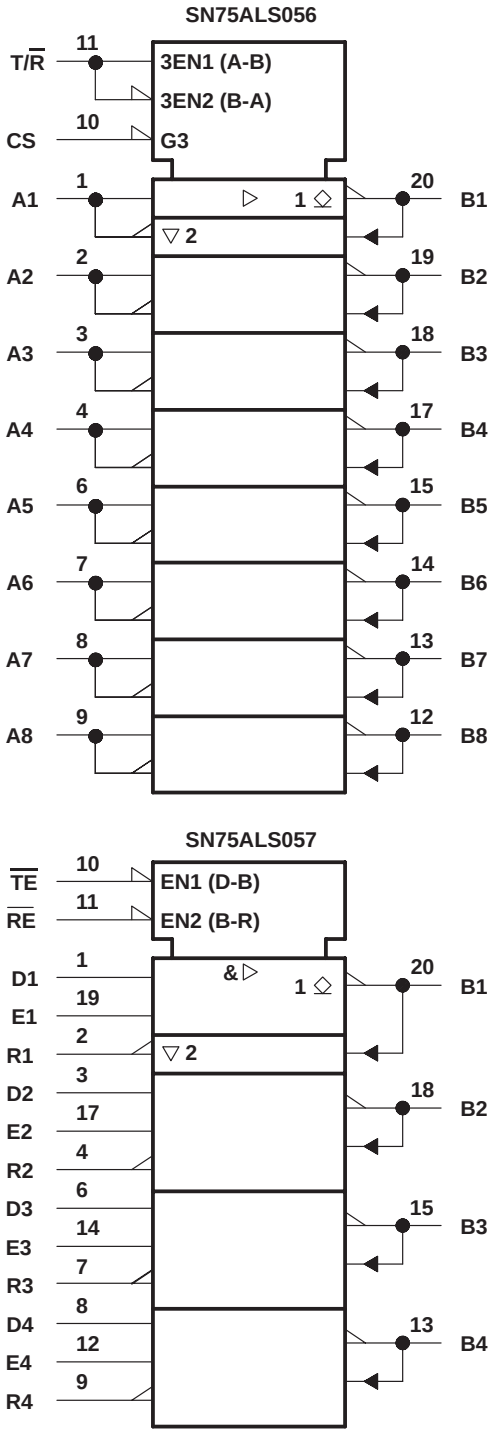
The SN75ALS056 is an eight-channel, monolithic, high-speed, advanced low-power Schottky (ALS) device designed for two-way data communication in a densely populated backplane. The SN75ALS057 is a four-channel version with independent driver-input (Dn) and receiver-output (Rn) pins and a separate driver disable for each driver (En).

These transceivers feature open-collector driver outputs with series Schottky diodes to reduce capacitive loading to the bus. By using a 2-V pullup termination on the bus, the output signal swing is approximately 1 V, which reduces the power necessary to drive the bus load capacitance. The driver outputs generate trapezoidal waveforms that reduce crosstalk between channels. The drivers are capable of driving an equivalent dc load as low as 18.5 Ω. The receivers have internal low-pass filters to further improve noise immunity.

The SN75ALS056 and SN75ALS057 are characterized for operation from 0°C to 70°C.

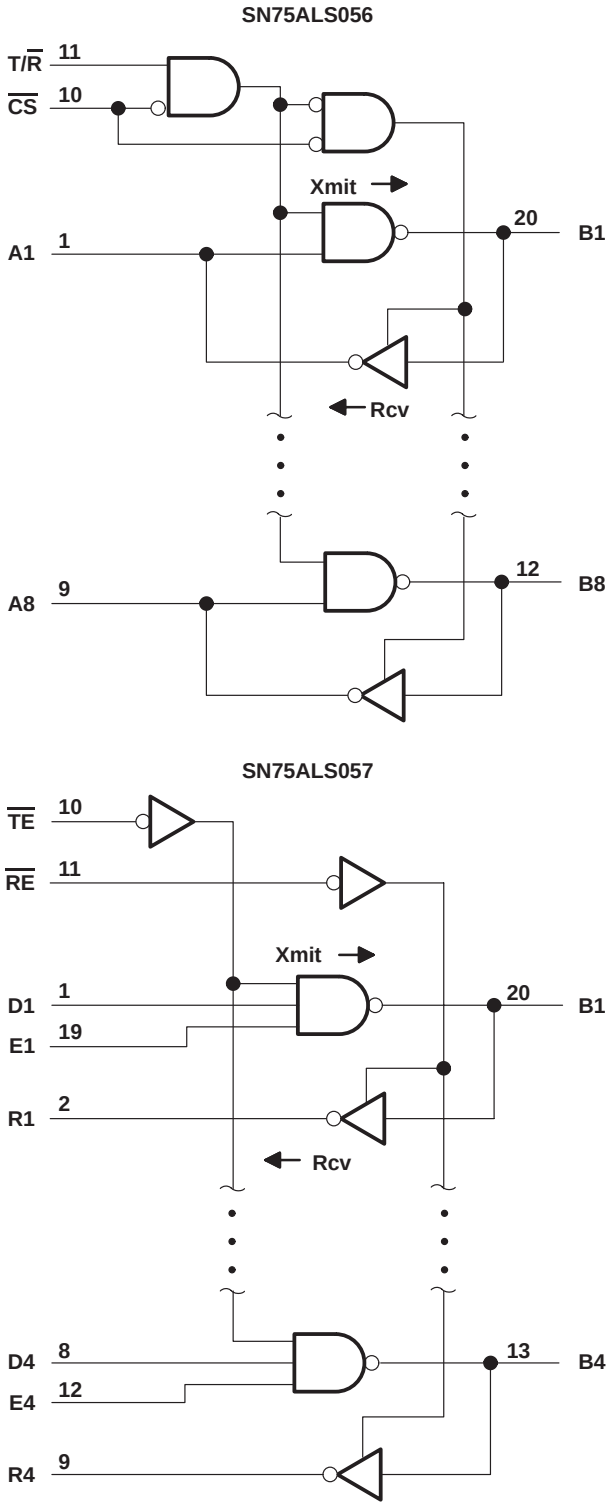
† The transceivers are suitable for IEEE Standard 896 applications to the extent of the operating conditions and characteristics specified in this data sheet.

logic symbol†



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Function Tables

SN75ALS056
TRANSMIT/RECEIVE

CONTROLS		CHANNELS
$\overline{CS}$	T/$\overline{R}$	A ↔ B
L	H	T(A B)
L	L	R(B A)
H	X	D

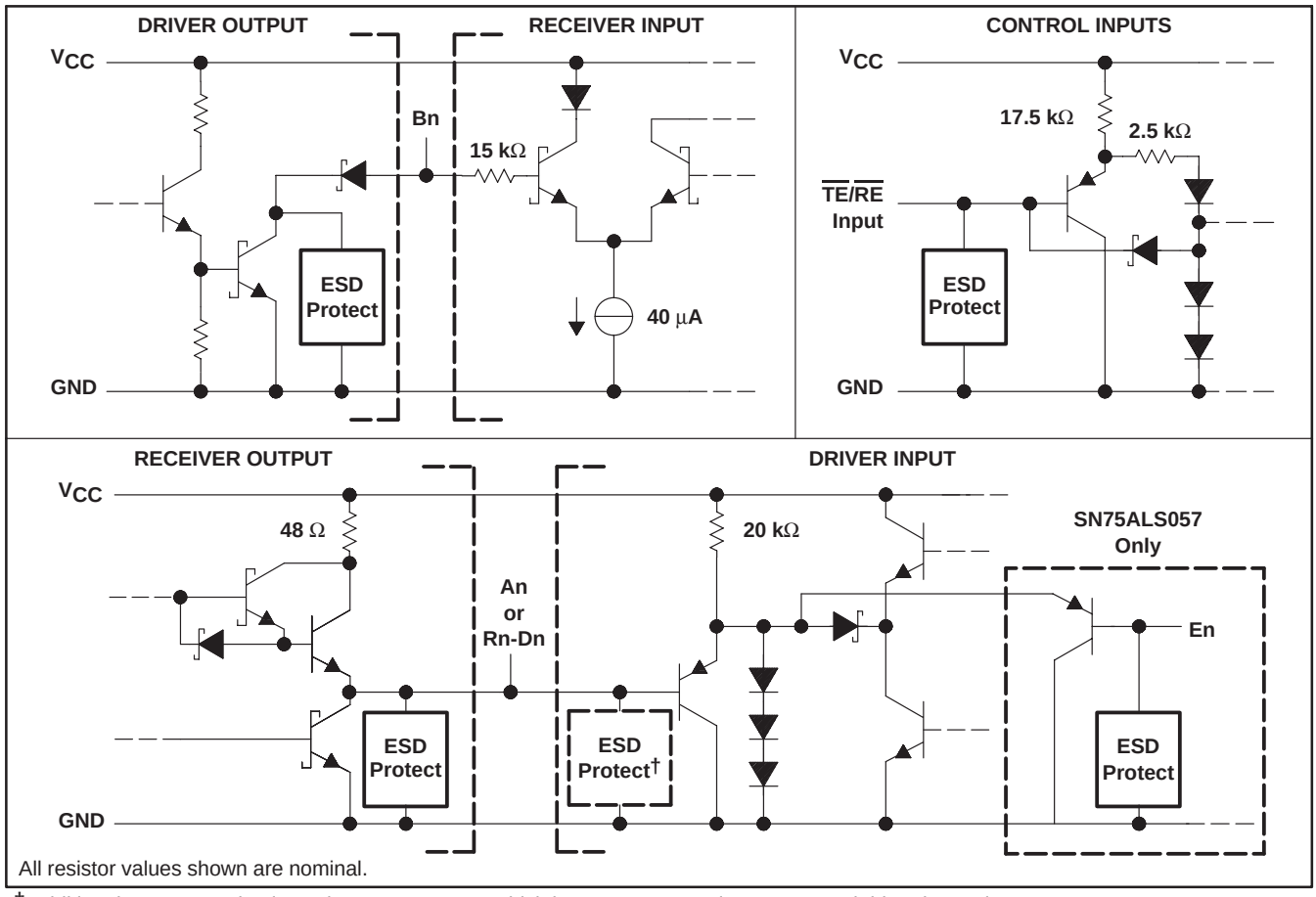
SN75ALS057
TRANSMIT/RECEIVE

CONTROLS			CHANNELS			
$\overline{TE}$	$\overline{RE}$	En	D	B	B	R
L	L	L	D			R
L	L	H	T			R
L	H	L	D			D
L	H	H	T			D
H	L	X	D			R
H	H	X	D			D

H = high level, L = low level, R = receive, T = transmit,
D = disable, X = irrelevant

Direction of data transmission is from An to Bn for the SN75ALS056 and from Dn to Bn for the SN75ALS057. Direction of data reception is from Bn to An for the SN75ALS056 and from Bn to Rn for the SN75ALS057. Data transfer is inverting in both directions.

schematics of inputs and outputs



All resistor values shown are nominal.

† Additional ESD protection is on the SN75ALS057, which has separate receiver-output and driver-input pins.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, V_{CC} (see Note 1) . . . . . 6 V
Control input voltage, V_I . . . . . 5.5 V
Driver input voltage, V_I . . . . . 5.5 V
Driver output voltage, V_O . . . . . 2.5 V
Receiver input voltage, V_I . . . . . 2.5 V
Receiver output voltage, V_O . . . . . 5.5 V
Continuous total power dissipation . . . . . See Dissipation Rating Table
Storage temperature range, T_{stg} . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: DW or N package . . . . . 260 °C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 125°C$ POWER RATING
DW	1025 mW	8.2 mW/°C	656 mW	—
N	1150 mW	9.2 mW/°C	736 mW	—

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level driver and control input voltage, V_{IH}	2			V
Low-level driver and control input voltage, V_{IL}			0.8	V
Bus termination voltage	1.9		2.1	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN75ALS056			UNIT
				MIN	TYP†	MAX	
V_{IK}	Input clamp voltage at An, T/$\overline{R}$, or $\overline{CS}$		I_I = –18 mA			–1.5	V
V_{IT}	Receiver input threshold voltage at Bn			1.405		1.69	V
V_{OH}	High-level output voltage at An		Bn at 1.2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8V, I_{OH} = – 400 μA	2.4			V
V_{OL}	Low-level output voltage	An	Bn at 2 V ,$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	An at 2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, V_L = 2 V, R_L =18.5 Ω,, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	An, T/$\overline{R}$ or $\overline{CS}$	$V_I = V_{CC}$			40	μA
		Bn	V_I = 2 V, V_{CC} = 0 or 5.25 V, An at 0.8 V, T/$\overline{R}$ at 0.8 V			100	
I_{IL}	Low level input current at An, T/$\overline{R}$, or $\overline{CS}$		V_I = 0.4 V			–400	μA
I_{OS}	Short-circuit output current at An		An at 0, Bn at 1.2 V, $\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V	–40		–120	mA
I_{CC}	Supply current					75	mA
$C_{O(B)}$	Driver output capacitance				4.5		pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	SN75ALS057			UNIT
				MIN	TYP†	MAX	
V_{IK}	Input clamp voltage at Dn, En, $\overline{TE}$, or $\overline{RE}$		I_I = –18 mA			–1.5	V
V_{IT}	Receiver input threshold voltage at Bn			1.41		1.69	V
V_{OH}	High-level output voltage at Rn		Bn at 1.2 V, $\overline{RE}$ at 0.8 V, I_{OH} = –400 μA	2.4			V
V_{OL}	Low-level output voltage	Rn	Bn at 2 V, $\overline{RE}$ at 0.8 V, I_{OL} = 16 mA			0.5	V
		Bn	Dn at 2 V, En at 2 V, $\overline{TE}$ at 0.8 V, V_L = 2 V, R_L = 18.5 Ω, See Figure 1	0.75		1.2	
I_{IH}	High-level input current	Dn, En, $\overline{TE}$, or $\overline{RE}$	$V_I = V_{CC}$			40	μA
		Bn	V_I = 2 V, V_{CC} = 0 or 5.25 V, Dn at 0.8 V, En at 0.8 V, $\overline{TE}$ at 0.8 V			100	
I_{IL}	Low-level input current at Dn, En, $\overline{TE}$, or $\overline{RE}$		V_I = 0.4 V			–400	μA
I_{OS}	Short-circuit output current at Rn		Rn at 0, Bn at 1.2 V, $\overline{RE}$ at 0.8 V	–40		–120	mA
I_{CC}	Supply current					40	mA
$C_{O(B)}$	Driver output capacitance				4.5		pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN75ALS056 DRIVER			UNIT
					MIN	TYP†	MAX	
t_{PLH1}	Propagation delay time, low-to-high-level output	$\overline{CS}$	Bn	An and T/$\overline{R}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω,, C_L = 30 pF, R_L2 not connected, See Figure 2			24	ns
t_{PHL1}	Propagation delay time, high-to-low-level output						20	
t_{PLH2}	Propagation delay time, low-to-high-level output	An	Bn	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω,, R_L2 not connected, C_L = 30 pF, See Figure 2,			19	ns
t_{PHL2}	Propagation delay time high-to-low-level output						18	
t_{PLH3}	Propagation delay time, low-to-high-level output	T/$\overline{R}$	Bn	$V_{I(An)}$ = 5 V, CS at 0.8 V, R_L1 = 18 Ω, C_L = 30 pF, R_L2 not connected, V_L = 2 V, See Figure 3,			25	ns
t_{PHL3}	Propagation delay time, high-to-low-level output						35	
t_{TLH}	Transition time, low-to-high-level output	An	Bn	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 2 V, V_L = 2 V, C_L = 30 pF, R_L1 = 18 Ω, R_L2 not connected, See Figure 2	1	3	11	ns
t_{THL}	Transition time, high-to-low-level output				1	3	6	

† Typical values are at V_{CC} = 5 V, T_A = 25°C

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN75ALS056 RECEIVER		UNIT
					MIN	MAX	
t_{PLH4}	Propagation delay time, low-to-high-level output	Bn	An	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 4		18	ns
t_{PHL4}	Propagation delay time, high-to-low-level output					18	
t_{PLZ1}	Output disable time from low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 not connected, C_L = 15 pF, See Figure 3		20	ns
t_{PZL1}	Output enable time to low level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 2 V, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 3		40	ns
t_{PHZ1}	Output disable time from high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 0, V_L = 0, R_L1 = 390 Ω, R_L2 not connected, C_L = 15 pF, See Figure 3		17	ns
t_{PZH1}	Output enable time to high level	T/$\overline{R}$	An	$\overline{CS}$ at 0.8 V, $V_{I(Bn)}$ = 0, V_L = 0, R_L1 not connected, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 3		15	ns
t_{PLZ2}	Output disable time from low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 5 V, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		18	ns
t_{PZL2}	Output enable time to low level	$\overline{CS}$	An	Bn at 2 V, T/$\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 5 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, See Figure 5		15	ns
t_{PHZ2}	Output disable time from high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, C_L = 5 pF, V_L = 0, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		8	ns
t_{PZH2}	Output enable time to high level	$\overline{CS}$	An	Bn at 0.8 V, T/$\overline{R}$ at 0.8 V, C_L = 30 pF, V_L = 0, R_L1 not connected, R_L2 = 1.6 kΩ, See Figure 5		17	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	An	$\overline{CS}$ at 0.8 V, T/$\overline{R}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, V_L = 5 V, See Figure 6	3		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN75ALS057 DRIVER			UNIT
					MIN	TYP†	MAX	
t_{PLH1}	Propagation delay time, low-to-high-level output	$\overline{TE}$	Bn	Dn, En, $\overline{RE}$ at 2 V, V_L = 2 V, R_L2 not connected, R_L1 = 18 Ω, See Figure 2, C_L = 30 pF			24	ns
t_{PHL1}	Propagation delay time, high-to-low-level output						20	
t_{PLH2}	Propagation delay time, low-to-high-level output	Dn or En	Bn	$\overline{TE}$ at 0.8 V, $\overline{RE}$ at 2 V, V_L = 2 V, R_L1 = 18 Ω, R_L2 not connected, C_L = 30 pF, See Figure 2			19	ns
t_{PHL2}	Propagation delay time, high-to-low-level output						18	
t_{TLH}	Transition time, low-to-high-level output	Dn or En	Bn	$\overline{RE}$ at 2 V, V_L = 2 V, $\overline{TE}$ at 0.8 V, R_L1 = 18 Ω,, R_L2 not connected, C_L = 30 pF, See Figure 2	1	3	11	ns
t_{THL}	Transition time, high-to-low-level output				1	3	6	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN75ALS057 RECEIVER		UNIT
					MIN	MAX	
t_{PLH4}	Propagation delay time, low-to-high-level output	Bn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 2 V, V_L = 5 V, R_L1 = 390 Ω,, R_L2 = 1.6 kΩ,, C_L = 30 pF, See Figure 4		18	ns
t_{PHL4}	Propagation delay time, high-to-low-level output					18	
t_{PLZ2}	Output disable time from low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, C_L = 5 pF, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		18	ns
t_{PZL2}	Output enable time to low level	$\overline{RE}$	Rn	Bn at 2 V, $\overline{TE}$ at 2 V, V_L = 5 V, C_L = 30 pF, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, See Figure 5		15	ns
t_{PHZ2}	Output disable time from high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, C_L = 5 pF, R_L1 = 390 Ω, R_L2 not connected, See Figure 5		17	ns
t_{PZH2}	Output enable time to high level	$\overline{RE}$	Rn	Bn at 0.8 V, $\overline{TE}$ at 2 V, V_L = 0, C_L = 30 pF, R_L1 not connected, R_L2 = 1.6 kΩ, See Figure 5		17	ns
$t_{w(NR)}$	Receiver noise rejection pulse duration	Bn	Rn	$\overline{TE}$ at 2 V, $\overline{RE}$ at 0.8 V, V_L = 0, R_L1 = 390 Ω, R_L2 = 1.6 kΩ, C_L = 30 pF, See Figure 6	3		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN75ALS057 DRIVER PLUS RECEIVER		UNIT
					MIN	MAX	
t_{PLH6}	Propagation delay time, low-to-high-level output	Dn	Rn	$\overline{RE}$ at 0.8 V, $\overline{TE}$ at 0.8 V, R_L1 = 390 Ω, R_L2 = 1.6 kΩ,, C_L = 30 pF, See Figure 7		40	ns
t_{PHL6}	Propagation delay time, high-to-low-level output					40	

PARAMETER MEASUREMENT INFORMATION

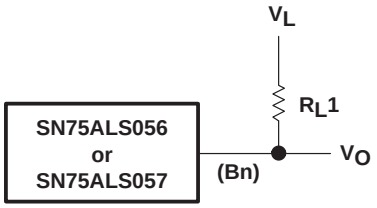
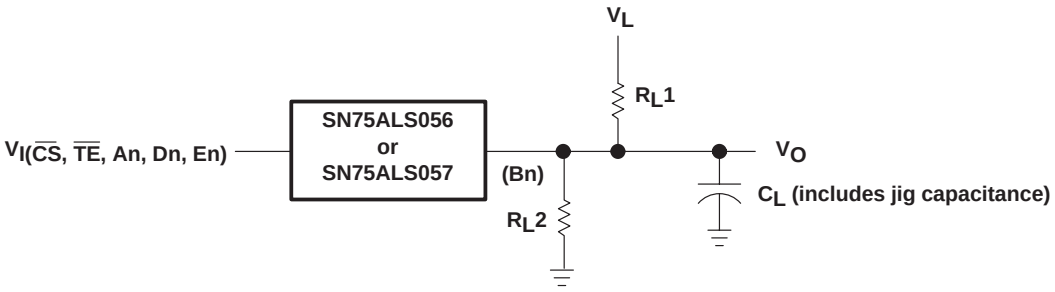
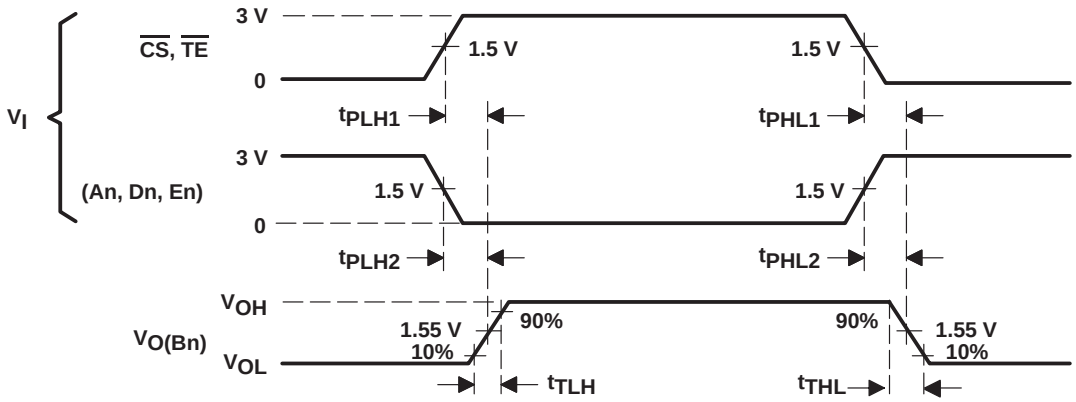


Figure 1. Driver Low-Level-Output-Voltage Test Circuit

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

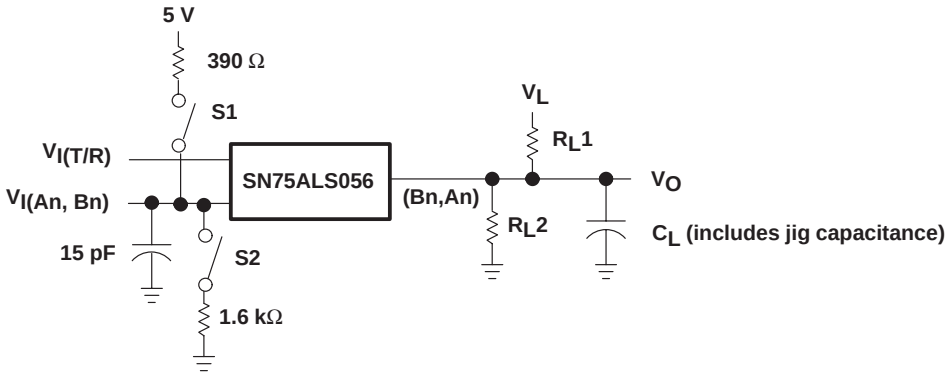


VOLTAGE WAVEFORMS

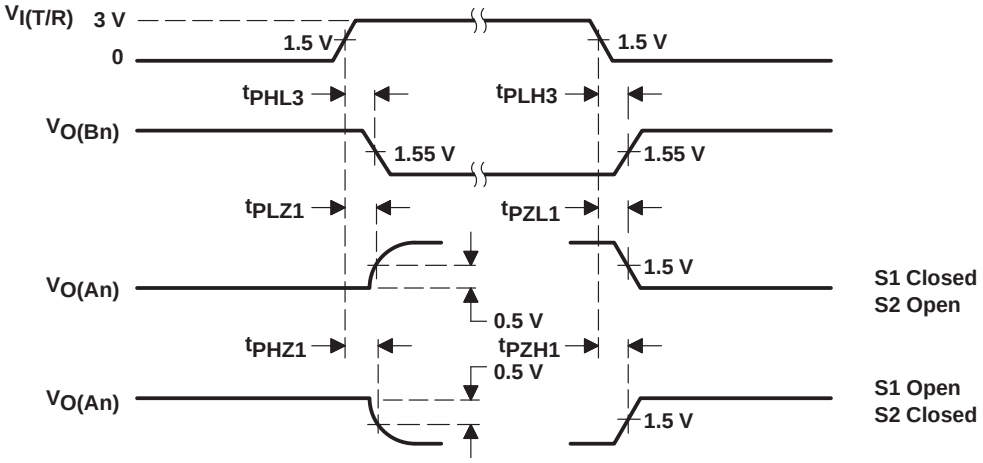
NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 2. Driver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



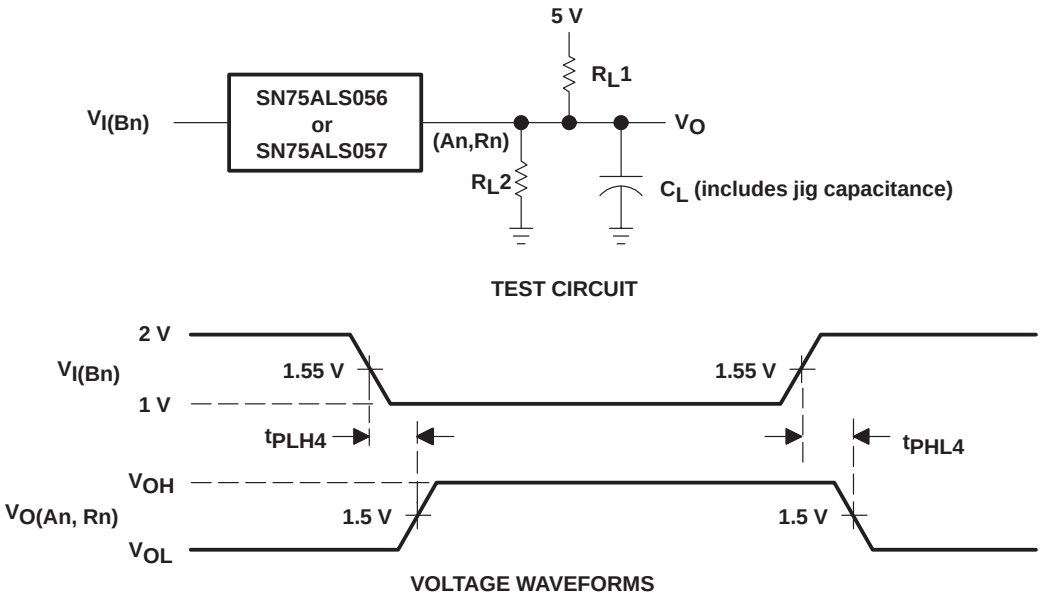
TEST CIRCUIT



VOLTAGE WAVEFORMS

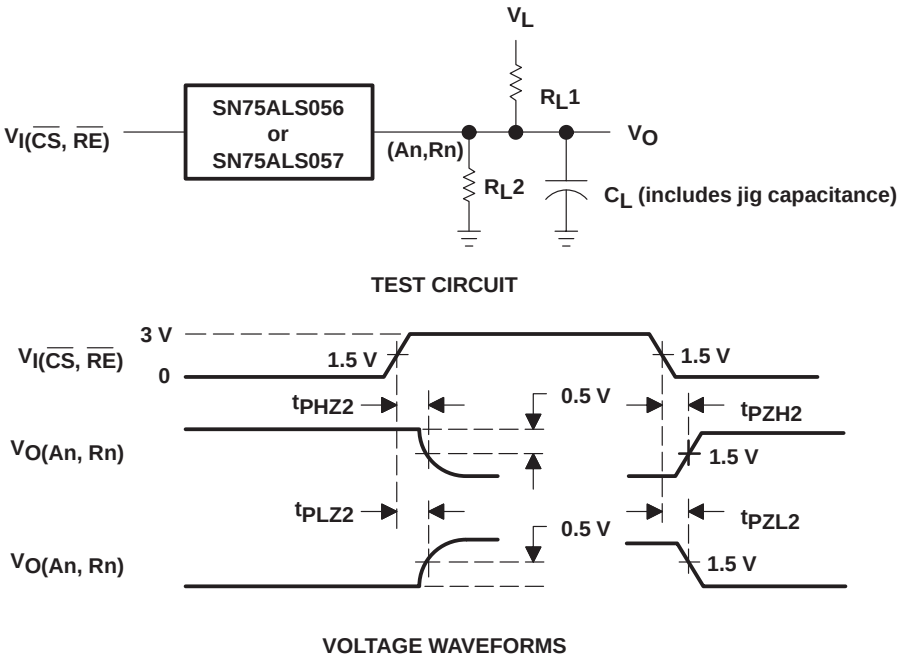
NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 3. Propagation Delay From T/$\overline{R}$ to An or Bn Test Circuit and Voltage Waveforms



NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

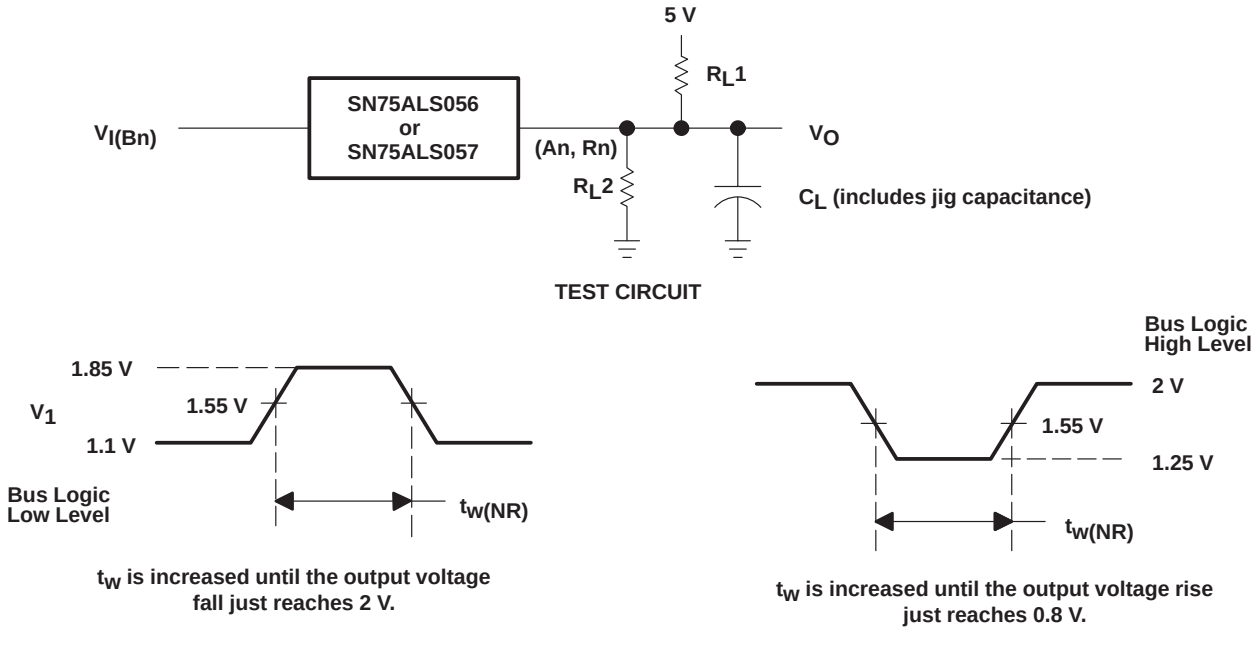
Figure 4. Receiver Test Circuit and Voltage Waveforms



NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

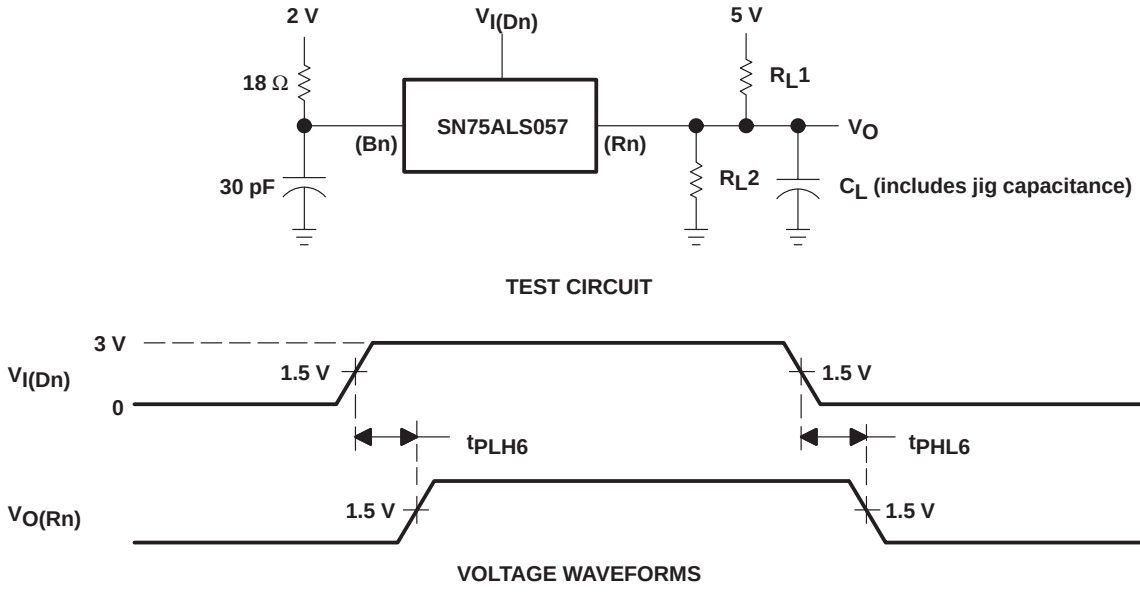
Figure 5. Propagation Delay From $\overline{CS}$ to An or $\overline{RE}$ to Rn Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 6. Receiver Noise-Immunity Test Circuit and Voltage Waveforms



NOTE A: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 7. Driver Plus Receiver Delay-Times Test Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS056DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS056	Samples
SN75ALS057DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS057	Samples
SN75ALS057DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS057	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

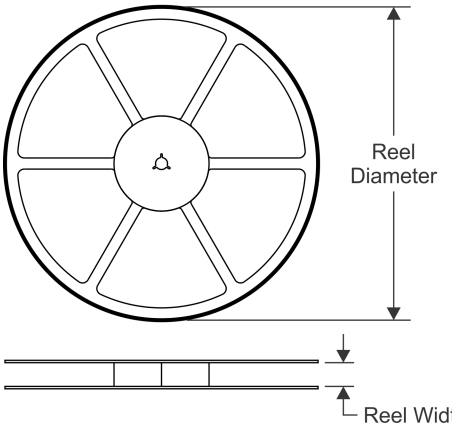
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

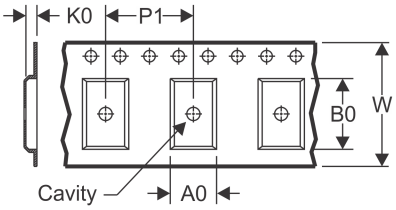
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

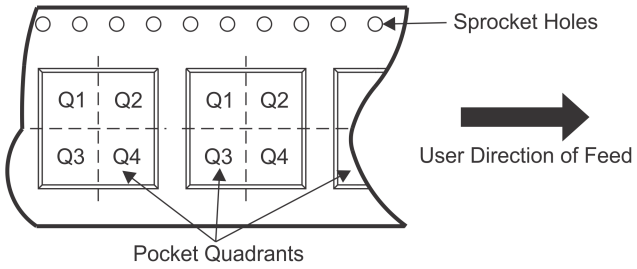


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

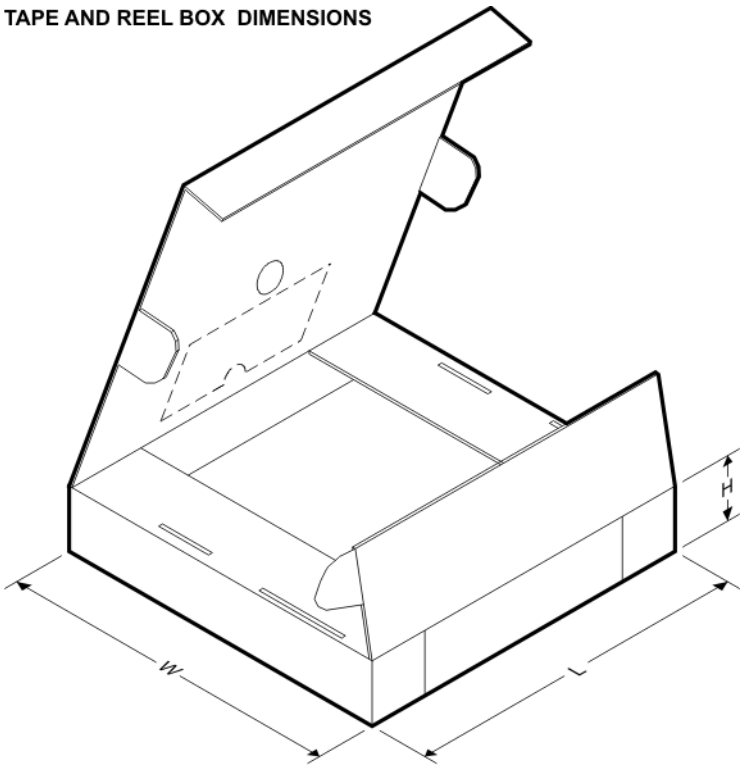
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS057DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

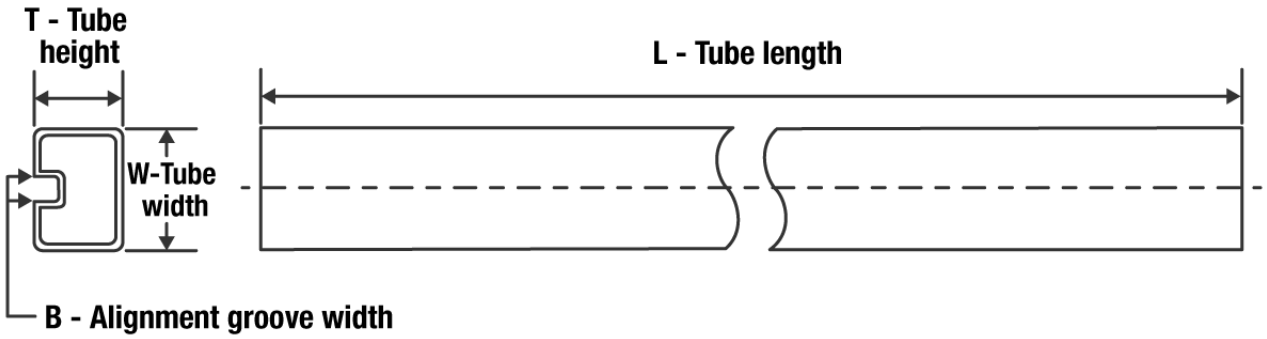
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

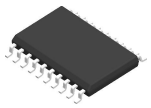
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS057DWR	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS056DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75ALS057DW	DW	SOIC	20	25	506.98	12.7	4826	6.6

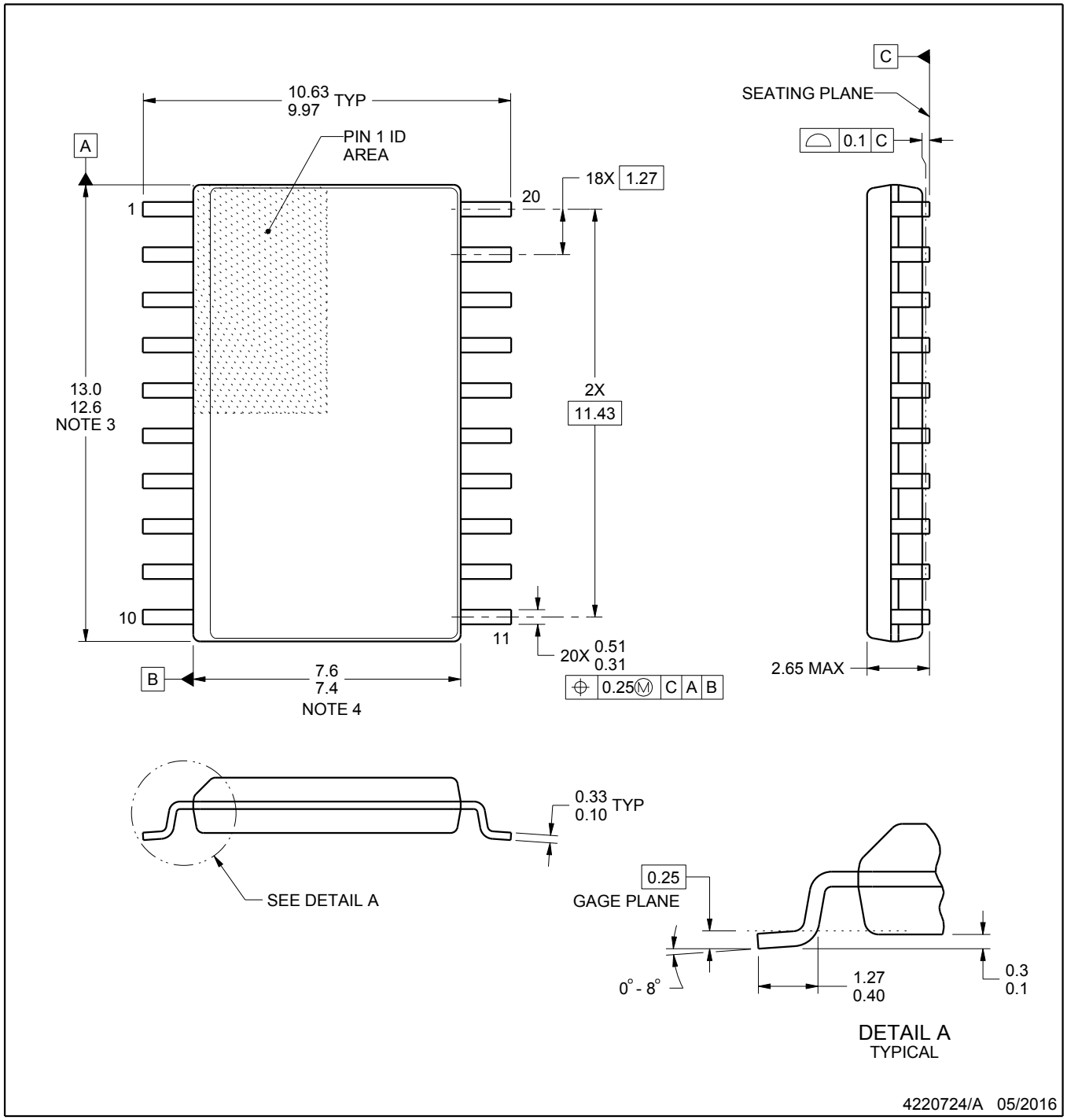


PACKAGE OUTLINE

DW0020A

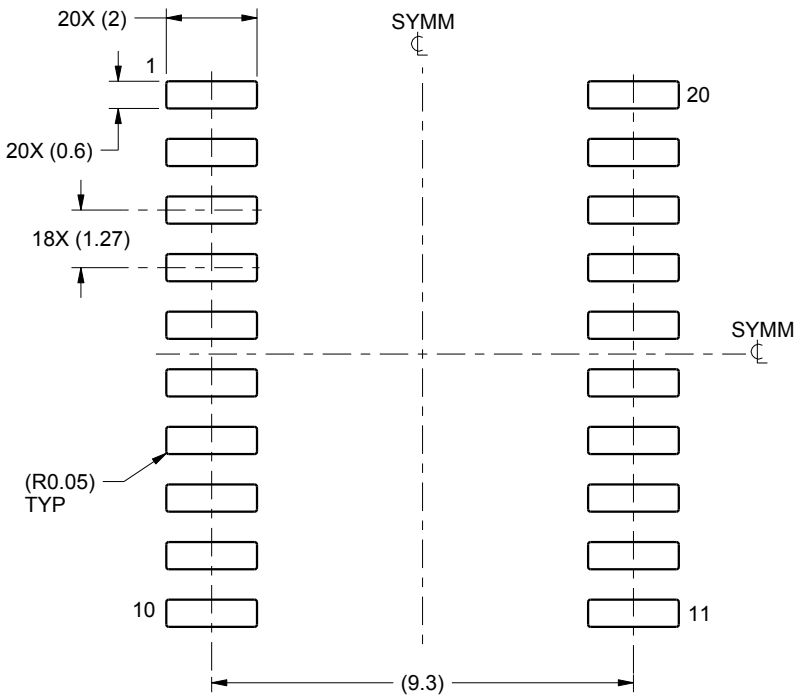
SOIC - 2.65 mm max height

SOIC

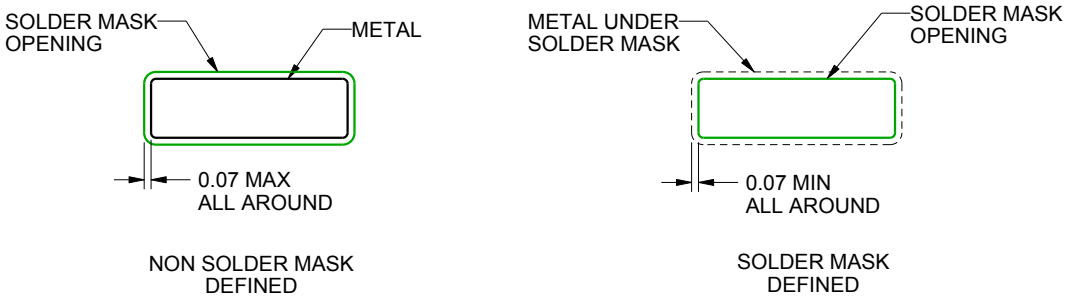


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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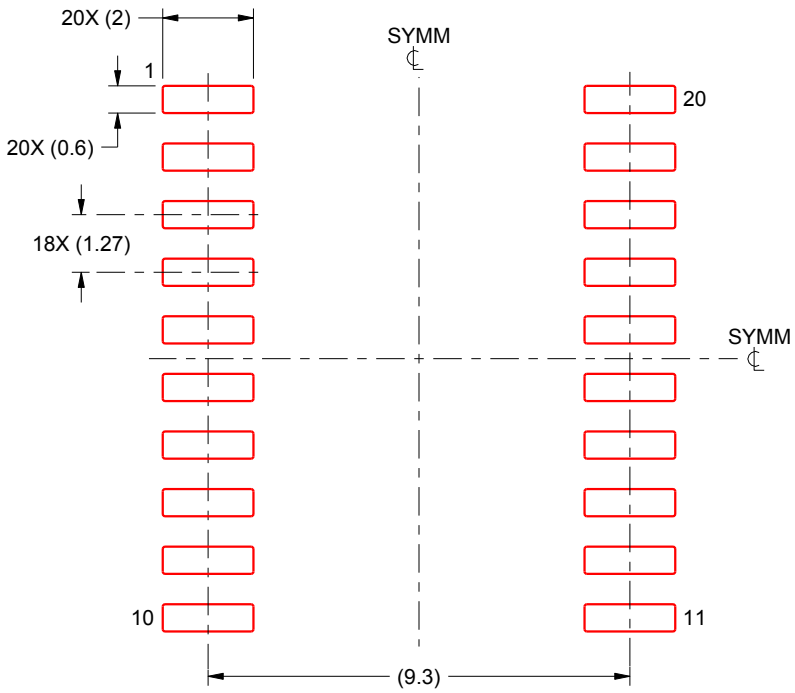
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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