User's Guide

CDCDB800/803 Ultra-Low Additive Jitter, 8-Output PCIe Gen1 to Gen5 Clock Buffer Evaluation Board

ABSTRACT

This user guide describes how to set up and operate the CDCDB800 evaluation module (EVM). By default, the CDCDB800EVM supports the use of the CDCDB800—an 8-output LP-HCSL clock buffer intended for PCIe Gen1 to Gen5.

The CDCDB800EVM also allows the user to verify the functionality and performance specifications of the CDCDB800 and after rework the CDCDB803. Refer to the CDCDB800 and CDCDB803 datasheets for functional description and specifications.

The evaluation board is equipped with 50-Ω SMA connectors and impedance controlled 50-Ω microstrip input and 85-Ω microstrip output transmission lines for best performance.

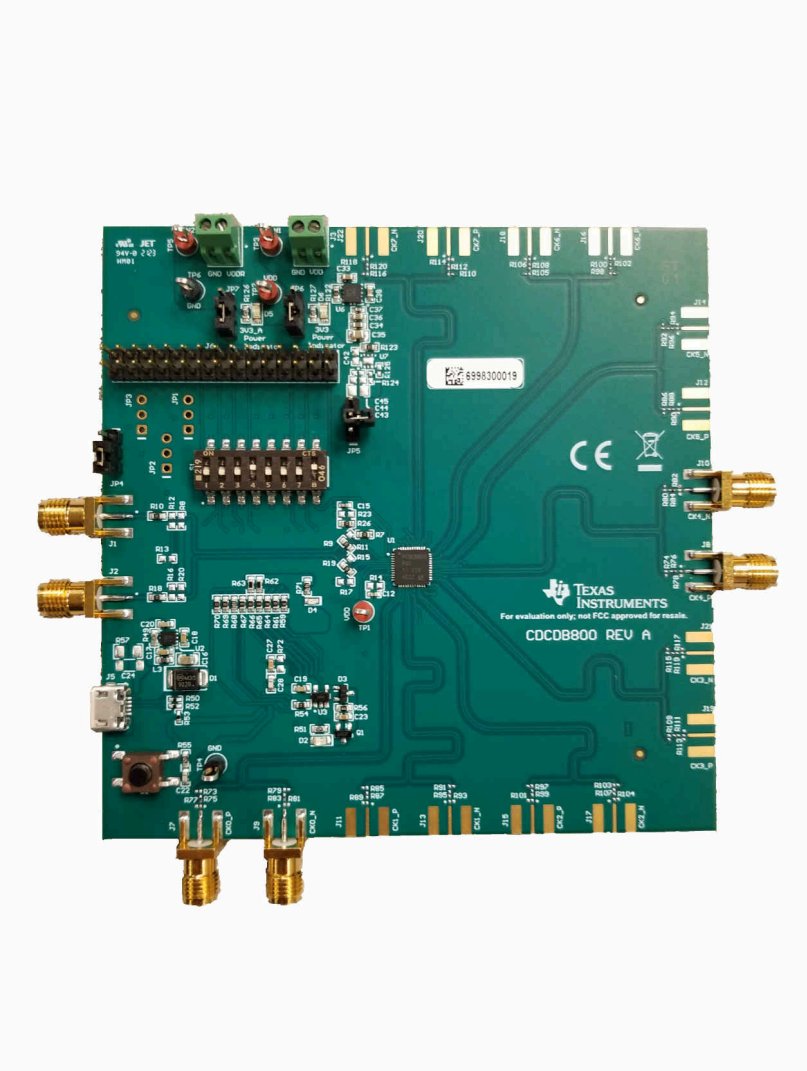

Figure 1-1. CDCDB800/803 Evaluation Board

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1 Trademarks

All trademarks are the property of their respective owners.

2 General Description

2.1 Features

- Easy-to-use evaluation board to fan out low-phase noise clocks
- Simple, fast device configuration and setup
- 8 LP-HCSL outputs with integrated 85-Ω output terminations
- 8 hardware output enable (OE#) controls
- DIP switch control of device configuration
- Differential or single-ended input clock accepted
- EVM supports all 8 differential LVDS outputs. Both output banks are available for testing by default

3 Quick Setup

To quickly set up and operate the board with basic equipment, refer to the setup procedure below and test setup shown in Figure 3-1.

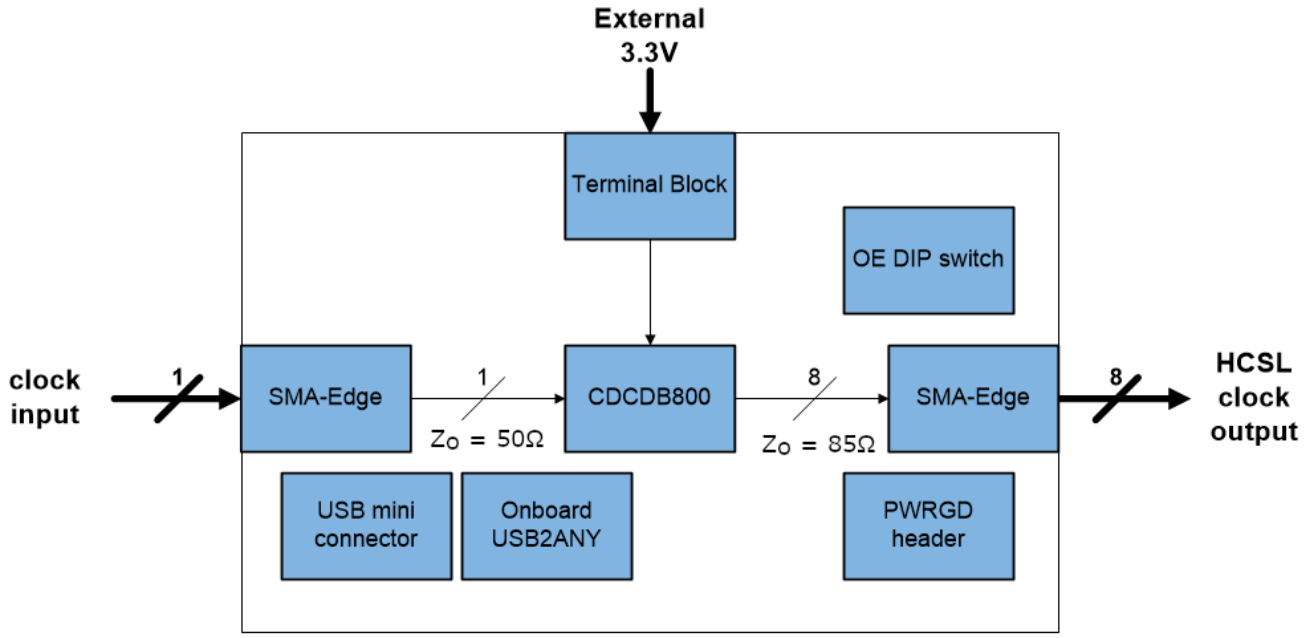

Figure 3-1. CDCDB800 Evaluation Board Quick Start Setup

3.1 Setup Procedure

1. Verify the jumpers match the states shown in Table 3-1 to reflect the default output clock interfaces configured on the EVM.

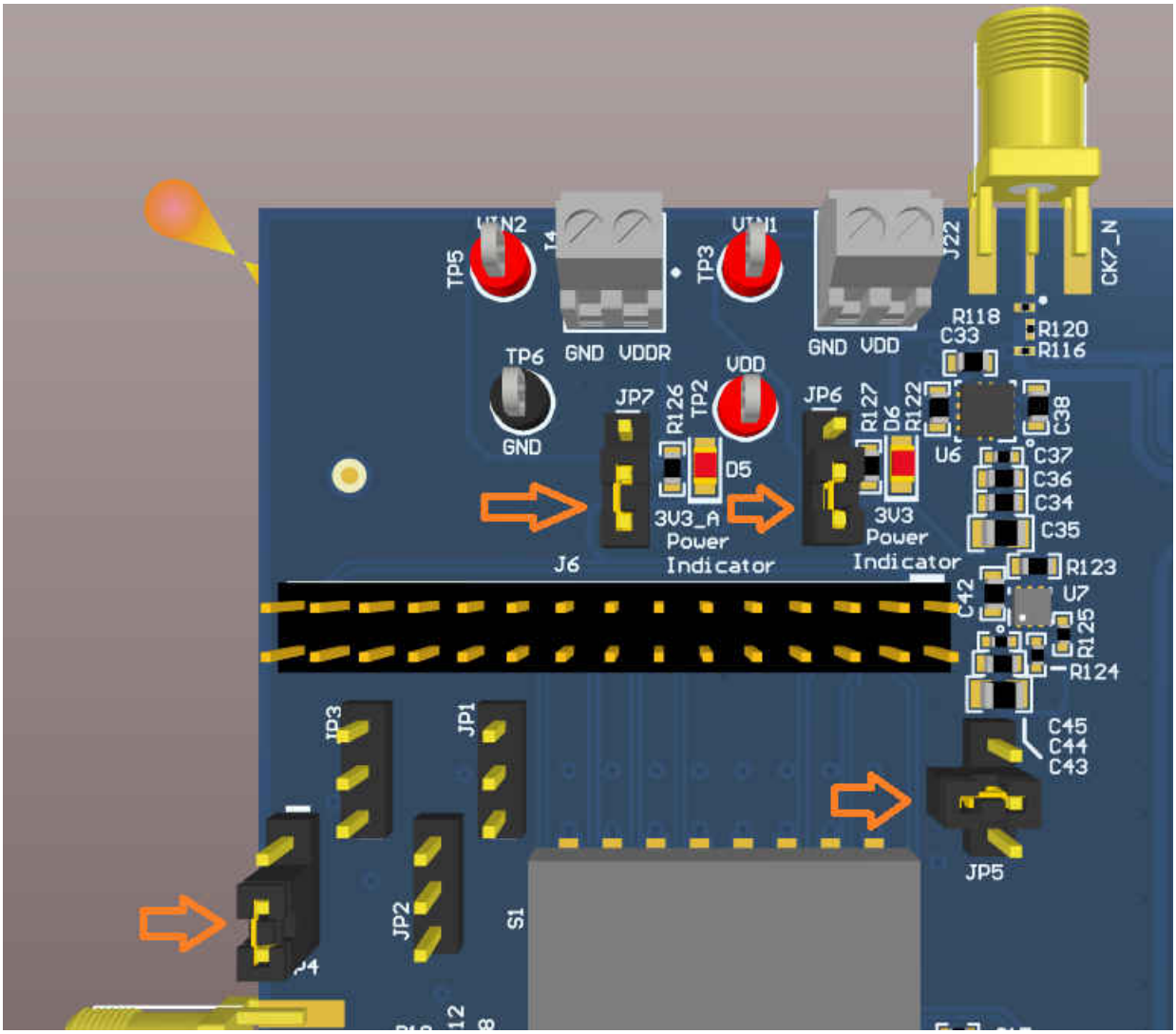

Figure 3-2. Default Jumper Configuration

2. Connect a 3.3-V to 5-V power supply to VDD and VDD_R as well as associating GND terminals of the 2 power blocks. This powers the on-board LDO regulator to supply 3.3 V to the VDD and VDDR rails of the IC. Both VDD and VDDR have associated '3V3' and '3V3_A' LEDs that should be lit red when ON.

   Set the desired clock output using the output selection control switches, S1[1:7], as seen in Table 3-1.

Table 3-1. DIP Switch Selection

Selected Output	S1 Pin	Default Setting
OE1#	1	ON
OE2#	2	OFF
OE3#	3	OFF
OE4#	4	ON
OE5#	5	OFF
OE6#	6	OFF
OE7#	7	OFF

Table 3-1. DIP Switch Selection (continued)

Selected Output	S1 Pin	Default Setting
CKPWRGD_PD#	8	ON

3. Connect and measure any clock output SMA labeled CKx_P or CKx_N to an oscilloscope or other test instrument using SMA cable(s). The output clock will be a level-translated/buffered copy of the selected clock input.

Note

Populated output clocks are DC-coupled to the SMA connectors.

Note

Any active output trace(s) without proper load termination can cause signal reflections on the board, which can couple onto nearby outputs and degrade signal quality and measurement accuracy. To minimize these effects, be sure to properly terminate any unused output trace with a 50-Ω SMA load, or else disconnect any unused output trace from the device output pin by removing the series 0-Ω resistor. An unused output or output bank may also be disabled using the output mode control switch.

4 Signal Path and Control Switches

The CDCDB800 supports single-ended or differential clocks on CLKin_P (J1) and CLKin_N (J2). To achieve the maximum operating frequency and lowest additive jitter, TI recommends to use a differential input clock with high slew rate (>3 V/ns).

The device provides up to 8 LP-HCSL outputs with pin-selectable output enable (HCSL, or Hi-Z).

All control pins are configured with the control DIP switch, S1. Table 3-1 shows this default setting, and Table 4-1 shows the REFout enable logic.

Table 4-1. REF out Enable Selection

REFout Enable Mode	S1[1:7] REFout_EN State
Disabled/Hi-Z	OFF
Enabled	ON

5 Power Supplies

The power supply section on the EVM provides flexibility to power the device using the onboard regulator(s) or direct supply input(s). A combination of 0-Ω resistor options allows the user to modify the EVM power supply configuration, if desired.

By default, 3.3 V is supplied to VDD and VDDR input through the onboard LDO regulator, U6. To power the regulator, connect a 3.3-V to 5-V input voltage and ground from an external power source to the terminal block, J3.

To modify the EVM with a different power supply configuration, populate the resistor options as shown in EVM Power Supply Configuration Options. Then, apply the appropriate voltage(s) to the EVM power input(s).

If the EVM is configured for dual direct supplies, connect a 3.3-V supply to both VDD and VDDR supply and associated ground to the labeled terminal blocks.

Decoupling capacitors and 0-Ω resistor footprints, which can accommodate ferrite beads, can be used to isolate the EVM power input(s) from the device power pins.

Table 5-1. EVM Power Supply Configuration Options

	TPS73533 LDO Regulator (U6) 3.3 V (DEFAULT)	**Dual Direct Supplies 3.3 V**
VDD port (J3)	Apply 4 V to 6 V	Apply 3.3 V ± 5%
VDDR port (J4)	Not used	Apply 3.3V ± 5%
U6 (3V3_INT)	3.3V (VDD & VDDR)	Not used
R121	0	OPEN
JP6	SHUNT 2-3	SHUNT 1-2
JP7	SHUNT 2-3	SHUNT 1-2
C46 (decoupling cap)	OPEN	22 uF

6 Clock Inputs

The SMA inputs labeled CLKin_P (J1) & CLKin_N (J2) can be configured to receive a differential clock or single-ended clock. The best performance is achieved with an AC differential input clock—the default configuration. Input transmission lines use 50-Ω single-ended impedance, 100-Ω differential impedance.

CLKin paths include footprint options to provide the user with flexibility in configuring the termination, biasing, and coupling for the device inputs. Please take care to follow the Vin electrical parameters shown in the datasheet SNAS818.

6.1 Configuring Board for CDCDB803

To modify the EVM with CDCDB803, populate the resistor options as shown in Table 6-1.

Table 6-1. EVM Configuration Options

	CDCDB800		CDCDB803	
Pin	**Required Change**	**Signal Name**	**Required Change**	**Signal Name**
1	NO CHANGE	CKPWRGD	NO CHANGE	CKPWRGD
2	R26	GNDR	R23	VDDR
3	R7	VDDR	R9	CLKIN_P
4	R11	CLKIN_P	R15	CLKIN_N
5	R19	CLKIN_N	JP1	SADR0
6	NO CHANGE	SMBD	NO CHANGE	SMBD
7	NO CHANGE	SMBC	NO CHANGE	SMBC
8	NO CHANGE	NC	JP2	SADR1
9	NO CHANGE	NC	NO CHANGE	NC
10	R6	VDD	OPEN (Remove R6)	NC
11	OPEN (Remove R14)	OE0#	R14	VDD
12	NO CHANGE	NC	JP3	OE0#

7 Clock Outputs

Output transmission lines use 42.5-Ω single-ended impedance, 85-Ω differential impedance. EVM supports LP-HCSL outputs AC-coupled to the SMA connectors labeled CKx_P/N.

Active output traces should be properly terminated; otherwise any unused output pin can be disconnected from the output trace by removing the 0-Ω series resistor.

See previous table Table 3-1 for switch settings.

8 Using SMBus

The user can program the CDCDB800 or CDCDB803 through TI software – TICSPRO available for download on ti.com.

Go to the TICS Pro toolbar and click **Select Device** → **Clock Distribution with Divider** → **CDCDB800**. Navigate to the **Main** tab and click **Scan SMBus**. The device should be found at **'0xD8'**.

With SMBus, control of the outputs is possible with the associated DIP switch OEx# turned OFF. See the datasheet for implementation.

8.1 CDCDB803 SMBus Address

After board rework, including the addition of JP1 (SADR1) and JP2 (SADR0) jumpers, additional SMBus addresses may be used when programming the device.

9 Schematics

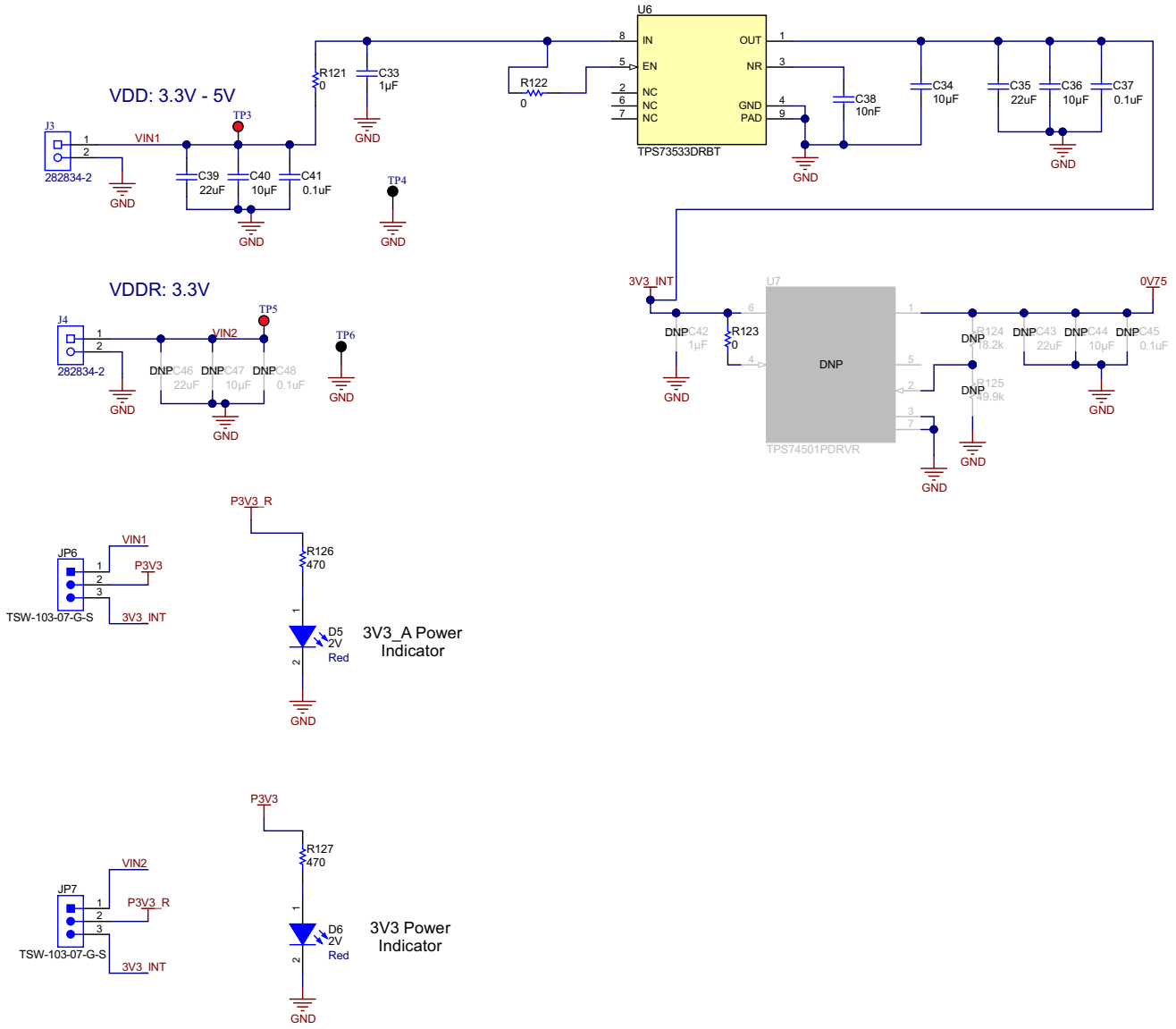

Figure 9-1. Schematic Sheet #1

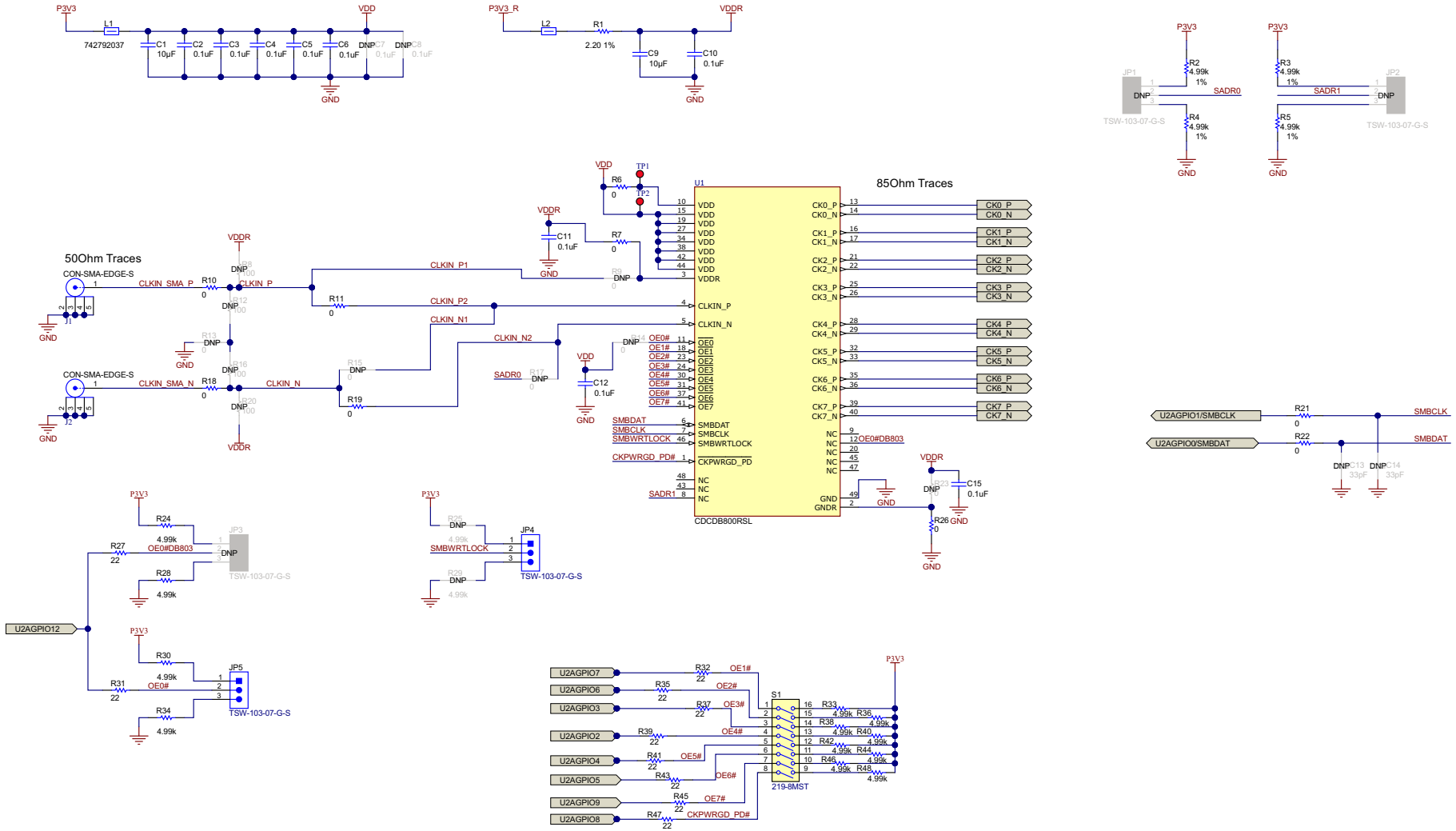

Figure 9-2. Schematic Sheet #2

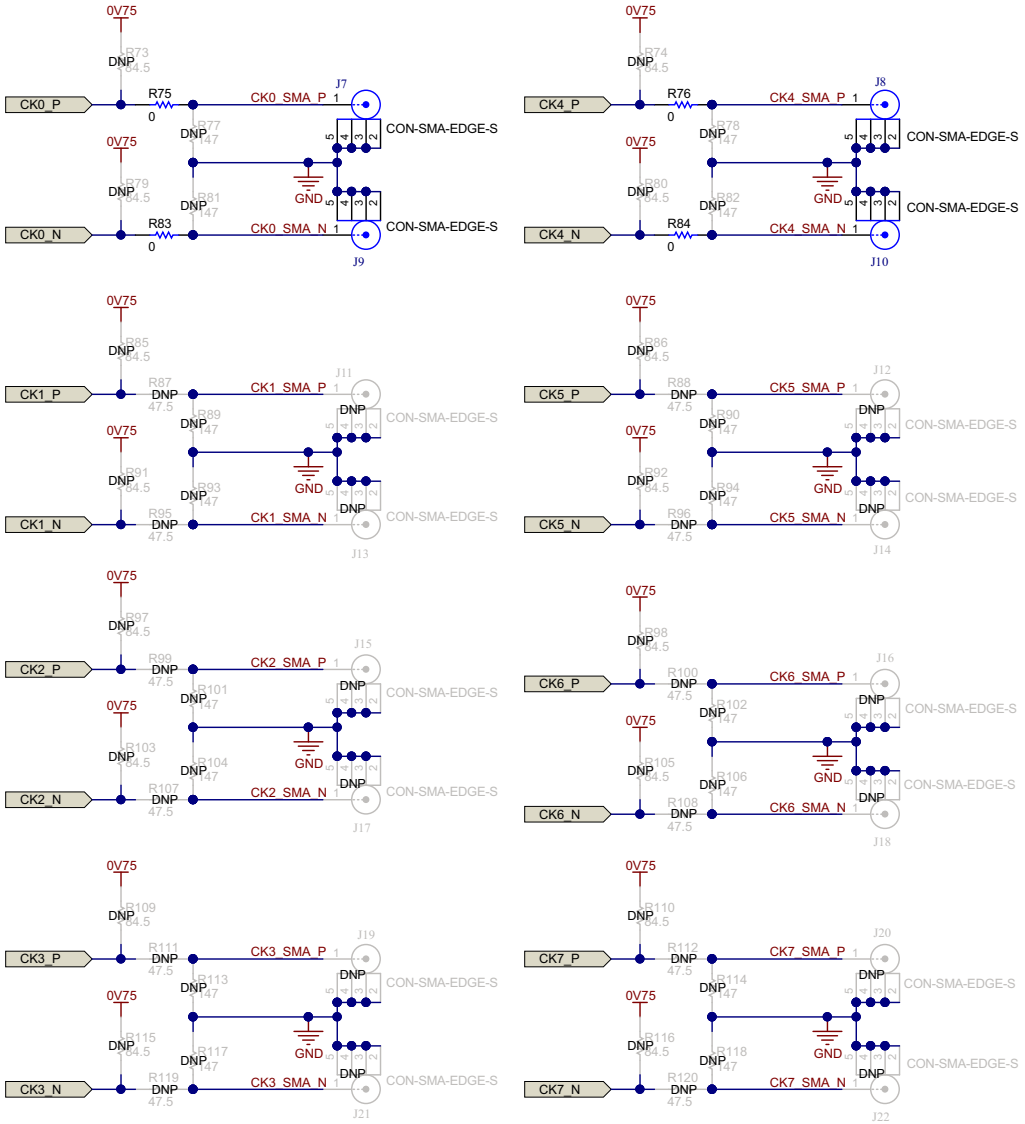

Figure 9-3. Schematic Sheet #3

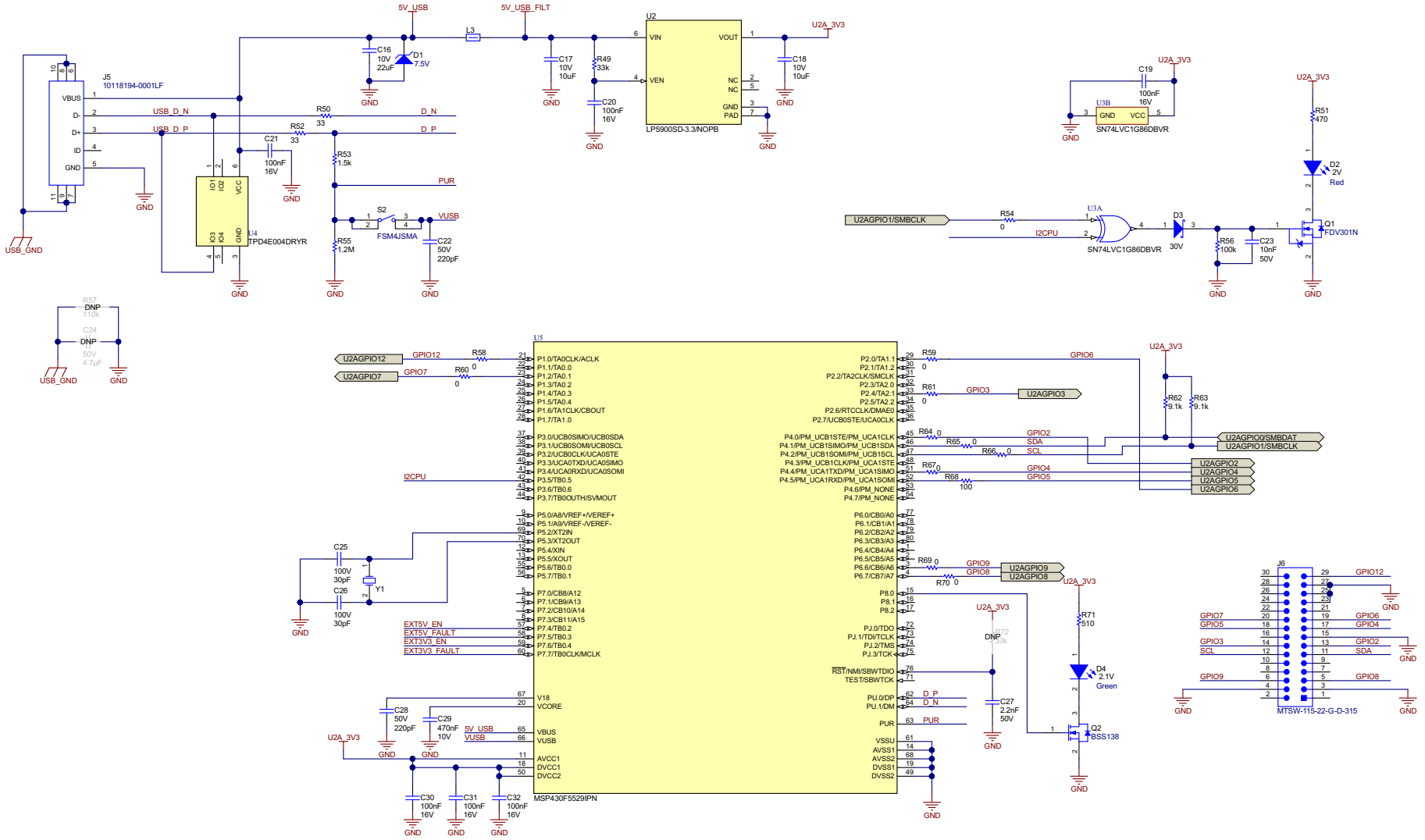

Figure 9-4. Schematic Sheet #4

10 Bill of Materials

Table 10-1. CDCDB800EVM Bill of Materials

Designator	Description	Manufacturer	Part Number	Quantity
C1, C9, C36, C40	CAP, CERM, 10 µF, 16 V,+/- 20%, X6S, 0603	MuRata	GRM188C81C106MA73D	4
C2, C3, C4, C5, C6, C10, C11, C12, C15, C37, C41	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0402	MuRata	GRM155R71A104KA01D	11
C16, C35, C39	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805	Taiyo Yuden	LMK212BJ226MG-T	3
C17, C18	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0603	TDK	C1608X5R1A106M080AC	2
C19, C20, C21, C30, C31, C32	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	Kemet	C0603C104J4RACTU	6
C22, C28	CAP, CERM, 220 pF, 50 V, +/- 1%, C0G/NP0, 0603	AVX	06035A221FAT2A	2
C23	CAP, CERM, 0.01 uF, 50 V, +/- 5%, X7R, 0603	Kemet	C0603C103J5RACTU	1
C25, C26	CAP, CERM, 30 pF, 100 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C2A300JA01D	2
C27	CAP, CERM, 2200 pF, 50 V, +/- 10%, X7R, 0603	Kemet	C0603C222K5RACTU	1
C29	CAP, CERM, 0.47 uF, 10 V, +/- 10%, X7R, 0603	MuRata	GRM188R71A474KA61D	1
C33	CAP, CERM, 1 uF, 35 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E1X7R1V105K080AC	1
C34	CAP, CERM, 10 uF, 10 V, +/- 20%, X7R, 0603	MuRata	GRM188Z71A106MA73D	1
C38	CAP, CERM, 0.01 uF, 10 V, +/- 10%, X7R, 0603	AVX	0603ZC103KAT2A	1
D1	Diode, Zener, 7.5 V, 550 mW, SMB	ON Semiconductor	1SMB5922BT3G	1
D2, D5, D6	LED, Red, SMD	Lite-On	LTST-C170KRKT	3
D3	Diode, Schottky, 30 V, 0.2 A, SOT-23	Diodes Inc.	BAT54-7-F	1
D4	LED, Green, SMD	Lite-On	LTST-C190GKT	1
H1, H2, H3, H4	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)	4
J1, J2, J7, J8, J9, J10	CONN SMA JACK STR EDGE MNT	RF Solutions Ltd.	CON-SMA-EDGE-S	6
J3, J4	Terminal Block, 2x1, 2.54mm, TH	TE Connectivity	282834-2	2
J5	Receptacle, USB 2.0, Micro-USB Type B, R/A, SMT	FCI	10118194-0001LF	1
J6	Header, 100mil, 15x2, Gold, TH	Samtec	MTSW-115-22-G-D-315	1
JP4, JP5, JP6, JP7	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S	4
L1, L2	Ferrite Bead, 330 ohm @ 100 MHz, 2 A, 0805	Wurth Elektronik	742792037	2
L3	Ferrite Bead, 60 ohm @ 100 MHz, 3.5 A, 0603	TDK	MPZ1608S600ATAH0	1
LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	Brady	THT-14-423-10	1

Table 10-1. CDCDB800EVM Bill of Materials (continued)

Designator	Description	Manufacturer	Part Number	Quantity
Q1	MOSFET, N-CH, 25 V, 0.22 A, SOT-23	Fairchild Semiconductor	FDV301N	1
Q2	MOSFET, N-CH, 50 V, 0.22 A, SOT-23	Fairchild Semiconductor	BSS138	1
R1	RES, 2.20, 1%, 0.1 W, 0603	Panasonic	ERJ-3RQF2R2V	1
R2, R3, R4, R5, R24, R28, R30, R33, R34, R36, R38, R40, R42, R44, R46, R48	RES, 4.99 k, 1%, 0.063 W, 0402	Yageo America	RC0402FR-074K99L	16
R6, R26, R121, R122, R123	RES, 0, 5%, 0.125 W, 0603	Vishay/Beyschlag	MCT06030Z0000ZP500	5
R7, R10, R11, R18, R19	RES, 0, 5%, 0.1 W, 0603	Yageo	RC0603JR-070RL	5
R21, R22, R54, R58, R59, R60, R61, R64, R65, R66, R67, R69, R70	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06030000Z0EA	13
R27, R31, R32, R35, R37, R39, R41, R43, R45, R47	RES, 22, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060322R0JNEA	10
R49	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060333K0JNEA	1
R50, R52	RES, 33, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040233R0JNED	2
R51, R126, R127	RES, 470, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603470RJNEA	3
R53	RES, 1.5 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW04021K50JNED	1
R55	RES, 1.2 M, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW06031M20JNEA	1
R56	RES, 100 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100KJNEA	1
R62, R63	RES, 9.1 k, 5%, 0.1 W, 0603	Yageo	RC0603JR-079K1L	2
R68	RES, 100, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100RJNEA	1
R71	RES, 510, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603510RJNEA	1
R75, R83	RES, 0, 5%, 0.05 W, 0201	Vishay-Dale	CRCW02010000Z0ED	2
R76, R84	RES, 47.5, 1%, 0.05 W, 0201	Yageo America	RC0201FR-0747R5L	2
S1	Switch, Slide, SPST 8 poles, SMT	CTS Electrocomponents	219-8MST	1
S2	Switch, Tactile, SPST-NO, 0.05A, 12V, SMT	TE Connectivity	FSM4JSMA	1
SH1, SH2, SH3, SH4	Shunt, 100mil, Gold plated, Black	Samtec	SNT-100-BK-G	4
TP1, TP2, TP3, TP5	Test Point, Multipurpose, Red, TH	Keystone	5010	4
TP4, TP6	Test Point, Multipurpose, Black, TH	Keystone	5011	2
U1	8-output LP-HCSL clock buffer capable of distributing the reference clocks for PCIe Gen 1-5, QPI, UPI, SAS, and SATA interfaces	Texas Instruments	CDCDB800RSL	1
U2	150-mA Ultra-Low Noise LDO for RF and Analog Circuits Requires No Bypass Capacitor, NGF0006A (WSON-6)	Texas Instruments	LP5900SD-3.3/NOPB	1
U3	Single 2-Input Exclusive-OR Gate, DBV0005A (SOT-23-5)	Texas Instruments	SN74LVC1G86DBVR	1

Table 10-1. CDCDB800EVM Bill of Materials (continued)

Designator	Description	Manufacturer	Part Number	Quantity
U4	4-Channel ESD Protection Array for High-Speed Data Interfaces, DRY0006A (USON-6)	Texas Instruments	TPD4E004DRYR	1
U5	25 MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85 degC, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	Texas Instruments	MSP430F5529IPN	1
U6	500mA, Adjustable, Low Quiescent Current, Low-Noise, High-PSRR, Single-Output LDO Regulator, DRB0008A (VSON-8)	Texas Instruments	TPS73533DRBT	1
Y1	Crystal, 24.000 MHz, 20pF, SMD	ECS Inc.	ECS-240-20-5PX-TR	1
C7, C8, C45, C48	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0402	MuRata	GRM155R71A104KA01D	0
C13, C14	CAP, CERM, 33 pF, 100 V, +/- 5%, C0G/NP0, 0603	AVX	06031A330JAT2A	0
C24	CAP, CERM, 4.7 µF, 50 V,+/- 10%, X7R, 1206	TDK	C3216X7R1H475K160AE	0
C42	CAP, CERM, 1 uF, 35 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	TDK	CGA3E1X7R1V105K080AC	0
C43, C46	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805	Taiyo Yuden	LMK212BJ226MG-T	0
C44, C47	CAP, CERM, 10 µF, 16 V,+/- 20%, X6S, 0603	MuRata	GRM188C81C106MA73D	0
FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	0
J11, J12, J13, J14, J15, J16, J17, J18, J19, J20, J21, J22	CONN SMA JACK STR EDGE MNT	RF Solutions Ltd.	CON-SMA-EDGE-S	0
JP1, JP2, JP3	Header, 100mil, 3x1, Gold, TH	Samtec	TSW-103-07-G-S	0
R8, R12, R16, R20	RES, 100, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW0603100RFKEA	0
R9, R13, R15, R17	RES, 0, 5%, 0.1 W, 0603	Yageo	RC0603JR-070RL	0
R14, R23	RES, 0, 5%, 0.125 W, 0603	Vishay/Beyschlag	MCT06030Z0000ZP500	0
R25, R29	RES, 4.99 k, 1%, 0.063 W, 0402	Yageo America	RC0402FR-074K99L	0
R57	RES, 110 k, 1%, 0.25 W, 1206	Yageo America	RC1206FR-07110KL	0
R72	RES, 33 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	Vishay-Dale	CRCW060333K0JNEA	0
R73, R74, R79, R80, R85, R86, R91, R92, R97, R98, R103, R105, R109, R110, R115, R116	RES, 84.5, 1%, 0.05 W, 0201	Yageo America	RC0201FR-0784R5L	0
R77, R78, R81, R82, R89, R90, R93, R94, R101, R102, R104, R106, R113, R114, R117, R118	RES, 147, 1%, 0.05 W, 0201	Yageo America	RC0201FR-07147RL	0
R87, R88, R95, R96, R99, R100, R107, R108, R111, R112, R119, R120	RES, 47.5, 1%, 0.05 W, 0201	Yageo America	RC0201FR-0747R5L	0

Table 10-1. CDCDB800EVM Bill of Materials (continued)

Designator	Description	Manufacturer	Part Number	Quantity
R124	RES, 18.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040218K2FKED	0
R125	RES, 49.9 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	Vishay-Dale	CRCW040249K9FKED	0
U7	500-mA LDO With Power-Good, DRV0006A (WSON-6)	Texas Instruments	TPS74501PDRVR	0

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