PCN Number:	20220718001.1	**PCN Date:**	July 19, 2022
Title:	Qualification of STATS ChipPac as an additional assembly site for selected Devices		
Customer Contact:	PCN Manager	**Dept:**	Quality Services
Proposed 1st Ship Date:	Oct 16, 2022	**Sample Requests accepted until:**	Aug 19, 2022*

***Sample requests received after Aug 18, 2022 will not be supported.**

Change Type:

☒	Assembly Site	☐	Design	☐	Wafer Bump Site
☐	Assembly Process	☐	Data Sheet	☐	Wafer Bump Material
☐	Assembly Materials	☐	Part number change	☐	Wafer Bump Process
☐	Mechanical Specification	☐	Test Site	☐	Wafer Fab Site
☐	Packing/Shipping/Labeling	☐	Test Process	☐	Wafer Fab Materials
				☐	Wafer Fab Process

PCN Details

Description of Change:

Texas Instruments Incorporated is announcing the qualification of STATS ChipPac as an alternate Assembly site for devices listed below in the product affected section. There are no construction differences of the devices between the two assembly sites.

Reason for Change:

Supply continuity

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Impact on Environmental Ratings

Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.

RoHS	REACH	Green Status	IEC 62474
☒ No Change	☒ No Change	☒ No Change	☒ No Change

Changes to product identification resulting from this PCN:

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
Amkor	AMP	KOR	Gwangju
STATS ChipPac	**SCK**	**KOR**	**INCHEON**

Sample product shipping label (not actual product label)

Product Affected:	
DRA829JMTGBALFR	DRA829VMTGBALFR

TI Information
Selective Disclosure

Automotive New Product Qualification Summary
(As per AEC-Q100 and JEDEC Guidelines)

Jacinto7- DRA829xxx and TDA4VM88xxx

Product Attributes

Attributes	Test Vehicle: DC2AAALF	Qual Device: XJ721EGALF (ES 1.0)	Qual Device: XJ721EGALF (ES 1.1)	Qual Device: XJ721EGALF (ES 1.2)
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range	-40 to +125 C	-40 to +125 C	-40 to +125 C	-40 to +125 C
Product Function	Microprocessor	Microprocessor	Microprocessor	Microprocessor
Wafer Fab Supplier	TSMC-F14	TSMC-F14	TSMC-F14	TSMC-F14
Assembly Site	SCK	SCK	SCK	SCK
Package Type	Flip Chip BGA	Flip Chip BGA	Flip Chip BGA	Flip Chip BGA
Package Designator	ALF	ALF	ALF	ALF
Ball/Lead Count	827	827	827	827

- QBS: Qual By Similarity
- Qual Device XJ721EGALF is qualified at LEVEL3-250C

Qualification Results
Data Displayed as: Number of lots / Total sample size / Total failed

	Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Test Vehicle: DC2AAALF	Qual Device: XJ721EGALF (ES 1.0)	Qual Device: XJ721EGALF (ES 1.1)	Qual Device: XJ721EGALF (ES 1.2)
Test Group A – Accelerated Environment Stress Tests											
	PC	A1	JEDEC J-STD-020 JESD22-A113	3	77	Preconditioning	(level 3 @ 250C peak +5/-0C)	-	3/982/0		
	THB	A2	JEDEC JESD22-A101	3	77	**Auto Biased Temp Humidity	85C/85%RH, (1000 Hours)	-	3/231/0		
	UHST	A3	JEDEC JESD22-A102, A118, or A101	3	77	**Unbiased HAST	110C/85%RH (264 Hours)	-	3/231/0		
	TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	**T/C -55C/125C	-55C/+125C (1000 Cycles)	-	3/231/0 (c)		
	PTC	A5	JEDEC JESD22-A105	1	45	**Power Temperature Cycle	-40C/105C (1000 Cycles)	-	1/45/0		
	HTSL	A6	JEDEC JESD22-A103	1	45	**High Temp. Storage Bake	150C (1000 Hours)	-	1/77/0 (c)		
Test Group B – Accelerated Lifetime Simulation Tests											
	HTOL	B1	JEDEC JESD22-A108	3	77	HTOL - CMOS	132C Tj (1000 Hours)	-		3/231/1 (a)	
	ELFR	B2	AEC Q100-008	3	800	EFR2	135C Tj (48 Hours)	-		2/1630/0	1/811/2 (b)

Test Group C – Package Assembly Integrity Tests											
	PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions (Cpk>1.67)	-	-	3/30/0	-	-
	SBS	C5	AEC Q100-010	3	50	Solder Ball Shear (Cpk>1.67)	Solder Balls		3/150/0 (BGAs)		
Test Group D – Die Fabrication Reliability Tests											
	EM	D1	JESD61	-	-	Electromigration	-	Completed Per Process Technology Requirements			
	TDDB	D2	JESD35	-	-	Time Dependant Dielectric Breakdown	-	Completed Per Process Technology Requirements			
	HCI	D3	JESD60 & 28	-	-	Hot Injection Carrier	-	Completed Per Process Technology Requirements			
	NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	Completed Per Process Technology Requirements			
	SM	D5	-	-	-	Stress Migration	-	Completed Per Process Technology Requirements			
Test Group E – Electrical Verification Tests											
	CDM	E3	AEC Q100-011	1	3	Auto ESD CDM	500V, 750V (corner pins)	-	-	-	1/3/0
	ED	E5	AEC Q100-009	3	30	Electrical Char.	-	-	-	-	5/90/0
Additional Tests											
	BLR			-	-	BLR - Temp Cycle, -40/125C BLR TC	-40/125C (1000 cycles) (2000 cycles)	1/32/0 1/32/0	-	-	-
	MQ			-	-	Manufacturability	Automotive MQ required	-	3/pass		

A1 (PC): Preconditioning:
Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.

Ambient Operating Temperature by Automotive Grade Level:
Grade 0 (or E): -40°C to +150°C
Grade 1 (or Q): -40°C to +125°C
Grade 2 (or T): -40°C to +105°C
Grade 3 (or I): -40°C to +85°C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):
Room/Hot/Cold: HTOL, ED
Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room: AC/uHAST

Green/Pb-free Status:
Qualified Pb-Free (SMT) and Green

TI Qualification ID: 20180413-125477

Note:

(a) 8D reports available on request.
(b) 8D reports available on request.
(c) Electrically Induced Physical Damage (EIPD)

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

Location	E-Mail
WW Change Management Team	PCN_ww_admin_team@list.ti.com

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